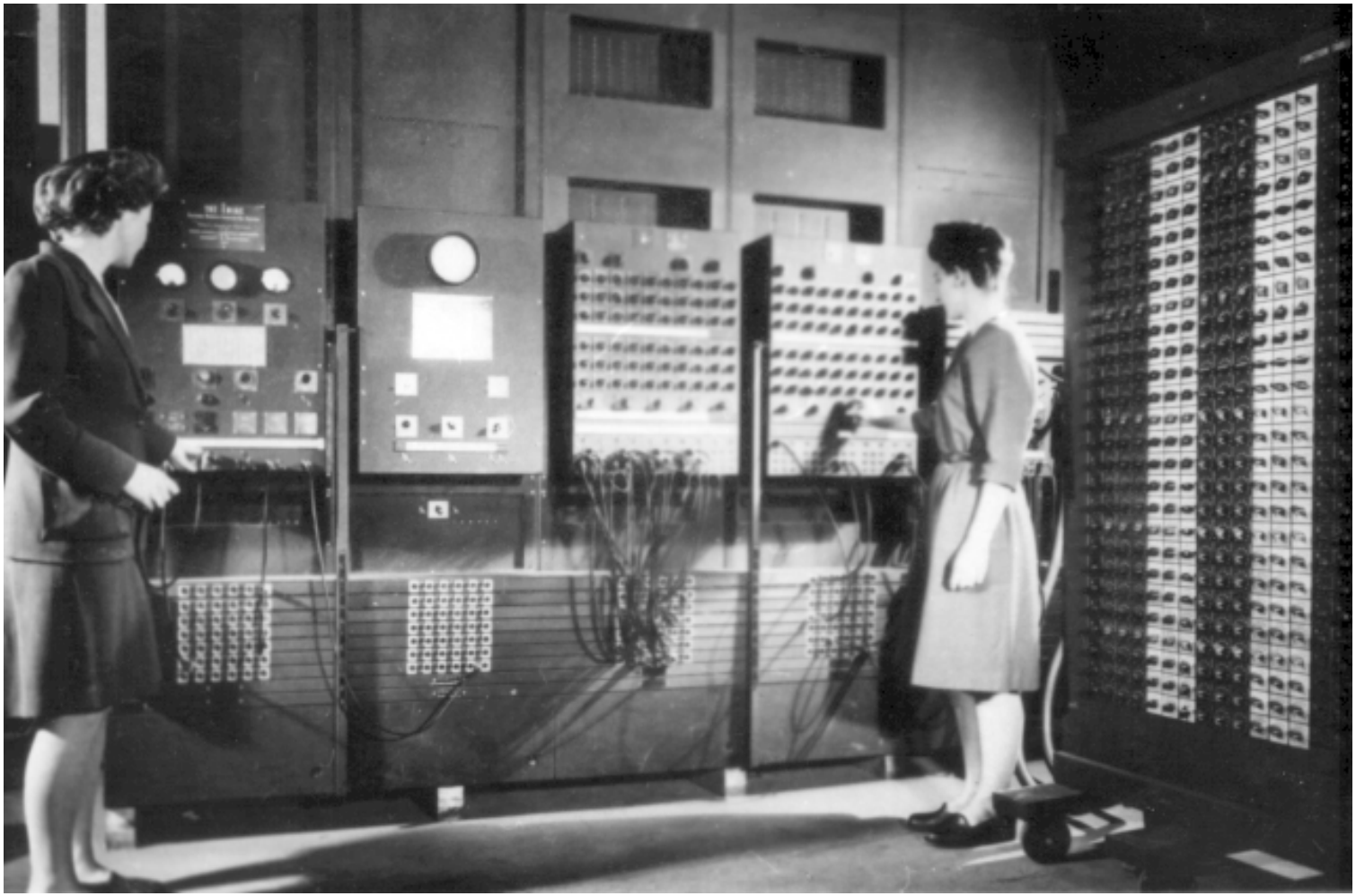
Silicon Compilers - Version 2.0

Andreas Olofsson
Program Manager, DARPA/MTO

International Symposium on Physical Design
March 25-28, Monterey, CA

A Brief History of EDA

ENIAC: A world without Moore's Law



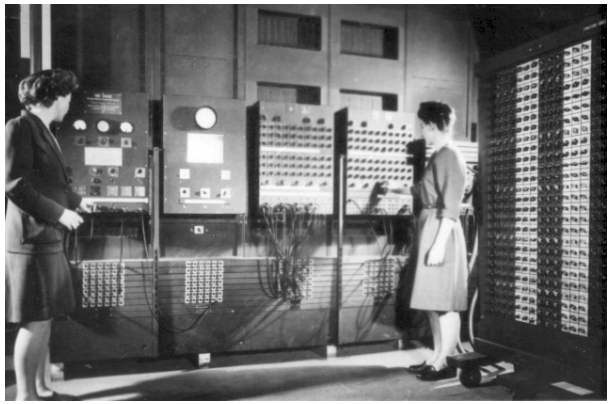
https://en.wikipedia.org/wiki/ENIAC

Source: https://en.wikipedia.org/wiki/ENIAC

- First all electric computer
- 357 mults/sec
- $6.7M (adjusted)
- 20,000 vacuum tubes
- 27 tons
- 5M solder joints!
- 50% uptime
- 2 week compilations

The modern miracle of Moore's Law

https://www.allpar.com/history



https://en.wikipedia.org/wiki/ENIAC

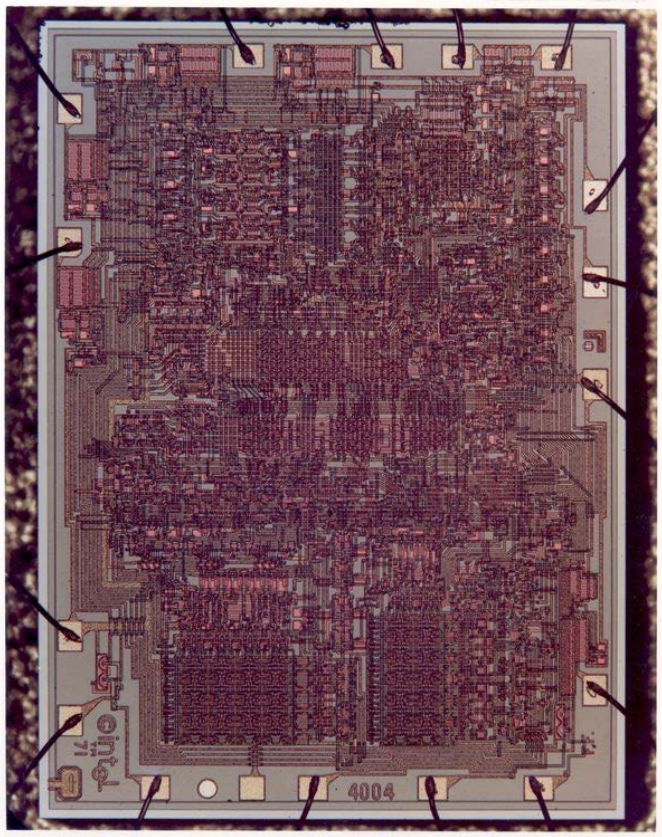
https://www.caranddriver.com/chevrolet/cruze

https://en.wikipedia.org/wiki/Titan_(supercomputer)

	1946	Today
Speed, mph (S)	78	102
Efficiency, mpg (E)	14.6	22
Cost, $K (C)	1.7	27
(S * E) / C	669	83

	1946	Today
Speed, OPS/S (S)	359	17.9e15
OPS/W (E)	0.002	2e9
Cost, $M (C)	6.5	97
(S * E) / C	0.11	3e23

1970's: Heroic human efforts



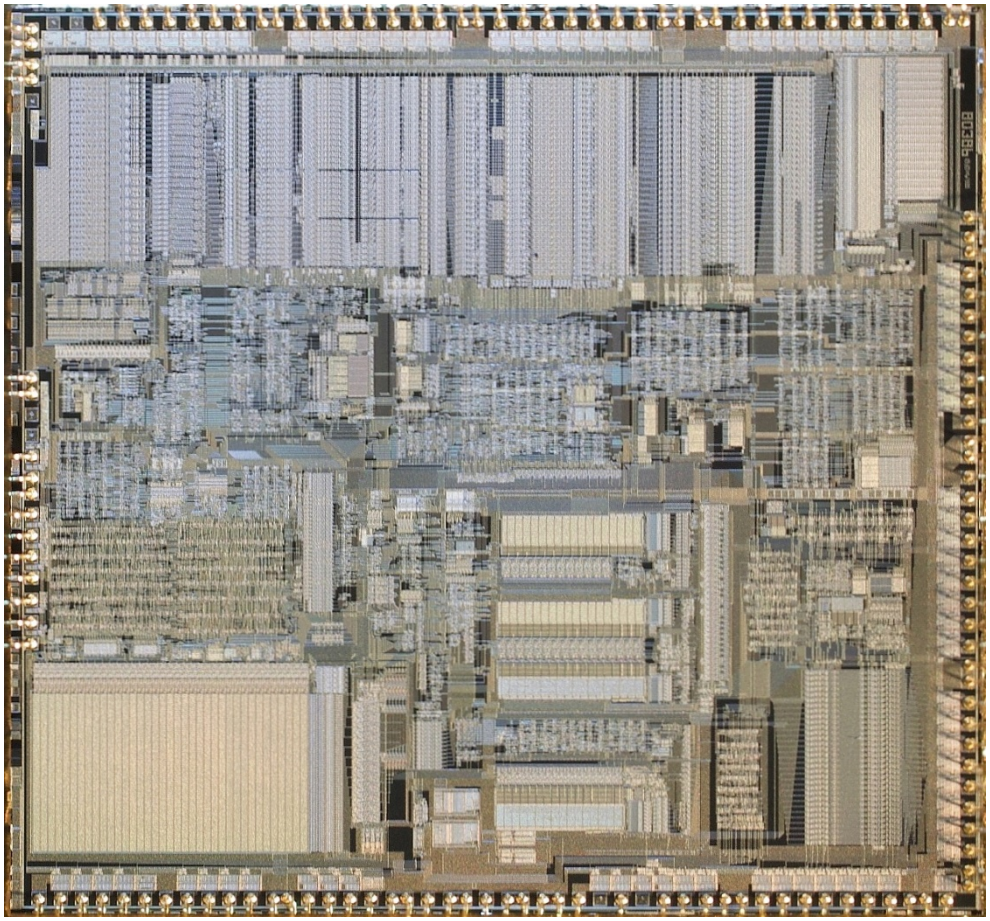
Source: https://en.wikipedia.org/wiki/Intel_400

- Intel 4004 (1971-1981)
- 10-um feature size
- 2,300 transistors

Source: http://www.computerhistory.org/revolution/artifact/287/1614

Rubylith operators

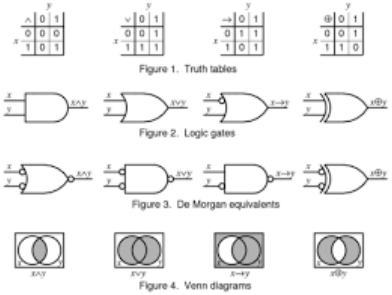
1980's: The birth of modern EDA



Source: https://en.wikipedia.org/wiki/Intel_80386

- Intel 80386 (1985-2007)
- 1-um feature size
- 275,000 transistors

Synthesis

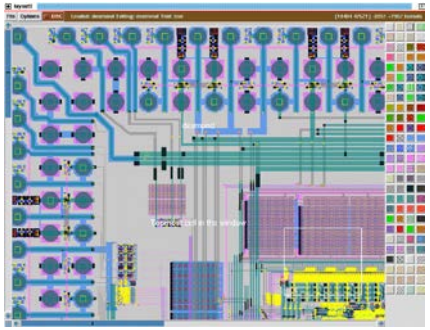


Source: https://en.wikipedia.org/wiki/Logic_synthesis

Place and Route

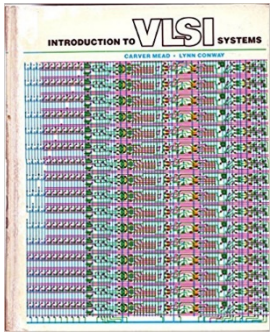
Source: http://venividiwiki.ee.virginia.edu/mediawiki/

Layout Systems



Source: http://opencircuitdesign.com/magic/

Framework



Source: Introduction to VLSI systems by Carver Mead

Birth of Modern EDA

Synopsys Cadence Mentor Graphics

1990's-Today: Managing complexity

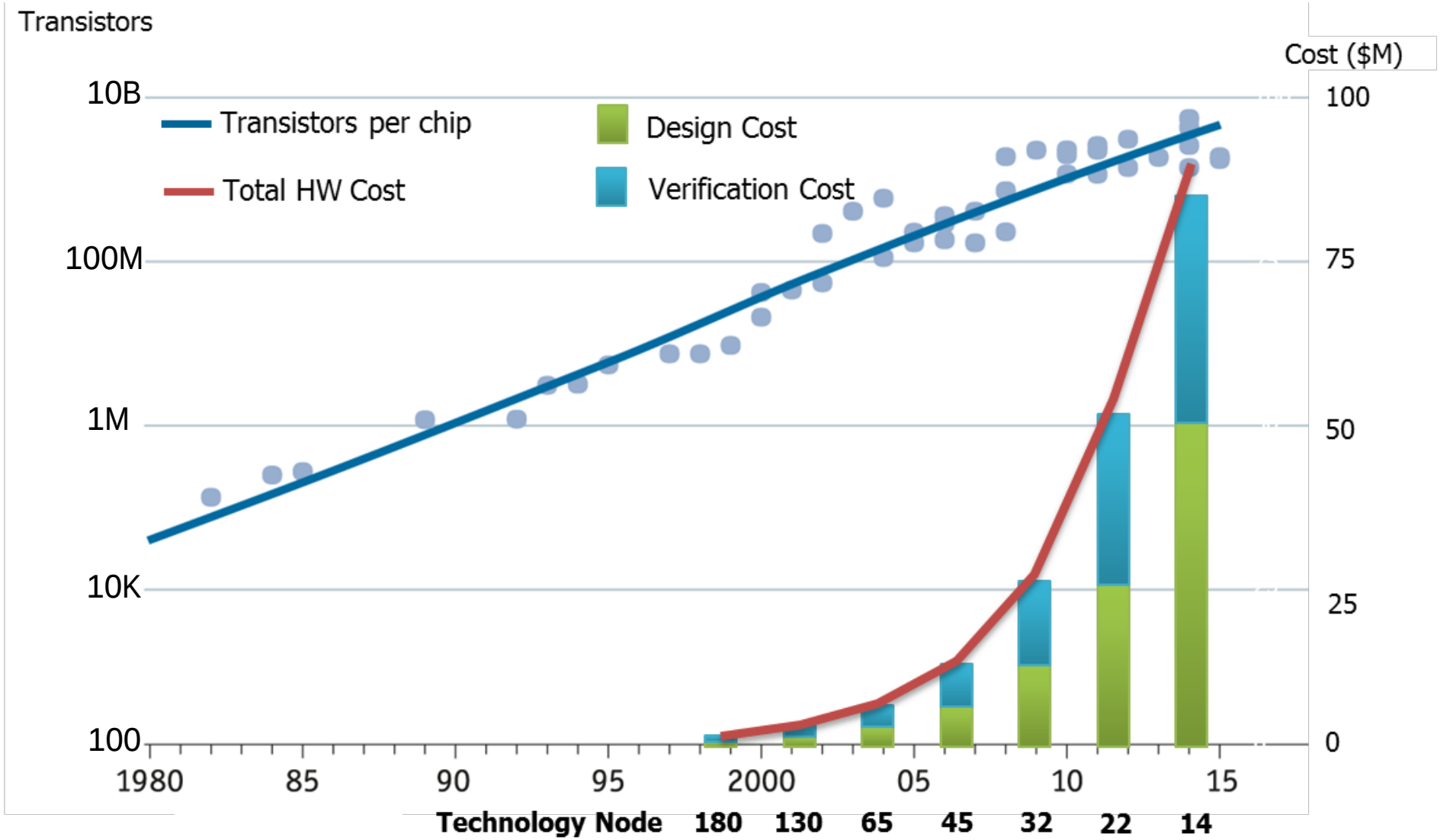
Source: https://nvidianews.nvidia.com/file?fid=59129280a138351b9447113c

It took several thousand engineers several years to create, at an approximate development cost of $3 billion. –Jensen Huang

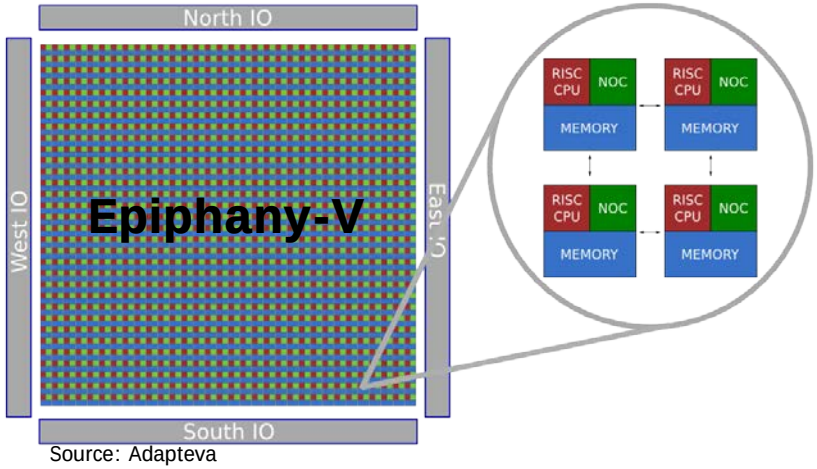
- NVIDIA V100 (2017-)
- 0.012um feature size
- 21,000,000,000 transistors

Death by a million papercuts…correctness, application performance, IP integration, power management, firmware, system integration, wire delays, place and route optimization, clocking, packaging, signal integrity, triple patterning, antenna effects, ESD, muti voltage, power gating, multi threshold, area minimization, routing congestion, on-chip variability, self heating, electro migration, SEUs, signal integrity, power delivery networks, decoupling, model accuracy, abstraction layers, low voltage operations, cooling, security, formal proofs, design for test, metal density rules, OPC concerns, timing convergence, yield optimization, static and dynamic power minimization, scan compression, memory BIST, area minimization…

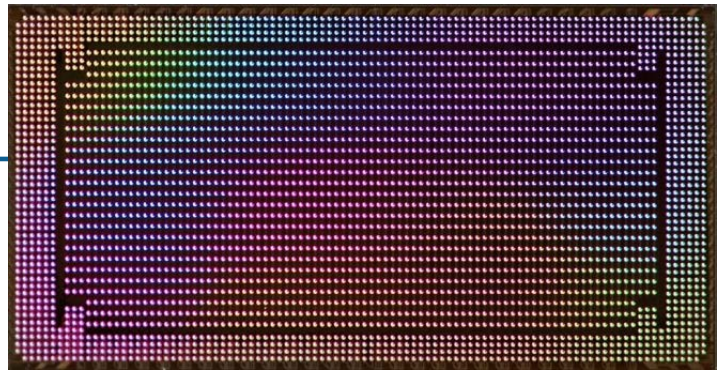
Has EDA failed to keep up with Moore's Law?



It's not that simple....



Source: Adapteva



	Value
Process	TSMC 16FF+
Transistors	4.5B
Die Area	117 mm^2
Flip Chip Bumps	3,460
I/O Signals	1,040
Clock Domains	1,152
Voltage Domains	2,052
Frequency	500Mhz*
32 Performance	2 TFLOPS
64 bit Performance	1 TFLOPS
Memory Bandwidth	16 TB/sec
NOC Bandwidth	0.75 TB/sec
Typical Power	~10W
Minimum Power	1mW

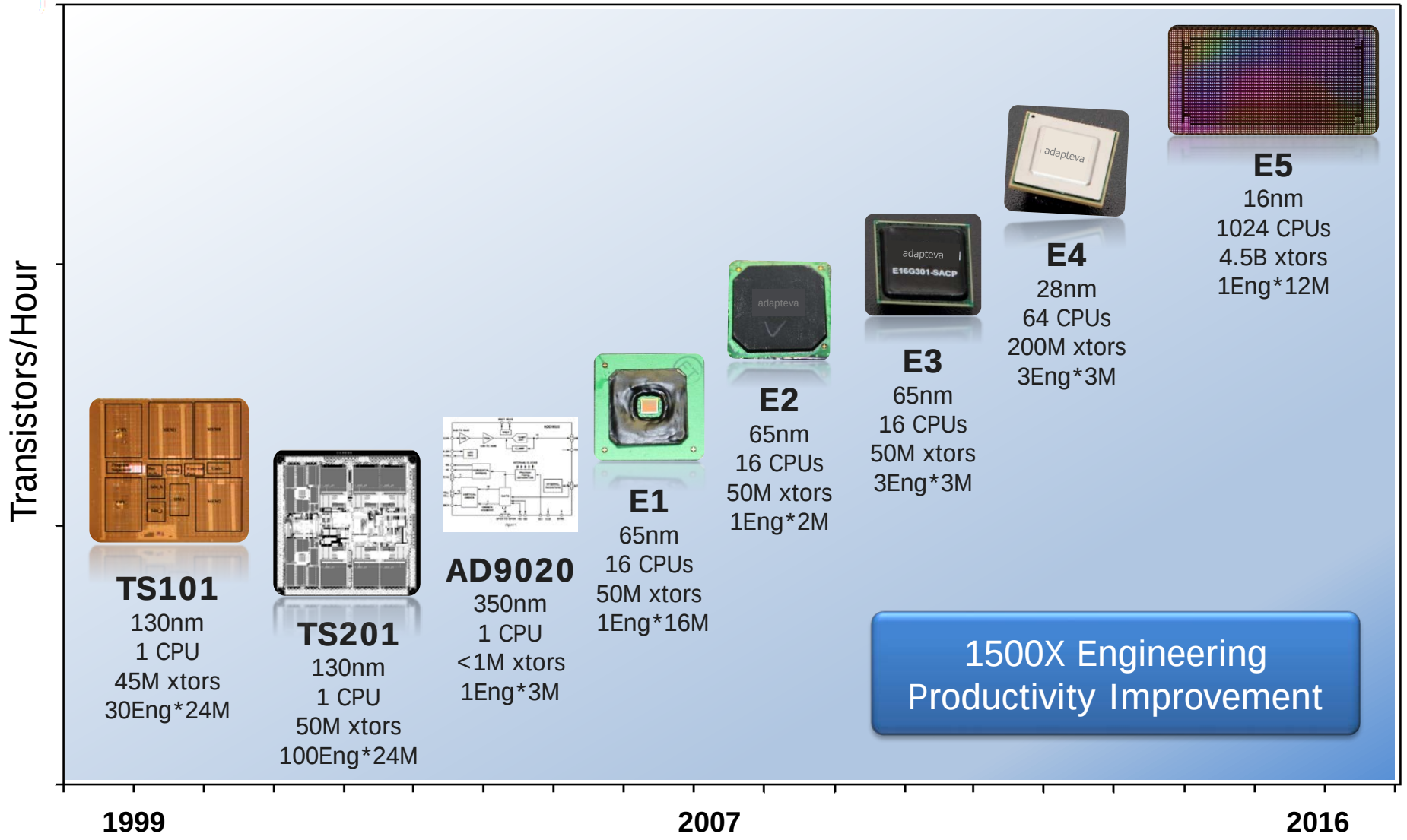
"Server Farm":

- **One** 2010 Dell PowerEdge T610 with a quad-core Xeon 5500 and 32GB DDR3
- One RTL to GDS EDA license
- 12 month design, 24hr spins

Source: Dell

Designer	Responsibility	Man-Hours
Contractor A	FPU	200
Contractor B	Verification	200
Contractor C	EDA Services	112
Ola Jeppsson	Simulator/SDK	500
Andreas Olofsson	Remainder	4,100

My personal EDA interaction over 20 years



http://www.analog.com
http://www.adapteva.com
http://www.ieee.org

My view: EDA needs to move to 100% automation

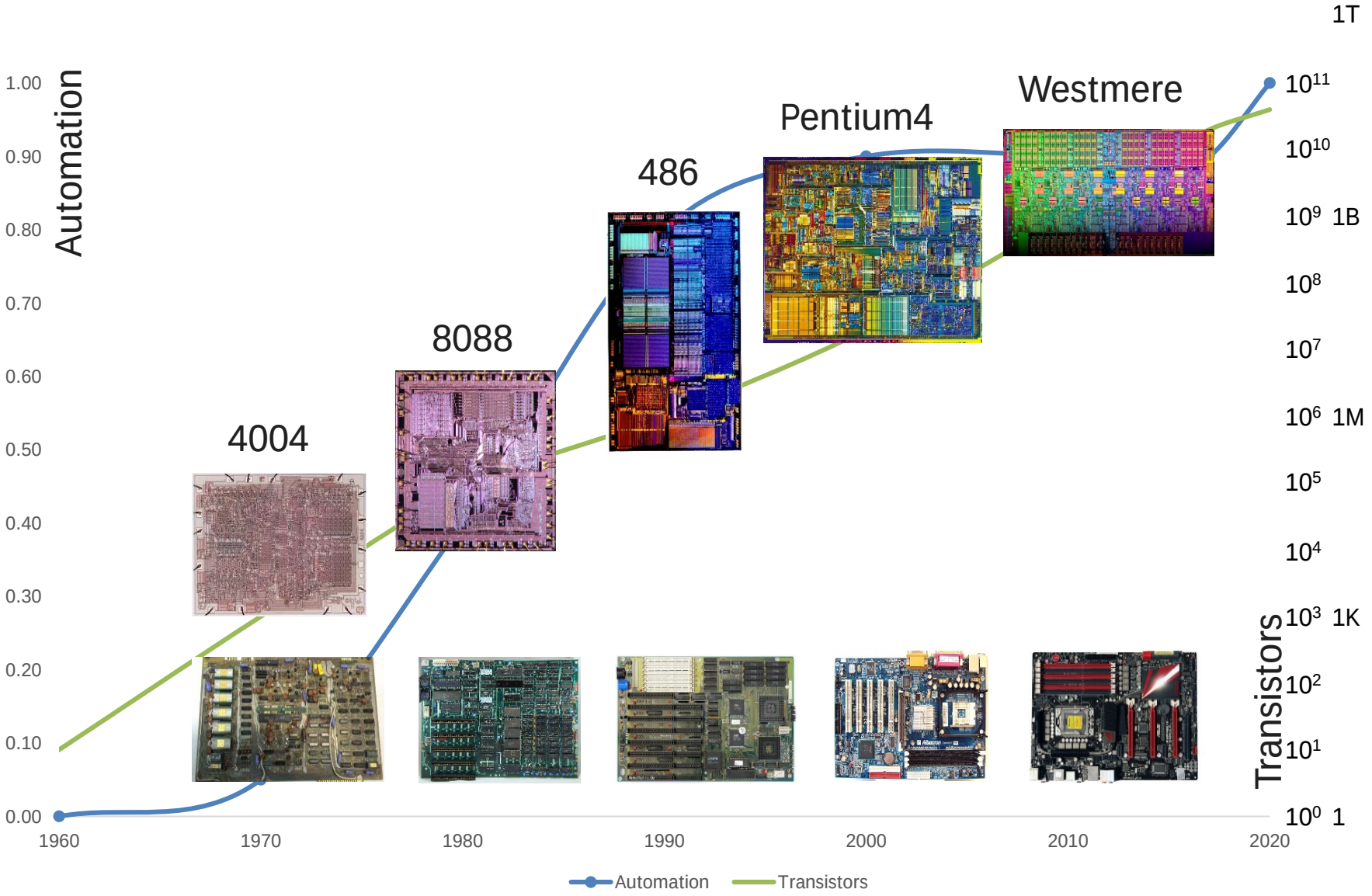


Image source: Intel

Making the case for democratizing EDA

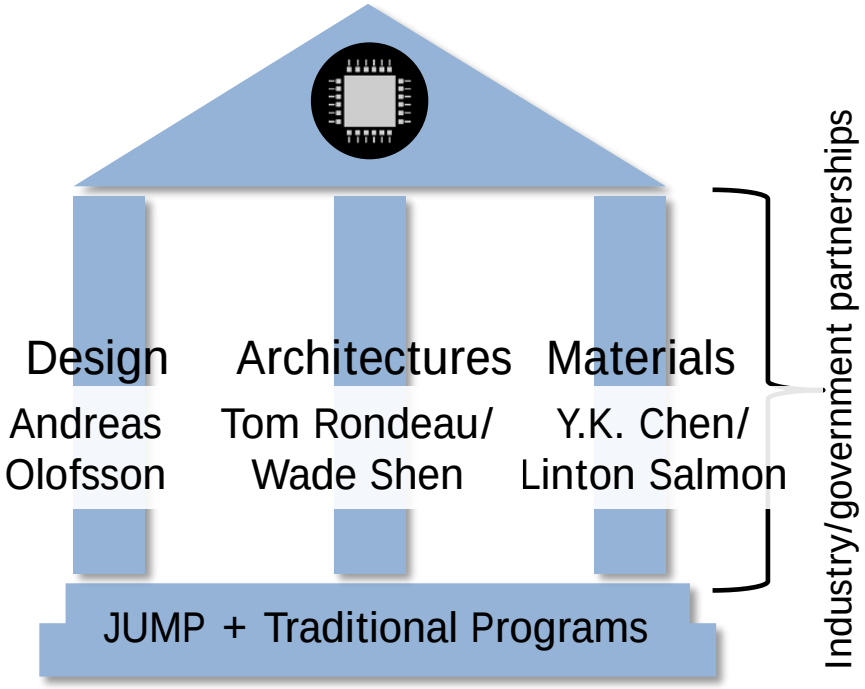
- "Supercomputing for everyone"
- $99 FPGA + 18 CPU cores @ 5W
- No NDAs!
- Open source and open access
- $900K raised in 30 days
- First ever crowd funded chip
- 10,000 boards shipped
- 100+ community publications

Open works!

Metric	Before	After	Boost
Customers	5	10,000	2000x
Universities	1	200	200x
Site traffic	20	1,000	50x
Twitter Followers	20	6,000	50x
Publications	2	150	75X
Govt customers	2	10	5x

Electronic Resurgence Initiative (ERI) Introduction

Electronics Resurgence Initiative: Introduction



$141M in Current Efforts (FY18)
$75M of New Page 3 Funding (FY18)

Page 3 Investments

- **Design**

How do we lower the design barrier to specialization?

- **Architectures**

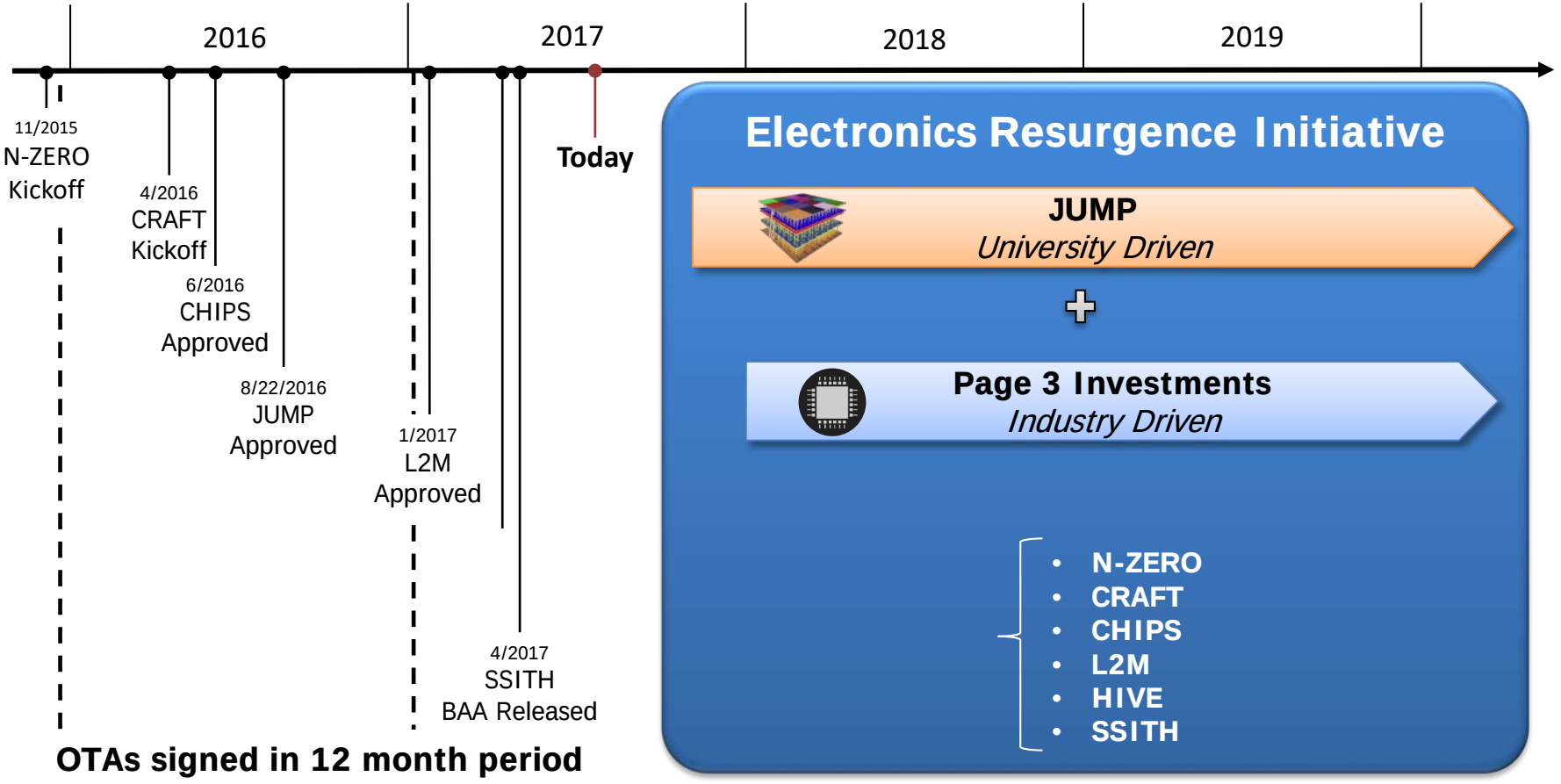
How do we manage the complexity of specialization with new architectures?

- **Materials**

How do we integrate new materials for specialized functions?

Resting on a foundation of existing research programs are newly formulated thrusts that all sum into the Electronics Research Initiative, a four-year push with anticipated annual investments in the $200 million range.

Recent DARPA investments and momentum



Intel Qualcomm Rambus XILINX Micron
Keysight Technologies
Cadence
NVIDIA
Flexlogix Technologies, Inc

ERI "Page 3" Program Service Announcement

Materials & Integration

- *Monolithic Integration of an SoC in Three Dimensions (3DSoC)*, Linton Salmon
- *Framework for Novel Compute (FRANC),* Y.K. Chen

Architecture:

- *Software Defined Hardware (SDH),* Wade Shen
- *Domain-Specific System on Chip (DSSoC),* Thomas Rondeau

Design

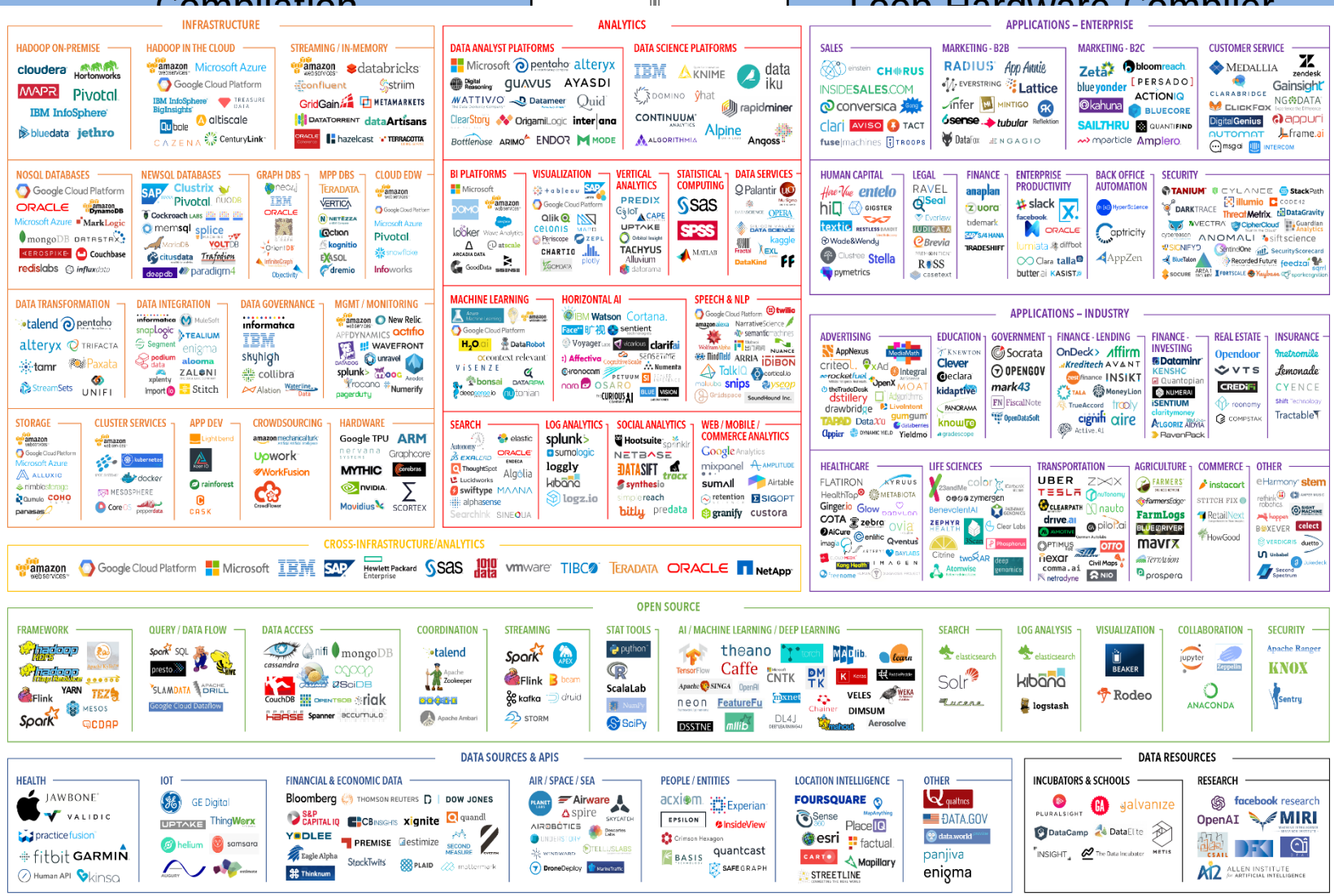
- *Intelligent Design of Electronic Assets (IDEA),* Andreas Olofsson
- *Posh Open Source Hardware (POSH),* Andreas Olofsson

Building a Hardware Compiler at DARPA

We are building a universal hardware compiler

Modern Software Compilation

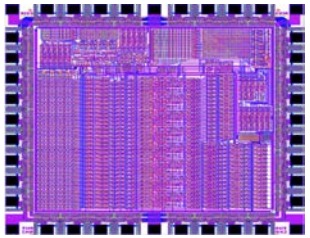
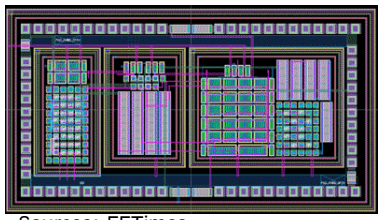
A Universal No Human In the Loop Hardware Compiler



Source: mattturck.com/bigdata2017

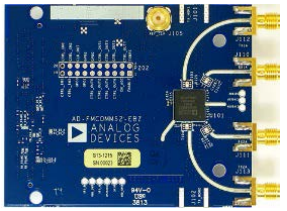
How is hardware compilation handled today?

Analog Design:
- Schematic input
- 1K-100K signals
- 100% EDA assisted manual labor
- 2-4 experts
- 3-18 months

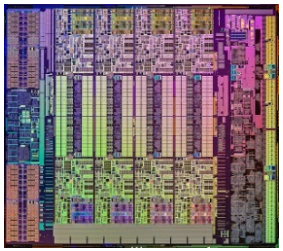
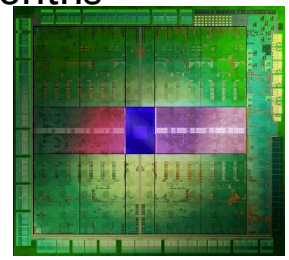
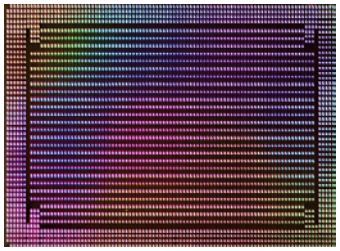
Sources: EETimes

Board Design:
- Schematic input
- 1-10K signals
- 100% EDA assisted manual labor
- 2-4 experts
- 3-6 months

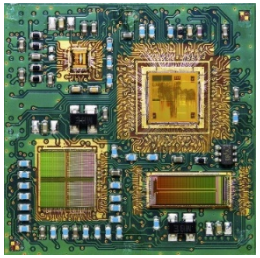
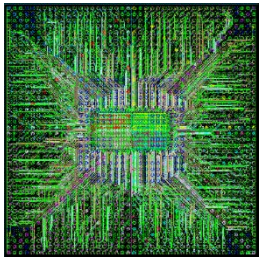
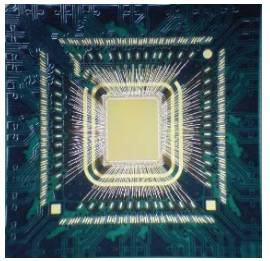

Sources: Analog Devices, Raspberry Pi

Digital Design:
- Verilog netlist input, constraints, scripts
- 10M-1B signals
- 99% automated place and route
- 1-100 experts
- 3-18 months

Sources: Intel, NVIDIA, Adapteva

Package Design
- Excel spreadsheet input
- 1K signals
- 100% manual labor
- 2-4 experts
- 2-8 weeks

Sources: Axis, Adapteva

Why now? What has changed?

Traditional Algorithmic EDA Research

1983

Optimization by Simulated Annealing

S. Kirkpatrick, C. D. Gelatt, Jr., M. P. Vecchi

with N, so that in practice exact solutions can be attempted only on problems involving a few hundred cities or less. The traveling salesman belongs to the large class of NP-complete (nondeterministic polynomial time complete) problems, which has received extensive study in the past 10 years (3). No method for exact solution with a computing effort bounded by a power of N has been found for any of these problems, but il

1987

An Intelligent Compiler SubSystem for a Silicon Compiler

David L. Johannsen
Steve K. Tsubota
Ken McElvain
3/27/87

1988

How to automate analog IC designs

Knowledge-based systems are relieving the labor-intensive bottlenecks usually associated with such building blocks as op amps and voltage reference

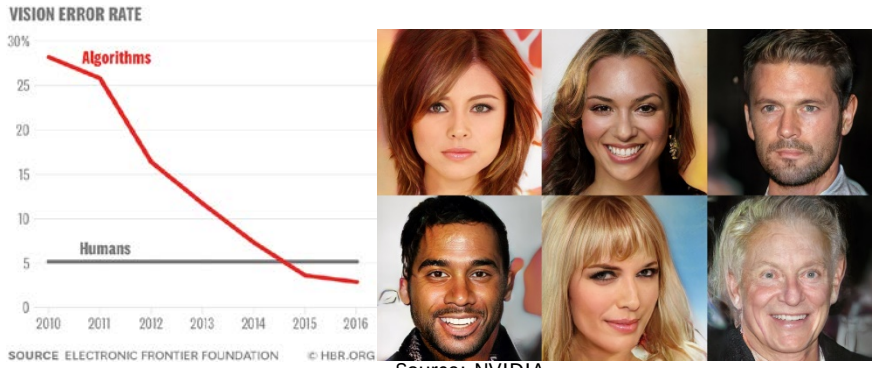
1993-2018 (stable evolutionary progress)
Optimization algorithms, Productivity & Integration

Cadence Synopsys Mentor Graphics

Ref-2003: The Tides of EDA, Alberto Sangiovanni-Vincentelli

A New Machine Learning Based EDA Approach

- ML Algorithm Innovations
- Data driven
- Massive compute (Moore's Law)
- Replacing existing heuristics/humans



Source: NVIDIA

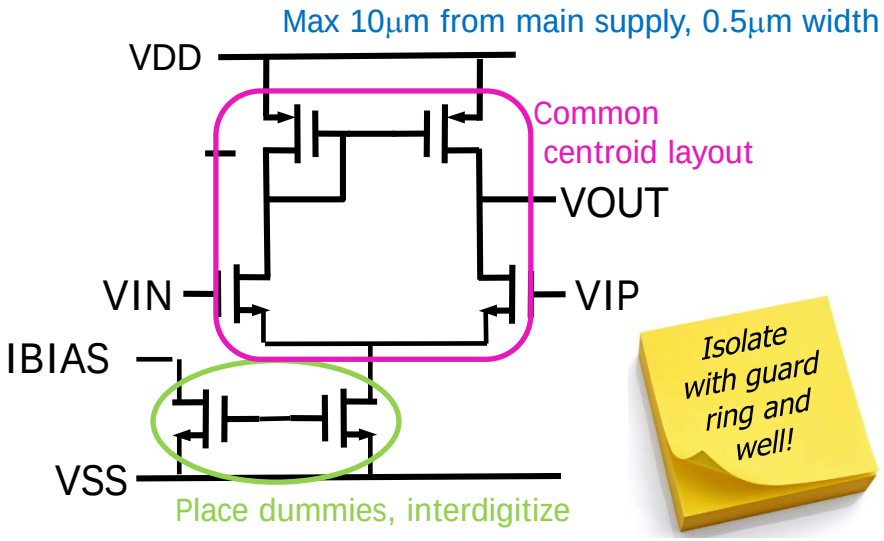
Source: DeepMind

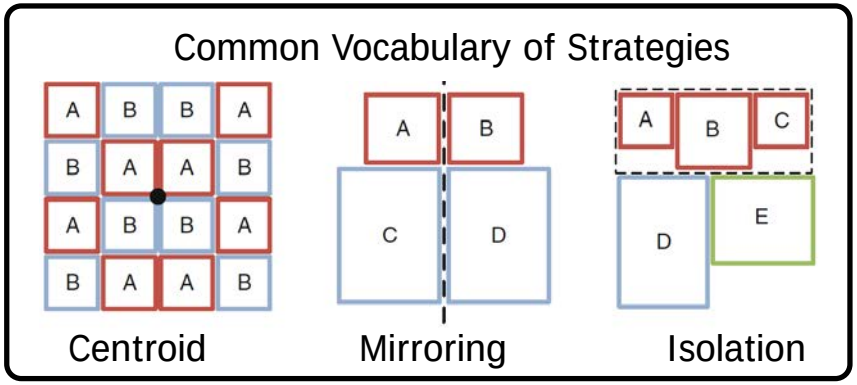
Can we map a layout cost function to ML?
Can we access/label enough quality data?

Why now? (how this approach is different)

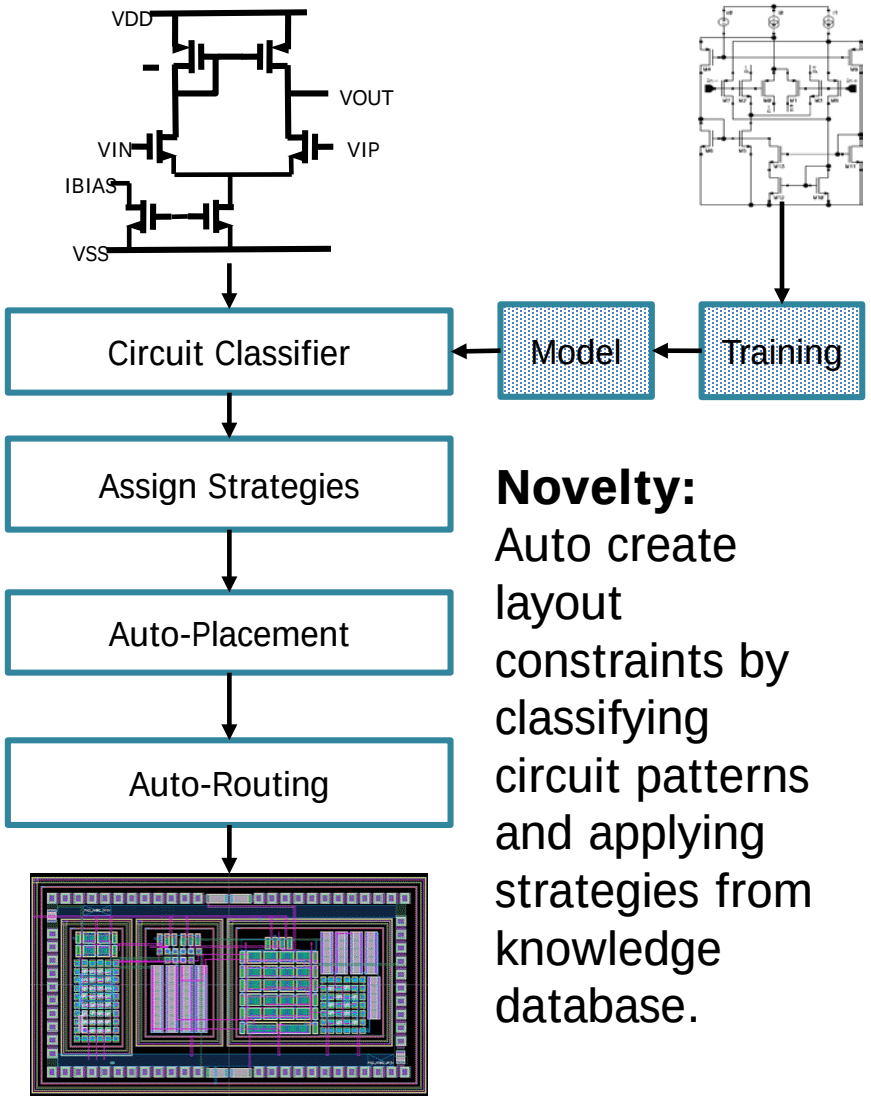
Today

Designer provides manual constraints to layout person (or EDA tool)





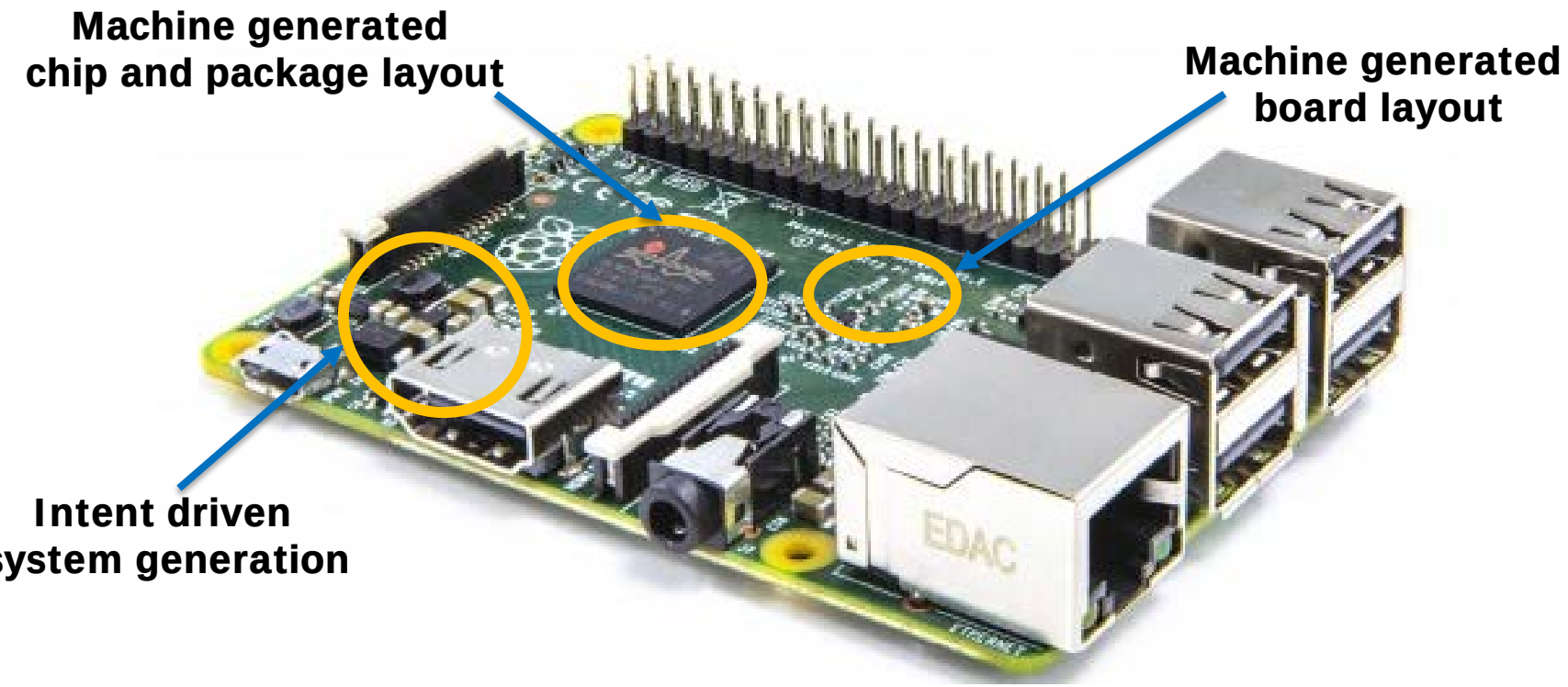
IDEA



Novelty: Auto create layout constraints by classifying circuit patterns and applying strategies from knowledge database.

Intelligent Design of Electronic Assets (IDEA)

IDEA Program Objective

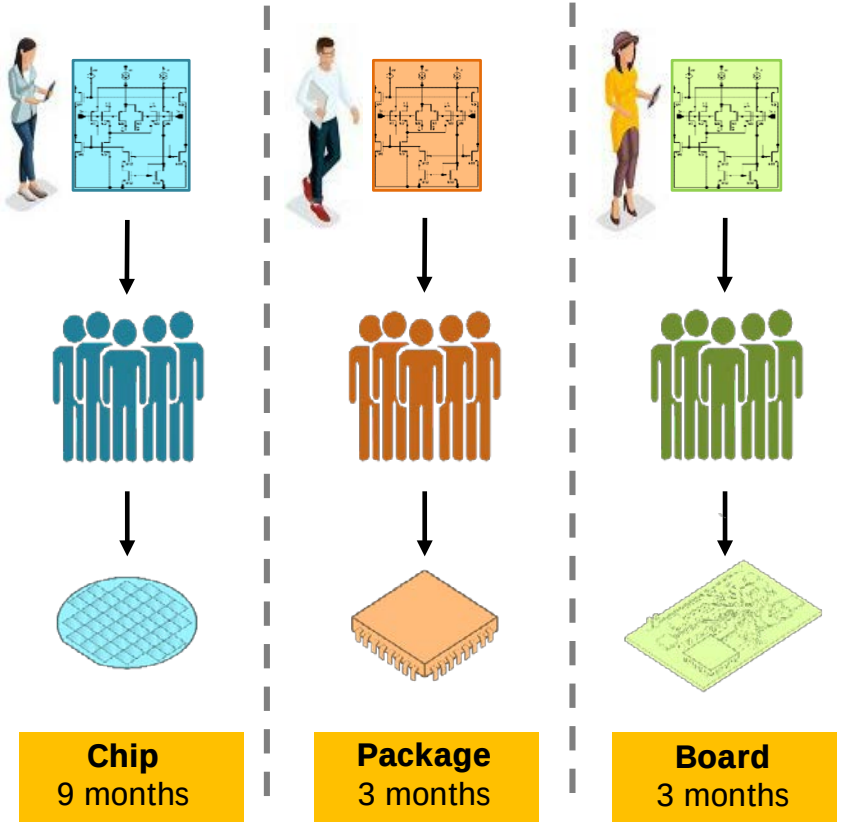


IDEA will create a no-human-in-the-loop hardware compiler for translating source code to layouts of System-On-Chips, System-In-Packages, and Printed Circuit Boards in less than 24 hours

Image source: Raspberry Pi

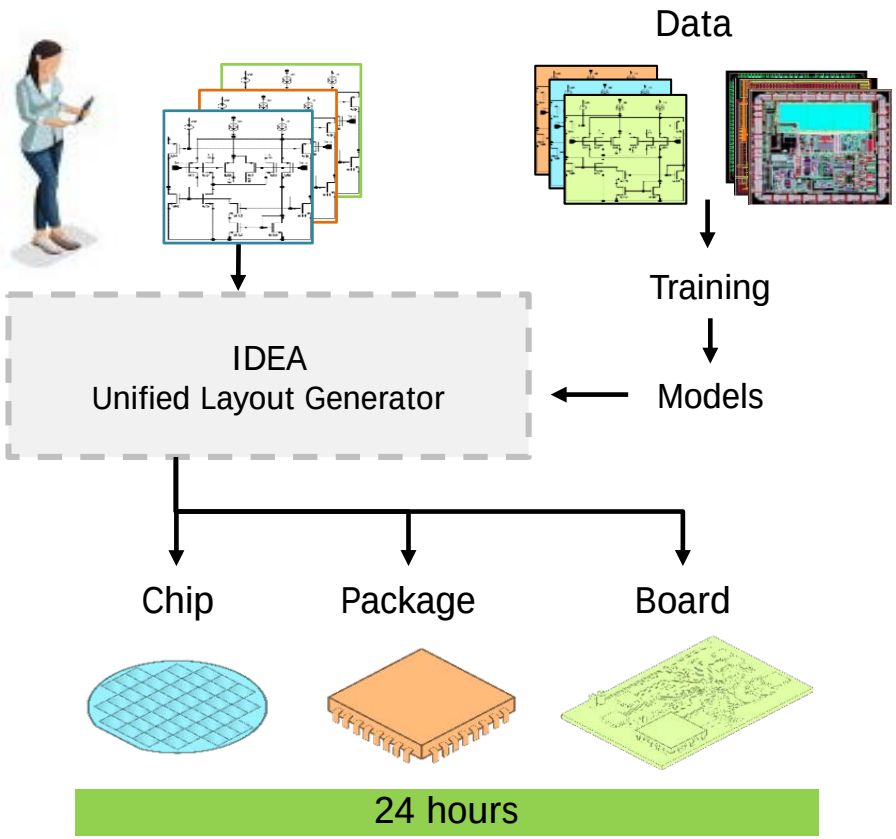
TA1: A unified electrical circuit layout generator

Today



- Knowledge embedded in humans
- Limited knowledge reuse
- Reliance on scarce resources

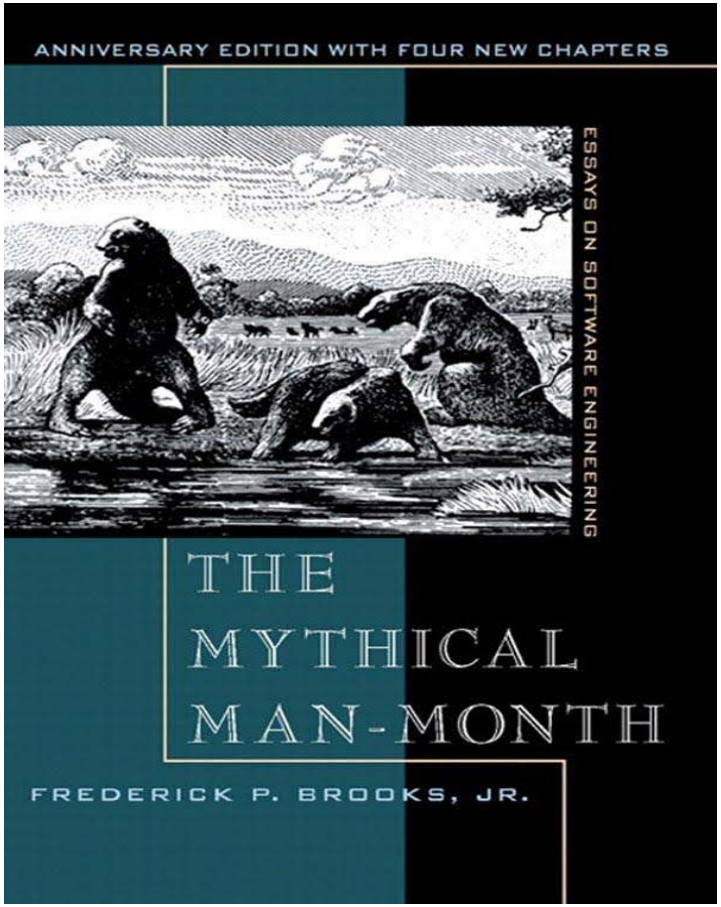
IDEA



- Knowledge embedded in software
- 100% automation
- 24 hour turnaround

Assessing IDEA Difficult Levels

- **Hard:**
  - Reinventing board/package design
  - Embedding knowledge in digital EDA tools
- **Harder:**
  - Making an EDA product
  - 24 hour turnaround time
- **Hardest:**
  - Robust fully autonomous analog layout



Source: Pearson InformIT

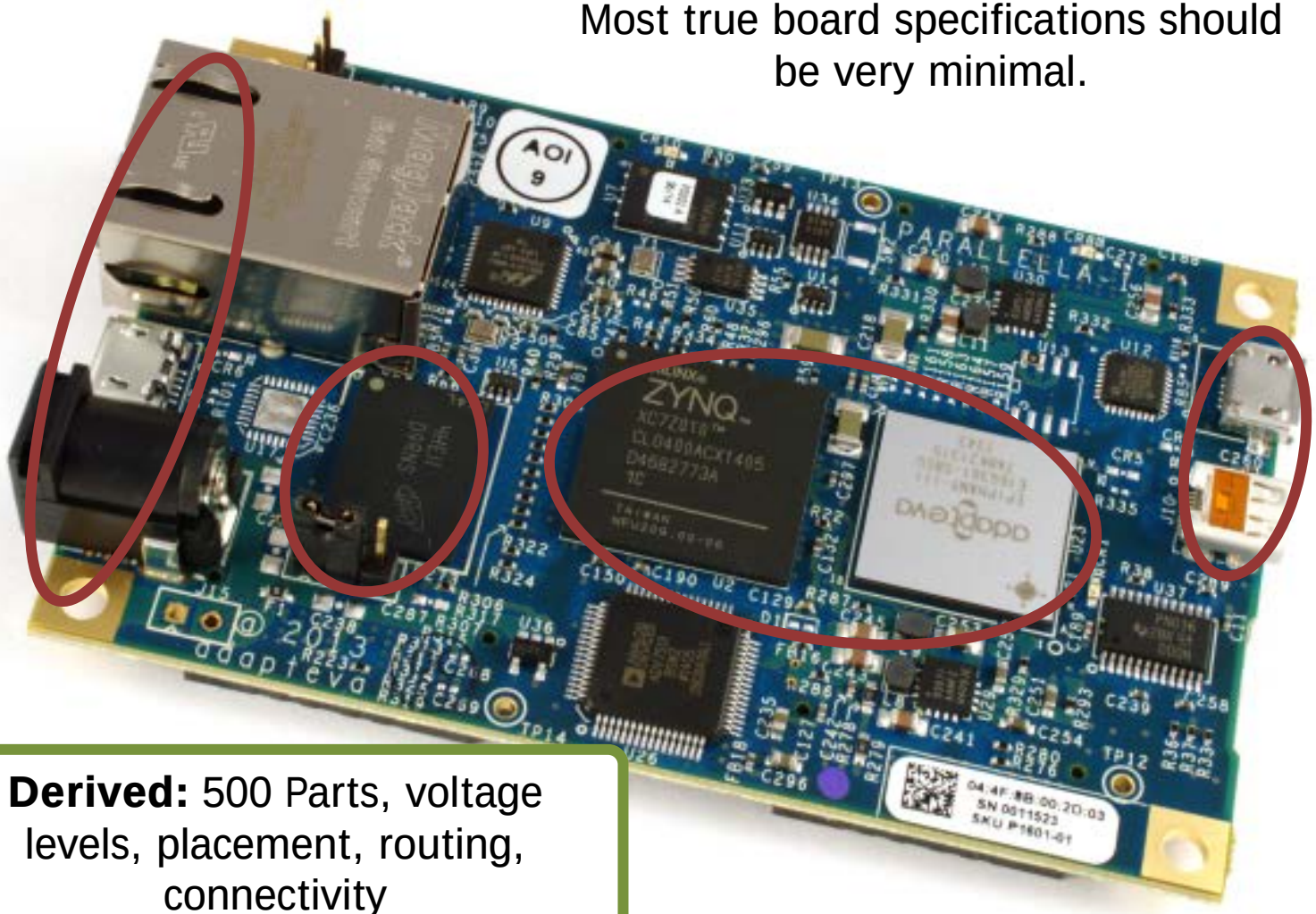
TA1: Metrics

Technical Area	Metrics	Phase 1	Phase 2
IDEA TA-1: Machine Generated Physical Layout	SoC Benchmarks	Government furnished benchmarks 14nm CMOS PDK	Government furnished benchmarks 7nm & 14nm CMOS PDK
	Board Benchmarks	BeagleBone Black[1]	Open Compute Server[2]
	SiP Benchmarks	Government furnished benchmarks	Government furnished benchmarks
	Benchmark $PPA_{IDEA}/PPA_{Traditional}$ (3)	0.5	1
	Package Complexity	Up to 2 die, 2.5D	Up to 1024 die, 2.5D
	Automation	100%	
	Turnaround time	24 hours	
	Deliverable	Software, license[4], software documentation	

TA2: Intent Driven Synthesis

True Specs:
5V
Ethernet
USB
HDMI
1GB RAM
128MB Flash
FPGPA
20 GFLOPS
ARM A9

Intent: Specify what, not how! Most true board specifications should be very minimal.



Derived: 500 Parts, voltage levels, placement, routing, connectivity

Image source: Adapteva

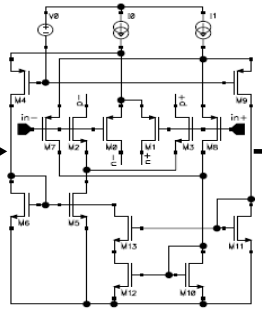
TA2: Reinventing Board Development

Today

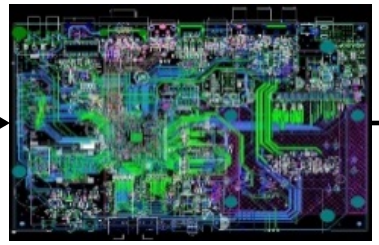
Manual Part Selection

Google

Manual Schematic



Manual Layout

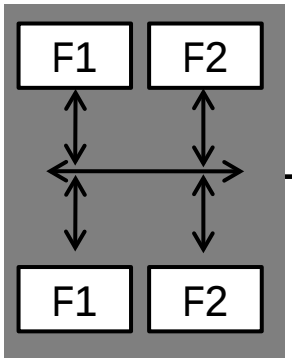


Source: Raspberry Pi

- 100% Manual
- Error prone
- Rarely optimal

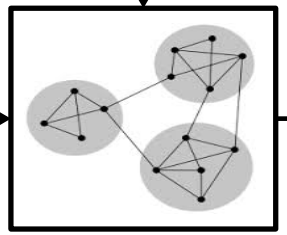
IDEA

Intent

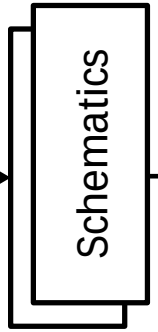


Inexact Description

System Generator



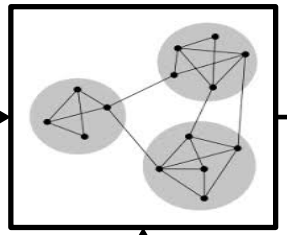
Open Parts DB

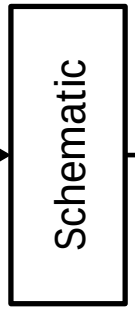


Potential Solutions

Pruning

Goal Optimizer





Layout Generator

New Concept: Machine synthesized board from intent and open COTS parts library.

TA2: An Open 5M+ Component IC Database

Today


TPS65218

TPS65218x Power Management for ARM® Cortex™-A8/A9 SOCs and FPGA

1 Features

- Two Low-Quiescent Current, High Efficiency Step-Down Converters for Battery Backup Domain
  - DCDC5: 1.0 V Output
  - DCDC6: 1.8 V Output
  - VIN Range from 2.2 to 5.5 V
  - Supplied from System Power or Coin-Cell Backup Battery
- Three Adjustable Step-Down Converters With Integrated Switching FETs:
  - DCDC1: 1.1 V Default up to 1.8 A
  - DCDC2: 1.1 V Default up to 1.8 A
  - DCDC3: 1.2 V Default up to 1.8 A
  - VIN Range from 2.7 to 5.5 V
  - Adjustable Output Voltage Range 0.85 to 3.5 V
  - Power Save Mode at Light Load Current
  - 100% Duty Cycle for Lowest Dropout
  - Active Output-Discharge When Disabled
- One Adjustable Buck-Boost Converter With Integrated Switching FETs:
  - DCDC4: 3.3 V Default up to 1.0 A
  - VIN Range from 2.7 to 5.5 V
  - Adjustable Output Voltage Range 0.85 to 3.4 V
  - Active Output-Discharge When Disabled
- Adjustable General-Purpose LDO (LDO1)
  - LDO1: 1.8 V Default up to 400 mA
  - VIN Range from 1.8 to 5.5 V
  - Adjustable Output Voltage Range from 0.9 to 3.4 V
  - Active Output-Discharge When Disabled
- 5-V Load Switch With 100-mA/ 500-mA Selectable Current Limit
  - VIN Range From 3.0 to 5.5 V
  - 500 mΩ (Max) Switch Impedance at 5 V
- Low Voltage Load Switch With 350-mA Current Limit
  - VIN Range From 1.2 to 3.6 V
  - 110 mΩ (Max) Switch Impedance at 1.35 V
- High Voltage Load Switch (LS3) With 100-mA/ 500-mA Selectable Current Limit
  - VIN Range from 1.8 to 10.0 V
  - 500 mΩ (Max) Switch Impedance
- Supervisor With Built-in Supervisor Function Monitors
- Protection, Diagnostics, and Control:
  - Undervoltage Lockout (UVLO)

XILINX

Zynq-7000 All Programmable SoC (Z-7030, Z-7035, Z-7045, and Z-7100): DC and AC Switching Characteristics

DS191 (v1.18) April 12, 2017 — Product Specification

Introduction

The Zynq®-7000 All Programmable SoCs are available in -3, -2, -2LI, -1, and -1LQ speed grades, with -3 having the highest performance. The -2LI devices operate at programmable logic (PL) V_{CCINT}/V_{CCBRAM} = 0.95V and are screened for lower maximum static power. The speed specification of a -2LI device is the same as that of a -2 device. The -1LQ devices operate at [illegible] and speed as the -1Q devices and are s[illegible] power. Zynq-7000 device DC and AC ch[illegible] specified in commercial, extended, indus[illegible] expanded (0-temp) temperature ranges[illegible] operating temperature range or unless o[illegible] the DC and AC electrical parameters are[illegible] particular speed grade (that is, the timing[illegible] a -1 speed grade industrial device are th[illegible] speed grade commercial device). Howe[illegible] speed grades and/or devices are availabl[illegible] commercial, extended, or industrial temp[illegible]

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

The available device/package combinations are outlined in:

DC Characteristics

Table 1: Absolute Maximum Ratings[illegible]

Symbol	
Processing System (PS)	
V_{CCPINT}	PS internal logic supply v[illegible]
V_{CCPAUX}	PS auxiliary supply voltag[illegible]
V_{CCPLL}	PS PLL supply
V_{CCO_DDR}	PS DDR I/O supply
V_{CCO_MIO}[2]	PS MIO I/O supply
V_{REF}	PS input reference voltag[illegible]
V_{MIN} [3][4][5][6]	PS MIO I/O input voltage
	PS DDR I/O input voltage
Programmable Logic (PL)	
V_{CCINT}	PL internal supply voltage
V_{CCBRAM}	PL supply voltage for the I
V_{CCAUX}	PL auxiliary supply voltag[illegible]
V_{CCO}	PL output drivers supply v[illegible]
V_{CCO}	PL output drivers supply v[illegible]
V_{CCAUX_IO}[2]	Auxiliary supply voltage

DS191 (v1.18) April 12, 2017

Product Specification

ANALOG DEVICES

RF Agile Transceiver

Data Sheet AD9361

FEATURES

[illegible]

APPLICATIONS

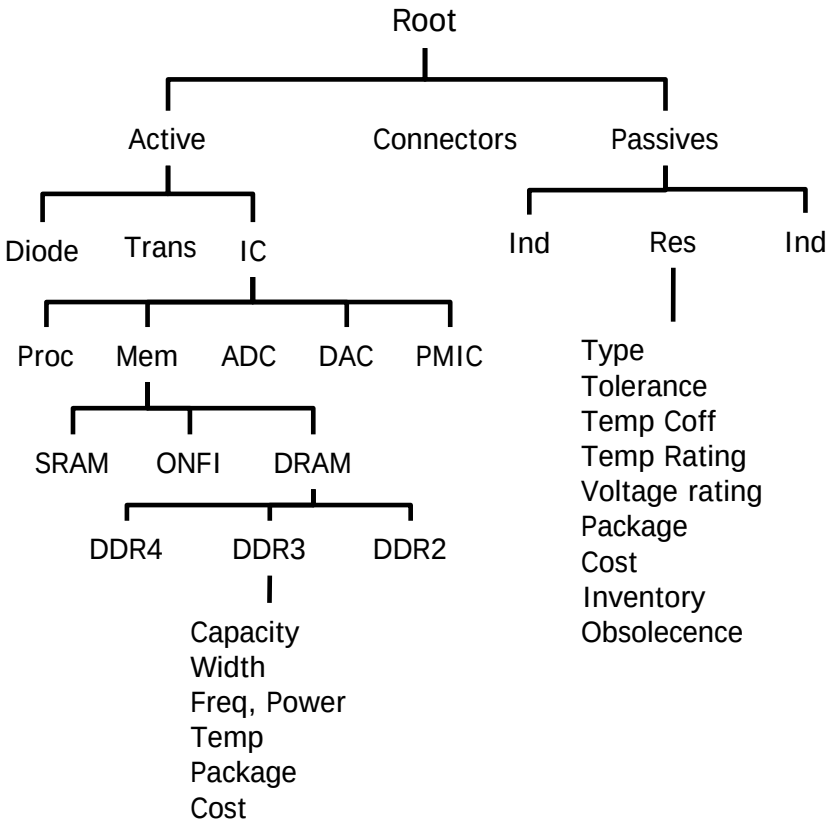
[illegible]

GENERAL DESCRIPTION

[illegible]

FUNCTIONAL BLOCK DIAGRAM

IDEA



- 5M+ parts in circulation
- Information embedded in datasheets and reference designs
- No standard models
- Automatic optimization not possible

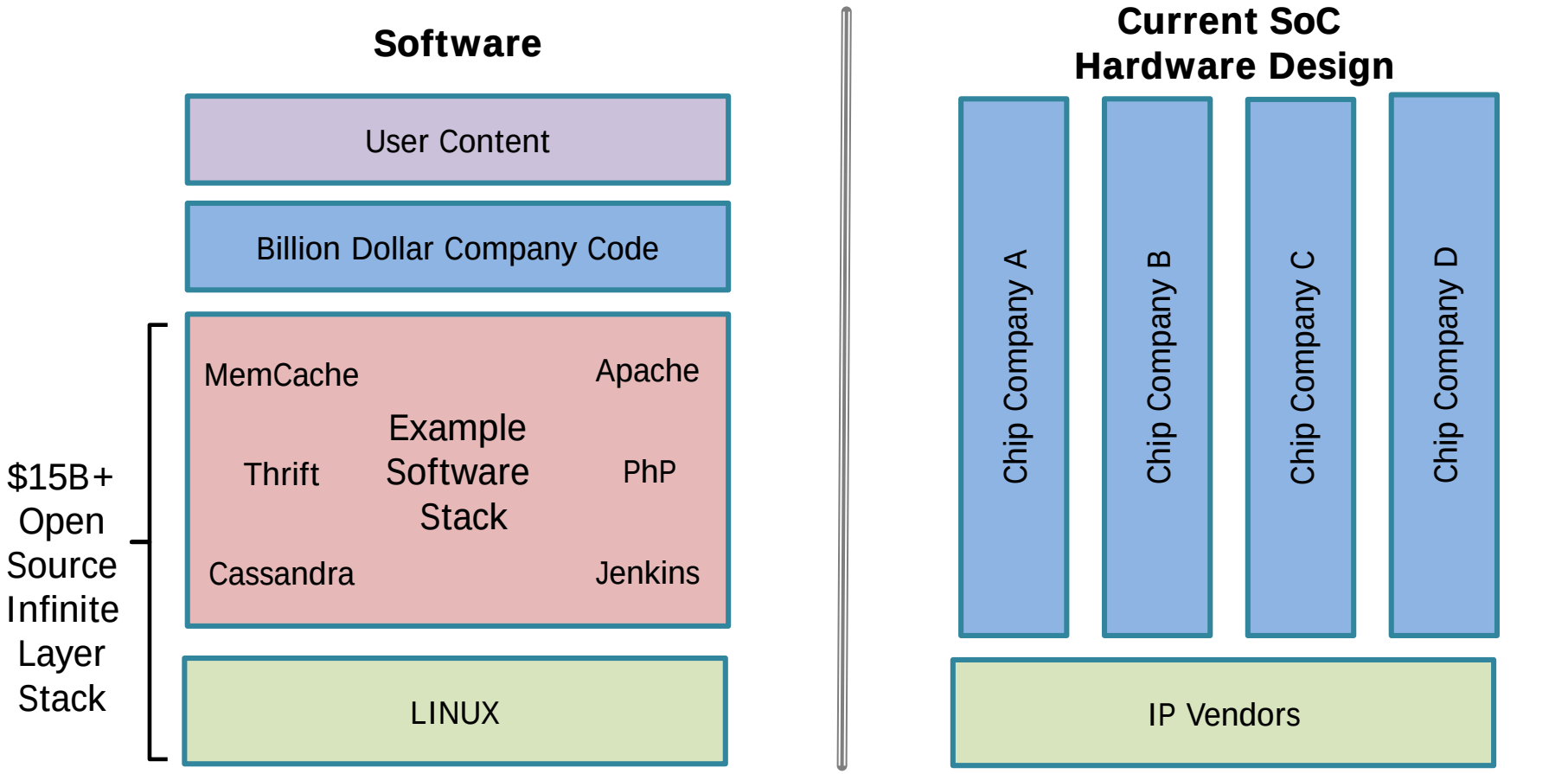
- IC standard models (LEF,LIB,IP-XACT)
- Extend standards for boards / SIPs
- Creation of 5M+ part DB
- Model all properties needed for constraint based system optimization

TA2: Metrics

Technical Area	Metrics	Phase 1	Phase 2
TA–2: Intent Driven System Synthesis	SoC Benchmark	SoC with 10 IPs	SoC with 100 IPs
	PCB Benchmark	BeagleBone Black	Open Compute Board
	SiP Benchmark	Establish pathway to SiP generation	Demonstrated fully automated layout of SiPs with >100 chiplets and >100,000 nets
	Benchmark $PPA_{IDEA}/PPA_{Traditional}$ (3)	0.5	1
	Automation	100%	
	Turn around time	24 hours	
	Deliverable	Software, license[4], documentation	

Posh Open Source Hardware **(POSH)**

Reinventing the Hardware IP Stack



POSH will create a viable open source hardware design and verification ecosystem that enables cost effective design of ultra-complex SoCs.

How is Hardware Different from Software?

	Software	Hardware
Programmers	Millions	Thousands
Writing Code	Easy	Hard
Reading Code	Hard	Very hard
Debugging	Hard	Near impossible
Cost of bugs	Low	Very high

What technologies are needed to make open source hardware viable?

The State of Open Source Hardware

Open Cores

GitHub

RISC-V

Open Compute Project

FOSSi Foundation

Still a long way to go!

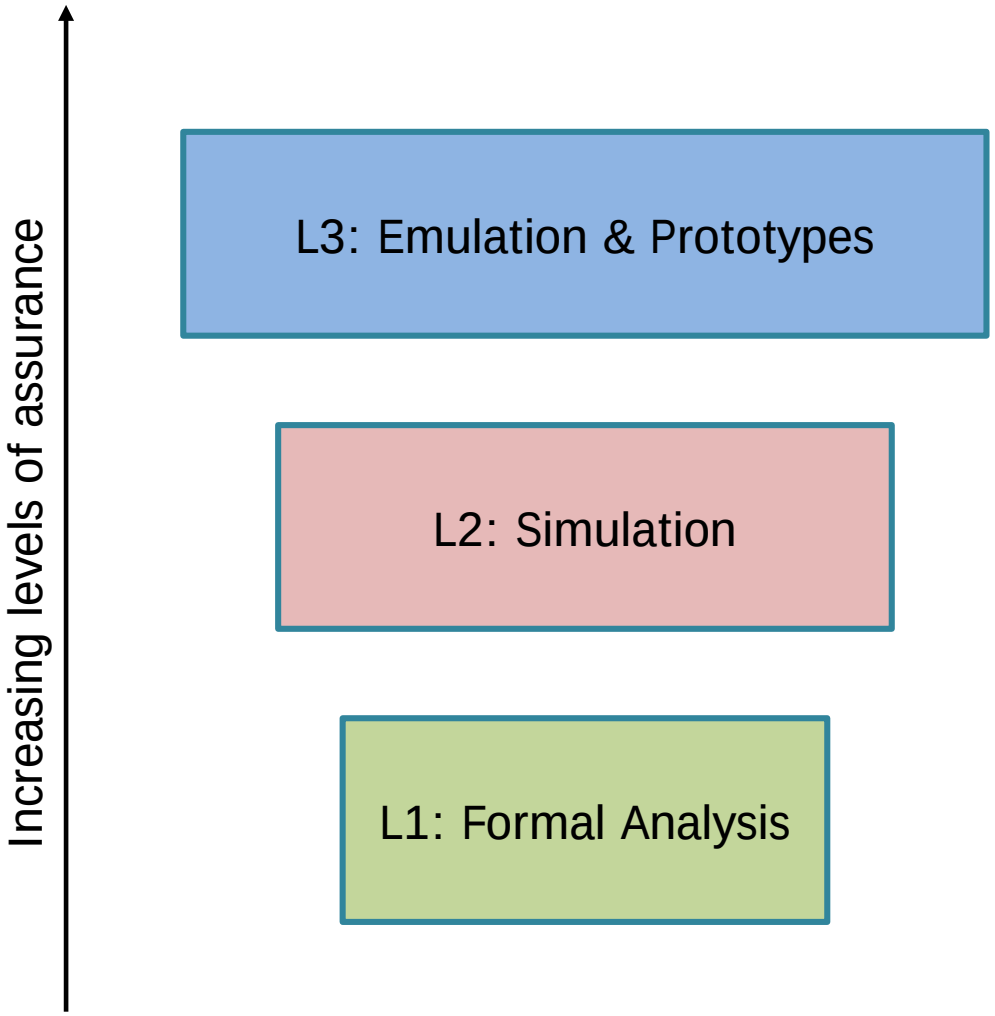
Sources: RISC-V, Open Compute, FOSSi, GitHub, OpenCores

POSH Program Structure

- **TA-1: Hardware Assurance Technology:** Development of hardware assurance technology appropriate for signoff quality validation of deeply hierarchical analog and digital circuits of unknown origin.
-
- **TA-2: Open Source Hardware Technology:** Development of design methods, standards, and critical IP components needed to kick-start a viable open source SoC eco-system.
-
- **TA-3: Open Source System-On-Chip Demonstration:** Demonstration of open source hardware viability through the design of a state of the art open source System-On-Chip.

TA1: Hardware Assurance Technology

Level	Description
L3	Accessible open API hardware emulation and prototyping platforms
L2	Scalable open API mixed accuracy simulation tools
L1	Formal tools for assessing relative and absolute quality of hardware library modules.



TA1: Hardware Example Metrics

- "Zero" engineering effort formal proofs of security, power, functionality properties for 1 billion transistor designs.
- 1MHz cycle-accurate simulation speed of a 1 billion transistor design.
- Demonstration of open source framework that automatically partitions large system simulations across hardware emulation, prototyping, cycle accurate simulation, and QEMU style software emulation resources.

TA2: Open Source Technology

Digital Circuit IP Blocks
FPGA Fabric
Multi-core 64-bit RISC-V processor sub-system
GPU (OpenGL ES 3.0)
PCI Express Controller
Ethernet Controller
Memory Controllers
USB 3.0 Controller
MIPI Camera Serial Interface controller
CPU Subsystem
H264 encoder/decoder
AES256 encrypt/decrypt
SHA-2/SHA-3 accelerator
Secure Digital Controller
High Definition Multimedia Interface
Serial ATA Controller
JESD204B Controller
NAND Flash Controller
CAN Controller

Mixed Signal Circuit IP Blocks	Description
Standard I/O interfaces PHYs	DDR, PCIe, SATA, USB, XAUI, CPRI
PLL	Range: 10MHz – 10GHz
DLL	Range: 10Mhz – 10GHz
Analog to Digital Converters	Range: 1 – 10,000 MSPS
Digital to Analog Converters	Range: 1 – 10,000 MSPS
Voltage Regulators	Input: 1.8V – 12V, Output 0.25V – 1.8V
Monitor circuits	Temperature, voltage, process

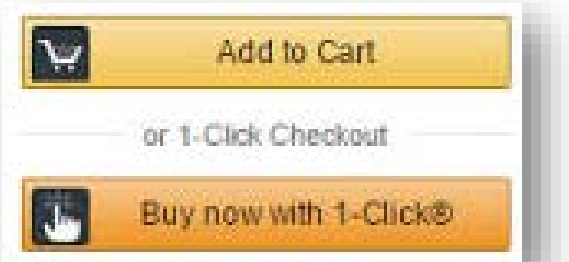
How can we cost effectively develop and maintain a high quality catalog of portable open source digital and analog components?

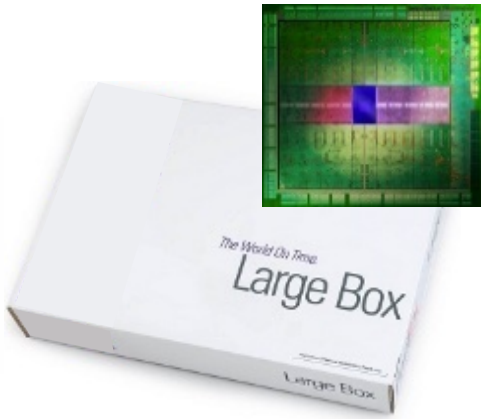
www.darpa.mil

Conclusion

IDEA/POSH End State – A Universal Hardware Compiler

```
$ git clone https://github.com/darpa/idea
$ git clone https://github.com/darpa/posh
$ cd posh
$ make soc42
```





IDEA/POSH Societal Implications