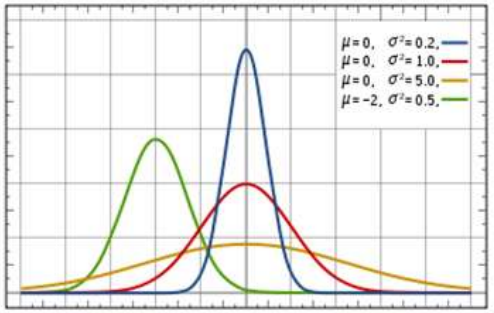

TAU 2013 Variation Aware Timing Analysis Contest

Debjit Sinha[1], Luís Guerra e Silva[2], Jia Wang[3], Shesha Raghunathan[4], Dileep Netrabile[5], and Ahmed Shebaita[6]

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[3]Illinois Institute of Technology, Chicago, USA

[4]IBM Systems and Technology Group, Bangalore, India

[6]Synopsys, Sunnyvale, USA

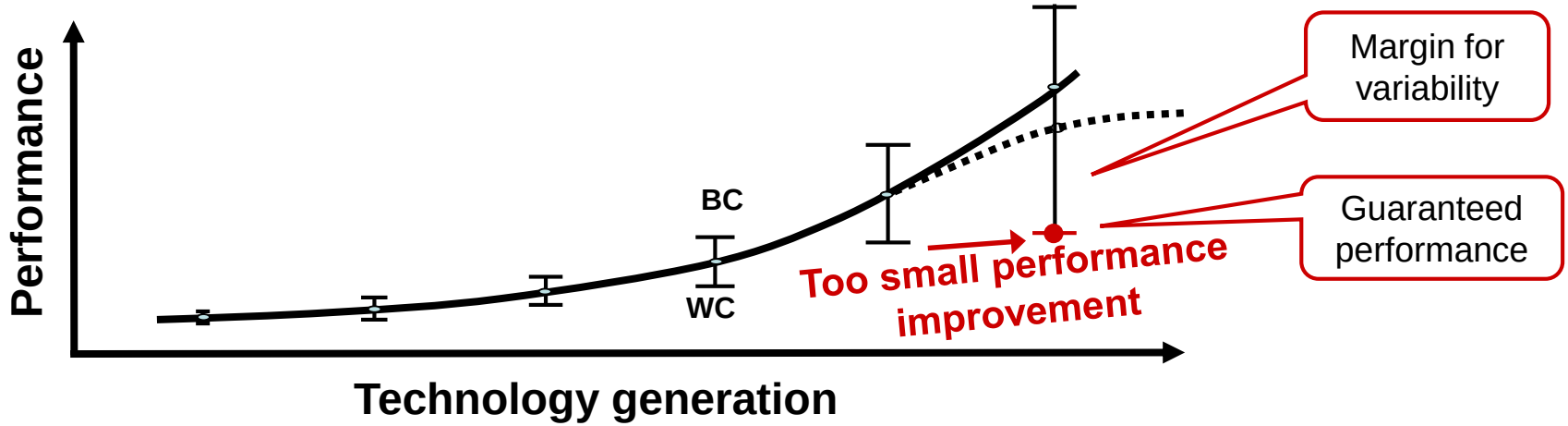
TAU/ISPD joint session, Stateline, NV – March 26, 2013

TAU Sponsors:

Variation aware timing

- Timing analysis key component of chip design closure flow
  - Pre/post route optimization, timing sign-off

- Increasing significance of variability



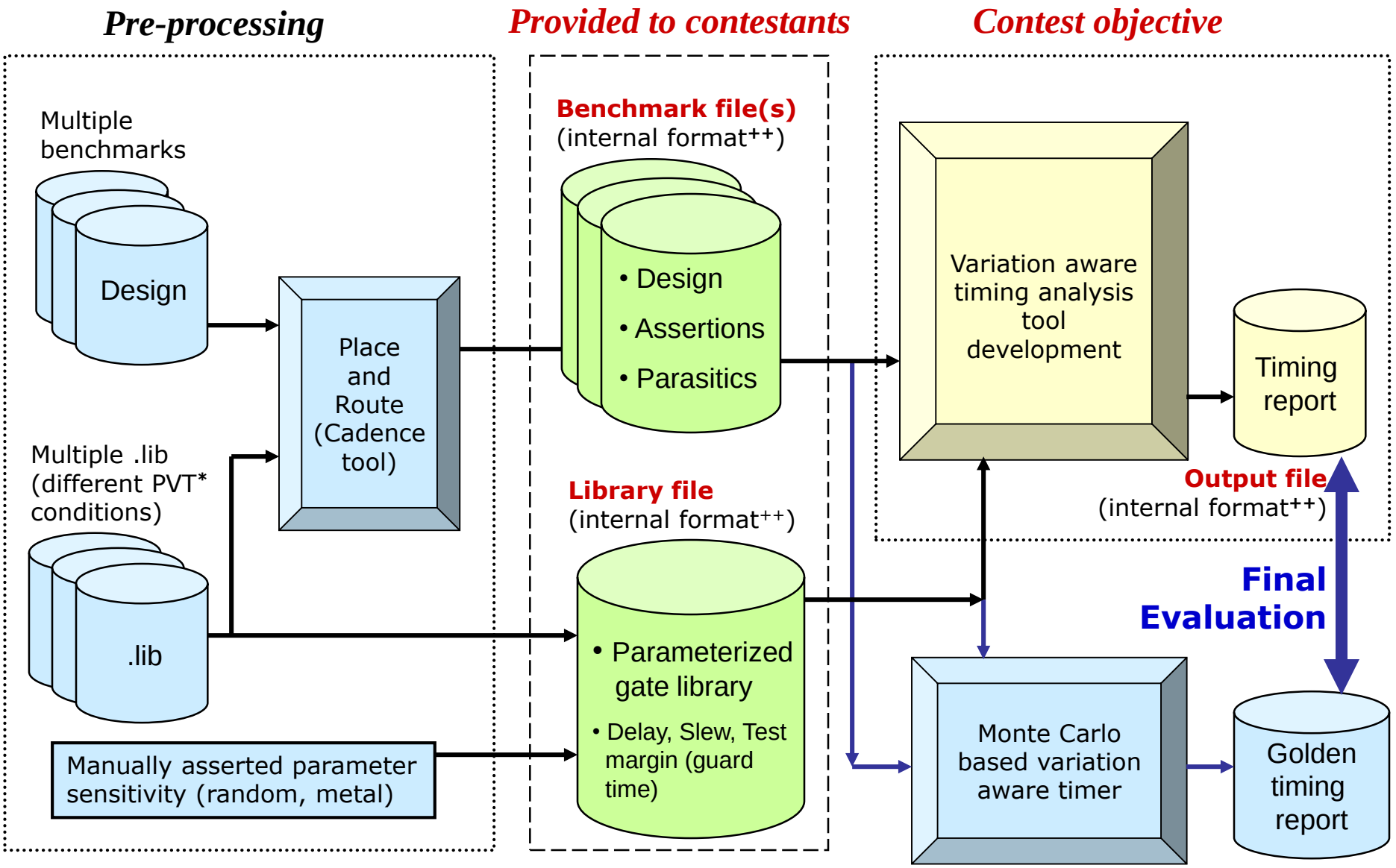
- Variability aware timing analysis essential
  - Growing chip sizes, complexity: Impacts timing analysis run-time
  - Trade-offs between modeling accuracy/complexity and run-time

TAU 2013 variation aware timing analysis contest

- Goal: Seek novel ideas for fast, variation aware timing analysis by means of the following
  - Increase awareness of variation aware timing analysis, provide insight into some challenging aspects
  - Encourage novel parallelization techniques (including multi-threading)
  - Facilitate creation of a publicly available variation aware timing analysis framework and benchmarks for research/future contests

- Trade-offs for timing model complexity
  - Wanted focus on variation aware timing, understanding challenges for variation aware timing, tool performance
    - Feedback from prior contest committee: Teams spend too much time on infrastructure (e.g., parsers, fixing library/benchmark file bugs)
  - Chose to expand on single corner timing analysis contest from

Timing analysis contest architecture



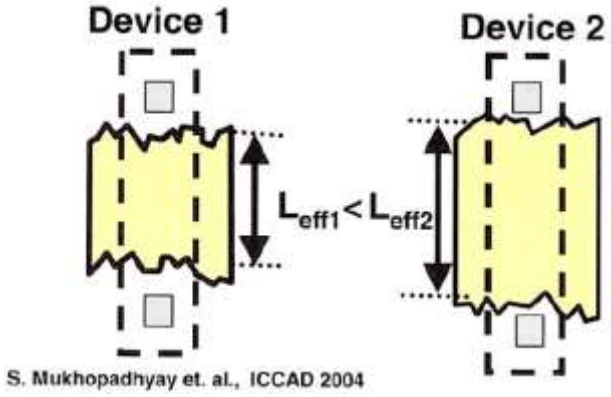
*PVT – Process, Voltage, Temperature

++Format identical/extension to/of PATMOS'11 contest

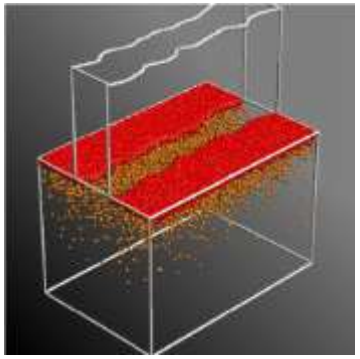
Sources of variability (**Parameters**)

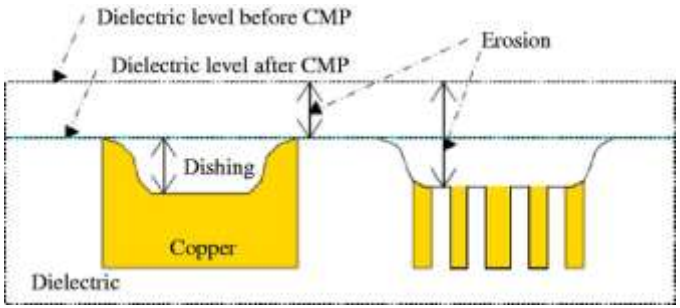
- Six global (inter-chip) sources of variability
  - Environmental: Voltage (**V**), Temperature (**T**)
  - Front end of line process: Channel length (**L**), Device width (**W**), Voltage threshold (**H**)
  - Back end of line process: Metal (**M**)
    - All metal layers assumed perfectly correlated

- Random variability (**R**)
  - Intra-chip (across chip) systematic variability ignored



S. Mukhopadhyay et. al., ICCAD 2004


M Hane et al., SISPAD 2003



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Variability modeling

- Parametric linear model*

$$\mu + a_v \Delta V + a_t \Delta T + a_l \Delta L + a_w \Delta W + a_h \Delta H + a_m \Delta M + a_r \Delta R$$

  - Each parameter ($\Delta V, \Delta T, \ldots, \Delta R$) assumed as unit normal Gaussian
  - Each sensitivity ($a_v, a_t, \ldots, a_r$) denotes first-order per-sigma sensitivity
  - Parameter may vary between [-3, 3] sigmas

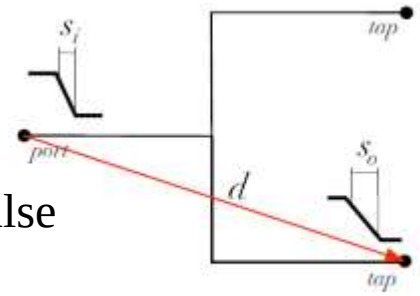
- Encouraged novel variability aware timing analysis techniques
  - **Statistical timing** [Fewer runs, pessimism relief for random variability, *modeling inaccuracies/simplifications*]
  - **Multi-corner timing** [Less complexity, faster analysis and potentially more accurate at each corner, *large number of corners, pessimistic for random variability*]
  - **Monte Carlo based timing** [Less complexity, most accurate, *very long run-times*]
    - Golden timer's approach: Used for accuracy evaluations only
  - **Hybrid/novel approach for variability aware timing** [?]

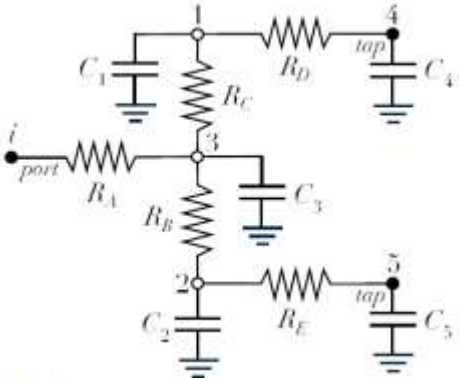
*non-linear with parametric slews

Interconnect (wire) modeling

- Interconnects modeled as resistance capacitance (RC) network
  - Single source (port), one or more sinks (taps)
  - No coupling capacitances, no grounded resistances

- Single corner timing model
  - Elmore delay model
    - First moment value of impulse response





Single corner delay from port to tap *5*:

$$d_5 = R_A(C_1+C_3+C_4)+(R_A+R_B)\,C_2+(R_A+R_B+R_E)\,C_5$$

  - Multi step output slew computation
    - Combination of input (port) slew, delay, and second moment value of impulse response – Introduces non-linearity [Kashyap *et al.*, TCAD'04]

$$s_o = \sqrt{s_i^2 + (2\beta_o - d_o^2)}$$

Output slew — Input slew — Elmore delay — Second moment value of impulse response

Interconnect (wire) modeling considering variability

- Wire parasitics (RC values) function of metal parameter (ΔM)
  - Provided sigma (corner) specific scale factors for parasitics
  - Tap capacitance contribution from gate input pin unaffected
  - Parametric input slew
- Parametric wire delay and output-slew
  - First order sensitivity to metal and other parameters may be computed via model-fitting (e.g. finite-differencing) for a statistical timer
  - Complex parametric output slew computation

Corner delay at nominal metal corner (0 sigma):

$$d_5 = R_A(C_1+C_3+C_4)+(R_A+R_B)\,C_2+(R_A+R_B+R_E)\,C_5$$

Corner delay at "thick" metal corner (σ sigma):

Tap gate pin cap

$$\begin{aligned} d_{5|\Delta M=\sigma} \;=\; & m_R^\sigma R_A(m_C^\sigma[C_1+C_3+C_4-C_{p,4}]+C_{p,4})+ \\ & (m_R^\sigma[R_A+R_B+R_E])\;(C_{p,5}+m_C^\sigma(C_5-C_{p,5})) \\ & +(m_R^\sigma[R_A+R_B])\;m_C^\sigma C_2 \end{aligned}$$

Corner specific scale factors

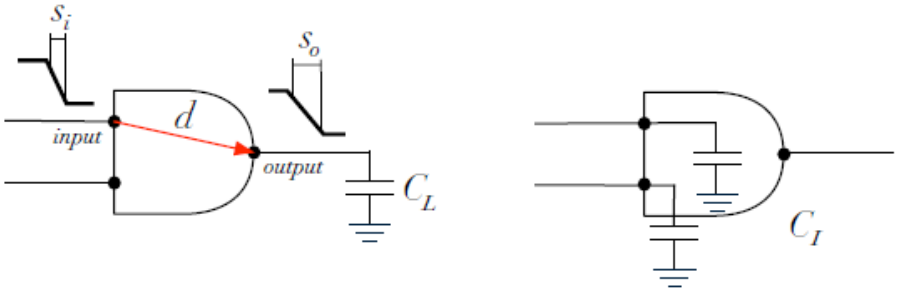
First order metal sensitivity:

$$\alpha^D_{m,5} = \frac{d_{5|\Delta M=\sigma} - d_{5|\Delta M=0}}{\sigma - 0}$$

Parametric wire delav:

$$d_5 + \alpha^D_{m,5}\Delta M$$

Combinational gate (cell) modeling



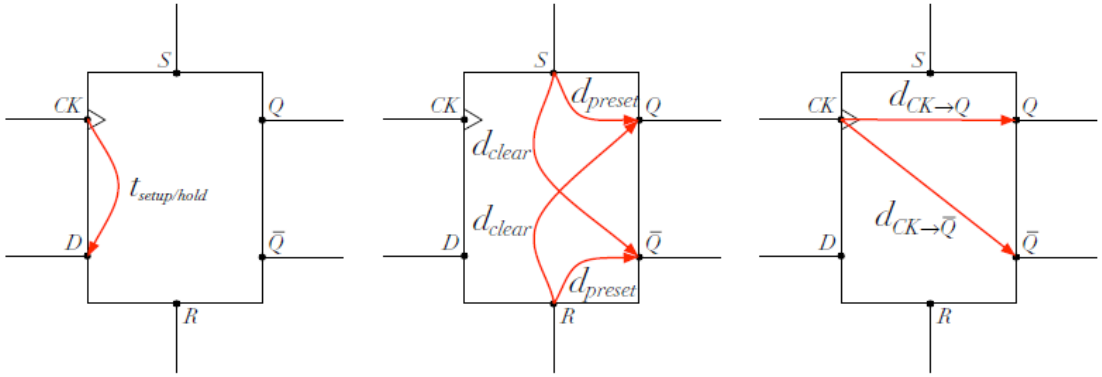
- Extended linear gate delay/slew model from PATMOS'11 contest to variation aware model

$$D = a\,(1 + k_{d,v}\,\Delta V + k_{d,t}\,\Delta T + k_{d,l}\,\Delta L + k_{d,w}\,\Delta W + k_{d,h}\,\Delta H + k_{d,r}\,\Delta R) + b\,C_L + c\,S_i$$

$$S_o = x\,(1 + k_{s,v}\,\Delta V + k_{s,t}\,\Delta T + k_{s,l}\,\Delta L + k_{s,w}\,\Delta W + k_{s,h}\,\Delta H + k_{s,r}\,\Delta R) + y\,C_L + z\,S_i$$

  - Sensitivities (*to parameters, input slew, load)* provided in gate library
  - Lumped load model (no effective Capacitance/current source models)
  - Note: Input slew (S_i) and load (C_L) are parametric models

Sequential gate (flip-flop) modeling



- Test (Setup/hold) margin or guard-times a linear function of slews at clock and data points

$$t_{setup} = g + h\, S_i^{CK} + j\, S_i^{D}$$

$$t_{hold} = m + n\, S_i^{CK} + p\, S_i^{D}$$

  - Sensitivities (*to input slews)* provided in gate library
  - Parametric slews → Parametric guard-time

Parametric timing analysis

- Traditional timing analysis/propagation
  - Forward propagation of signal arrival times (***at***), and ***slews***
  - Backward propagation of signal required arrival times (***rat***)
  - ***Slack*** computation
- Nuances
  - Worst slew propagation (when 2+ signals meet at a point)
  - Separate propagation for early, late modes, and rise, fall transitions
    - Needs ***maximum, minimum*** operations on parametric quantities
    - Could be expensive for statistical timing, inaccuracy concerns
  - Single clock domain
  - No coupling, common path pessimism reduction, loops

Projection techniques and tool output

- Projection of parametric values: 3 modes required for contest

$$\mu + a_v \Delta V + a_t \Delta T + a_l \Delta L + a_w \Delta W + a_h \Delta H + a_m \Delta M + a_r \Delta R$$

  - **MEAN**: Nominal value (μ)
  - **SIGMA_ONLY**: Standard deviation ($\sqrt{a_v^2 + a_t^2 + a_l^2 + a_w^2 + a_h^2 + a_m^2 + a_r^2}$)
  - **WORST_CASE**: Worst 3 sigma projection of metal parameter, random parameter, and all other parameters combined together *(via root sum square)*

$$(\mu \pm 3\sqrt{a_v^2 + a_t^2 + a_l^2 + a_w^2 + a_h^2} \pm 3|a_m| \pm 3|a_r|)$$

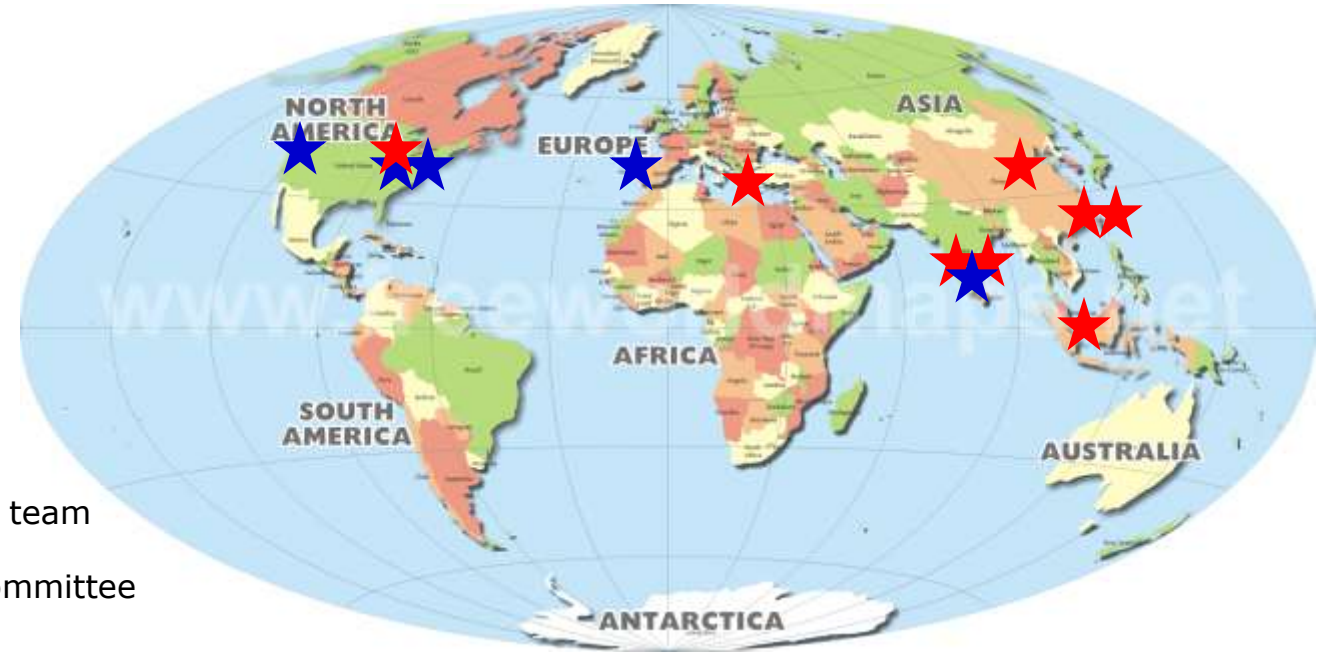
- Required tool output
  - Must report projected values (based on shell variable **$TAU_PROJECTION**)
  - Set of lines specifying for each primary output in design
    - Arrival times and slews (for early/late/rise/fall combinations)
  - Set of lines specifying for a subset of pins in design
    - Slacks

Contest timeline

Date	Activity
Oct 12, 2012	• Contest announced, webpage online (https://sites.google.com/site/taucontest2013) • Detailed 22 page *.pdf* **contest rules document** provided • **Benchmark suite** ver1.0 provided (24 testcases) • Variation aware **gate library** provided • Interconnect network parser and viewer utility provided (debug aid) • Informed that **source code** of winning tool from PATMOS'11 contest (thanks to Prof. Chang's team from NTU, Taiwan) available upon request to avoid infrastructure development (optionally re-use parsers, etc.)
Feb 8, 2013	• **Detailed calculations** for toy benchmark provided • **Monte Carlo results** for benchmarks ver1.0 provided • New variation aware gate library provided • Updated contest rules document • Contestants requested to provide **early binaries** of tool for compatibility testing
Feb 20, 2013	• 5 new large benchmarks provided (largest benchmark ~88K gates)
Feb 28, 2013 (**~4+ months**)	• **Final tool binaries due** for evaluation
Mar 27, 2013	• **Results announced**

Teams

- 8 teams
  - China (1 – Tsinghua Univ. Beijing)
  - Greece (1 – Univ. of Thessaly Volos)
  - India (2 – IIT Madras, IISc Bangalore)
  - Singapore (1 – No affiliation)
  - Taiwan (2 – National Tsing Hua Univ., National Chiao Tung Univ.)
  - USA (1 – Illinois Institute of Technology, Chicago)



Registered team

Contest committee member

Interesting tool characteristics

- Statistical, Monte Carlo based – No multi-corner timers
- Statistical maximum/minimum (*max/min*) operation nuances
  - Used Clark's [Operations Research'61] moment calculation approach, and Visweswariah *et al*. approach [DAC'04]
  - "Smart" – Compare means and do statistical *max/min* in select cases
  - Consider neglected correlation between signal inputs – Better accuracy of output distribution. Based on Naderjah *et al.* [IEEE TVLSI'08]
- Parallelization – Two teams employed *pthreads*
  - **Multi-threaded** netlist parsing
  - **Multi-threaded** wire pre-processing
  - Circuit levelization
  - **Multi-threaded** forward propagation
  - **Multi-threaded** backward propagation

Benchmarks

Netlist	# Gates	# PIs	# POs
simple.net	1	2	1
c3_slack.net	3	4	3
ff.net	3	2	2
c17.net	6	5	2
c17_slack.net	6	5	2
s27.net	18	6	1
s344.net	129	11	11
c432.net	134	36	7
s349.net	141	11	11
s400.net	150	5	6
s386.net	156	9	7
c499.net	176	41	32
c1355.net	180	41	32
c880.net	221	60	26
c1908.net	222	33	25
s526.net	233	5	6
s510.net	270	21	7
c2670.net	344	157	63
s1196.net	584	16	14
c3540.net	691	50	22
s1494.net	783	10	19
c5315.net	918	178	123
c7552.net	1147	206	107
c7552_slack.net	1147	206	107
c6288.net	1667	32	32

[Total netlists: 25]
Benchmarks ver 1.0

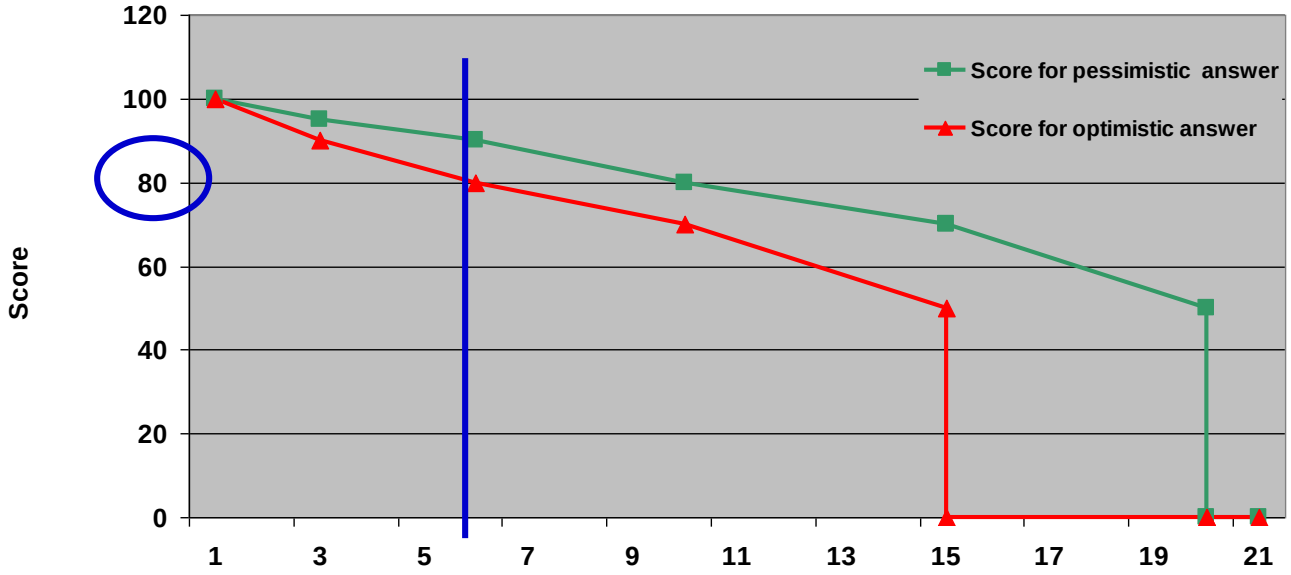
Netlist	# Gates	# PIs	# POs
wb_dma.net	2652	217	215
systemcdes.net	2852	132	65
tv80.net	4211	14	32
systemcaes.net	4517	260	129
mem_ctrl.net	7466	115	152
ac97_ctrl.net	7863	84	48
pci_bridge32.net	9210	162	207
usb_funct.net	10625	128	121
aes_core.net	21372	260	129
des_perf.net	79026	235	64
vga_lcd.net	88403	89	109

[Total netlists: 11]
Benchmarks ver 2.0

- 20 of 36 benchmarks used for final evaluations (> 250 gates)
- Largest test-case ~88.4K gates
- 6 large benchmarks not released to contestants earlier
- All benchmarks now available on webpage

Evaluation metrics

- Score model for each benchmark: **A * { 0.5 + 0.3/T + 0.2/M }**
  - **Accuracy score (A):** Equally weighted sum of *average-arrival time accuracy, average-slew accuracy, average-slack accuracy, worst accuracy, accuracy of worst design slack*
  - Based on **WORST-CASE** projected mode results only
  - Scoring different for pessimistic versus optimistic result



	1	3	6	10	15	15	20	20	21
Score for pessimistic answer	100	95	90	80	70	70	50	0	0
Score for optimistic answer	100	90	80	70	50	0	0	0	0

Evaluation metrics (contd.)

- Score model for each benchmark: **A * { 0.5 + 0.3/T + 0.2/M }**
  - **Run-time score (T):** Tool run-time (seconds) per 1K gates
  - Average run-time for single threaded statistical timer found ~ **1sec/1K** gate benchmark
  - **Memory score (M):** Tool peak memory (in 100Mbs) per 1K gates
  - Average memory for single threaded statistical timer found ~ **100Mb/1K** gate benchmark

- Final evaluation nuances
  - Evaluation on 2.33Ghz Quad core machine, 24Gb Ram, up to 8 threads
  - Accuracy paramount – Monte Carlo based timer to generate golden
  - Biased towards tools with better run-time/memory for similar accuracy
  - Final score is sum of all (20) benchmark scores

Tool comparison for **top 3 teams**

Team **Id**	**Team T13_11** *IIT Madras, India*	**Team T13_13** *National Tsing Hua University, Taiwan*	**Team T13_14** *National Chiao Tung University, Taiwan*
Timer	Statistical multi threaded	Statistical single threaded	Statistical single threaded
Num. benchmarks that crash tool	2	0	3
Missing pin slacks	Few	None	Few
~Average accuracy	0.72	1.0	0.45
~Average run-time	0.3	1.0 [~ 1sec/1K gates]	17.0 (*varied between 0.3 – 200*)
~Average memory	3.2	1.0 [~ 100Mb/1K gates]	0.3

- Accuracy scores indicated within 3% accuracy of statistical timing (for given benchmarks, library) for arrival times and slews
- Slack accuracy and worst timing accuracy using statistical timer usually within 10% of Monte Carlo results

Summary

- Variation aware timing analysis contest
  - Increase awareness of variation aware timing analysis, provide insight into some challenging aspects
    - **Parametric timing propagation**
    - **Model fitting/finite-difference concept, inaccuracies**
    - **Parametric maximum/minimum operations**
    - **Projection techniques – Pessimism relief**
  - Encourage novel parallelization techniques
    - **Multi-threaded timers**
  - Facilitate creation of a publicly available variation aware timing analysis framework and benchmarks for research/future contests
    - **Framework for potential concepts on parametric path tracing**
    - **Variability aware timing macro-modeling, coupling, etc.**

- Reference: Sinha *et al.*, TAU 2013 Variation aware timing analysis contest, ISPD 2013

Final results

- Plaques and cash awards for the top three teams

Team **Id**	**Team T13_11** *IIT Madras, India*	**Team T13_13** *National Tsing Hua University, Taiwan*	**Team T13_14** *National Chiao Tung University, Taiwan*
Timer	Statistical multi threaded	Statistical single threaded	Statistical single threaded
Num. benchmarks that crash tool	2	0	3
Missing pin slacks	Few	None	Few
~Average accuracy	0.72	1.0	0.45
~Average run-time	0.3	1.0 [~ 1sec/1K gates]	17.0 (*varied between 0.3 – 200*)
~Average memory	3.2	1.0 [~ 100Mb/1K gates]	0.3
Final score averaged over all benchmarks	**119**	**70**	**31**
POSITION	**1**	**2**	**3**

TAU 2013
Variation Aware Timing Contest

Third Place Award

Presented to

Yu-Ming Yang, Yu-Wei Chang,
Shih-Heng Huang and Iris Hui-Ru Jianga

National Chiao Tung University, Taiwan

For

iTimer

Jinjun Xiong	Chirayu Amin	Debjit Sinha
General Chair	Technical Chair	Contest Chair

TAU 2013
Variation Aware Timing Contest

Second Place Award

Presented to

Po-Yi Hsu, Sheng-Kai Wu,
Yung-Shun Lin and Wai-Kei Mak

National Tsing Hua University, Taiwan

For

HWL Timer

Jinjun Xiong	Chirayu Amin	Debjit Sinha
General Chair	Technical Chair	Contest Chair

TAU 2013
Variation Aware Timing Contest

First Place Award

Presented to

Jobin Jacob Kavalam, Sudharshan V,
Nitin Chandrachoodan and Shankar Balachandran

IIT Madras, India

For

IITimer

Jinjun Xiong	Chirayu Amin	Debjit Sinha
General Chair	Technical Chair	Contest Chair

Backup: Detailed scores

Final results:

TAU-TAC 2013 Results						Accuracy weight	0.5	Runtime weight	0.3	Memory weight	0.2												
Benchmark	#gates	Team 11						Team 13						Team 14									
		timeX10	memX10	T	M	A	Total	timeX10	memX10	T	M	A	Total	timeX10	memX10	T	M	A	Total				
ac97_ctrl	7863	10.2	4167060	0.12972148	0.52995803	69.6	222.026466	70.88	5726964	0.90143711	0.72834338	75.2	83.276305	442.31	2249160	5.62520666	0.28604349	19.7	24.6747571				
aes_core	21372	20.86	5239152	0.09760434	0.24514093	67.9	298.046437	218.56	18970840	1.02264645	0.88764926	78.5	79.9656527						0				
c2670	344	2.45	3582664	0.7122093	10.4147209	37.8	35.5481813	2.91	361944	0.84593023	1.05216279	39.3	41.0576465	2.1	144624	0.61046512	0.4204186	31.2	45.7749212				
c3540	691	2.63	3614676	0.38060781	5.23107959	27.6	36.6099083	5.29	671472	0.76555716	0.97173951	38	41.7121414	5.66	215240	0.81910275	0.31149059	25	37.7082095				
c5315	918	2.91	3620348	0.31699346	3.9437342	37.1	55.5425996	9.14	1226704	0.9956427	1.33627887	38.7	36.8030138	7.77	304060	0.84640523	0.33122004	30	43.7480504				
c6288	1667	3.06	3623836	0.18356329	2.17386683	15.4	34.2852615	9.91	1257612	0.5944811	0.75441632	32.2	40.8858659	9.43	367640	0.56568686	0.22053989	25.8	49.9796091				
c7552	1147	3.01	3617472	0.26242371	3.15385527	31.8	54.2700015	10.06	1257060	0.87707062	1.09595466	39.1	40.0593973	12.53	345956	1.092415	0.30161813	30.1	43.2751015				
c7552_slack	1147	3.07	3625324	0.26765475	3.16070096	53.9	90.7742841	10.93	1260572	0.95292066	1.09901656	78.7	78.4483544	12.6	345988	1.09851787	0.30164603	30.5	43.8017824				
des_perf	79026	94.1	9828860	0.11907473	0.12437502	46.8	216.565415	851.05	76043356	1.07692405	0.96225743	70.7	69.7395946						0				
mem_ctrl	7466	10.94	4154276	0.14653094	0.55642593	70.4	204.637738	100.57	9538156	1.34703991	1.27754567	77.7	68.3185584	384.27	2377588	5.14693276	0.3184554	20.6	24.4381627				
pci_bridge32	9210					0	0	116.59	10108840	1.26590662	1.09759392	75.9	69.7673602	19603.1	3583376	212.84582	0.38907448	20.5	20.8167222				
s1196	584	2.5	3587100	0.42808219	6.14229452	83.2	102.615645	3.61	372796	0.61815068	0.63834932	75	97.3969982	2.4	159500	0.4109589	0.27311644	29.7	58.2799655				
s1494	783	2.6	3605184	0.33205619	4.60432184	67.3	97.3763019	5.62	664640	0.71775223	0.8488378	78.2	90.2105663	4.16	205324	0.53128991	0.26222733	24.5	44.7703314				
s510	270	2.28	3556352	0.84444444	13.1716741	48.9	42.5648709	1.51	184704	0.55925926	0.68408889	79.3	105.372532	1	90964	0.37037037	0.3369037	21	39.9764703				
systemcaes	4517					0	0	59.38	5107244	1.31458933	1.13067168	76.7	69.4207219	2260.41	1703832	50.0422847	0.37720434	20.4	21.1387151				
systemcdes	2852	4.49	3750024	0.15743338	1.31487518	59.1	151.158511	25.13	2570400	0.88113604	0.90126227	76.5	81.2721117	106.39	728456	3.73036466	0.25541935	21.7	29.5868023				
tv80	4211	6.18	3867524	0.14675849	0.91843363	70.9	195.82132	48.14	4794636	1.14319639	1.13859796	78.1	73.2637926	43.57	1233372	1.0346711	0.2928929	20.5	30.1922087				
usb_funct	10625	12.99	4393824	0.12225882	0.41353638	61.4	211.059062	111.12	9889224	1.04583529	0.93075049	77.6	77.7344351	284.69	3072360	2.67943529	0.28916329	24.4	31.8081964				
vga_lcd	88403	124.46	10589148	0.14078708	0.11978268	42.3	181.914022	907.89	76556968	1.02699003	0.86599966	74.6	76.3204817						0				
wb_dma	2652	5.77	4164924	0.21757164	1.57048416	75.1	150.666027	32.03	3079712	1.20776772	1.16127903	78.8	72.5445431	61.47	971156	2.3178733	0.36619759	29.5	34.6796759				
				0.27809867	3.21051445	SUM	2381.48205			0.95801168	0.97813977	SUM	1393.57007			17.0451647	0.31374304	SUM	624.649682				
						Avg.	119.074103					Avg.	69.6785036					Avg.	31.2324841				

Accuracy score: