Local Merges for Effective Redundancy in Clock Networks

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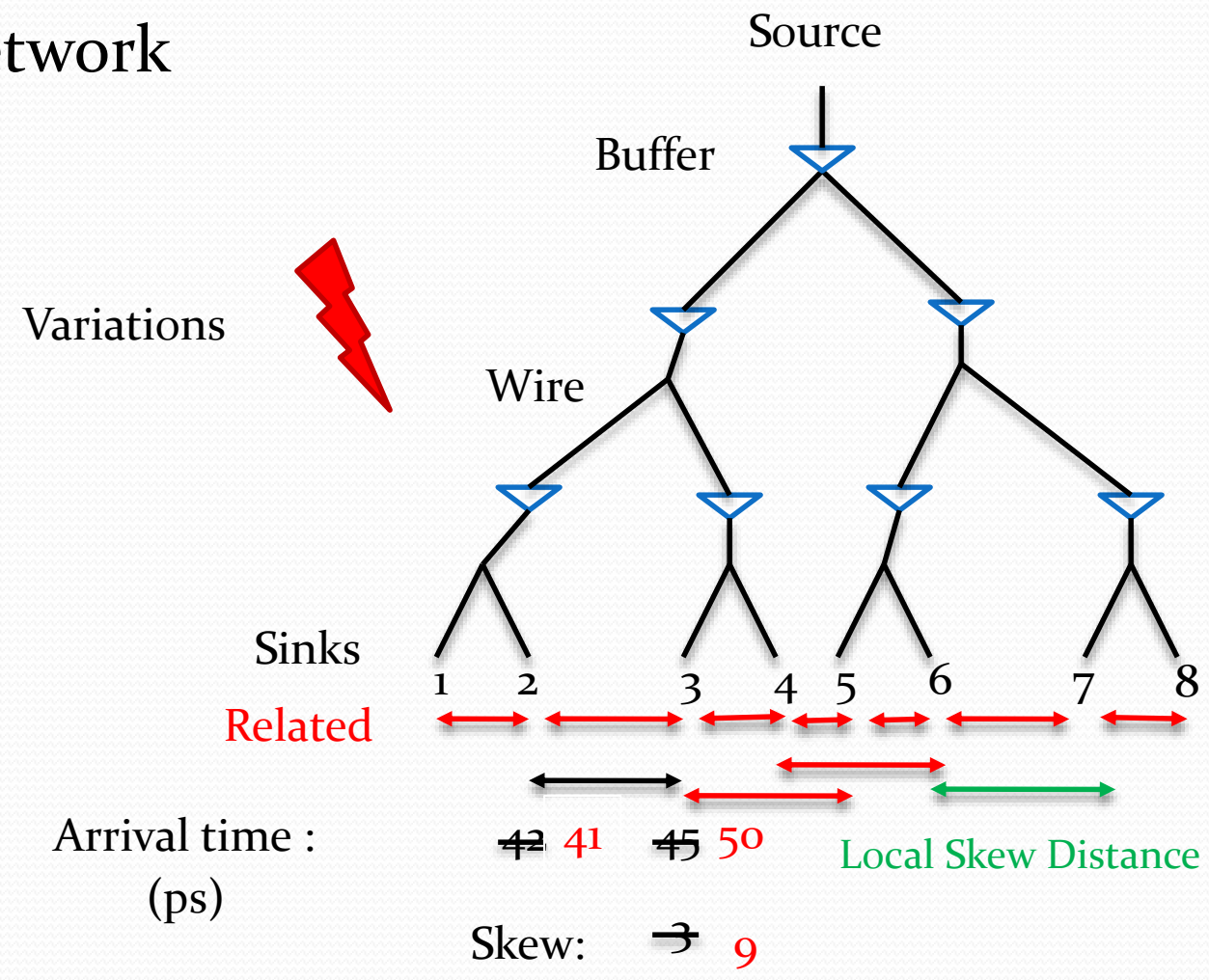
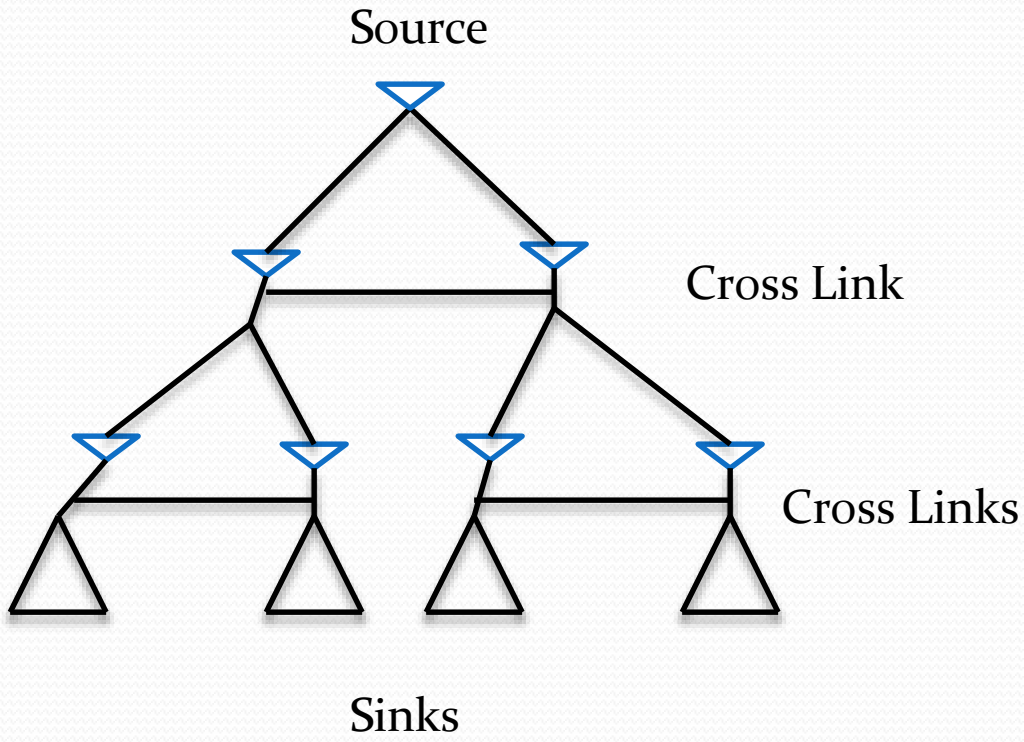
Introduction

- Sample clock network
  - Slew
  - Skew

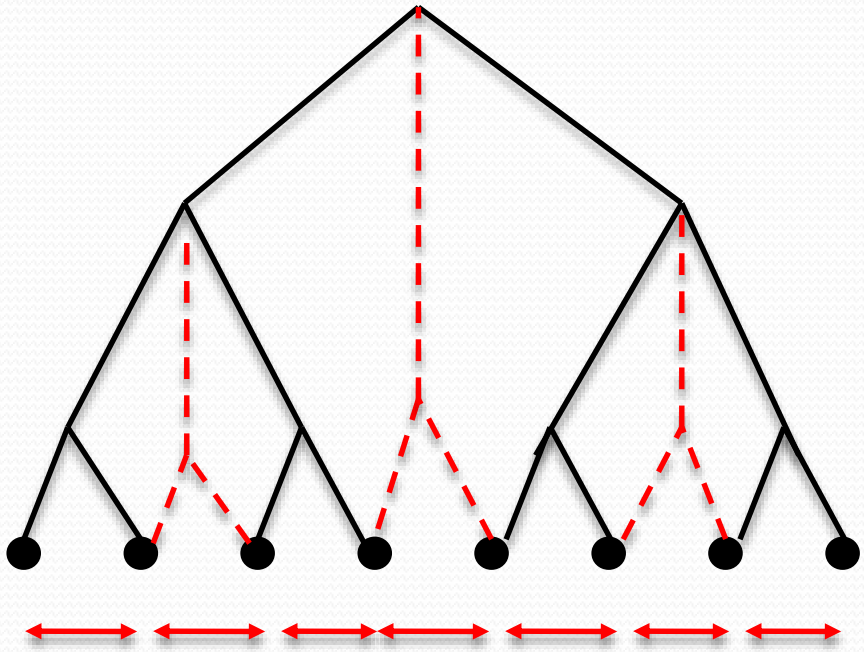


Previous Work – Cross Links



[8] T. Mittal and C.-K. Koh. Cross link insertion for improving tolerance to variations in clock network synthesis. In Proc. ISPD'11.
[11] A. Rajaram, J. Hu, and R. Mahapatra. Reducing clock skew variability via cross links. In Proc. DAC'04.
[12] A. Rajaram and D. Pan. Variation tolerant buffered clock network synthesis with cross links. In Proc. ISPD'06.
[13] A. Rajaram, D. Z. Pan, and J. Hu. Improved algorithms for link-based non-tree clock networks for skew variability reduction. In Proc. ISPD'05.

Previous Work – Multilevel fusion tree



[16] D.-J. Lee and I. L. Markov, “Multilevel Tree Fusion for Robust Clock Networks,” ICCAD, 2011.

Problem description

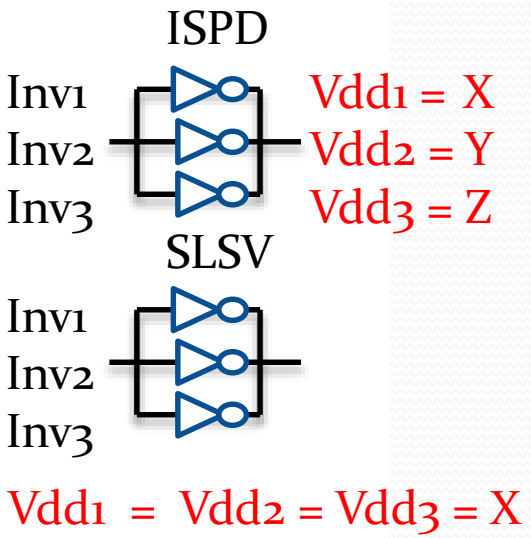
Construct a clock network given:

- Inverter/wire library, blockages, sink locations and loads.
- Process variation model (supply voltage/wire width)
  - ISPD 2010 contest model (ISPD)
  - Single Location Single Voltage (SLSV)

Minimize: Capacitance

Constraints:

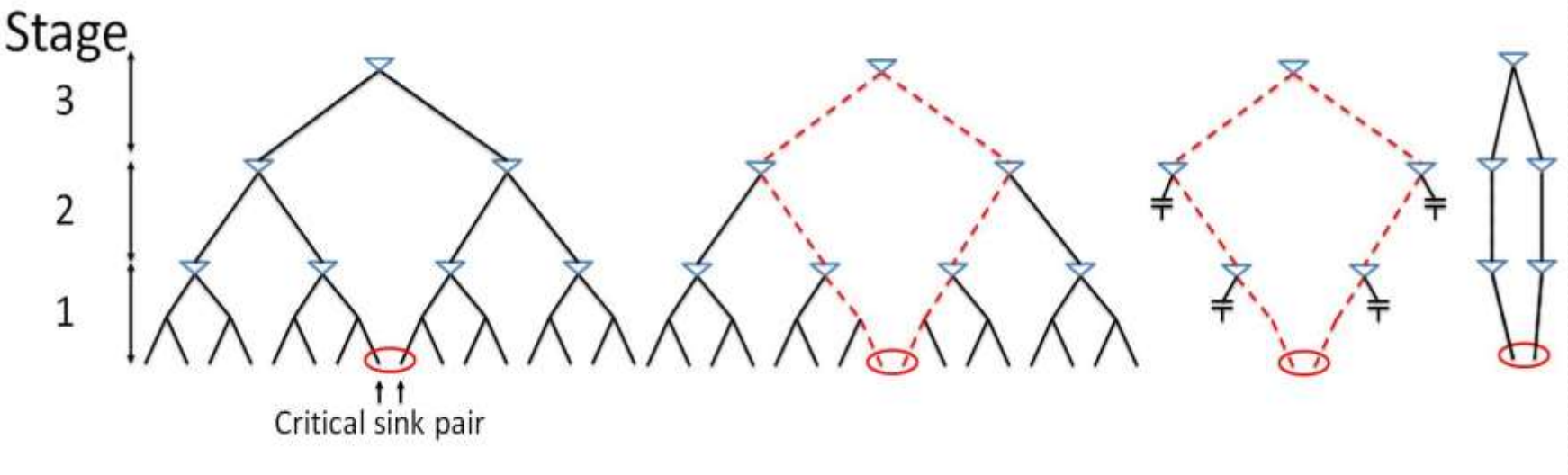
- 95% -Local skew (500 Monte Carlos simulations)
- Slew
- No inverters placed within blockages



[15] C. Sze. ISPD 2010 high performance clock network synthesis contest: Benchmark suite and results. pages 143–143, 2010.
[2] S. Bujimalla and C.-K. Koh. Synthesis of low power clock trees for handling power-supply variations. In Proc. ISPD'11.

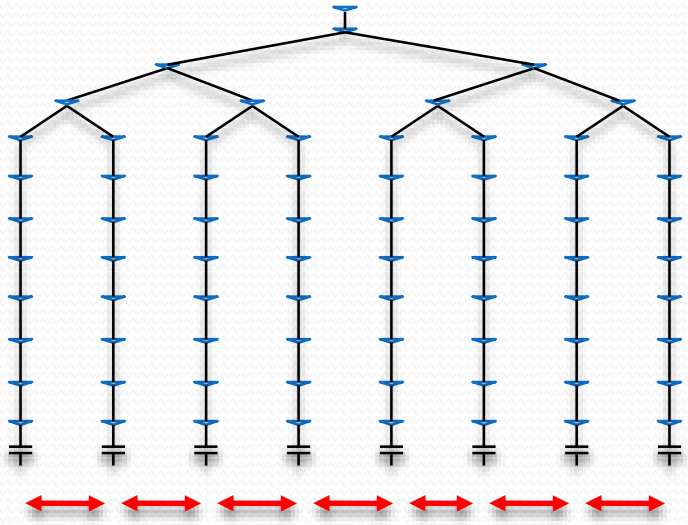
Experimental setup

- Consider sink pairs that are spatially close but topologically distant.

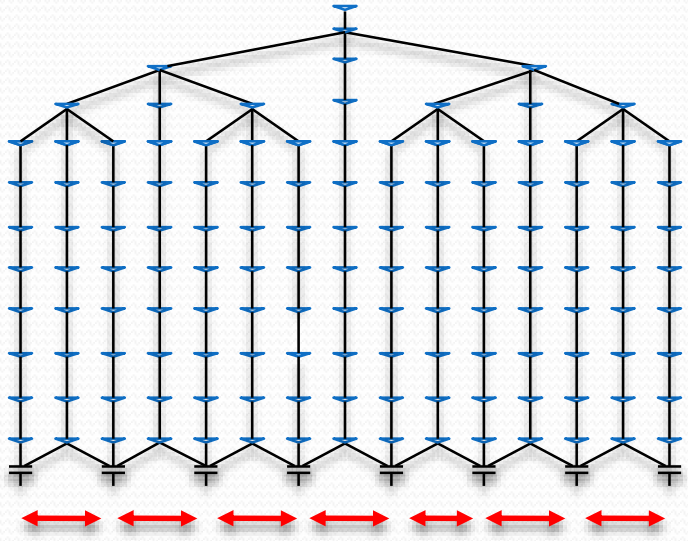


[16] D.-J. Lee and I. L. Markov, "Multilevel Tree Fusion for Robust Clock Networks," ICCAD, 2011.

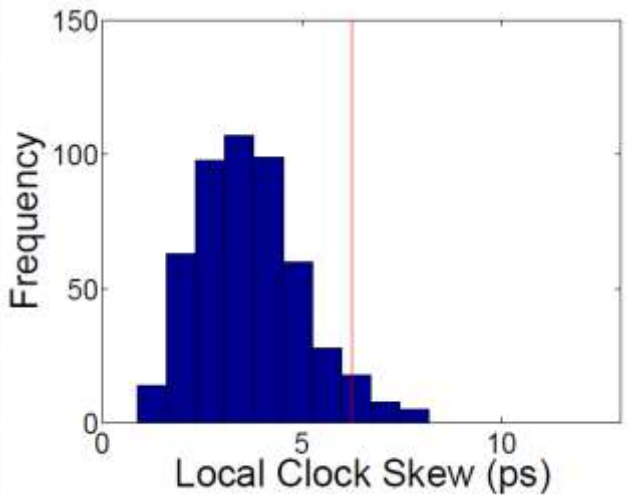
ISPD variations

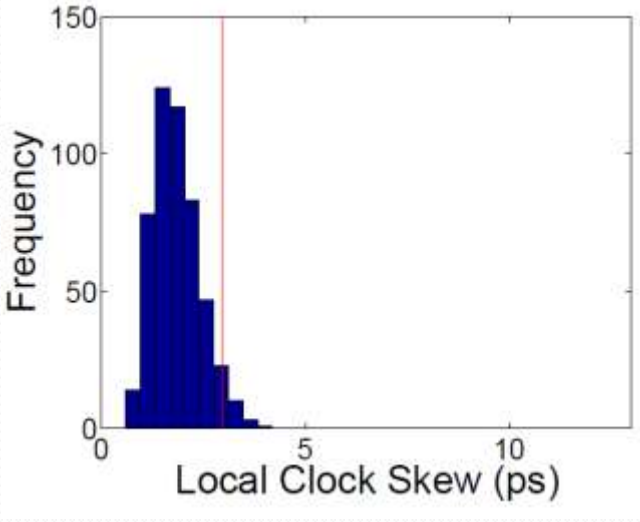


Related



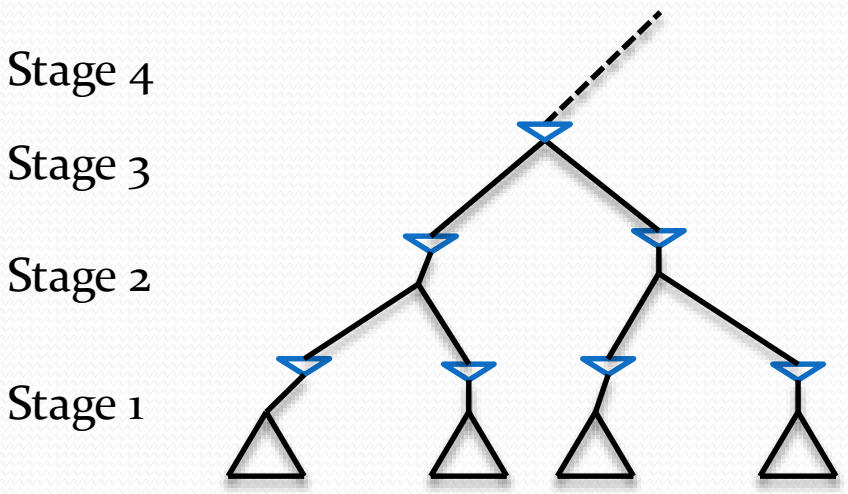
Related





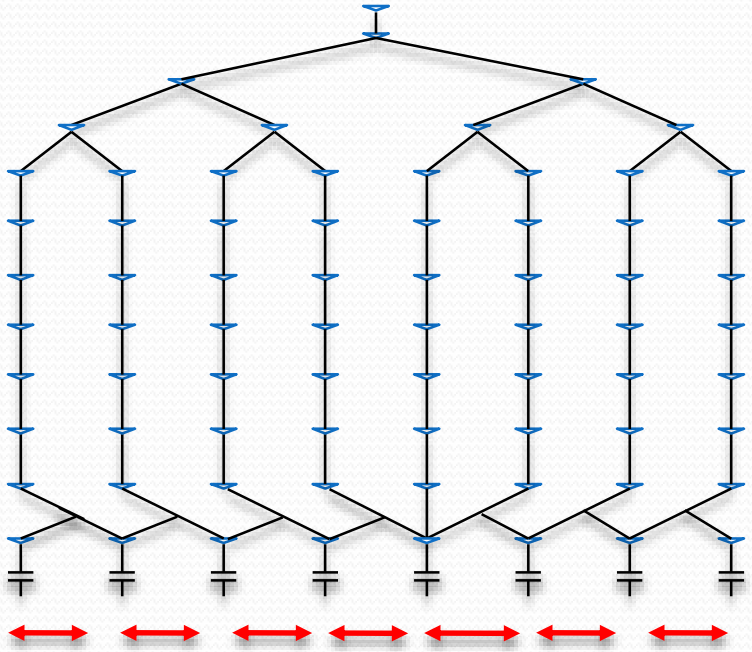
Case Study

Capacitance cost in a clock tree with 8 stages



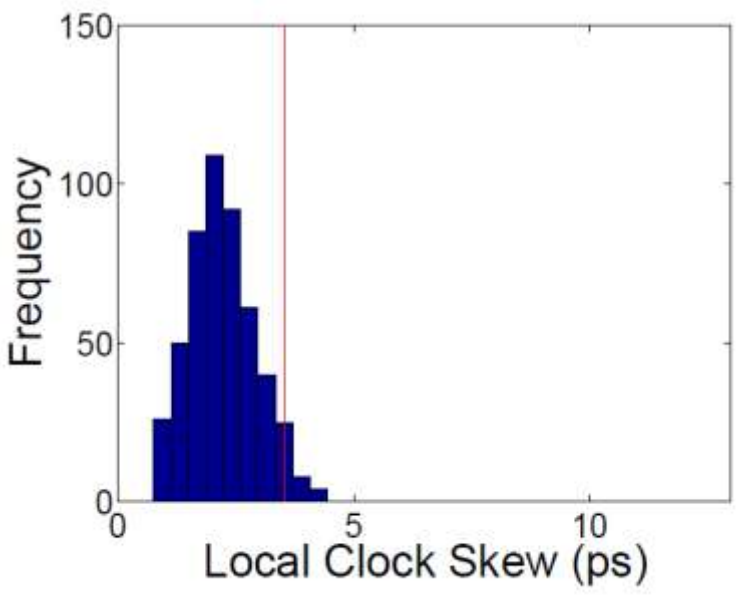
Stage	Total Cap
1	71 %
2	12 %
3	6 %
4	4 %
Rest	7 %

Proposal



Related

ISPD



Method

- Build tree stage 1
- Build special stage 2
  - Local merges
  - Sparsification
- Build tree stage 3+

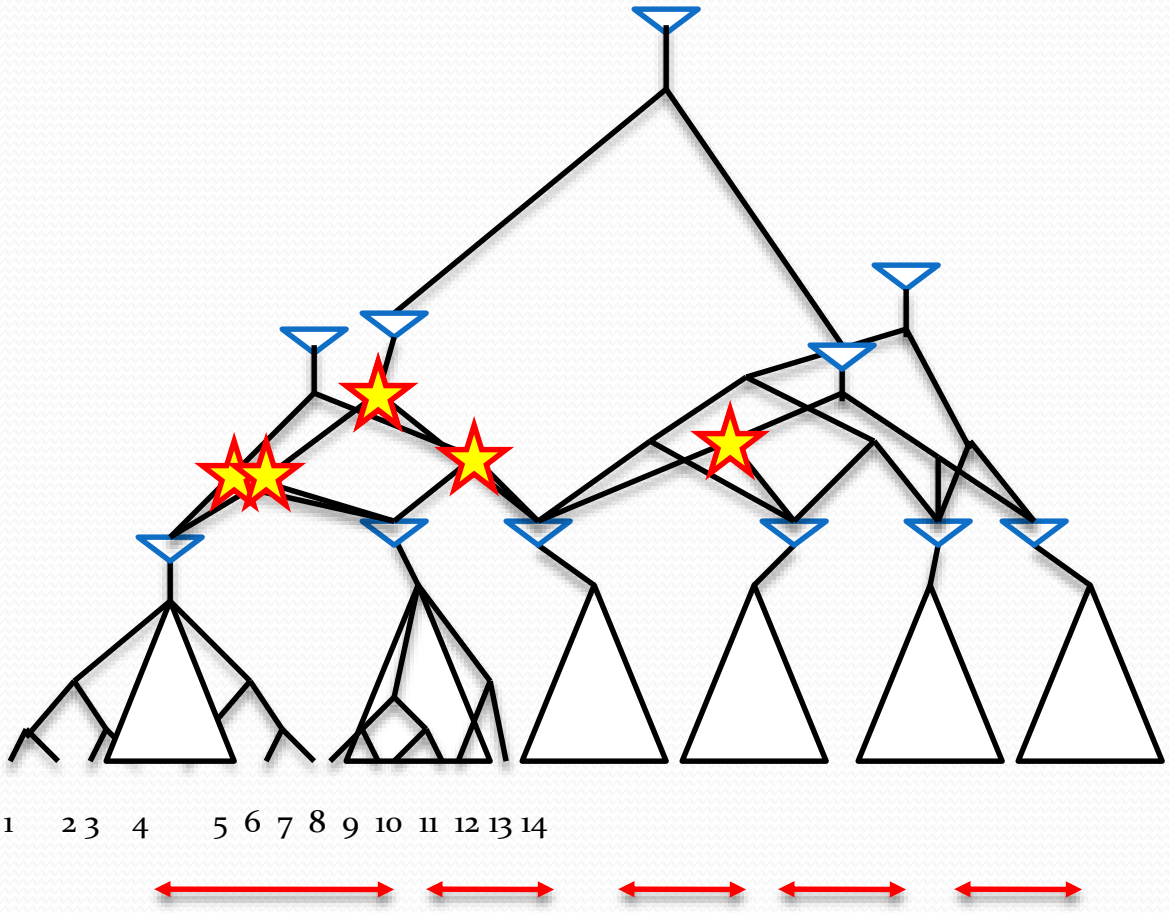


Table 2: Comparisons of 95% skew and cost under the ISPD model. An '*' indicates that the solution does not meet the skew requirement.

Ckt.	Method	Max Skew (ps)	95% Skew (ps)	Cap. (fF)	Run Time (s)
BM01	[3]	-	7.32	142.64	1092
	[2]	-	6.48	137.97	472
	Our work	6.65	5.35	130.82	680
BM02	[3]	-	7.42	265.21	4314
	[2]	-	7.38	268.29	1450
	Our work	*8.53	5.76	254.36	1621
...					
Norm.	[3]			1.11	
	[2]			1.01	
	Our work			1.00	

- ISPD
  - 1 % lower capacitance on average.
  - Significantly lower skew.

[2] Y.-C. Chang, C.-K. Wang, and H.-M. Chen. On construction low power and robust clock tree via slew budgeting. In Proc. ISPD'12.
[3] T. Mittal and C.-K. Koh. Cross link insertion for improving tolerance to variations in clock network synthesis. In Proc. ISPD'11.

Table 1: Comparisons of 95% skew and cost under the SLSV model. An '*' indicates that the solution does not meet the skew requirement.

Ckt.	Method	Max Skew (ps)	95% Skew (ps)	Cap. (fF)	Run Time (s)
BM01	[4]	*9.43	7.23	1168.10	675
	[1]	*11.40	*10.29	189.06	2324
	Our work	6.65	5.69	155.14	879
BM02	[4]	*8.99	7.35	2099.81	2140
	[1]	*14.19	*12.30	341.08	6723
	Our work	*7.69	6.26	292.99	1978
...					
Norm.	[4]			3.87	
	[1]			1.22	
	Our work			1.00	

- SLSV
  - 22% lower capacitance on average.
  - Satisfies BM01 and BM02 with 3x lower cap.
  - No sparsification on BM03 to meet skew constraint.

[1] S. Bujimalla and C.-K. Koh. Synthesis of low power clock trees for handling power-supply variations. In Proc. ISPD'11.
[4] L. Xiao, Z. Xiao, Z. Qian, Y. Jiang, T. Huang, H. Tian, and E. F. Y. Young. Local clock skew minimization using blockage-aware mixed tree-mesh clock network. In Proc. ICCAD'10.

Questions

- Thank you!