Clock Enable Timing Closure Methodology

Harish Dangat

Samsung Semiconductor

Agenda

- **Basics of Clock Gating**

- Fixing Clock Enable Timing in RTL-2-GDSII Flow

- Results

- Conclusion

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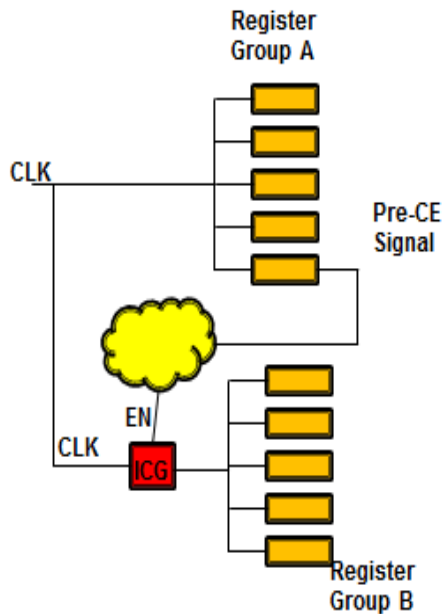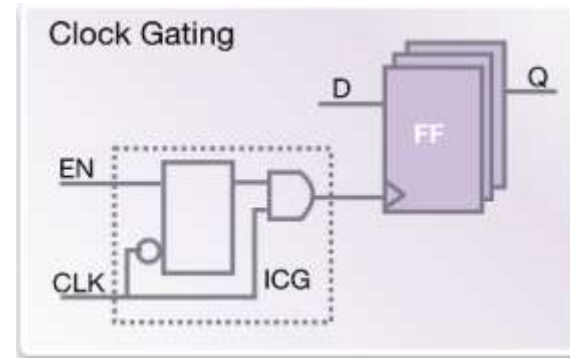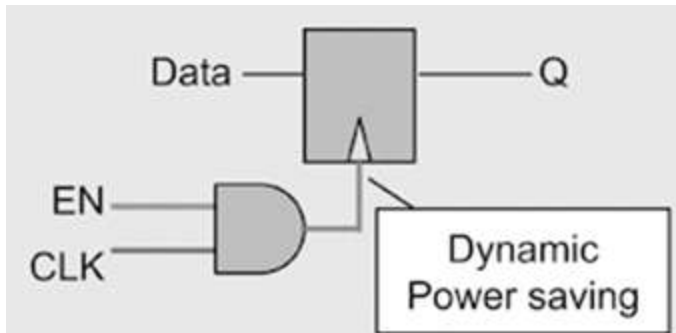SAMSUNG

Clock Gating Basic

Figure A – Clock Enable Signal Path

- Use internal (or external) signal to disable clock

- This saves Dynamic Power

- A must for low power design

- Creates new timing paths
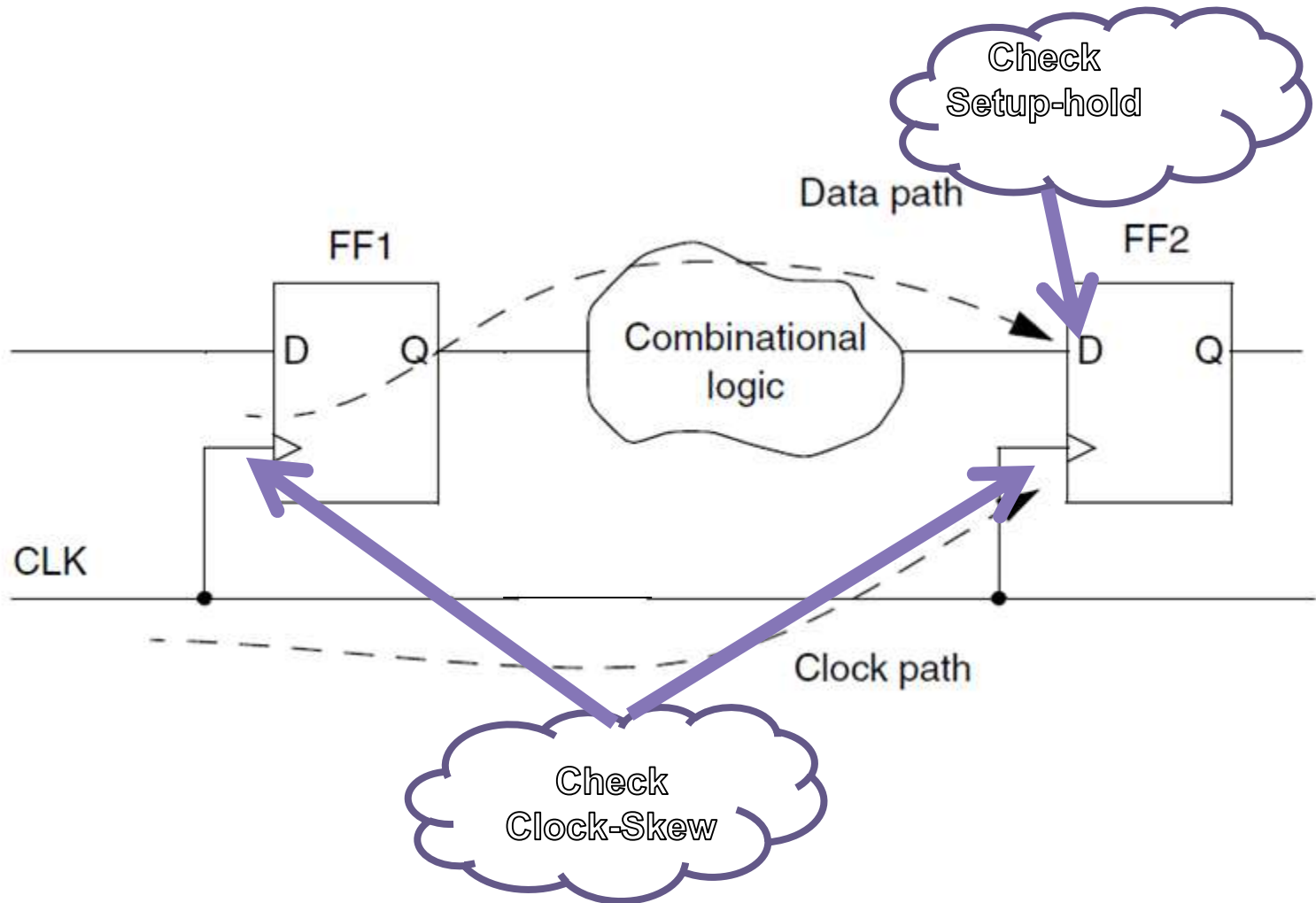
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Two Types of Clock Gating

- Using AND gate

- Using ICG Cell

Rest of presentation is about ICG type clock gating

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Register to Register Path

Check
Setup-hold

Data path

FF1

D   Q

Combinational logic

FF2

D   Q

CLK

Clock path

Check
Clock-Skew

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Register to Register Path with Clock Gating

Data path

FF1

FF2

D   Q   Combinational
logic   D   Q

CLK

Clock path

Check CE
Setup-hold

CE Path

D

1ns

CE clk Path

EN

CLK

GCLK

D

0.5ns

1ns

Clock gated clk Path

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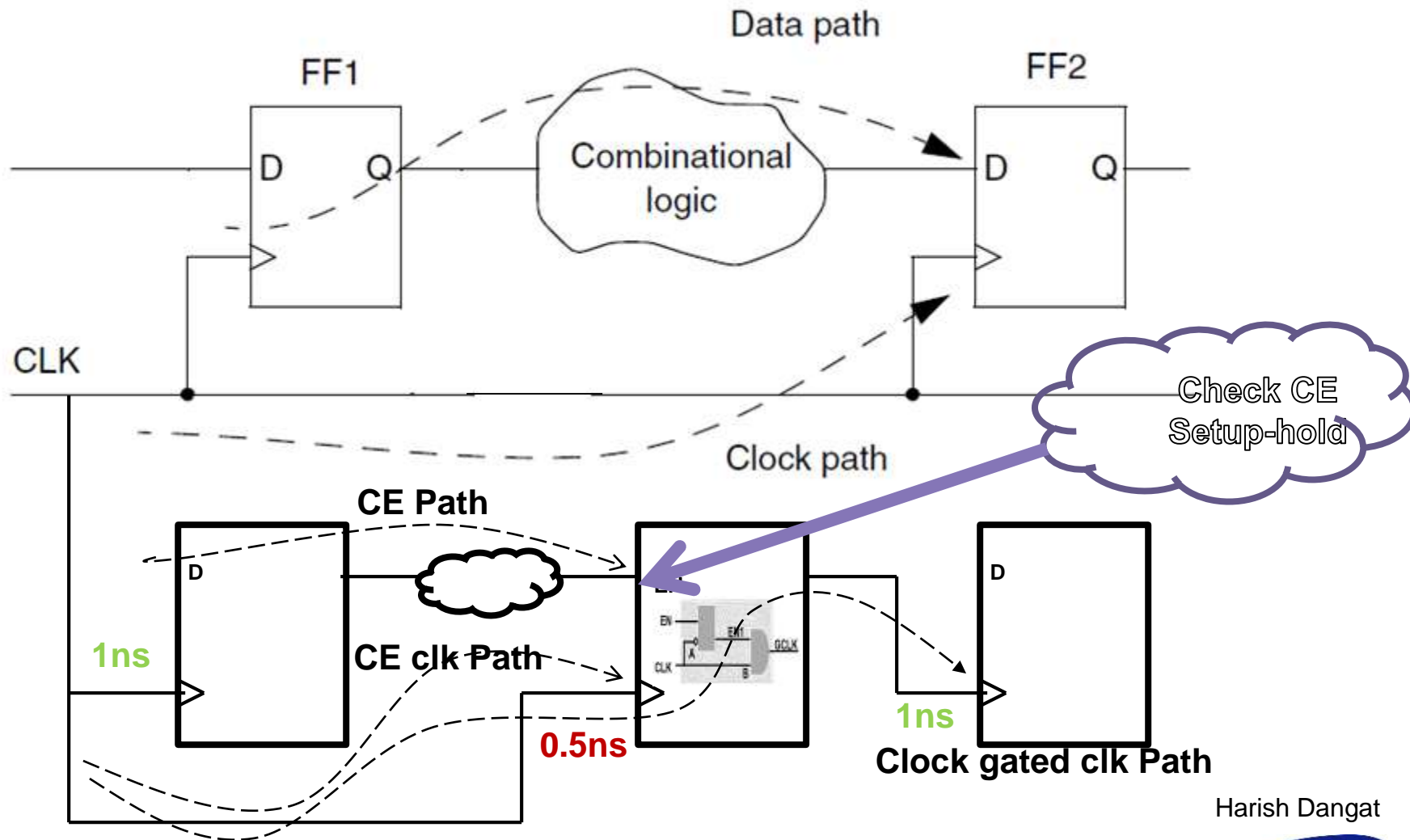
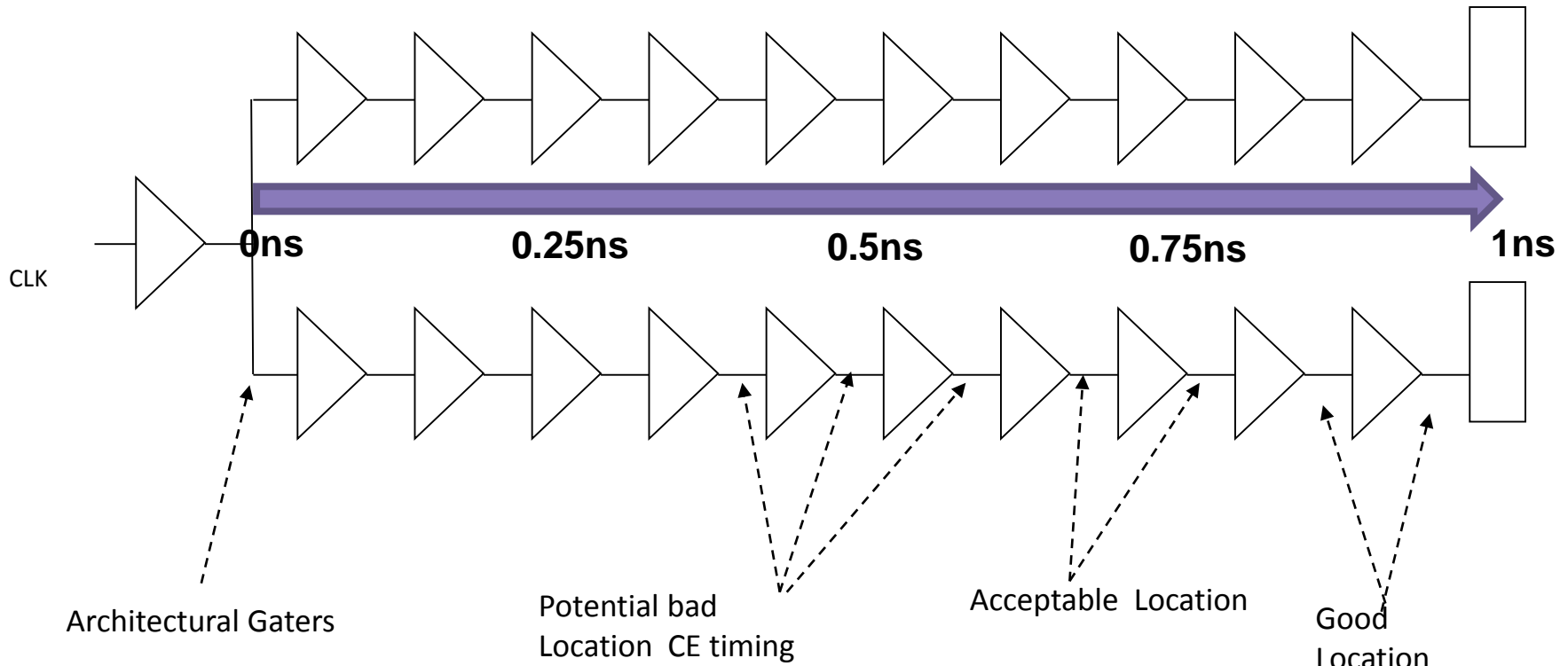# What is different about CE path

- Not noticed at Synthesis

- Timing available is less than cycle time

- ICG cells are not skew balanced with registers

- Violations are seen only after Clock Tree Synthesis

- Mostly affects timing critical blocks

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Effect of ICG Cells Location in Clock Tree

CLK

0ns   **0.25ns**   **0.5ns**   **0.75ns**   **1ns**

Architectural Gaters

Potential bad Location CE timing

Acceptable Location

Good Location

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Agenda

- Basics of Clock Gating

- **Fixing Clock Enable Timing in RTL-2-GDSII Flow**

- Results

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What to Do at RTL Level

- CE signal should be generated in the same module

- Generate CE signal from functionally related modules

- Simplify the logic that generates CE signal

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CE Timing at Synthesis Step

- ## Reduce cycle time to ICG cells

```
set_clock_latency  -(cycle_time/2) \

        [get_pin all_clock_gating_registers/CK]

set_clock_latency  0  [get_pin all_clock_gating_registers/ECK]
```

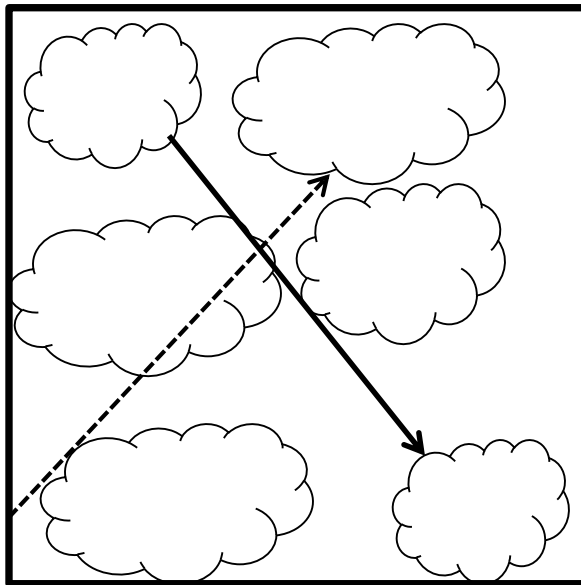- ## Set high setup time on ICG cells

```
set timing_scgc_override_library_setup_hold true

set_clock_gating_style -setup 400ps clock_gate
```
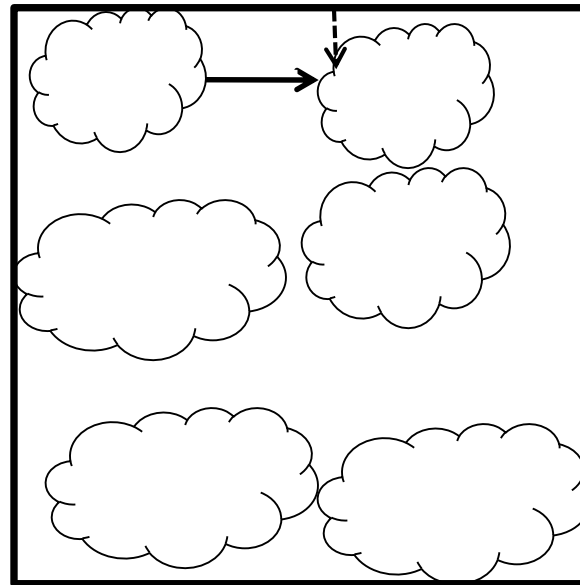
- ## Turn off bus sharing in Power Compiler

```
set_clock_gating_style -no_sharing
```

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CE Timing at Floorplan Step

- When placing modules, pay attention to CE signal connectivity

- If CE signal(s) are input pins, place them close to modules that receive it

CE timing problem

Good CE timing

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CE Timing at placement Step

- Tightening available cycle time by changing ICG setup time

```
set timing_scgc_override_library_setup_hold true

set_clock_gating_style -setup 400ps clock_gate
```

- Tightening available cycle time by changing ICG clock latency

```
set_clock_latency  -(cycle_time/2) \
        [get_pin all_clock_gating_registers/CK]

set_clock_latency  0  [get_pin all_clock_gating_registers/ECK]
```

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CE Timing at placement Step (cont)

- Create group path and add extra weight

```
group_path  -weight 5  -name CLOCK_ENABLE \
        -to [get_cell */*GATE_LATCH]
```

- Place ICG cells close to flops

```
set placer_disable_auto_bound_for_gated_clock false
```

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How to Select Latency?

- Apply global latency
  - Easy, Not very efficient

- Apply based on ICG depth and fanout
  - Less depth – more latency
  - More fanout – more latency

- Apply based on CTS results
  - More accurate

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CE Timing at Clock Tree Synthesis

- ## Clone ICG Cells

```
set icg_cells { icg_cell_1 icg_cell_2 }

split_clock_net -objects [get_cells $icg_cells] \
        -split_intermediate_level_clock_gates -gate_sizing

remove_ideal_network [all_fanout -flat -clock_tree]

remove_propagated_clock *

remove_clock_tree
```
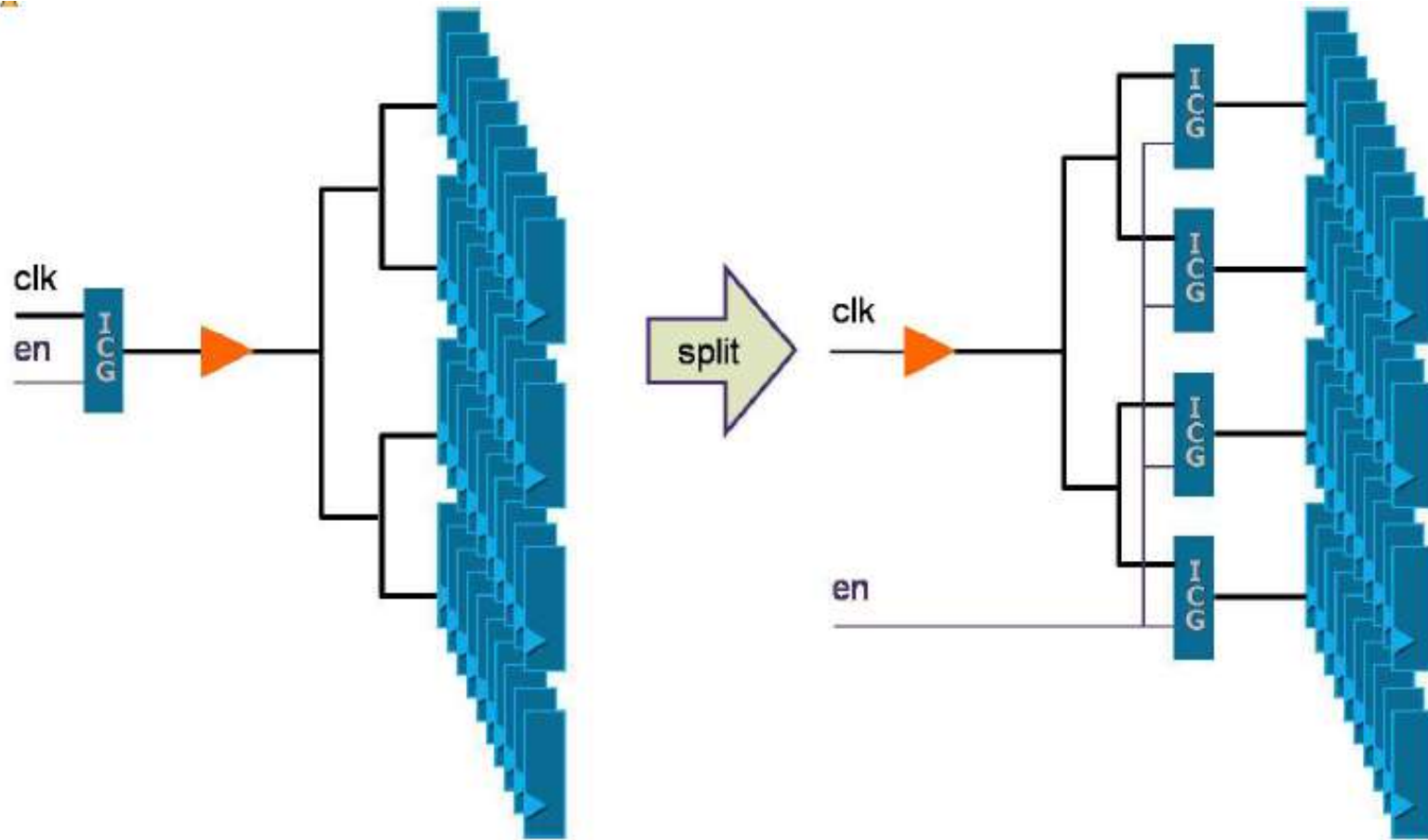
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ICG Cloning
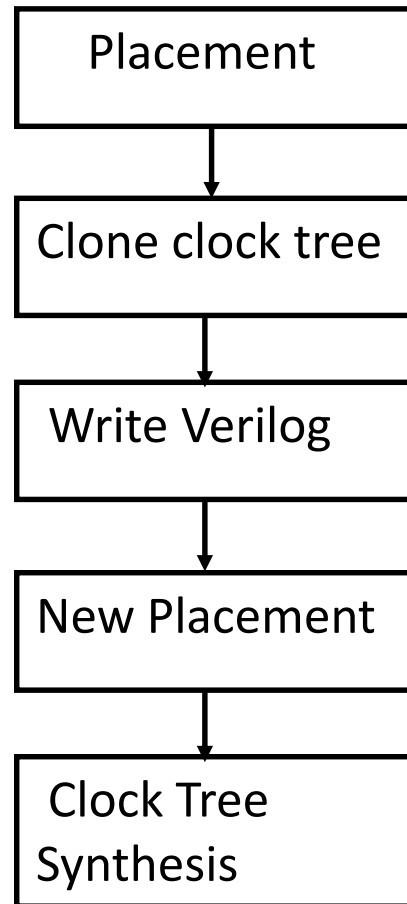

clk
en
split
clk
en

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CE Timing at Clock Tree Synthesis Cloning based on fanout and slack

```
foreach_in_collection CELLS [get_cells * -hier -filter "ref_name =~ *ICG*"] {

        set names [get_object_name $CELLS]

        set ckPins [get_object_name [get_pins -of_object [get_cells $CELLS] \

                -filter "full_name =~ */CLK"]]

        set eckPins [get_object_name [get_pins -of_object [get_cells $CELLS] \

                -filter "full_name =~ */ENABLE_CLK"]]

        set eckFanout [sizeof_collection [all_fanout -from [get_pins $eckPins] -flat]]

        set cgSlack [get_attribute [get_pins ${names}/ENABLE] max_slack

        if {$cgSlack > -0.150 && $eckFanout > 100} {

        echo "${names}/E"

}

remove_propagated_clock *

remove_clock_tree
```

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CE Timing at Clock Tree Synthesis Two Pass Flow

```
┌─────────────────────┐
│     Placement       │
└─────────────────────┘
           │
           ▼
┌─────────────────────┐
│   Clone clock tree  │
└─────────────────────┘
           │
           ▼
┌─────────────────────┐
│    Write Verilog    │
└─────────────────────┘
           │
           ▼
┌─────────────────────┐
│    New Placement    │
└─────────────────────┘
           │
           ▼
┌─────────────────────┐
│    Clock Tree       │
│    Synthesis        │
└─────────────────────┘
```

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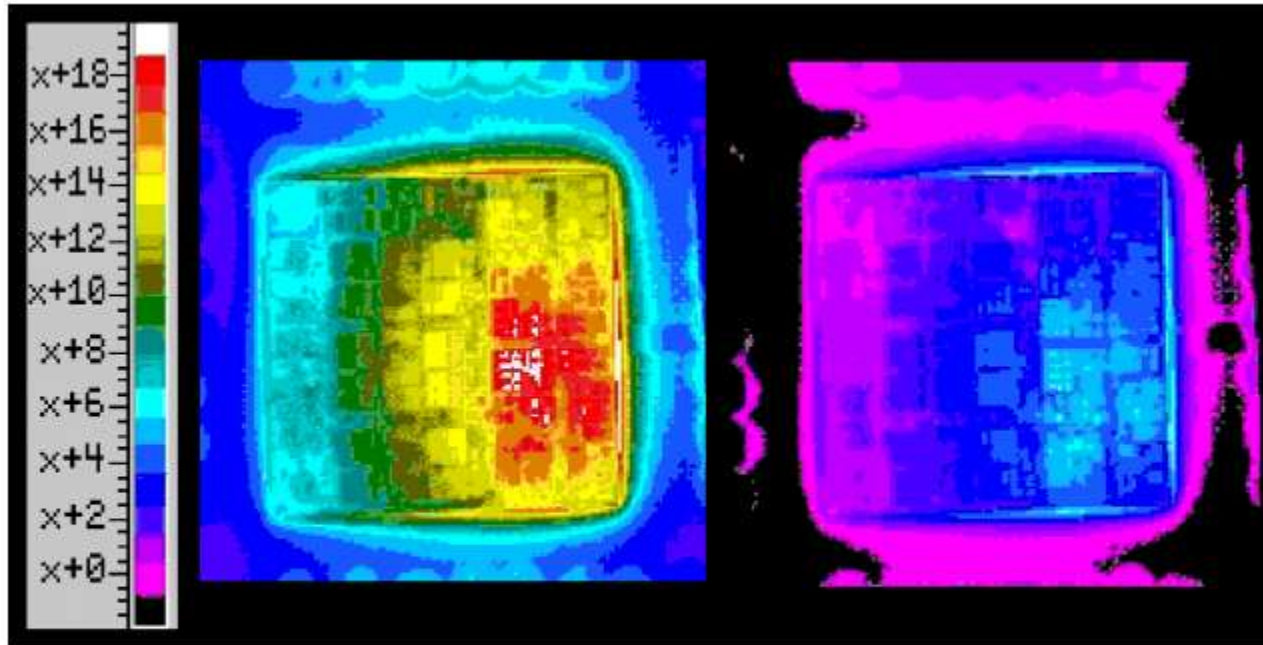
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Agenda

- Basics of Clock Gating

- Problems Created by Clock Gating

- Fixing Clock Enable Timing in RTL-2-GDSII Flow

- **Results**

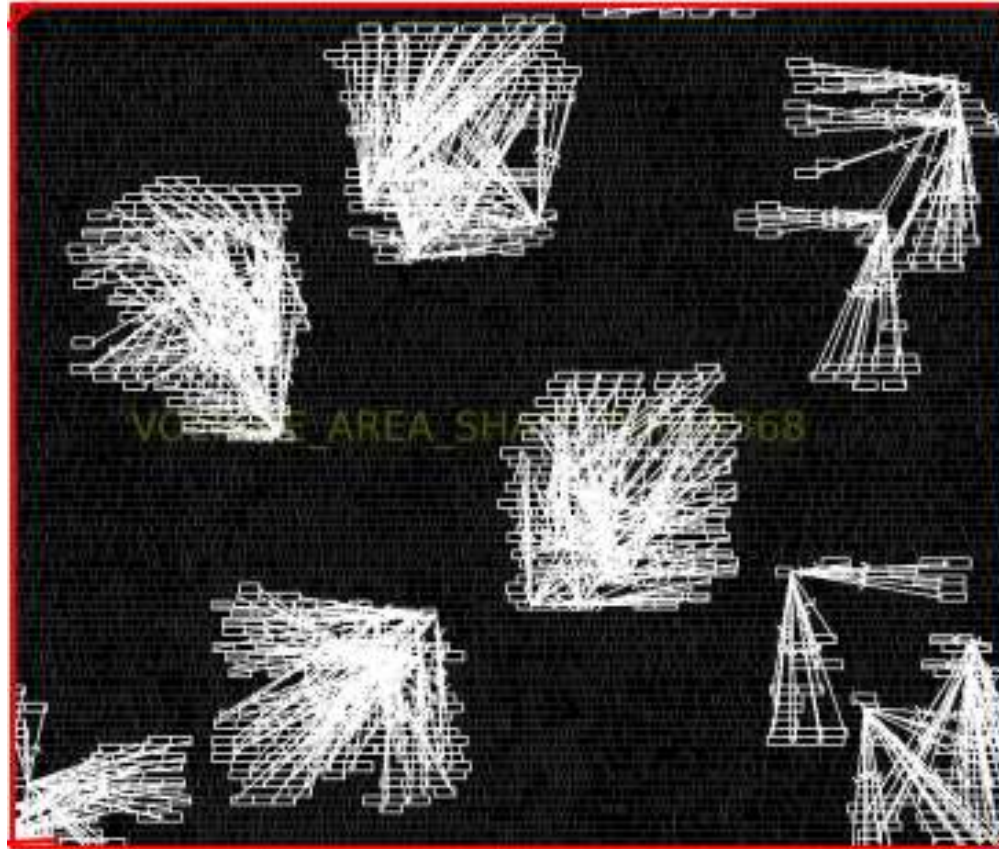- Conclusion

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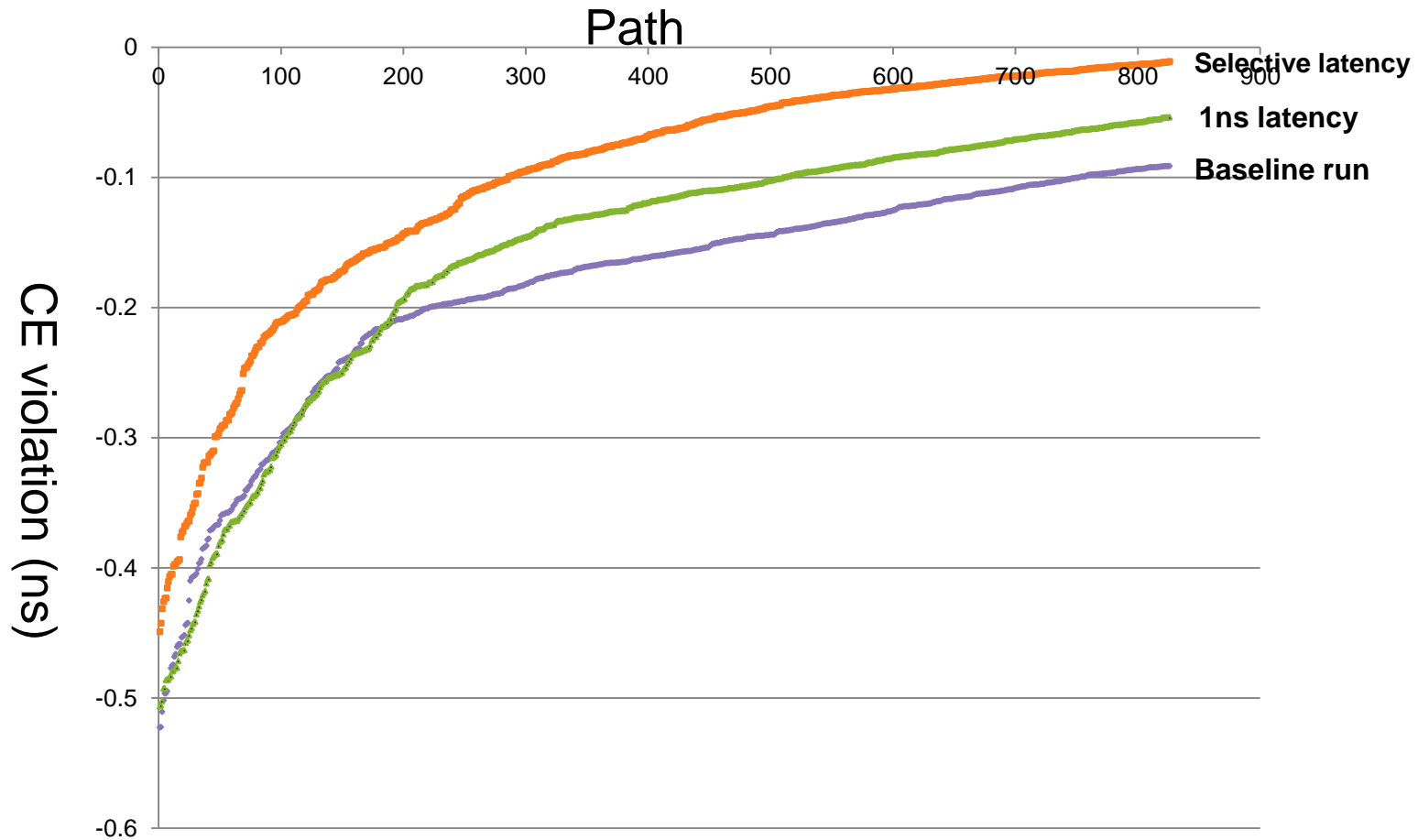
Die Temperature Without and With Clock Gating

Relative POWER5 processor temperature (Celsius)
- without clock gating (left) and with clock gating (right)

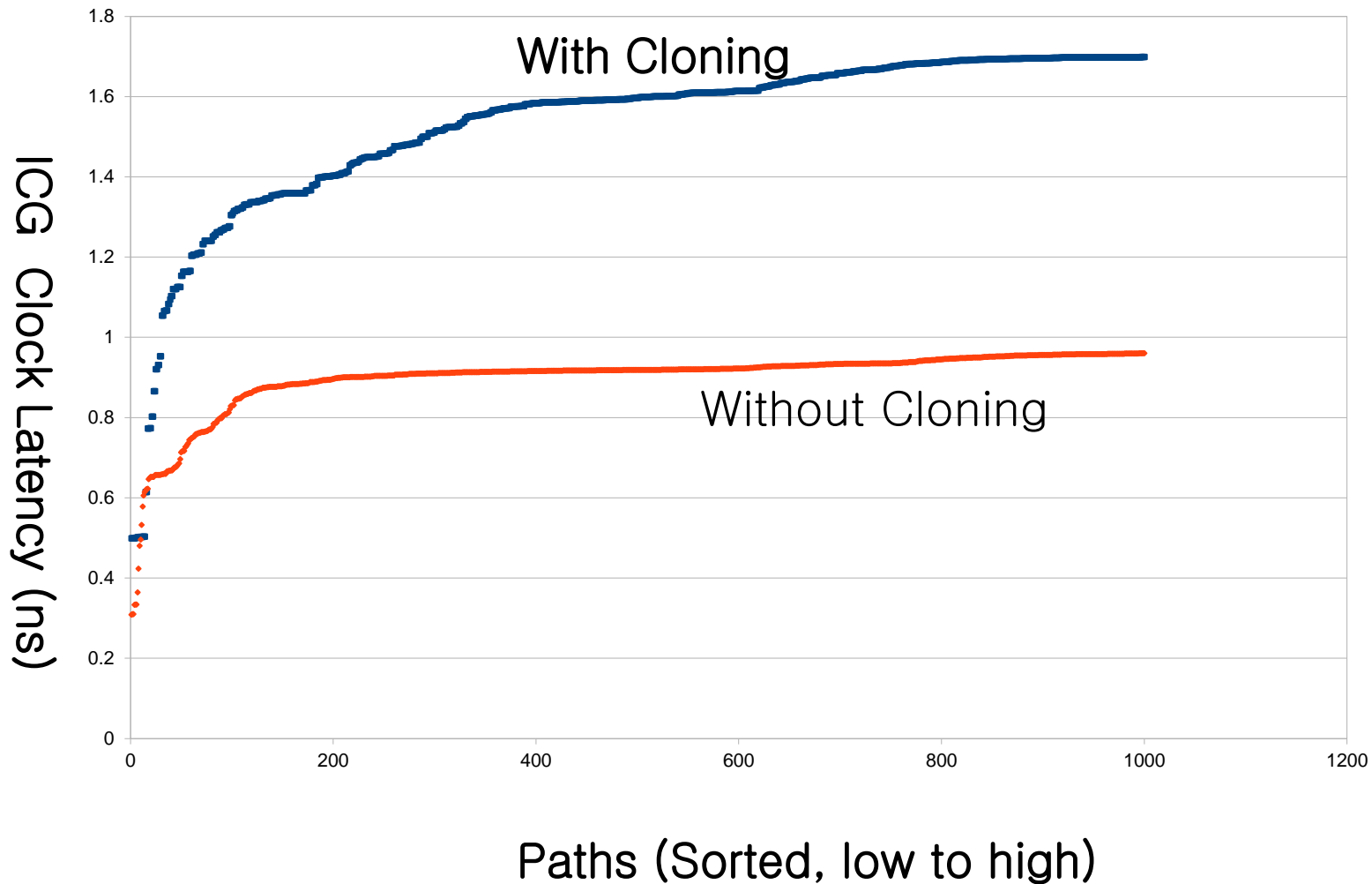Proceedings of the 11th Int'l Symposium on High-Performance Computer Architecture (HPCA-11 2005)
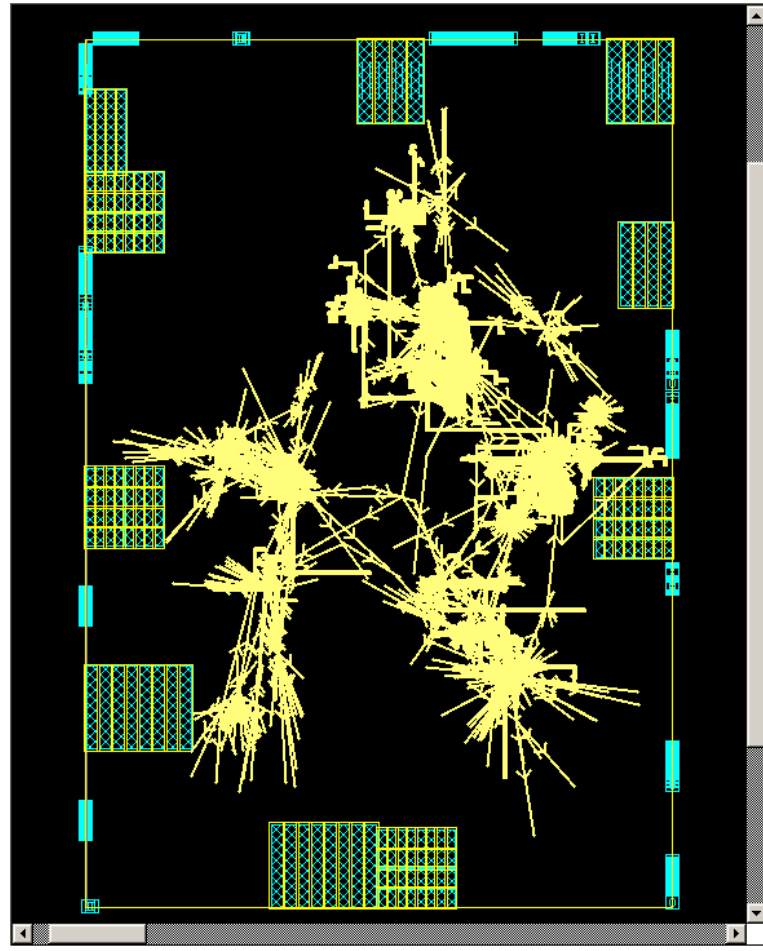
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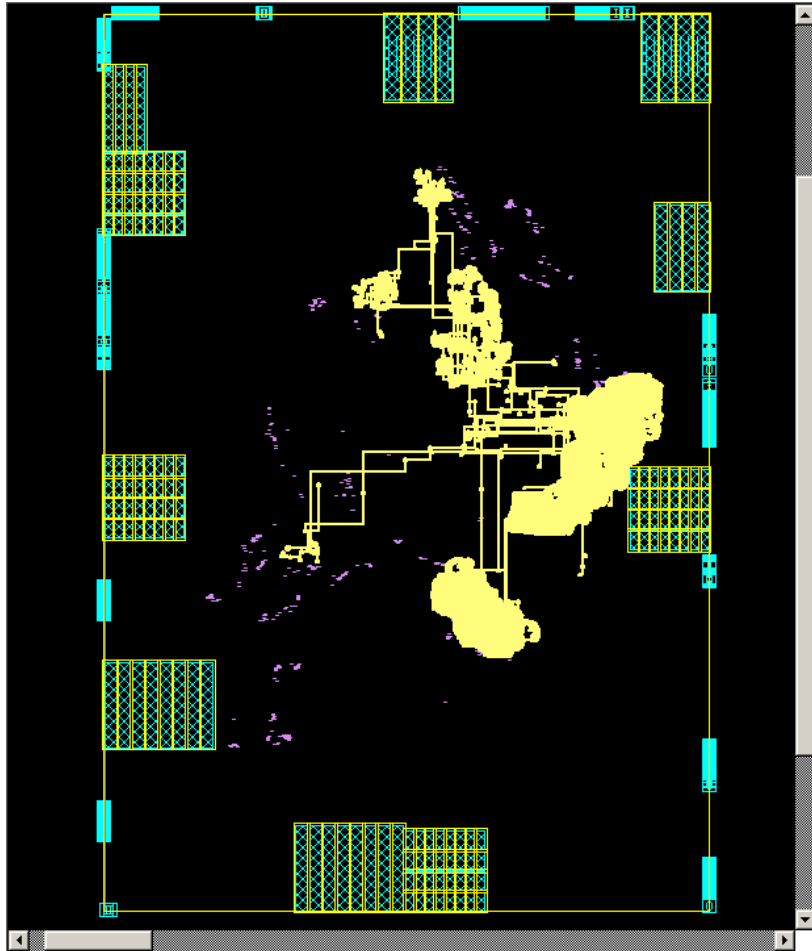# ICG Cells and Flops Autobound

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Comparing Latency Schemes

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Results – Effect on cloning on latency

With Cloning

Without Cloning

ICG Clock Latency (ns)

Paths (Sorted, low to high)

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Clock Subtree After Cloning

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Comparing Single Pass and Two pass flow

place_opt
clock_opt
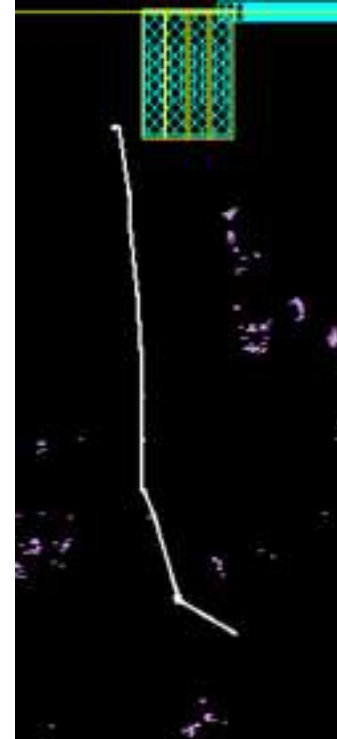
place_opt
clock_clone
new place_opt
clock_opt

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Different schemes to minimize latency

Path number (Sorted)

Selective Latency + clock split + useful skew + 2 pass

Selective Latency + clock split + useful skew

Selective latency

Base line run

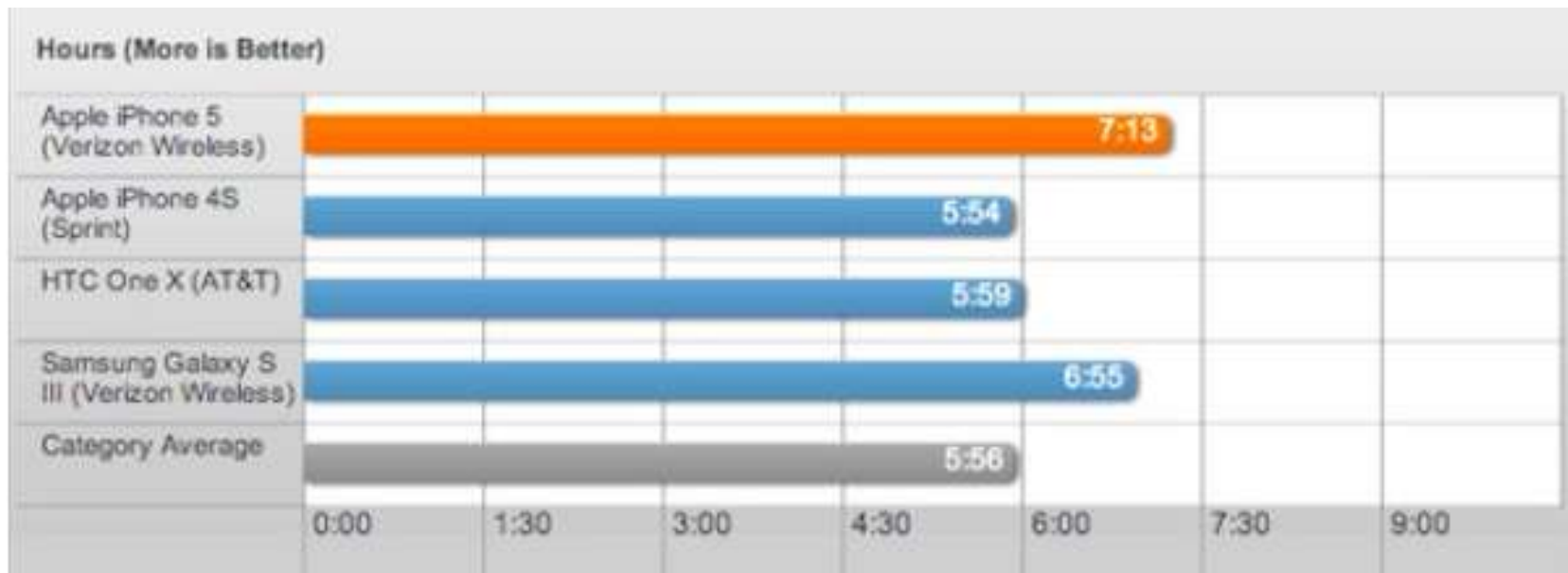CE violations (ns)

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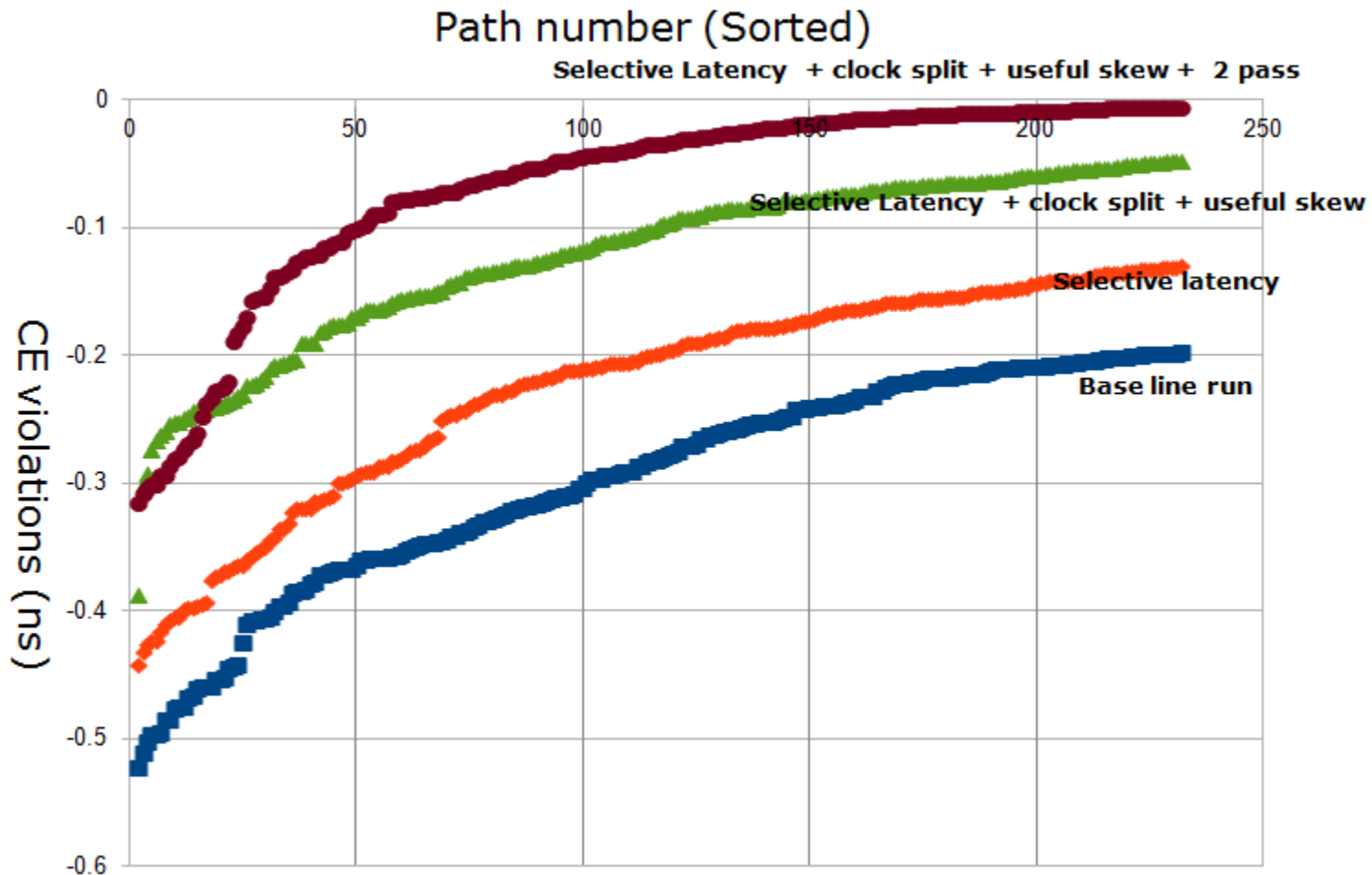
Conclusion

- Clock gating is requirement for low-power design

- Closing CE timing requires to pay attention at all stages of design

- By planning at every step, CE timing can be closed in high-speed low-power designs

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Thank You !

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BACKUP SLIDES

BACKUP SLIDES

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Battery Life is Important

Hours (More is Better)

	Hours
Apple iPhone 5 (Verizon Wireless)	7:13
Apple iPhone 4S (Sprint)	5:54
HTC One X (AT&T)	5:59
Samsung Galaxy S III (Verizon Wireless)	6:55
Category Average	5:56

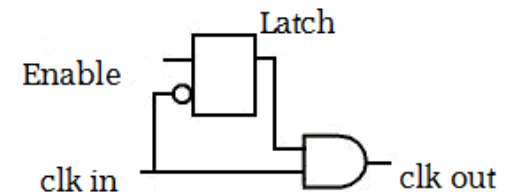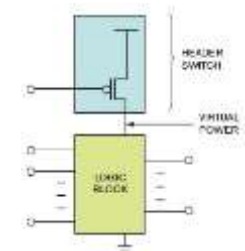**Smartphone power for continuous web access**

http://www.phonesreview.co.uk/2012/09/26/iphone-5-vs-samsung-galaxy-s3-battery-life-confrontation/
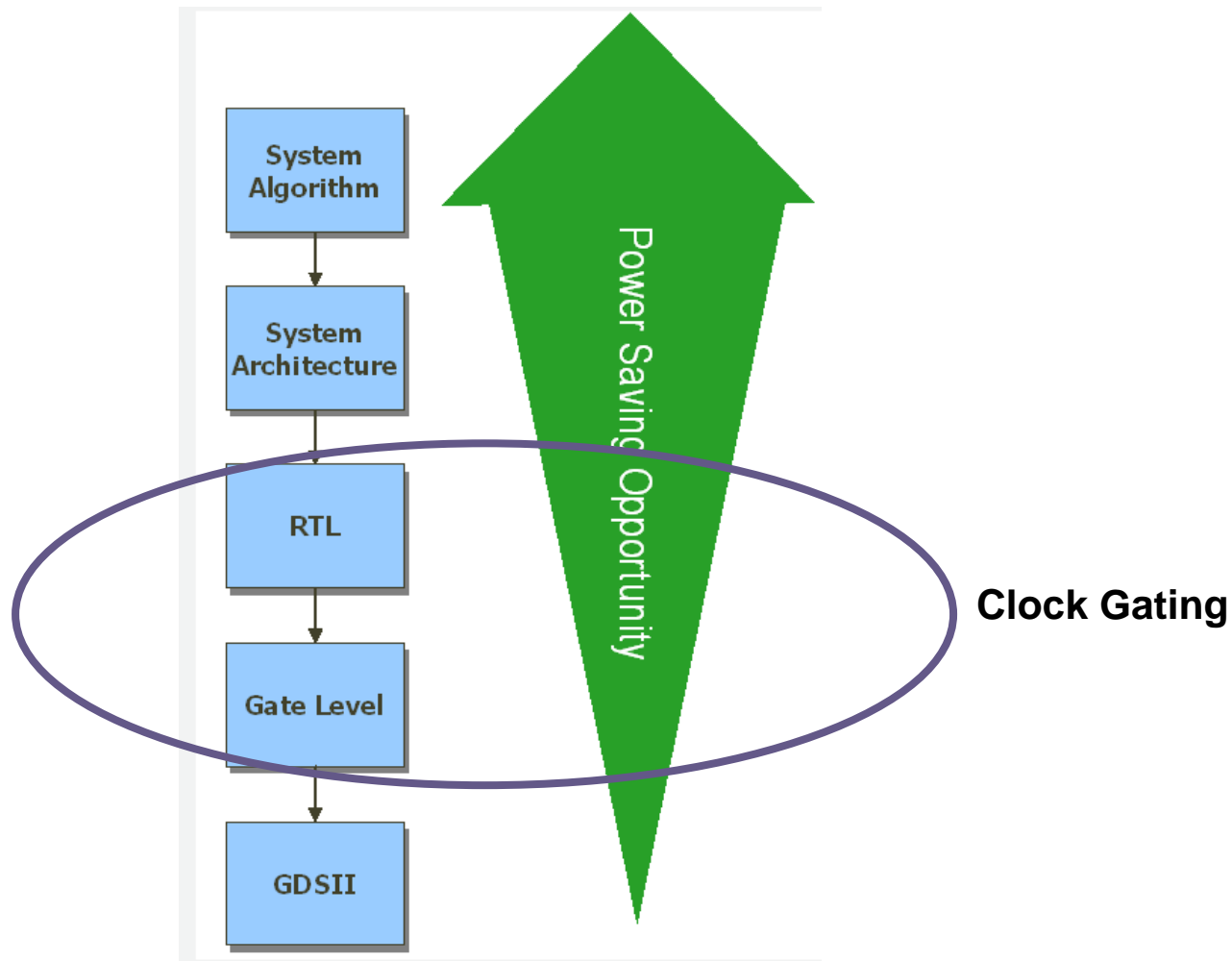
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How to Minimize Power

- Use process designed for low power

- Use low power architecture

- User power-gating

- Use Clock-gating

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Power Saving Opportunity

System Algorithm → System Architecture → RTL → Gate Level → GDSII

Power Saving Opportunity

Clock Gating

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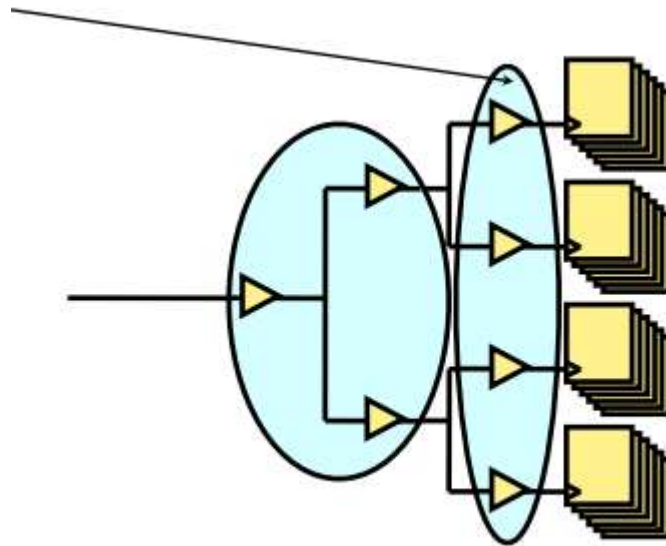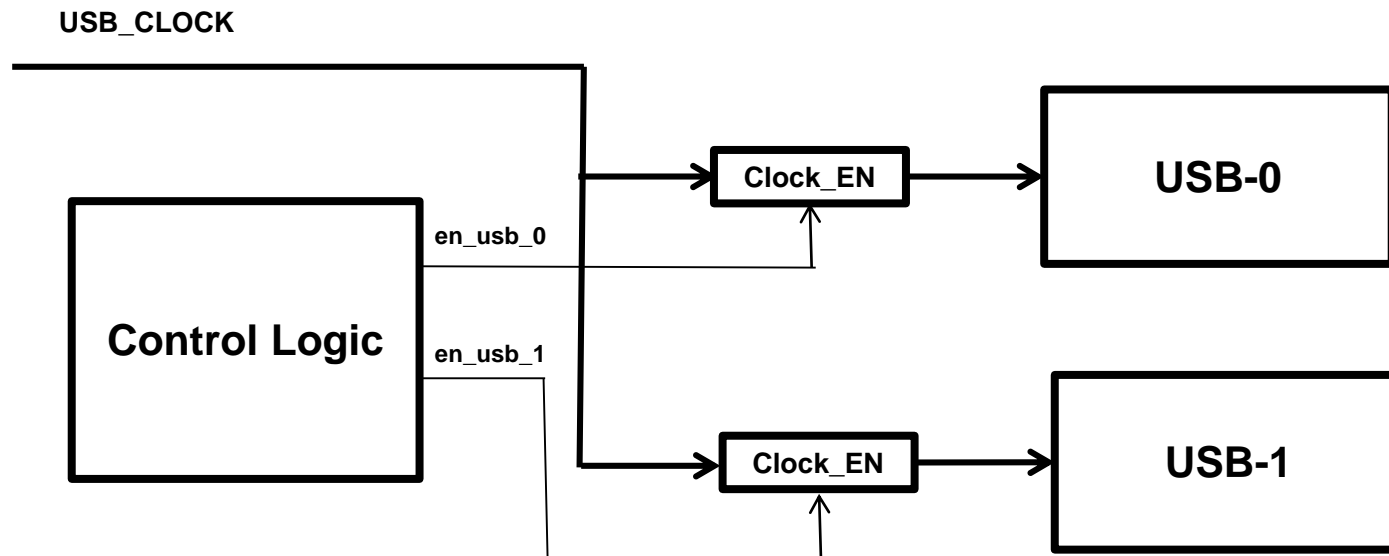
Few Facts About Clock Tree Power
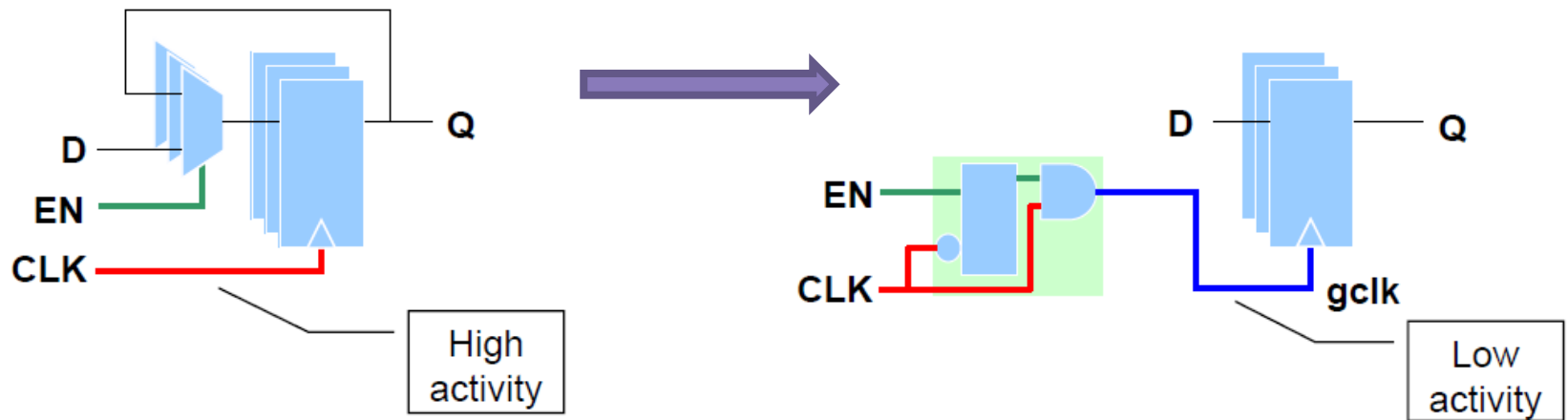
- 20% to 40% Dynamic power is consumed by clock tree

- About 80% clock tree power is consumed last stages of clock tree

Ref – ISPLED, 2008

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Architectural/Corse Grain Clock Gating

USB_CLOCK

Control Logic

en_usb_0

en_usb_1

Clock_EN

Clock_EN

USB-0

USB-1

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Automated/Fine Grain Clock Gating

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Example of Automated/Fine Grain Clock Gating

```
************************************************
Report : clock_gating
          -nosplit
Design : red_blk
Version: F-2011.09-SP5-1
Date   : Fri Aug 17 23:27:06 2012
************************************************


                    Clock Gating Summary
      ------------------------------------------------------
      | Number of Clock gating elements  |      3133       |

      | Number of Gated registers        |  26738 (76.90%) |

      | Number of Ungated registers      |  38077 (23.10%) |

      | Total number of registers        |     164815      |
      ------------------------------------------------------
```
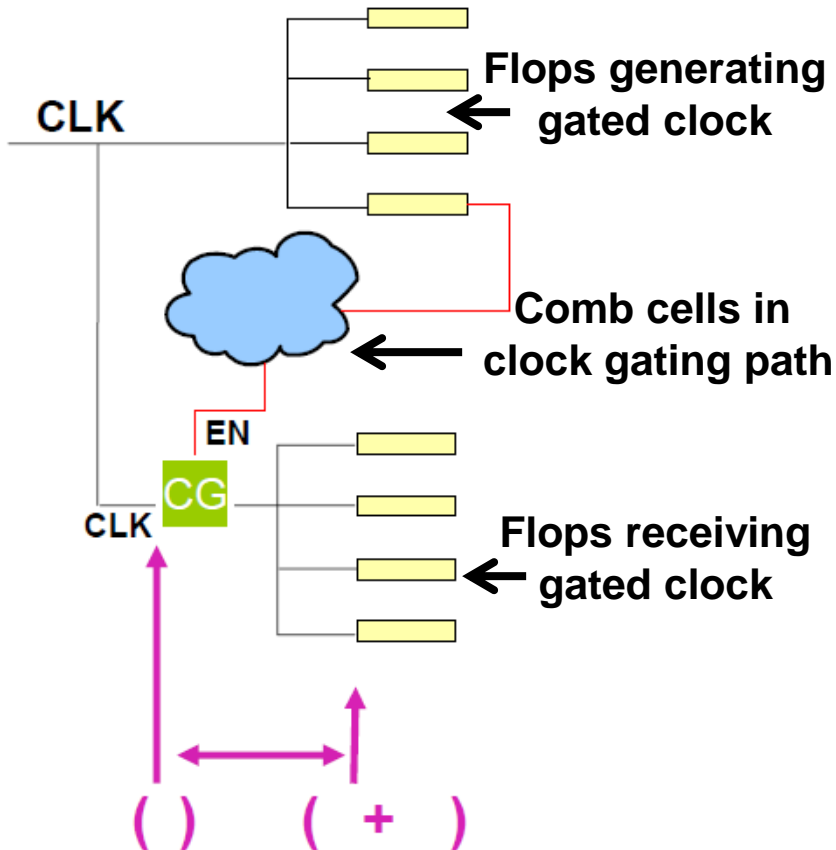
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What To Look For In ICG

Flops generating gated clock

CLK

Comb cells in clock gating path

EN

CG

CLK

Flops receiving gated clock

( )   (+)

- Too many flops used for generating CE signal

- Large delay in combinational path

- Generating flops placed away from ICG cells

- Flops used to generated ICG signal placed away from each other

- Too man flops receive gated clock

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What To Look For In ICG

Flops generating gated clock

Comb cells in clock gating path

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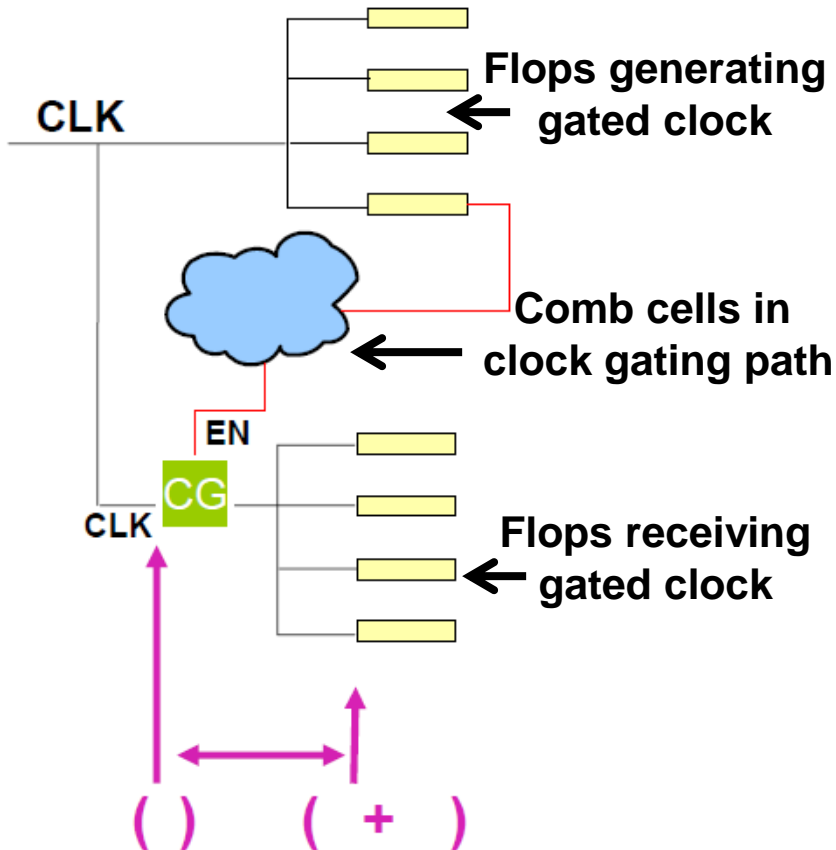
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What To Look For In ICG

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