A Top-Down Synthesis Methodology for Flow-Based Microfluidic Biochips Considering Valve-Switching Minimization

2013 ACM International Symposium on Physical Design

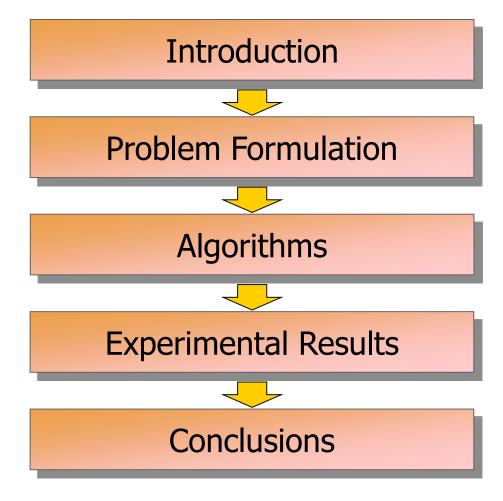
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Outline





What is Biochips?

General definition

 A chip with a small solid platform made of glass, plastic, or membrane which deals with the behavior, precise control and manipulation of fluids that are constrained to a small scale

Functionality

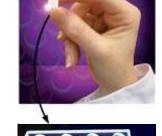
 Analysis, reaction, or detection of biological samples (DNA or human blood)

Application

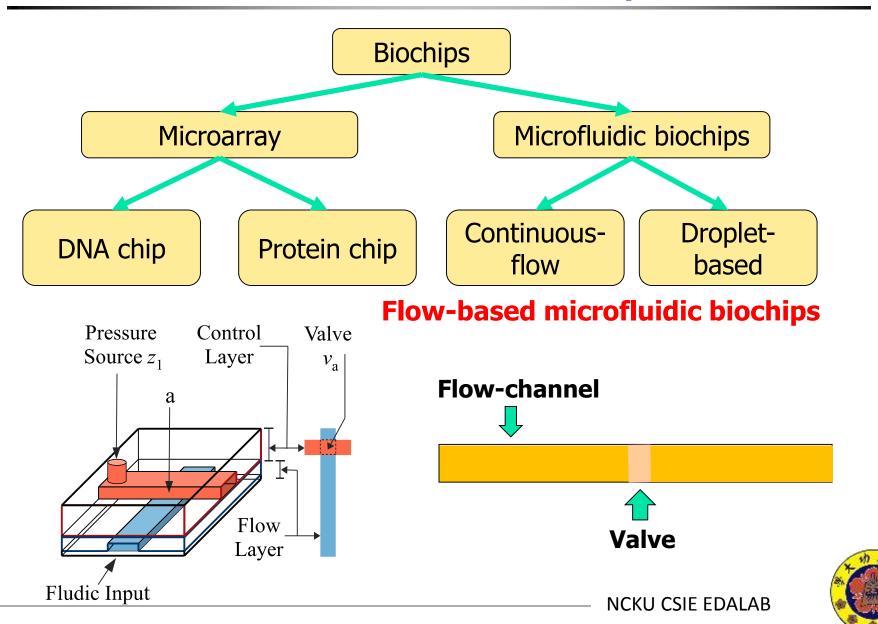
- Clinical diagnostics
- Environmental monitoring
- Automated drug discovery
- Cell culturing
- Protein crystallization







Classification of Biochips



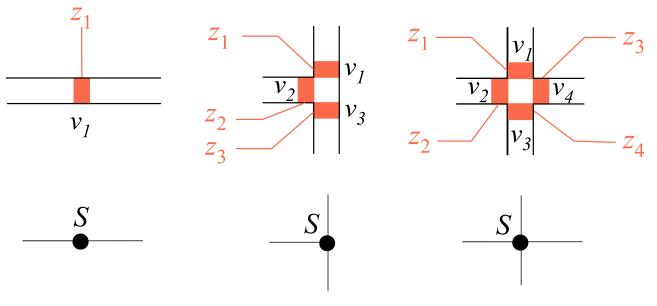
Valve: The Basic Unit of Flow-based Microfluidic Biochips

Functional component

Valves can be combined to form more complex units,
 e.g., latches, switches, mixers, multiplexers, micropumps

Reliability

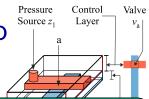
 The open and close activities (valve-switching) for a valve is limited





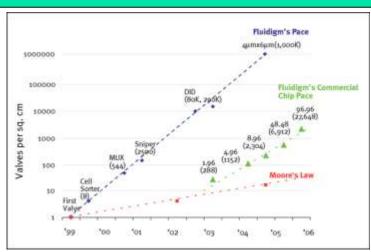
The Need of CAD Support

- Applications become more complicated
 - Large-scale bioassays
 - Multiple and concurrent assay operations on a biochip



A top-down synthesis methodology is needed

- Current methodologies
 - Manual
 - Full-custom

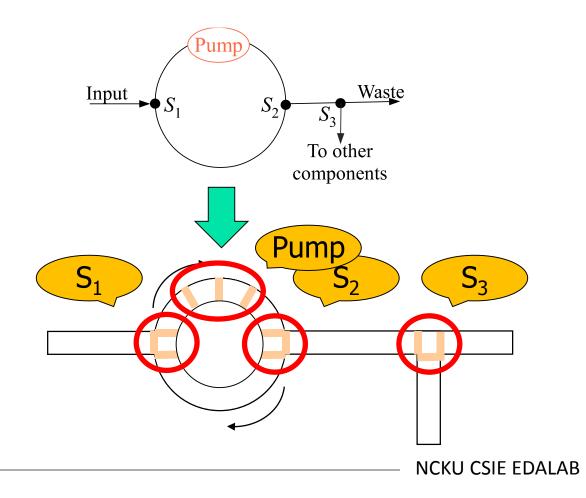


Source: Fluidigm



Component Model: Mixer

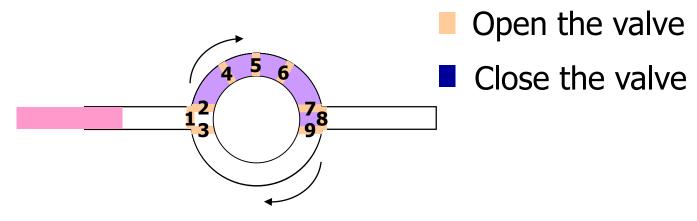
Microfluidic mixer





Motivation

Microfluidic mixer

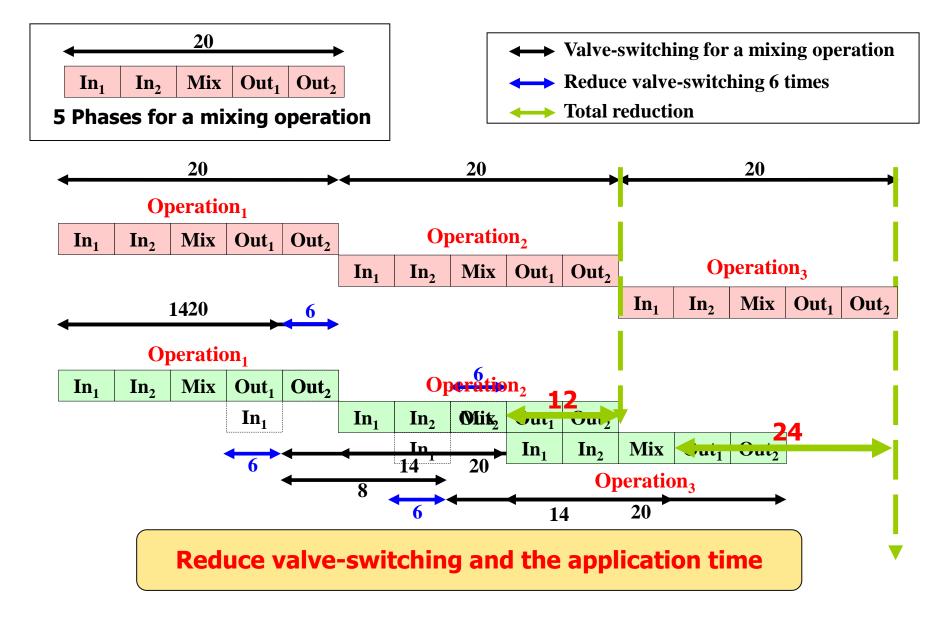


Valve-switching: 20 + Mixing

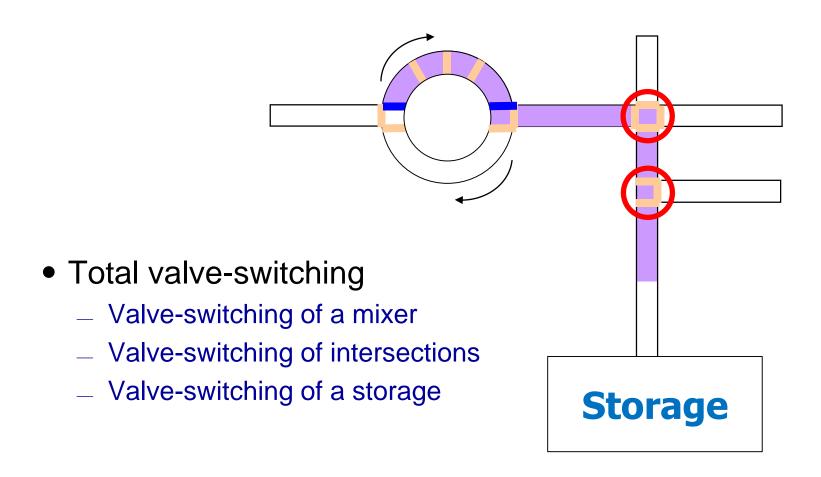
Phase	V ₁	V ₂	V ₃	V ₄	V ₅	V ₆	V ₇	V ₈	V ₉
1. lp1	0	0	0	0	0	0	0	0	0
2. lp2	0	0	0	0	0	0	0	0	0
3. Mix	D	0	0	Mix	Mix	Mix	0	0	0
4. Op1	0	0	0	0	0	0	0	0	0
5. Op2	0	0	•	0	0	0	0	0	



Group Continuous Operations

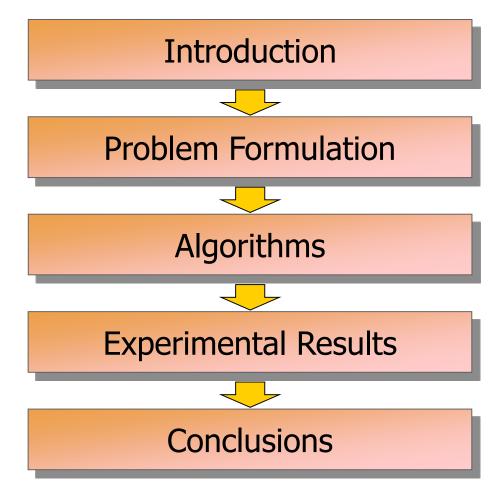


Transportation Issue





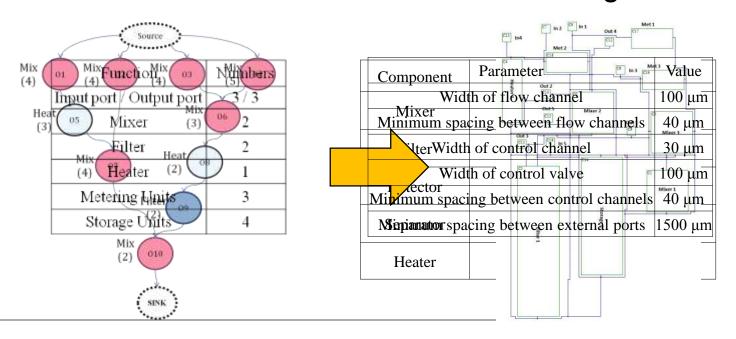
Outline





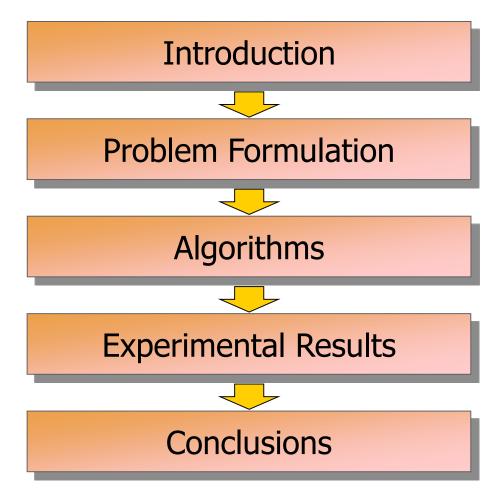
Problem Formulation

- Input: A biochemical application modeled as a sequential graph and a component library
- Objective: Synthesize a flow-based microfluidic biochip such that the valve-switching amount and application completion time are minimized
- Constraint: Resource constraints and design rules



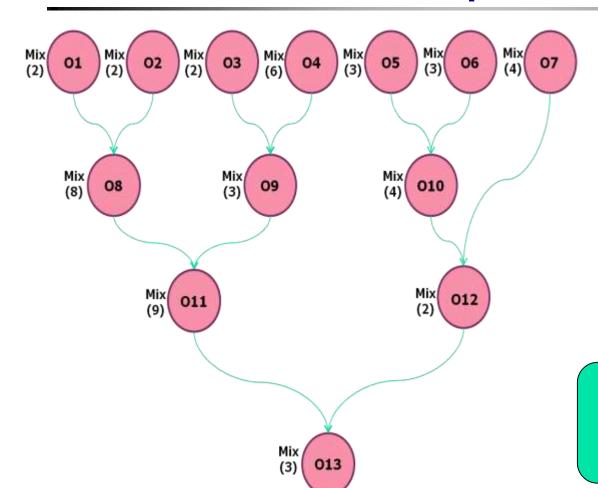


Outline





Input



Component	Phases
Mixer	$Ip_1/Ip_2/Mix/Op_1/Op_2$
Filter	Ip/Filter/Op ₁ /Op ₂
Detector	Ip / Detect / Op
Separator	Ip ₁ / Ip ₂ / Separat/ Op ₁ / Op ₂
Heater	Ip/Heat/Op

Component Library

Mixer: 3

Application Graph

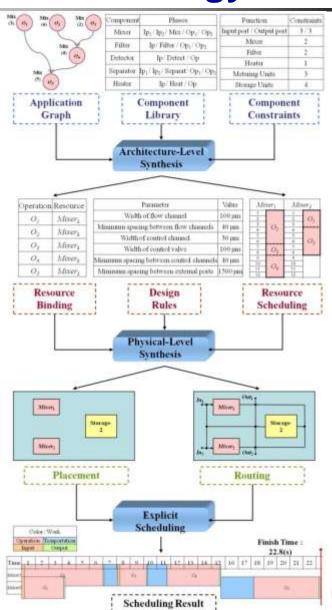
Resource Constraint

NCKU CSIE EDALAB



Top-Down Synthesis Methodology

- Architecture-level synthesis
 - Set-based minimum cost maximum flow (SMCMF)
 - Resource binding
 - Resource scheduling
- Physical-level synthesis
 - Incremental cluster expansion (ICE)
 - Placement
 - Routing
- Explicit scheduling
 - List-scheduling based approach
 - Total valve-switching amount
 - Application completion time





Set-based Minimum Cost Maximum Flow

Set-based

 Group continuous operations in a set to reduce the valveswitching activities

Maximum Flow

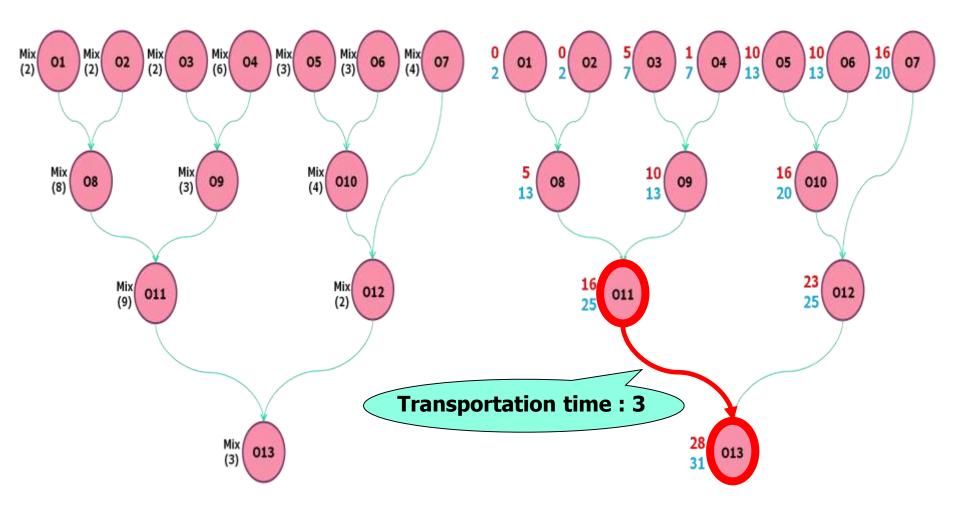
 Each flow path represents a component. Our goal here is to maximize the component parallelization.

Minimum Cost

 Find a way that not only satisfies the parallelization but also minimize the application completion time

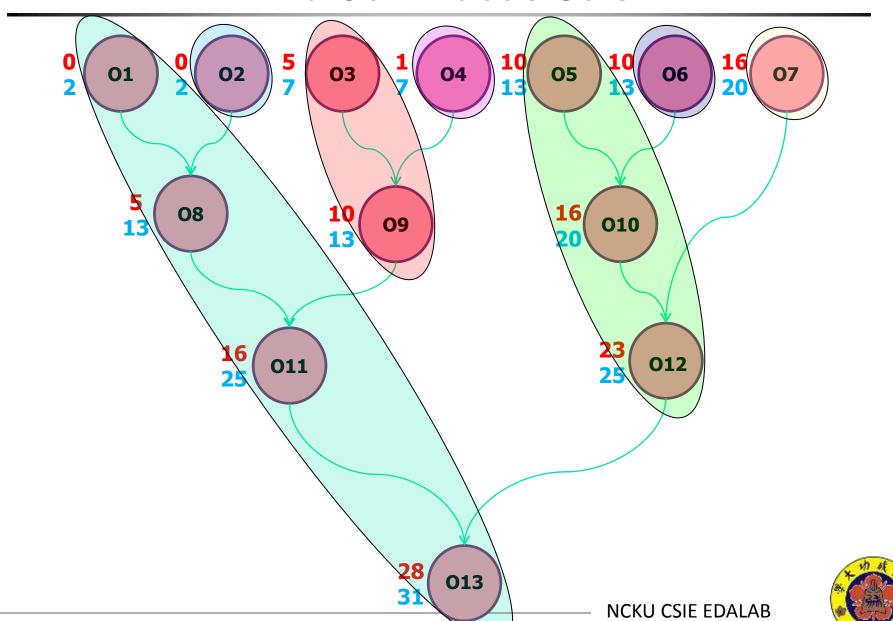


Time Evaluation



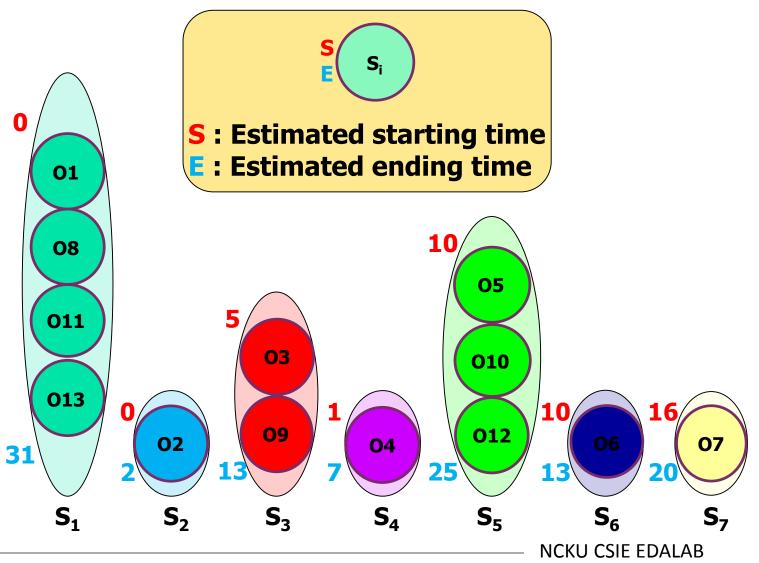


Find Continuous Sets



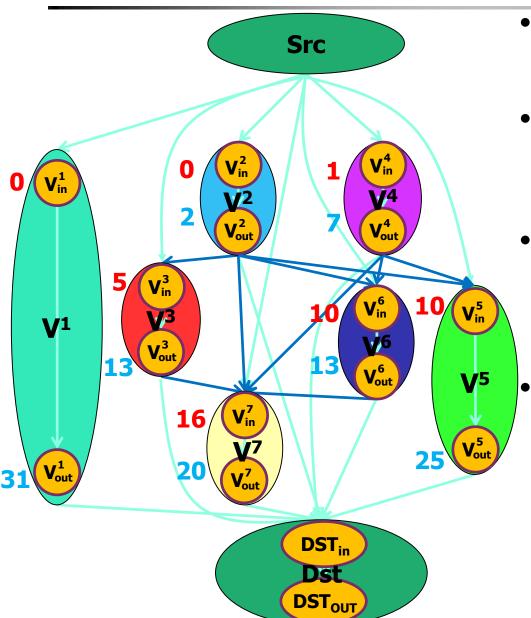


Continuous Sets





Build the Flow Network



Step1

- Create Src and Dst vertex
- Create a vertex Vi ε V for each Si

• Step2

- Separate Vⁱ → (Vⁱ_{in}, Vⁱ_{out})
- Create a directed edge Vⁱ_{in} → Vⁱ_{out}, cost=0 and capacity=1

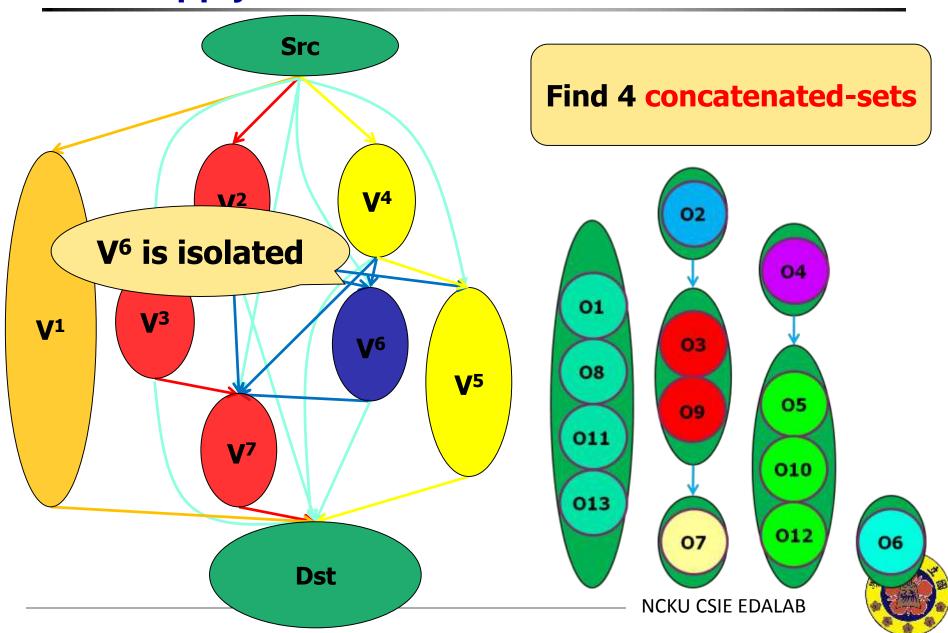
• Step3

- Separate Dst → (Dst_{in}, Dst_{out})
- Create a directed edge Dst_{in} → Dst_{out}, cost=0 and capacity=3 (given component numbers)

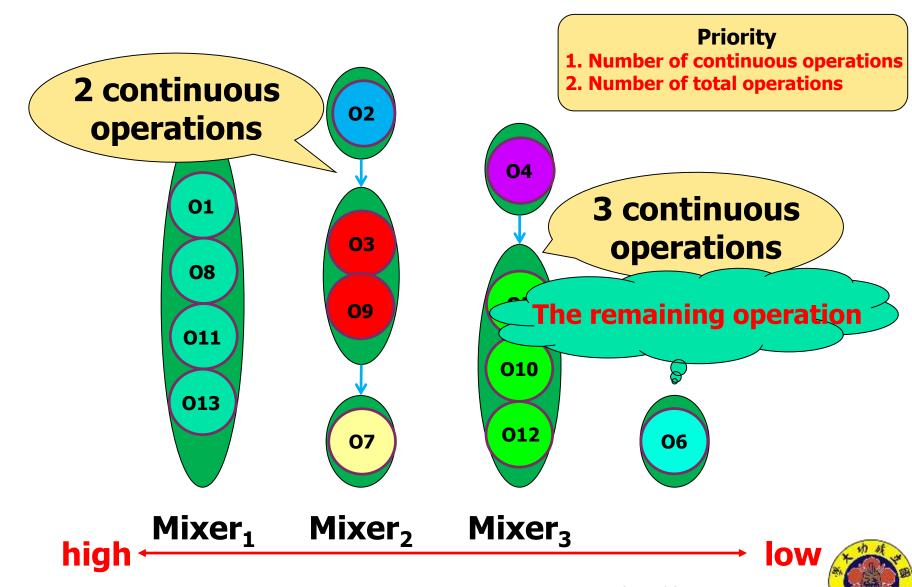
Step4

- − Create directed edges $Src \rightarrow V_{in}^{i}$ and $V_{out}^{i} \rightarrow Dst_{in}$, cost = 0 and capacity=1
- For each V_{out} and V_{in}, if V_{out} + T (transportation time) ≤ V_{in}, create a directed edge V_{out} → V_{in}, cost=f(x) and capacity=1. Here, x is defined as |(V_{out} -V_{in})| and f is proportional to x

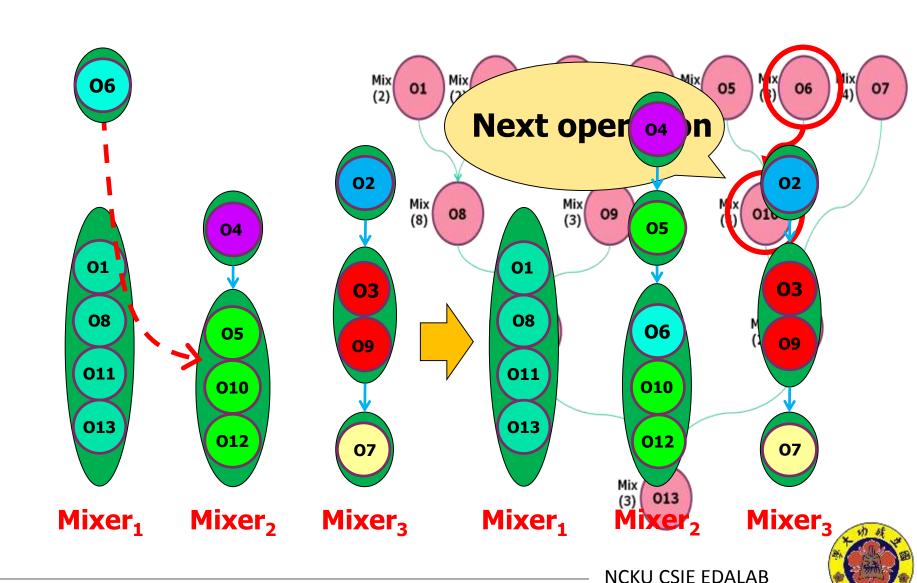
Apply Minimum Cost Maximum Flow



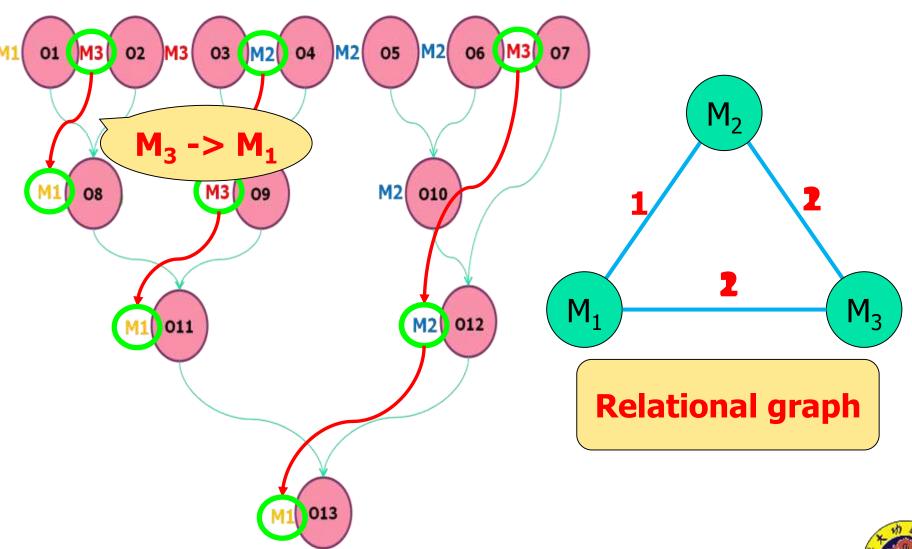
Sort by the Priority



Insert the Remaining Operation



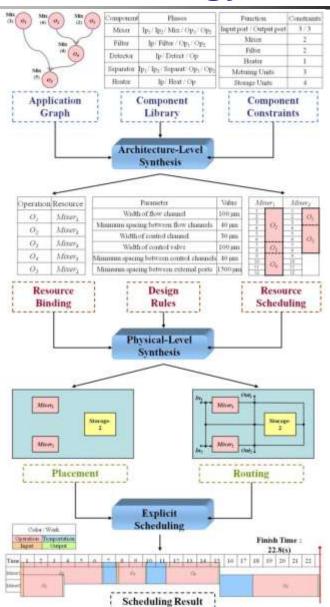
Relational Graph





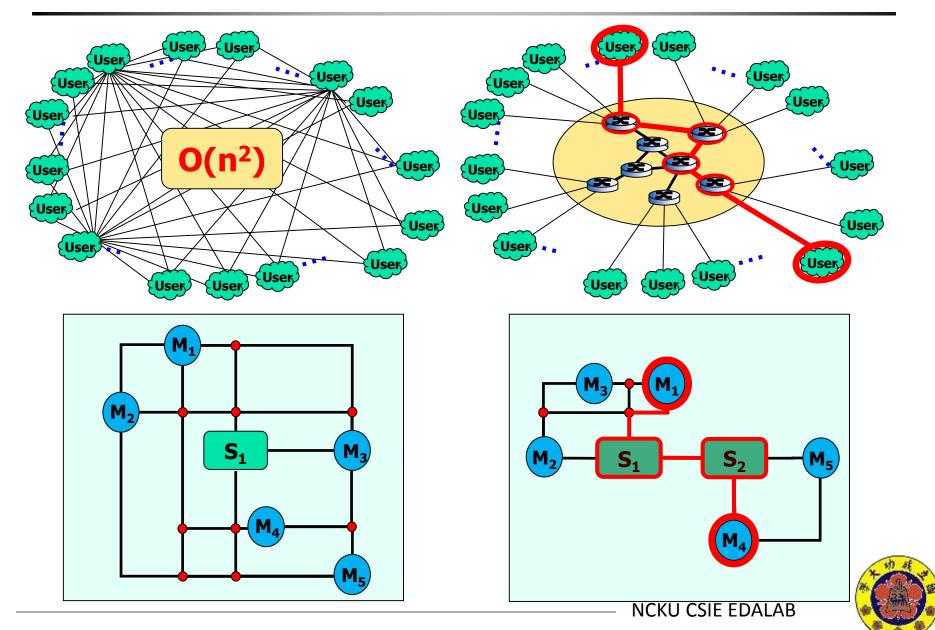
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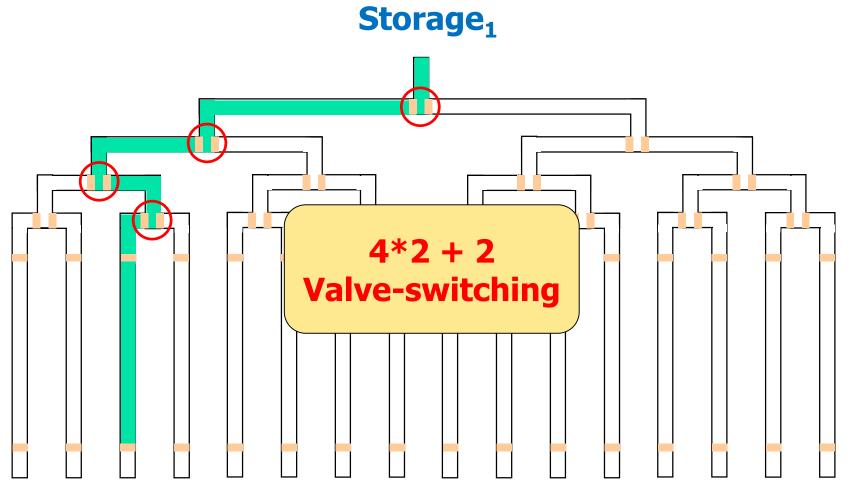




Motivation

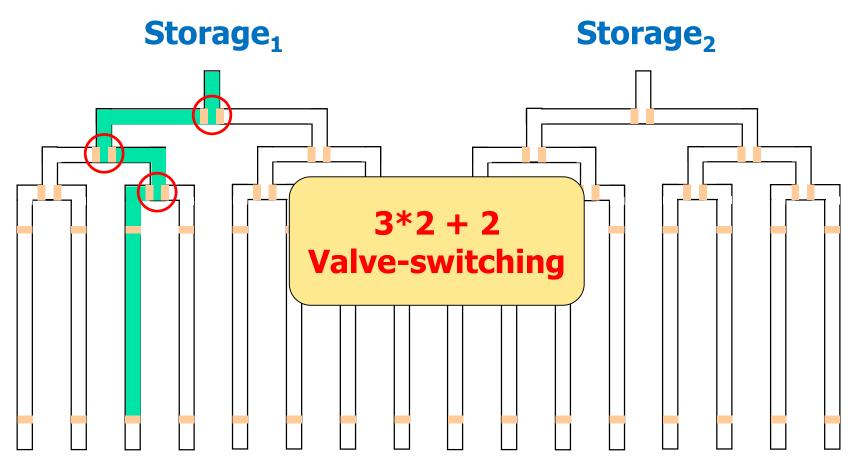


One Storage



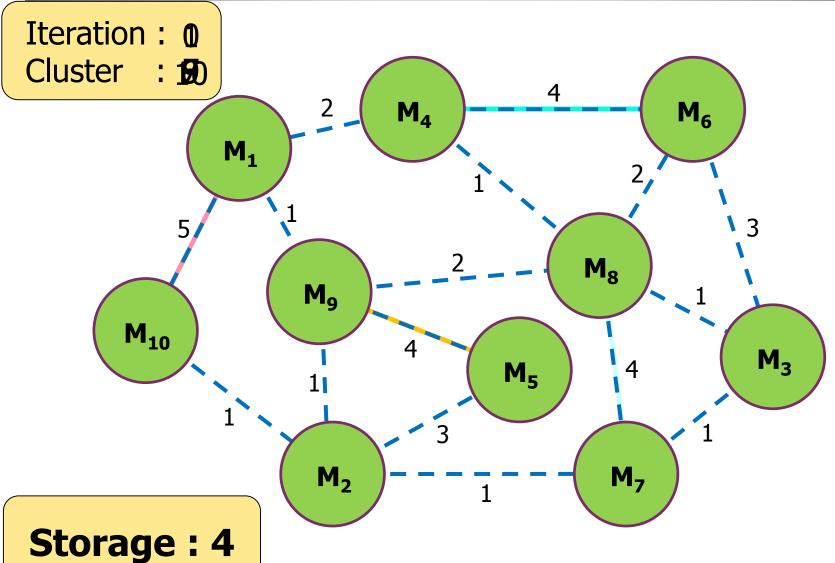


Two Storage



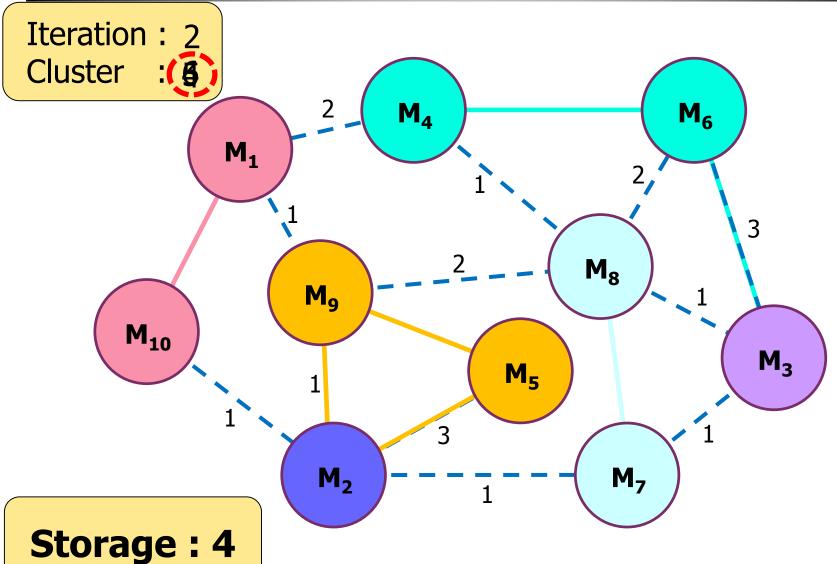


Find the Clusters



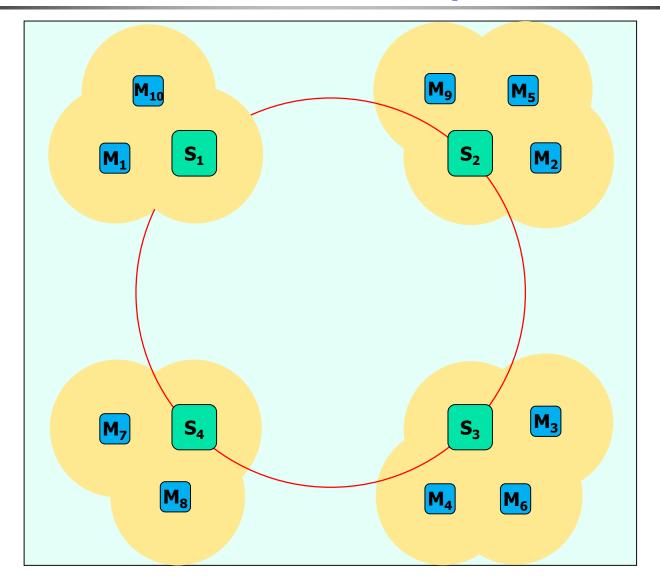


Find the Clusters



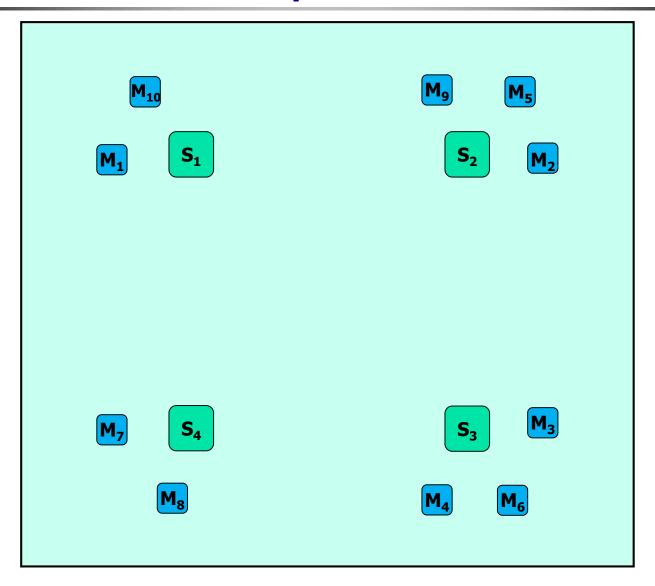


Incremental Cluster Expansion



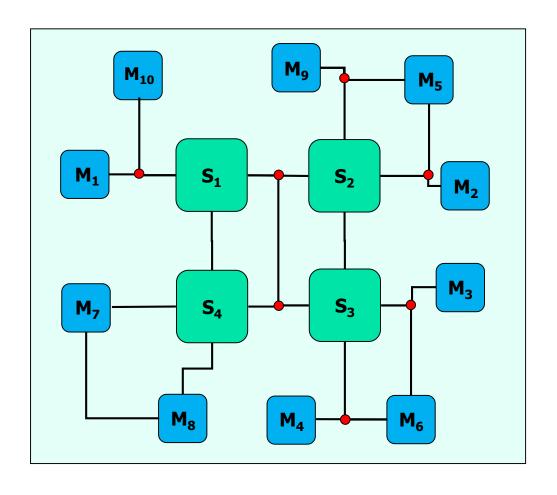


Compaction



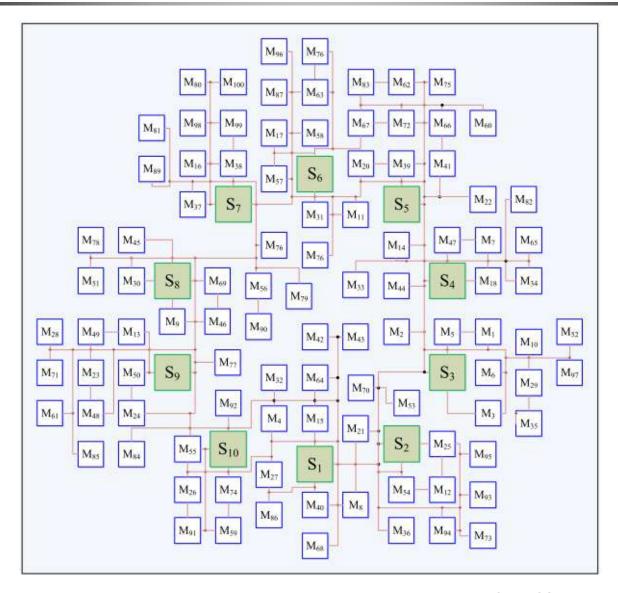


Routing by dijkstra's algorithm





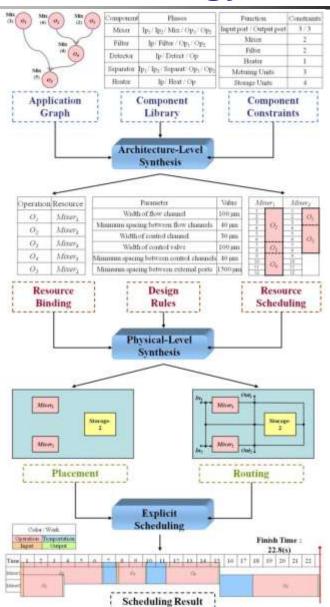
100 Mixers and 10 Storages





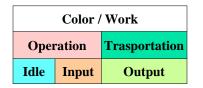
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 - Total valve-switching amount





Explicit Scheduling



Valve-switching amount 250 (62,188) **Application Completion Time: 28.5(s)**

Binding by SMCMF

Time	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		
Mixer1	Op1 Op8												Op11													Op13				
Mixer2	Op4								Op) 5			O	р6					Op	10			Op	12						
Mixer3	C	Op2 Op3								Op9			Op7														R	le)(

Reduce 140 valve-switching

29 30 31 32 33 34 35

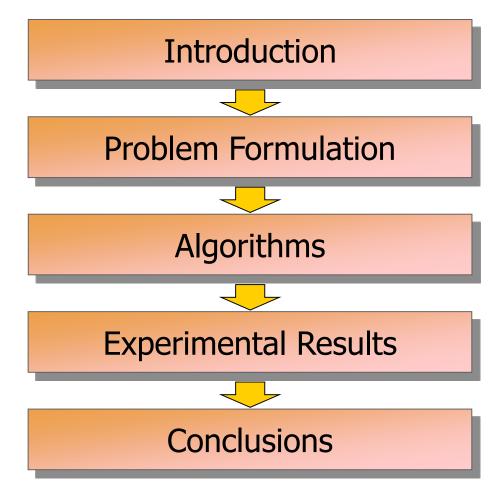
Binding by baseline method

Time	1	l	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	
Mixer1	1	O	p1			Op3					Op5	5			Op9					Op10												()p13				
Mixer2	2	O	p2						O	p8														Op1	1												
Mixer3	3			C)p4					Op	6			() p7					Ор												. — 1					

Valve-switching amoun (390(166,224) **Application Completion Time : 33.2(s)**



Outline





Experimental Settings

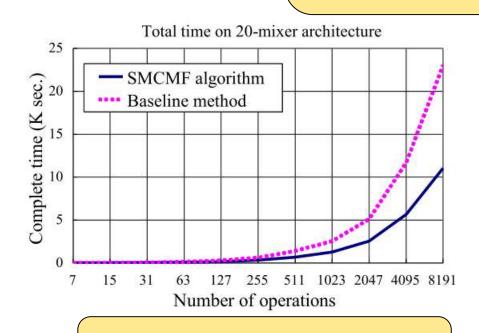
- Implemented our algorithm in C++ language on a PC with Core2 Quad processors at 2.66GHz and 3.25GB of RAM
- Compared set-based minimum cost maximum flow binding algorithm with list scheduling based binding algorithm (baseline method) on top-down synthesis methodology
- Tested on several synthetic benchmarks by
 - Adjusted operation numbers from 7 to 8191 and fixed mixers as 20 and storage as 1
 - Adjusted mixers from 10 ~ 100 and fixed operation numbers as 1023 and storage as 1
 - Adjusted storage from 1 ~ 10 and fixed operation numbers as 1023 and mixer as 100

Experimental Results (1/3)

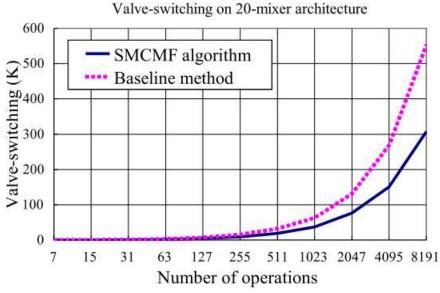
Operation : **7~8191**

Mixer: 20

Storage: 1



Application Completion Time



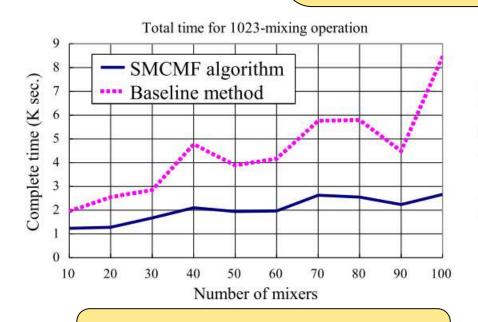
Valve-switching Amount

Experimental Results (2/3)

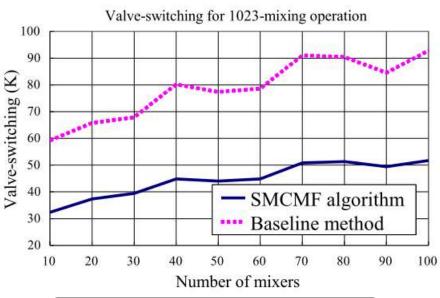
Operation: 1023

Mixer : **10** ~ **100**

Storage: 1



Application Completion Time



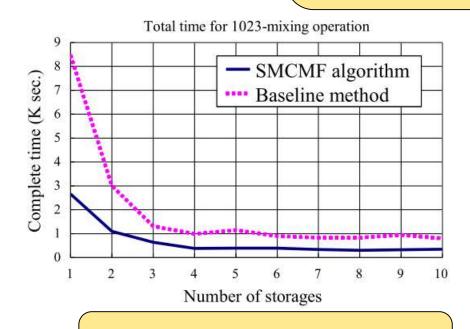
Valve-switching Amount

Experimental Results (3/3)

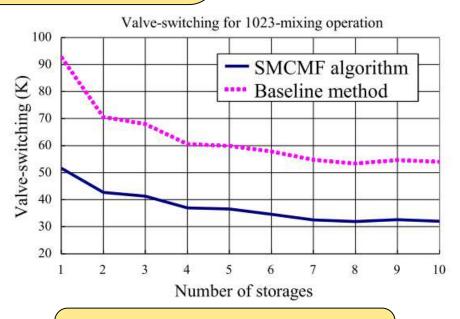
Operation: 1023

Mixer: 100

Storage : **1 ~ 10**

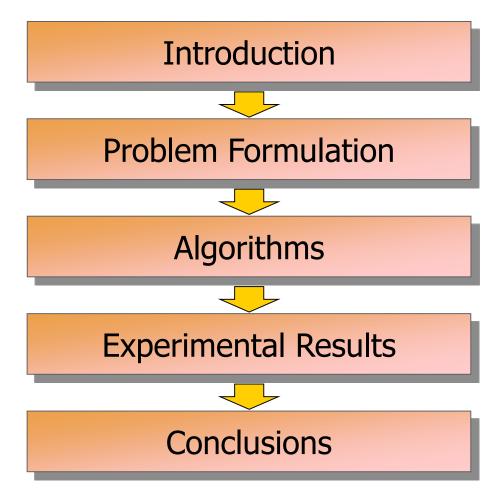


Application Completion Time



Valve-switching Amount

Outline





Conclusions

- The valve-switching activities for the components such as mixer and storage were modeled
- A first top-down synthesis methodology for flow-based microfluidic biochip was presented
- Two algorithms for architecture-level synthesis and physical-level synthesis were proposed
 - Set-based minimum cost maximum flow (SMCMF)
 - Incremental cluster expansion (ICE)
- The experimental results showed that our top-down synthesis methodology not only minimized the valveswitching amount but also reduced the application completion time



Thank You for Your Attention!

