Designing VeSFET-based ICs with CMOS-oriented EDA Infrastructure

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Outline

- Introduction
- Chain Canvas
- Standard cell based physical design flow
- Chain Canvas Vs. Basic Canvas
- Conclusions

Introduction

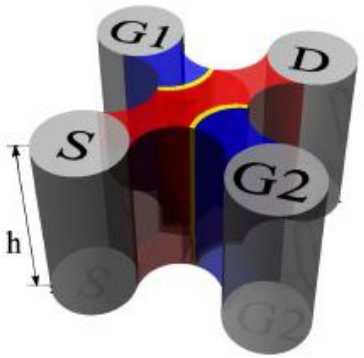
- Semiconductor markets are dominated by
  - ASICs: high NRE cost, high performance, high volume.
  - FPGAs: low NRE cost, low performance, small volume
- Medium volume?
  - VeSFET-based ASICs may fill the gap between ASICs and FPGAs. [1][2]
- New technology →huge efforts on design automation infrastructure.
- Can we re-use CMOS EDA infrastructure for VeSFET-based designs?
  - We focus on physical design flow in this talk.

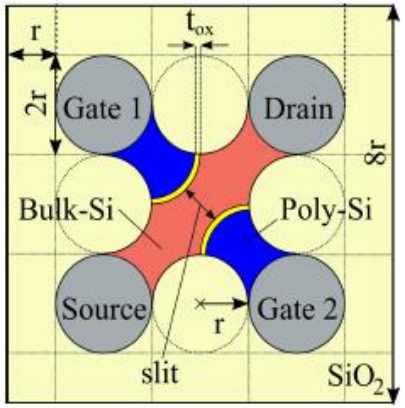
[1] W. Maly, *et. al*, *"Complementary Vertical Slit Field Effect Transistors," CMU*, CSSI Tech-Report , 2008.

[2] Y.-W. Lin, M. Marek-Sadowska, W. Maly, A. Pfitzner, and D. Kasprowicz, "Is there always performance overhead for regular canvas?" in *Proceedings of ICCD'08*, pp. 557-562, 2008.

Vertical Slit Field Effect Transistor

- 3D twin-gate transistor[1]
  - easy fabrication with SOI-like process
- Excellent electrical characteristics[2]
  - huge Ion/Ioff: 1e9
  - low DIBL: 13mV/V
  - near ideal subthreshold swing: 65mV/decade
  - low gate capacitance





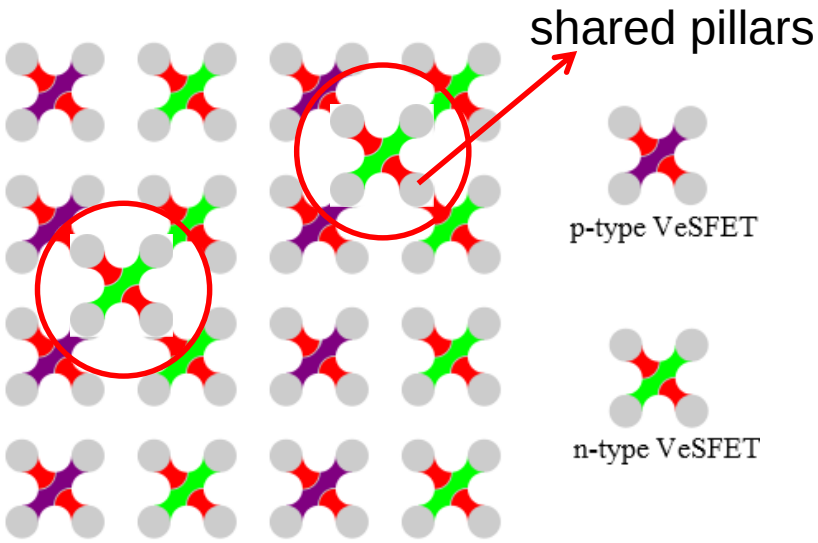
VeSFET Structure[1]

65nm VeSFET
r=50nm
h=200nm
tox=4nm
$N_{sub}= 4e^{17}/cm^3$

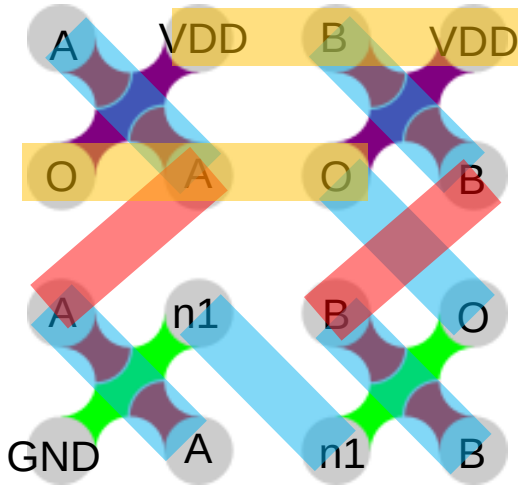
[1]. W. Maly, *et. al*, *"Complementary Vertical Slit Field Effect Transistors," CMU*, CSSI Tech-Report , 2008.
[2]. W. Maly, *et. al*, "Twin gate, vertical slit FET (VeSFET) for highly periodic layout and 3D integration," in *Proc. of MIXDES'11*, pp.145-150, 2011.

VeSFET based-IC Paradigm

- Regular layout patterns
  - Canvases: geometrically identical VeSFETs arrays
    - The same radius *r* and height *h*
  - Circuits are customized by interconnects
    - Strictly parallel wires
    - Diagonal (45- or 135-degree) wires
  - Advanced layout style: pillar sharing



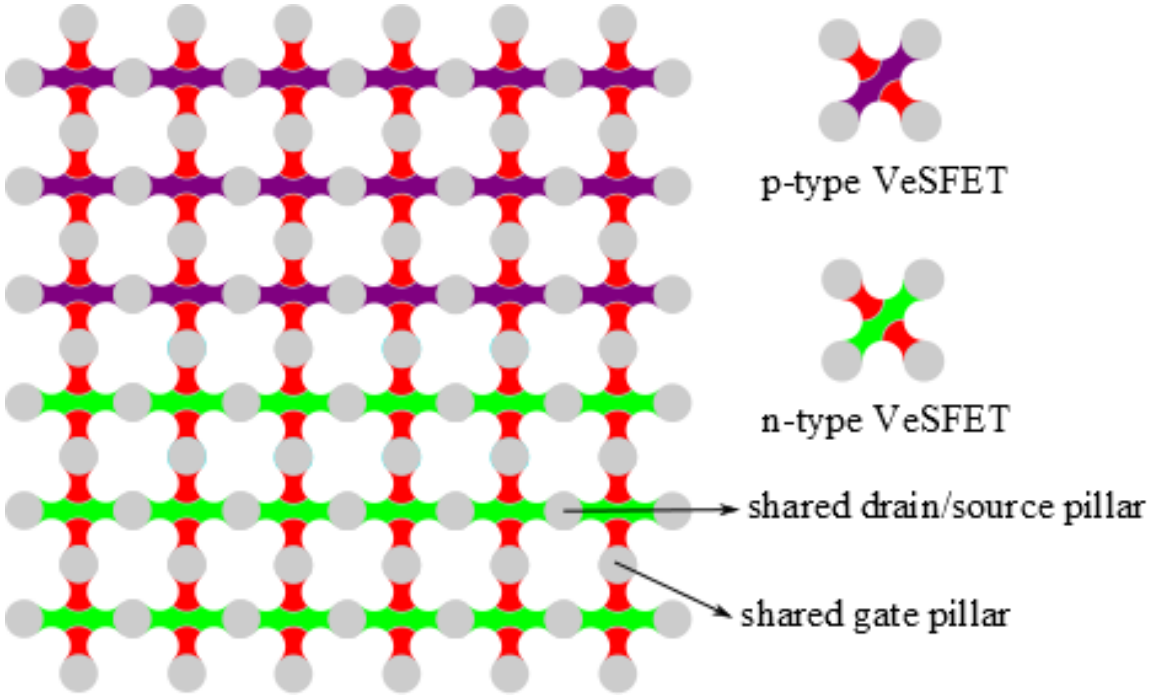
basic canvas



2-input NAND

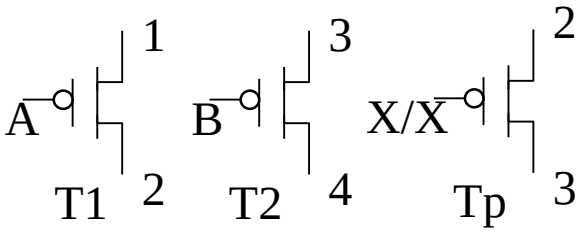
Chain Canvases

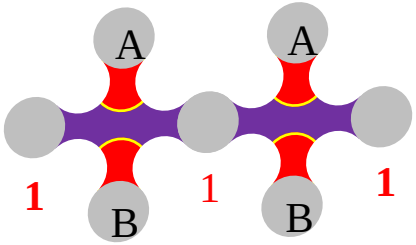
- Transistors are rotated by 45 degrees
- Each pillar is shared by two transistors
  - Transistors are chained
  - 2X transistor density
- The same interconnect design rules

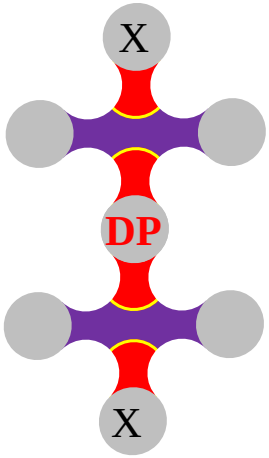


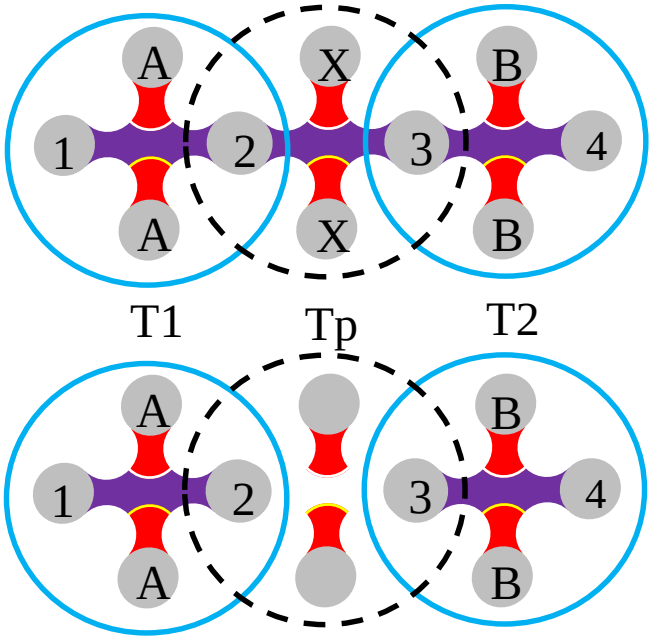
Transistor Isolation

- Some contacted transistors are unwanted.
- Isolation
  - Physical
  - Electrical
    - Apply cut-off voltage
    - Short drain and source
- Wasted area!



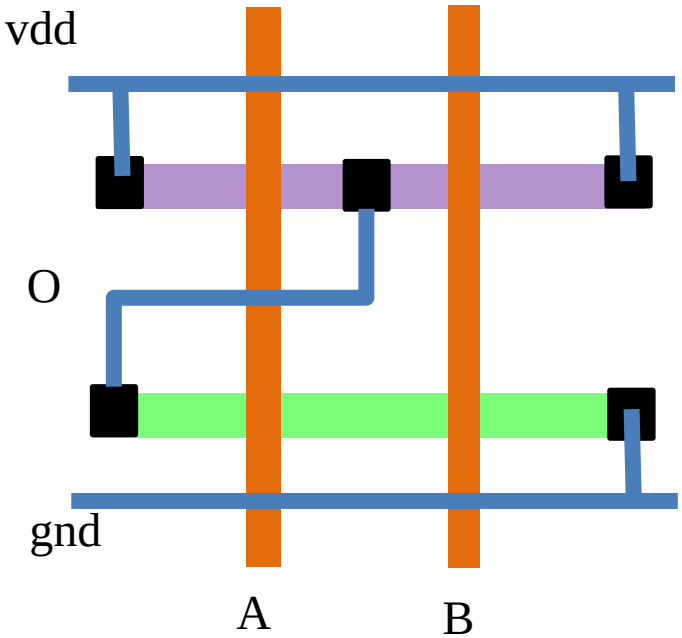




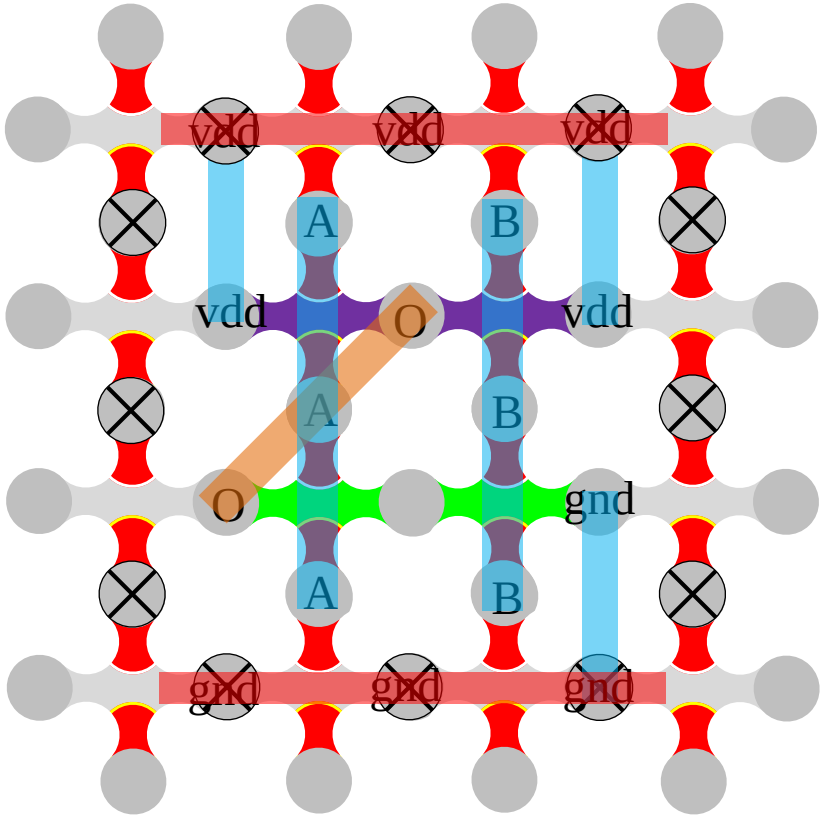


Static CMOS-like Standard Cell Generation

- CMOS-like layout patterns
  - aligned gate pillars connected by wires ⇔ aligned poly gates
  - shared drain/source pillars ⇔ diffusion abutment
- CMOS cell generation algorithms can be reused.

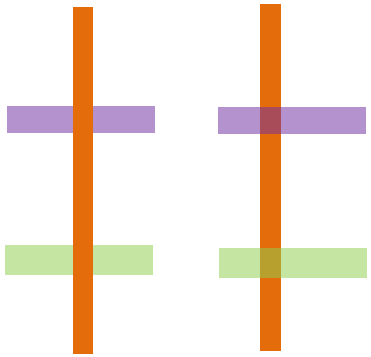


2-input NAND

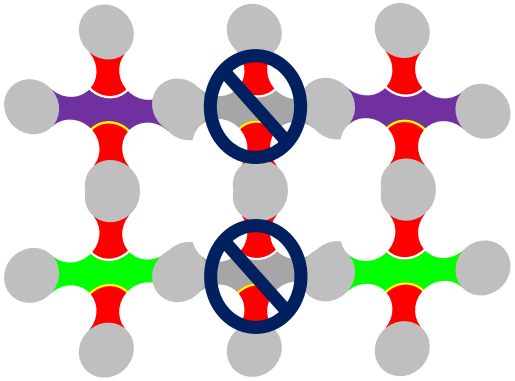


Static CMOS-like Standard Cell Generation

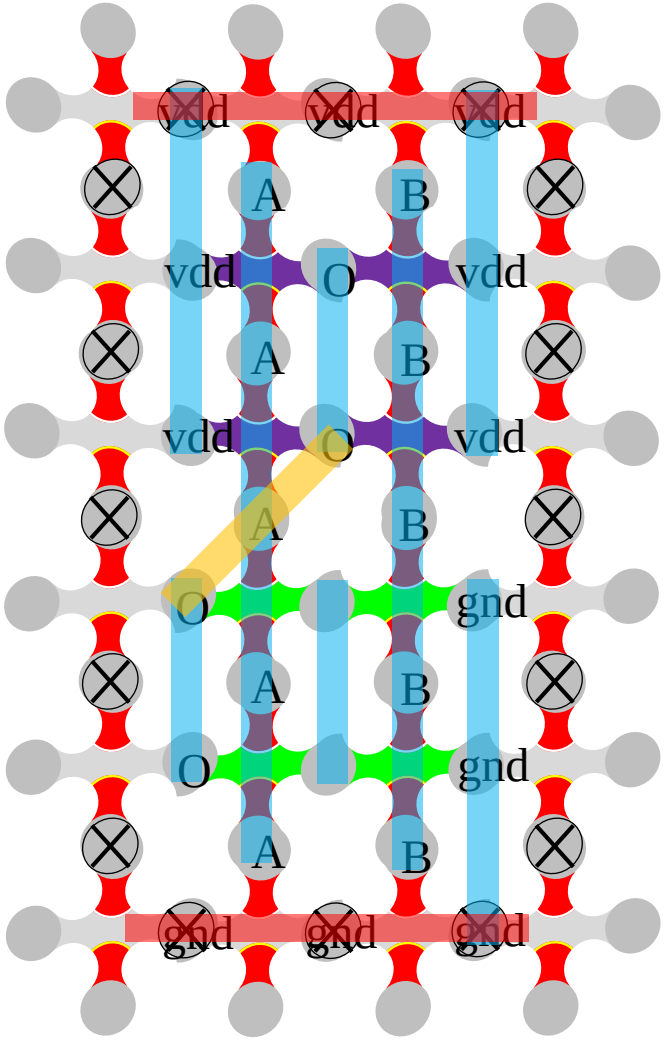
- Transistor isolation ⇔ Diffusion break
- Sizing by transistor duplication
  - Transistor size ⇑
  - => effective transistor density ⇑
- Vs. Basic Canvas cells
  - easier cell generation
  - shorter wires



CMOS diffusion break



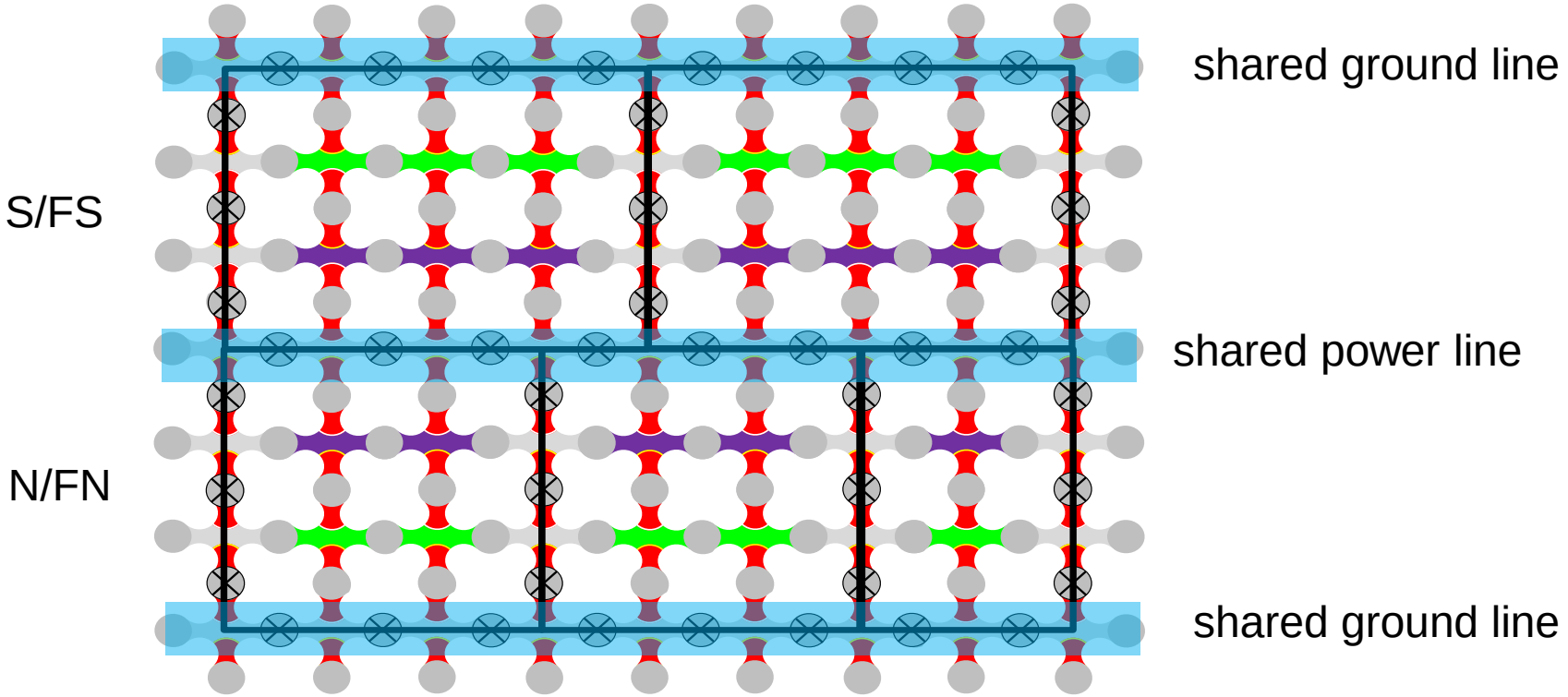
VeSFET transistor isolation



2-input NANDX2

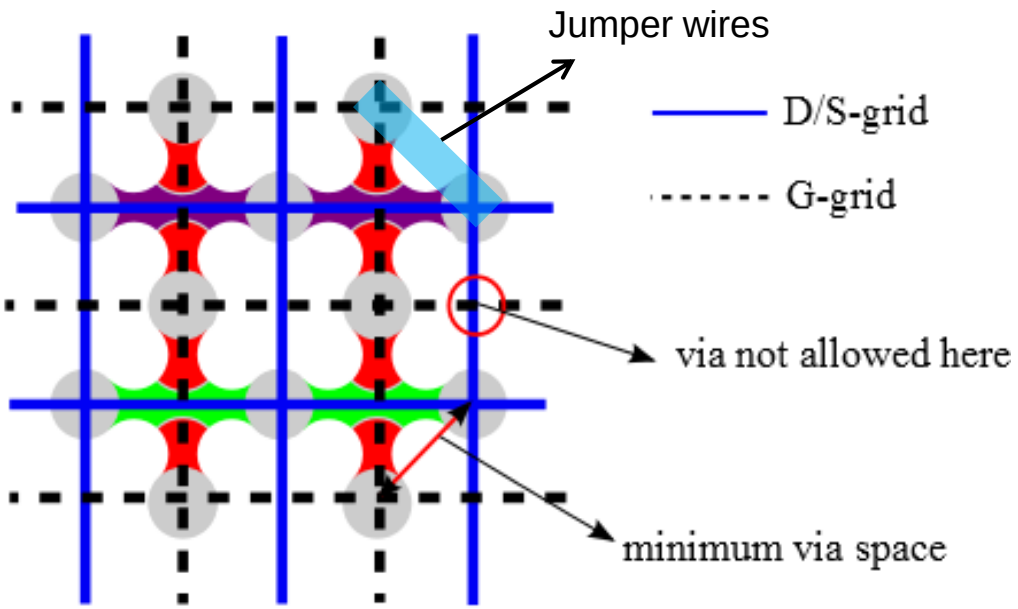
Row-based Standard Cell Placement

- Similar to CMOS standard cell placement.
- Neighboring rows share power/ground lines.
- Power/ground lines are also for transistor isolation.



Inter-cell Routing

- Two disjoint routing grids
  - Vias aligned with pillars: D/S pillars cannot connect to G pillars by only H/V wires
  - Jumper wires: diagonal wires bridging D/S- and G-grids.
- Most inter-cell nets have both D/S pins and G pins.
  - Routing each single net on both grids may need multi layers of jumper wires
  - Route each net on only one grid, only one layer of jumper wires
- Greedy net partitioning
  - Balance routing demands
  - Balance pin density.



Cell Level Comparison

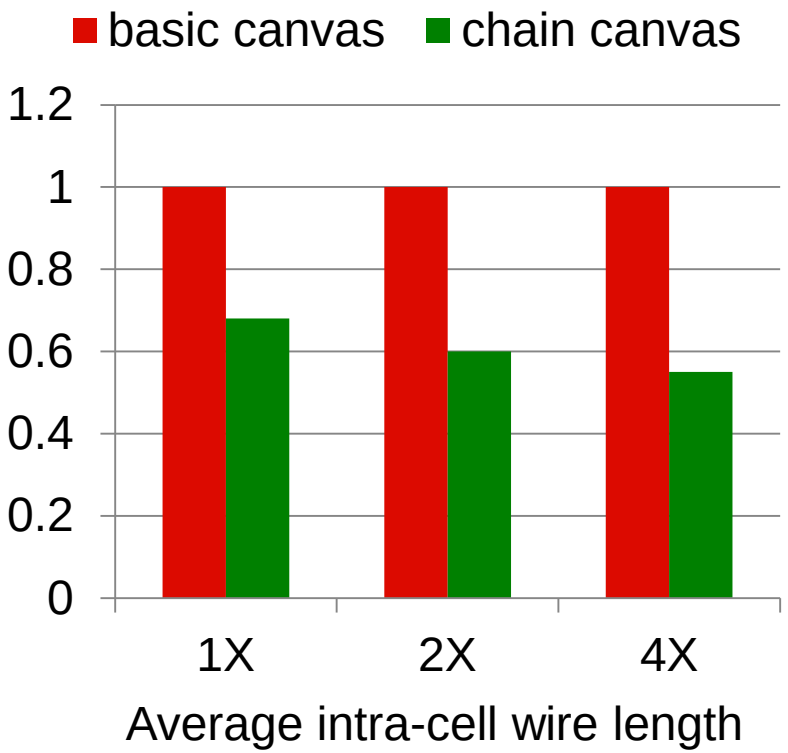
- Design INV, BUF, NAND2, NOR2, AOI21, OAI21 on both canvases
- Design 1X, 2X, 4X cells for each logic
- More pillar sharing → more area saving
  - Greater gate size
  - More gate inputs

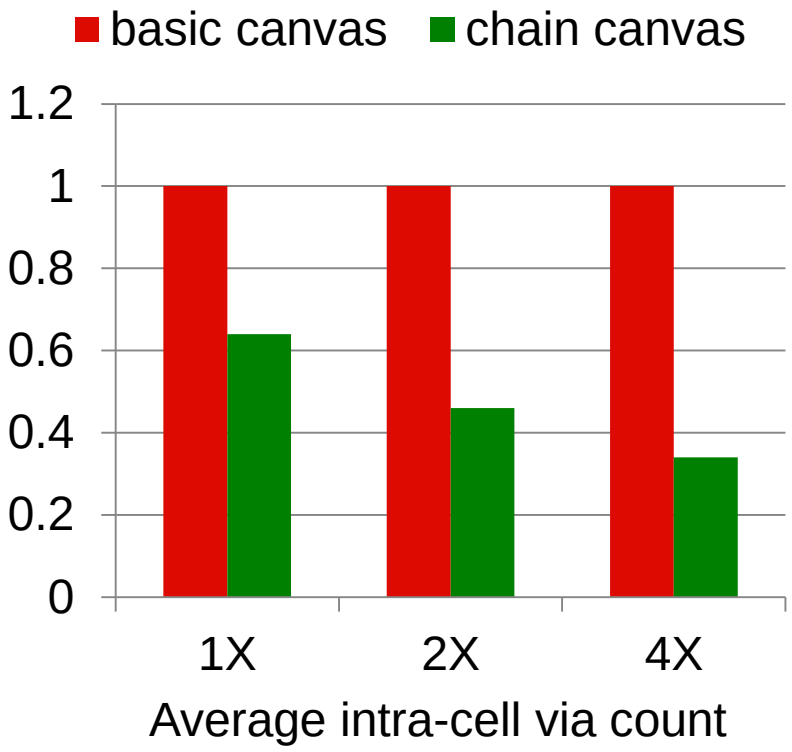
Table 1. # of pillars occupied by cells mapped on *BC* and *CC*

CELL	*Basic Canvas*			*Chain Canvas*		
	1X	***2X***	***4X***	***1X***	***2X***	***4X***
INV	8	16	32	12	18	30
BUF	16	32	64	18	30	54
NAND2	16	32	64	18	30	54
NOR2	16	32	64	18	30	54
AOI21	24	48	96	24	40	72
OAI21	24	48	96	24	40	72
AVG	**1**	**1**	**1**	**1.15**	**0.93**	**0.83**

Cell Level Comparison (Cont.)

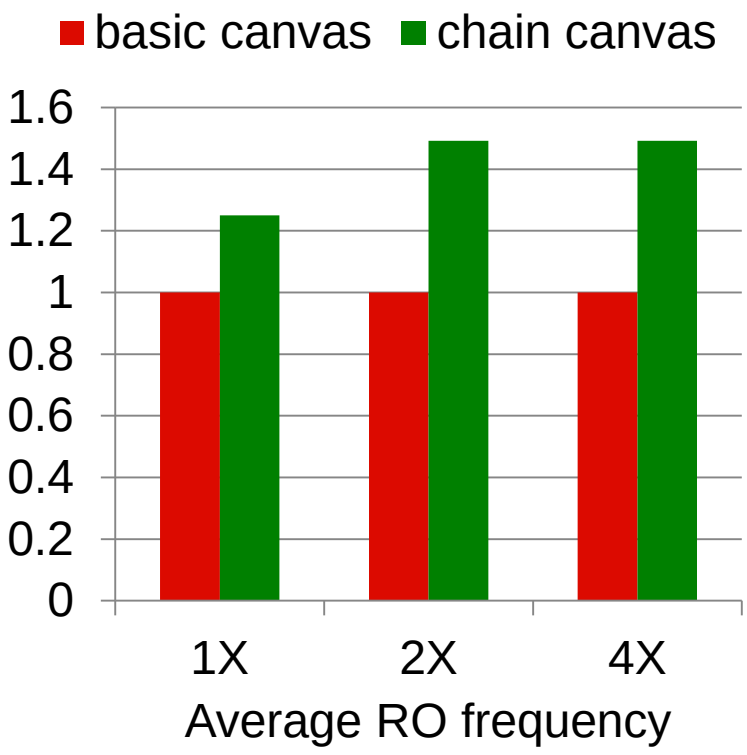
- Chain canvas
  - shorter wires
  - fewer vias
  - gate size ⇑, improvement ⇑

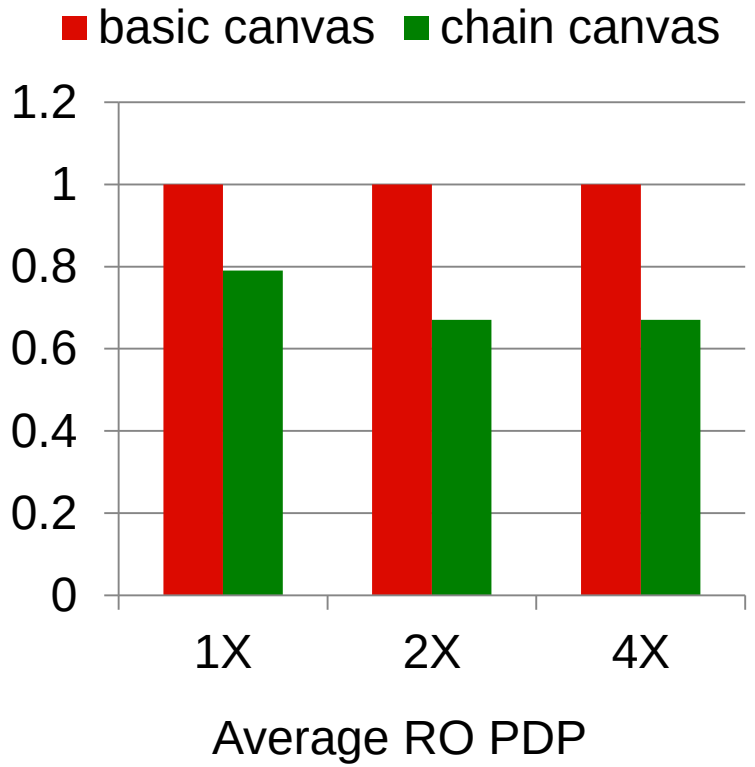




Cell Level Comparison (Cont.)

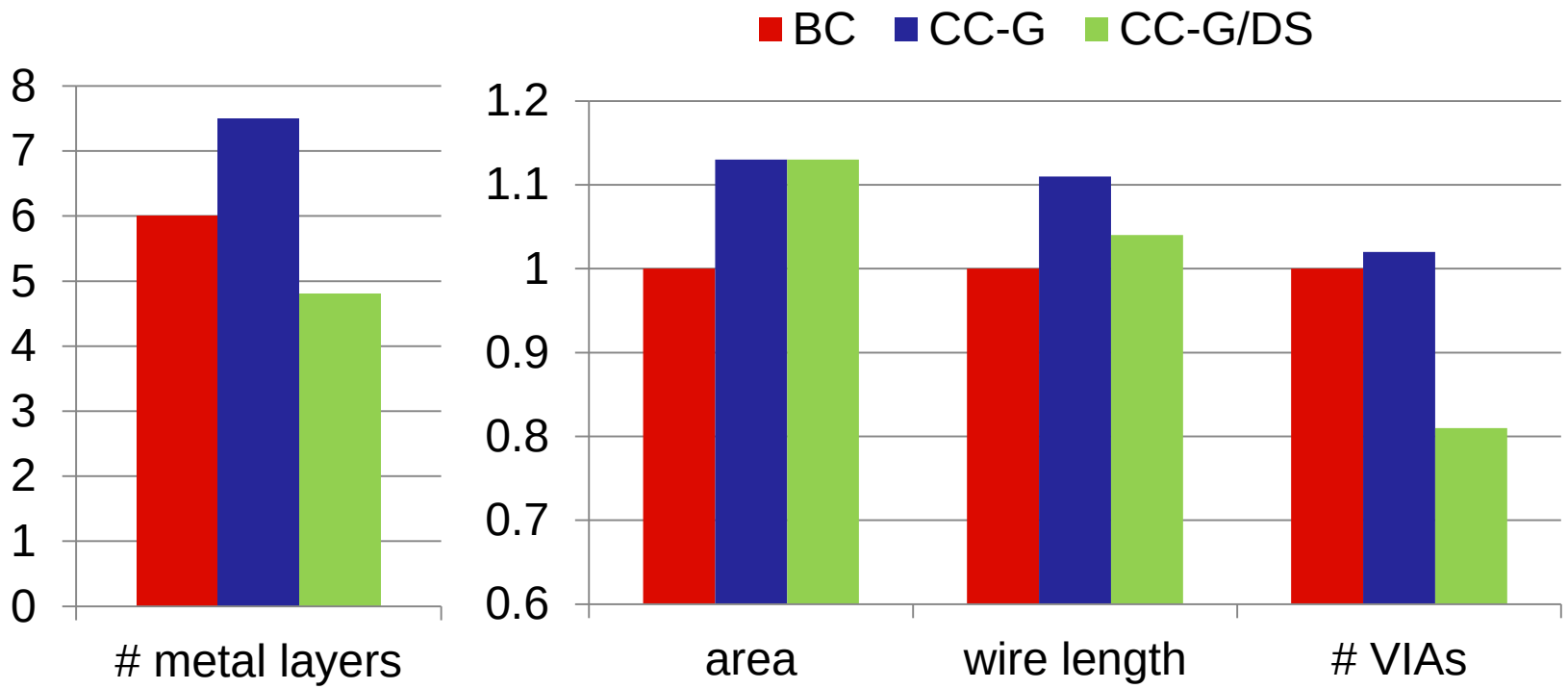
- Performance and power comparison
  - Smaller parasitic RC for CC-based cells.
  - Determine the frequency and power delay product (PDP) of a 5-stage ring oscillator.





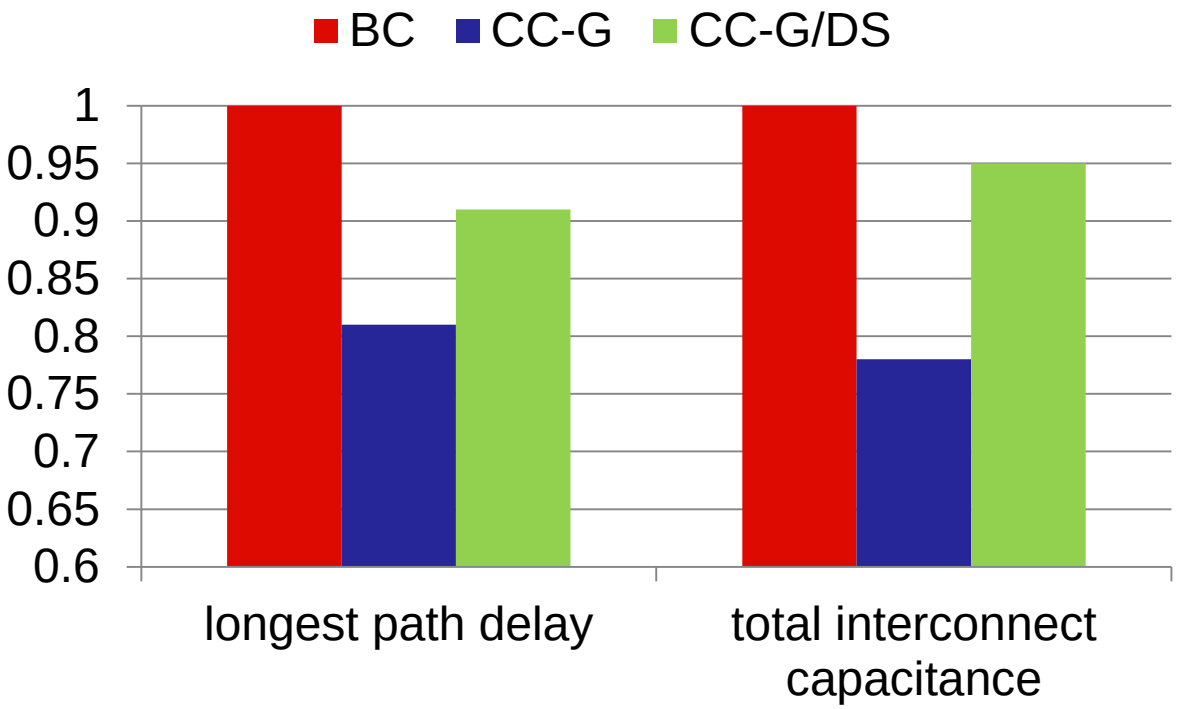
Circuit Level Comparison

- LGSynth91 benchmarks with thousands of gates
  - Mapped with a library of 6 1X cells(INV, BUF, NAND2, NOR2, AOI21, OAI21).
  - CC-G: G-grid only routing
  - CC-G/DS: nets evenly spread on both grids.



Circuit Level Comparison (Cont.)

- Static timing analysis
  - non-linear delay model for each cell.
  - parasitic inter-cell interconnect RC extracted by *Star-RC*.
- Power estimation
  - Total interconnect capacitance



Conclusions

- We propose *chain canvases,*
  - CMOS ASIC EDA infrastructure re-usable.
  - 2X transistor density.
  - Transistor isolation reduces transistor utilization.
  - Transistor utilization improves as gate size increases.
- Chain canvases Vs. Basic Canvases
  - Easier cell generation
  - better routability
  - smaller parasitic capacitance
  - better performance
  - lower power consumption
  - slightly greater footprint area using unit size gates

Thank you!

Q & A