ISPD 2013
Commemoration for Professor Y. Kajitani

Practicality on Placement Given by Optimality of Packing

Shigetoshi Nakatake
Univ. of Kitakyushu

Today's Talk

1) **Rect. packing-base analog placement**
   - ➔**Sequence-pair Packing**
   - ➔**Constraint-driven Optimization**

2) **With or without packing scenario,**

how do we develop analog placement?

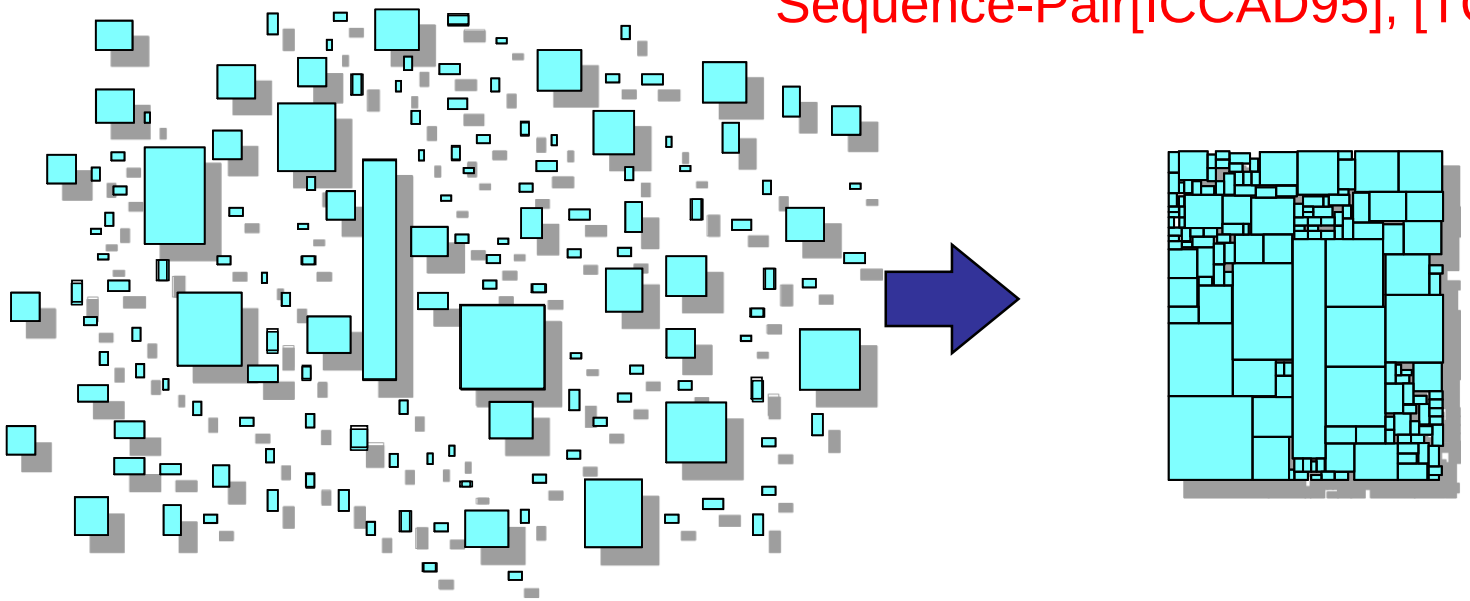
- ➔ **Analytical Analog placement with proximity constraints**

➔ **Comparison : w/ and w/o topological packing technique**

2D Rect. Packing

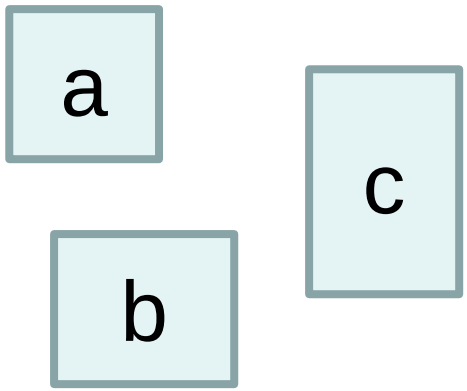
INPUT: A set of rectangles, each of which has width and height
OUTPUT: A placement of rectangles
SUBJECT TO: No overlapping of any pair of rectangles
OBJECTIVE: Minimize bounding box of all the rectangles

Sequence-Pair[ICCAD95], [TCAD96]

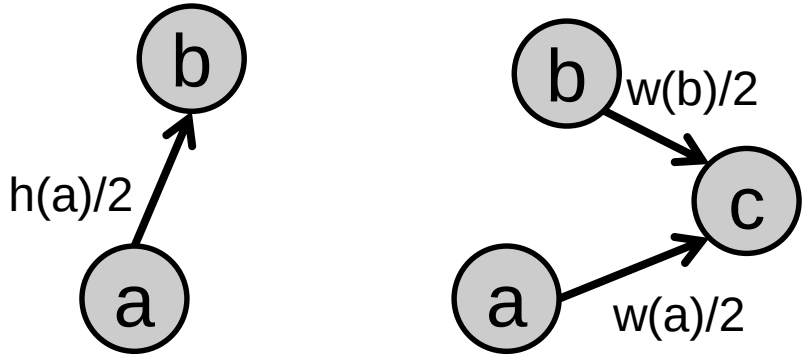


Topological Representation and Constraint Graphs

Placement
(w/o any overlapping):



Constraint graphs:



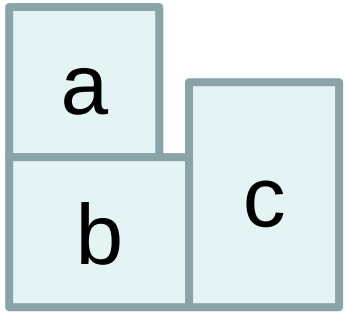
vertical const. graph horizontal const. graph

NOTE: Gv, Gh are weighted DAG

Topological description:

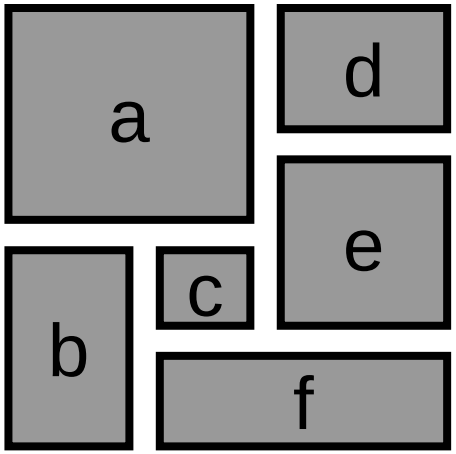
- a is left-of c (c is right of a)
- b is left-of c (c is right of b)
- b is below a (a is above b)

Compacted placement:



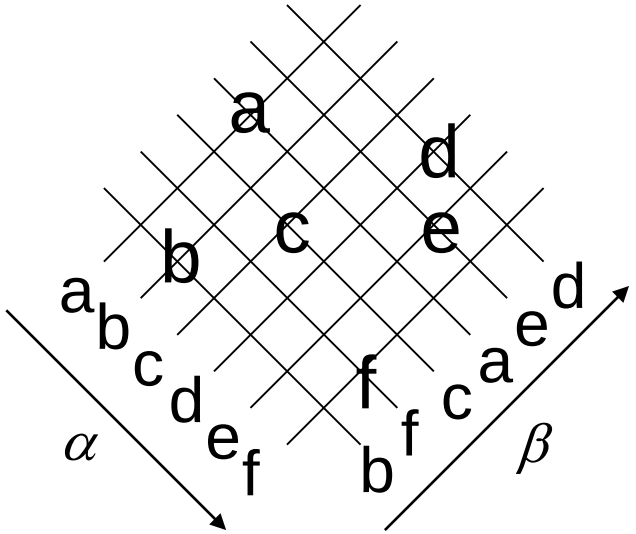
Sequence-Pair(1)

Placement



Sequence-Pair

$$SP = (\alpha, \beta) = (\text{abcdef}, \text{bfcaed})$$



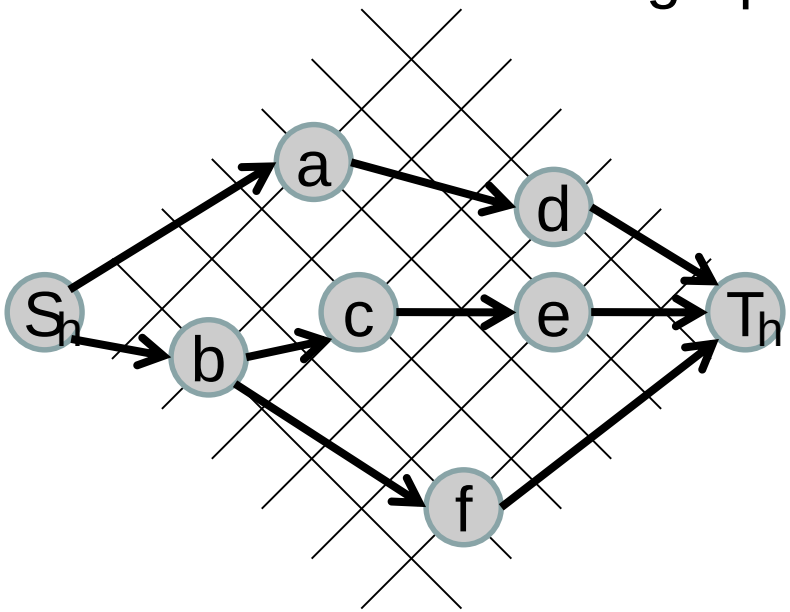
Oblique-Line-Grid: Equivalent Representation of SP

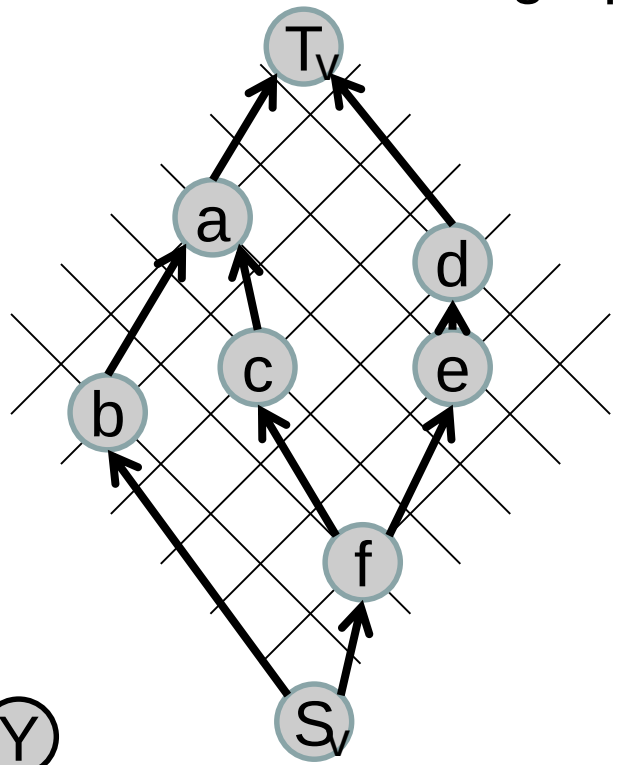
$\alpha^{-1}(X)$: position of X in α $\quad \alpha^{-1}(X) < \alpha^{-1}(Y), \beta^{-1}(X) < \beta^{-1}(Y) \Leftrightarrow$ X is left-of Y

$\beta^{-1}(X)$: position of X in β $\quad \alpha^{-1}(X) > \alpha^{-1}(Y), \beta^{-1}(X) < \beta^{-1}(Y) \Leftrightarrow$ X is below Y

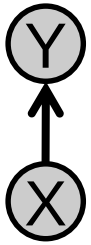
Sequence-Pair(2)

Gh: horizontal constraint graph Gv: vertical constraint graph





w(X)/2+w(Y)/2



h(X)/2+h(Y)/2

NOTE: w(X) , h(X): width, height of X

Sequence-Pair(3)

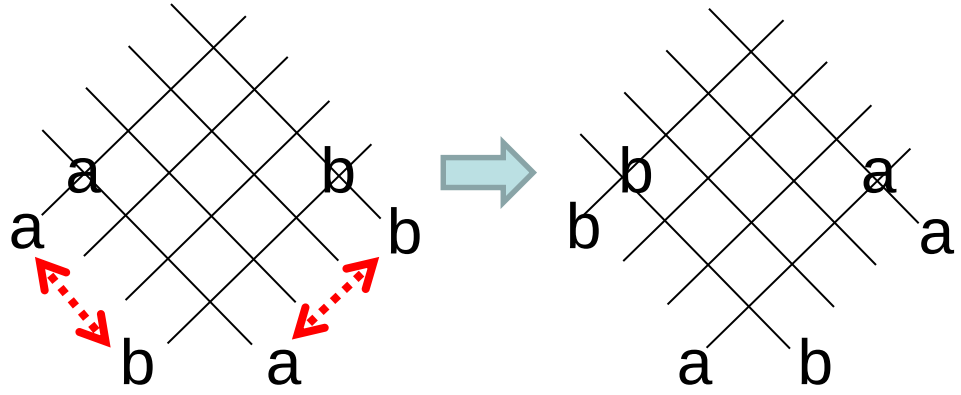
1. **Every placement** corresponds to a **sequence-pair**
2. Packing according to constraint graphs can generate a minimal area placement under the same topological description
3. A solution space induced by sequence-pairs always includes **an optimum placement** with respect to area

Sequence-Pair(4)

Application to simulated annealing

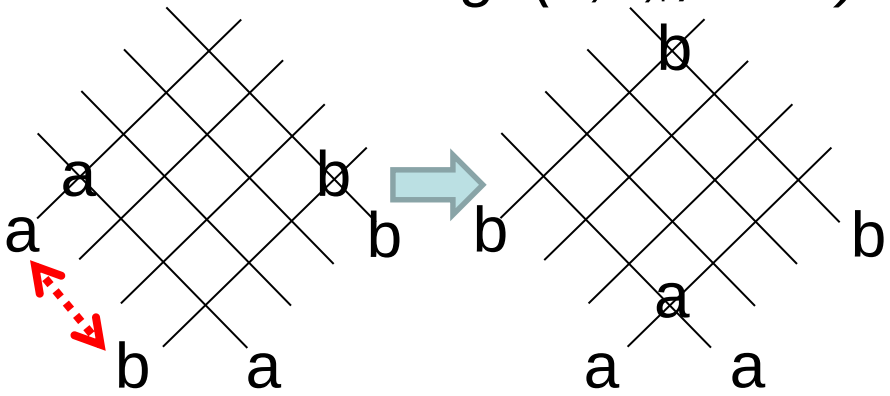
Moves:

1. FullExchange(a,b):

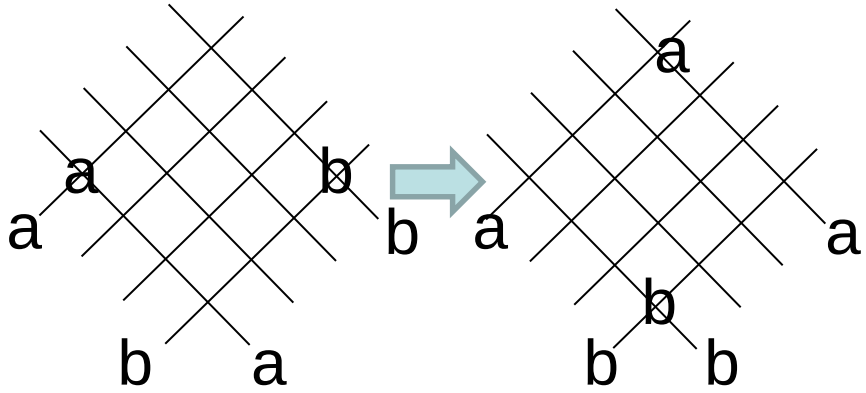


pair-exchange on both α and β

2. HalfExchange(a,b, α | β):



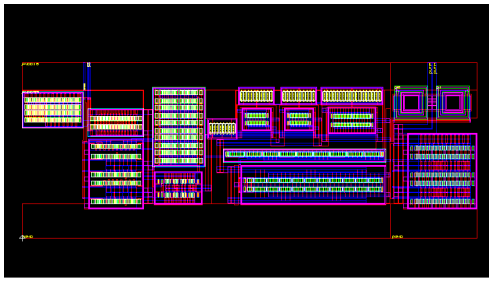
pair-exchange on α



pair-exchange on β

Practical Applications of Packing

- Building block placement
- Floorplanning for large scale circuits
- **Analog placement**
- 3D Cube packing
- Polygon packing
- Scheduling for dynamic reconfigurable system



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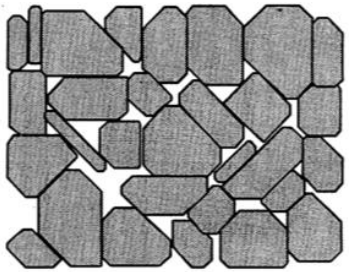
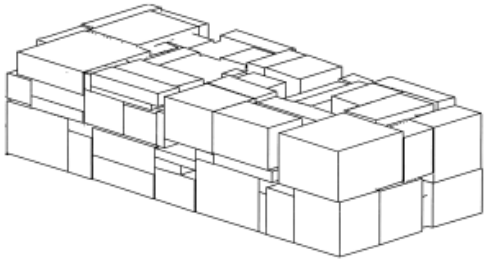
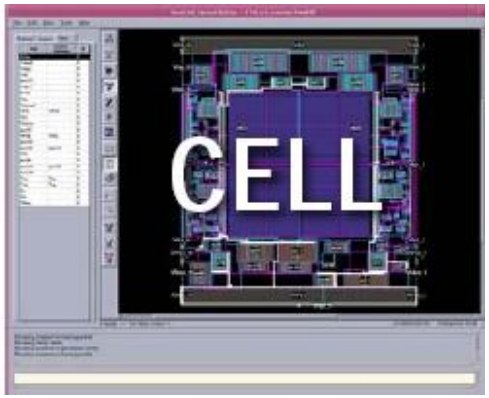




Analog Placement



Device Generation **Cell Design** **Block Design**

Each Placement…

1. Circuit netlist
2. Design rule
3. Specification / constraints

→ **?** →

Layout
(Layers w/ Geometry, Contacts, Wires…)

Analog Placement

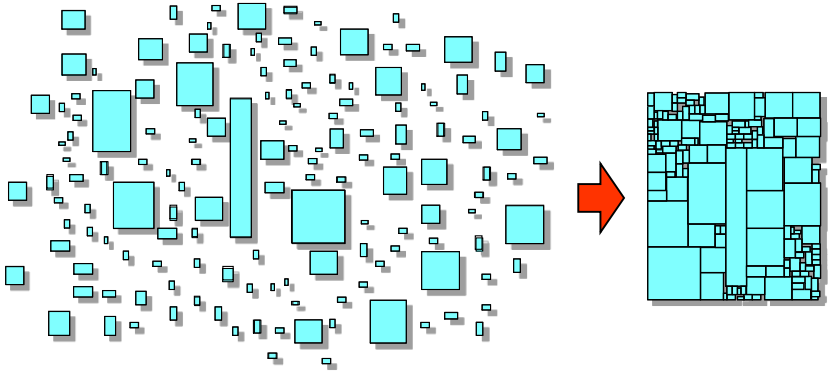
- **Geometry-based placement**
  - ILAC [CICC88], KOAN/ANAGRAM [ICCAD88]

  → larger area and time consuming
- **Topology-based placement** (modern)
  - BSG, Sequence-Pair, O-tree, B*-tree, TCG-S, …
  - Constraint-driven
    - symmetry, common-centroid, alignment and others

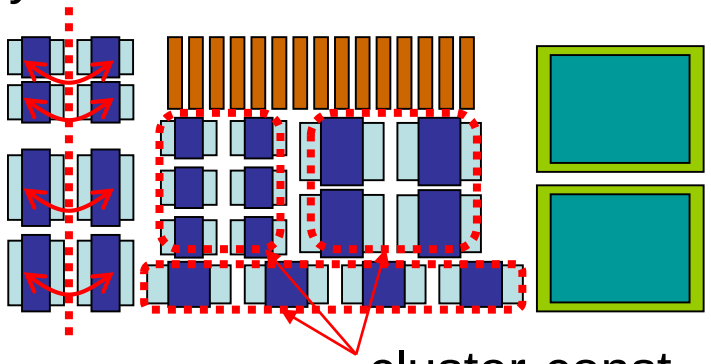
  → smaller area and rapid convergence

Constraint-driven Placement

1. Formulation as a rectangle packing problem
2. Extensions under constraints
   - **Separation Constraint**
   - **Alignment Constraint**
   - **Abutment Constraint**
   - **Boundary Constraint**
   - **Symmetry Constraint**
   - **Preplaced Constraint**
   - **Range Constraint**
   - **Cluster Constraint**

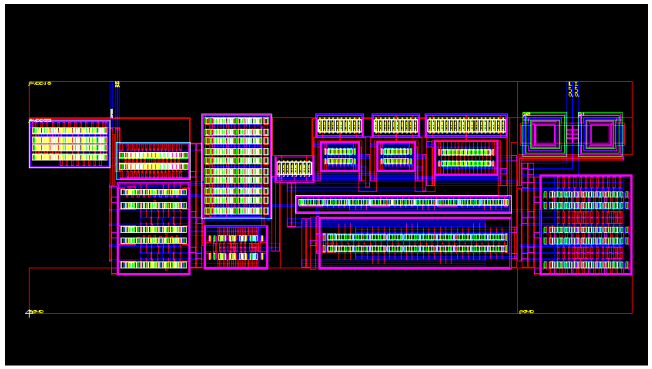


symm-const.



cluster-const.

Our Works in Constraint-driven Analog Layout

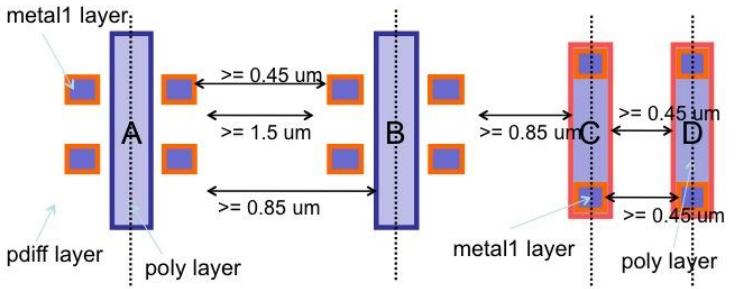


- **Placement**
  - ASPDAC04, GLSVLSI04, IEICE04, ISVLIS06a, ASPDAC09, ASPDAC08
  - AMPER produced by JEDAT
- **Routing**
  - GLSVLSI05, IEICE06
- **Compaction**
  - ASPDAC02, ISVLSI06b
  - GRANA produced by JEDAT

[ICCAD95] H.Murata, K.Fujiyoshi, S. Nakatake, Y.Kajitani, "*Rectangle-Packing Based on Module Placement*", ICCAD95, pp.472-479, 1995.
[TCAD96] VLSI H.Murata, K.Fujiyoshi, S.Nakatake, Y.Kajitani, "*Module Placement Based on Rectangle-Packing by the Sequence-Pair*", IEEE Trans. on CAD, vol.15, No.12, pp.1518-1524, 1996.
[ASPDAC02] Y.Kubo, S.Nakatake, Y.Kajitani, M.Kawakita, "*Explicit Expression and Simultaneous Optimization of Placement and Routing for Analog IC Layouts*", ASPDAC02, pp.467-472, 2002.
[ASPDAC04] T.Nojima, X.Zhu, Y.Takashima, S.Nakatake, Y.Kajitani, "*Multi-Level Placement with Circuit Schema Based Clustering in Analog IC Layouts*", ASPDAC04, pp.406-411, 2004.
[GLSVLSI04] T.Nojima, X.Zhu, Y.Takashima, S.Nakatake, Y.Kajitani, "*A Device-Level Placement with Multi-Directional Convex Clustering*", GLSVLSI04, pp.196-201, 2004.
[IEICE04] T.Nojima, X.Zhu, Y.Takashima, S.Nakatake, Y.Kajitani, "*A Device-Level Placement with Schema Based Clusters in Analog IC Layouts*", IEICE Trans. on Fundamentals, Vol.E87-A, No.12, pp.3301-3308, 2004.
[IEICE06] N. Fu, S. Nakatake, Y. Takashima, Y. Kajitani, "*The Oct-Touched Tile: A New Architecture for Shape-Based Routing* ", IEICE Trans. on Fundamentals, Vol.E89-A, No.2, pp.448-445, 2006 .
[ISVLSI06a] N Fu, S. Nakatake, M. Mineshima, "Multi-SP: A Representation with United Rectangles for Analog Placement and Routing", ISVLSI06, pp.38-43, 2006.
[ISVLSI06b] T.Nojima, S.Nakatake, T.Fujimura, K.Okazaki, Y.Kajitani, N.Ono, "Adaptive Porting of Analog IPs with Reusable Conservative Properties", ISVLSI06, pp.18-23, 2006.
[ASPDAC07] S.Nakatake, "Structured Placement with Topological Regularity Evaluation", ASPDAC07, pp.215-220, 2007.
[ASPDAC08] Q.Dong, S.Nakatake, "Constraint-Free Analog Placement with Topological Symmetry Structure", ASPDAC08, pp.186-191, 2008.

Analog Constraint Formulation

Separation Constraint

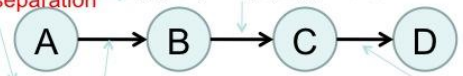


horizontal constraint graph:

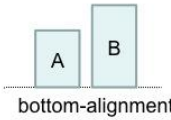
NOTE: w(X, L) = width of layer L of device X

maximal separation

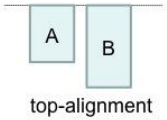
w(B,pdff)/2+w(C,poly)/2+0.85



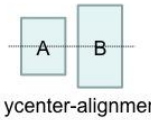
Alignment Constraint



bottom-alignment



top-alignment



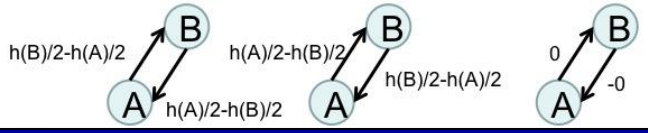
ycenter-alignment

sequence-pair condition:

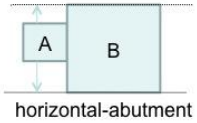
$\alpha^{-1}(A) < \alpha^{-1}(B), \beta^{-1}(A) < \beta^{-1}(B)$ or $\alpha^{-1}(B) < \alpha^{-1}(A), \beta^{-1}(B) < \beta^{-1}(A)$

SP=(…A…B…, …A…B…) SP= (…B…A…, …B…A…)

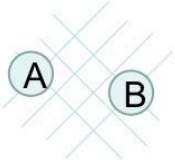
vertical constraint graph:



Abutment Constraint



horizontal-abutment

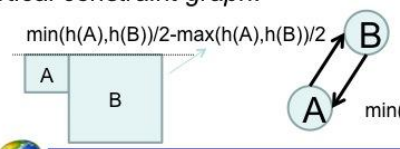


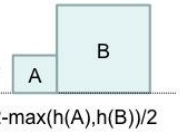
sequence-pair condition:

$\alpha^{-1}(A) < \alpha^{-1}(B), \beta^{-1}(A) < \beta^{-1}(B)$ and $\alpha^{-1}(X) < \alpha^{-1}(A)$ or $\alpha^{-1}(B) < \alpha^{-1}(X)$ or $\beta^{-1}(X) < \beta^{-1}(A)$ or $\beta^{-1}(B) < \beta^{-1}(X)$ for $\forall X (\neq A, B)$

vertical constraint graph:

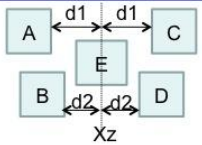
min(h(A),h(B))/2-max(h(A),h(B))/2





min(h(A),h(B))/2-max(h(A),h(B))/2

Symmetry Constraint



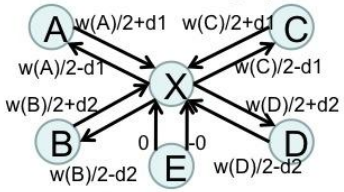
horizontal symmetry group
pair-symmetry: (A,C), (B,D)
self-symmetry: E

sequence-pair condition:

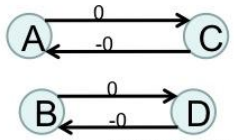
NOTE: sym(A)=C, sym(B)=D, sym(E)=E

$\alpha^{-1}(A) < \alpha^{-1}(B) \Leftrightarrow \beta^{-1}(sym(B)) < \beta^{-1}(sym(A))$

horizontal constraint graph:



vertical constraint graph:



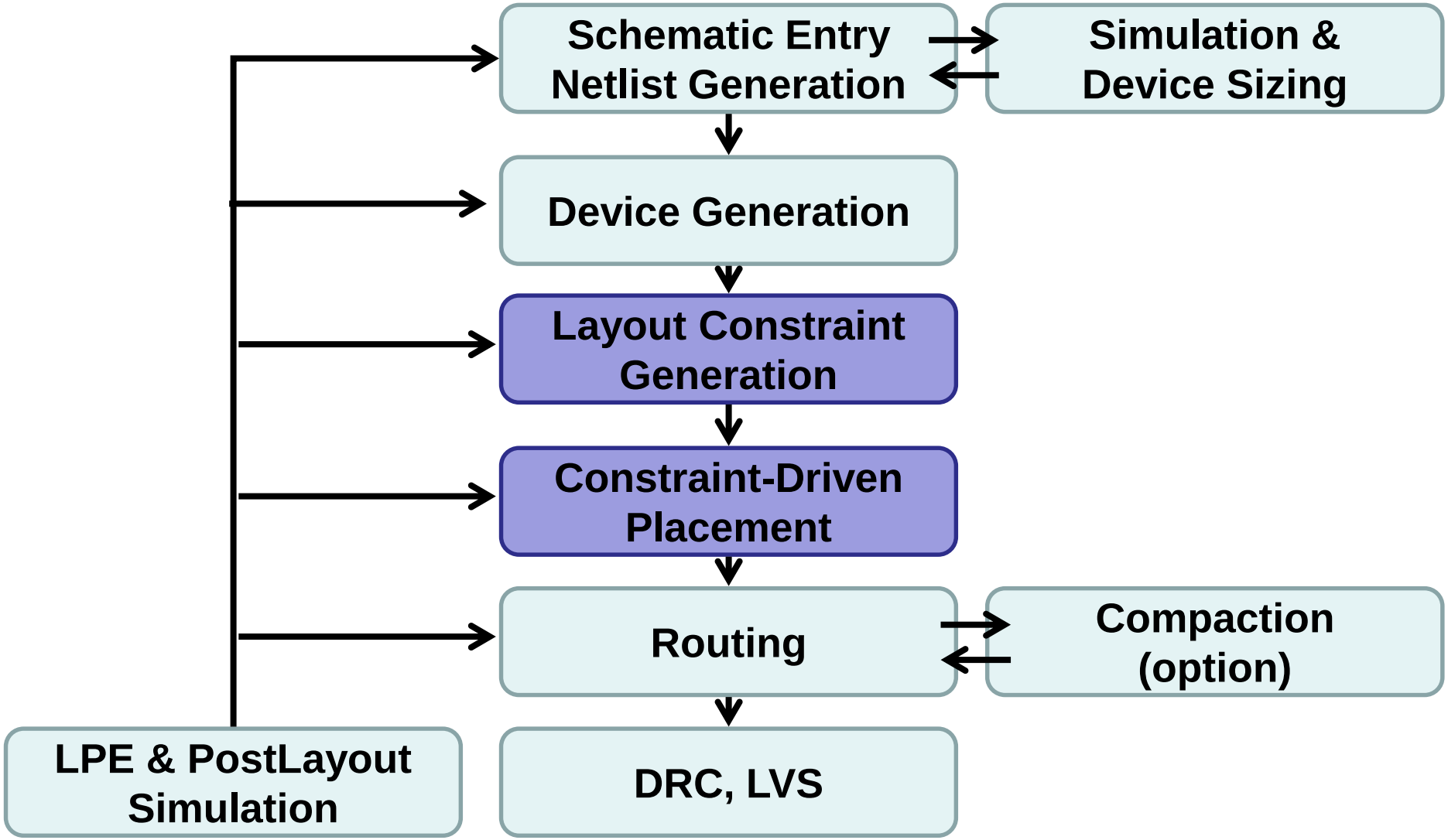
NOTE: ycenter-alignment

NOTE: X is dummy node, d1, d2 should be precalculated

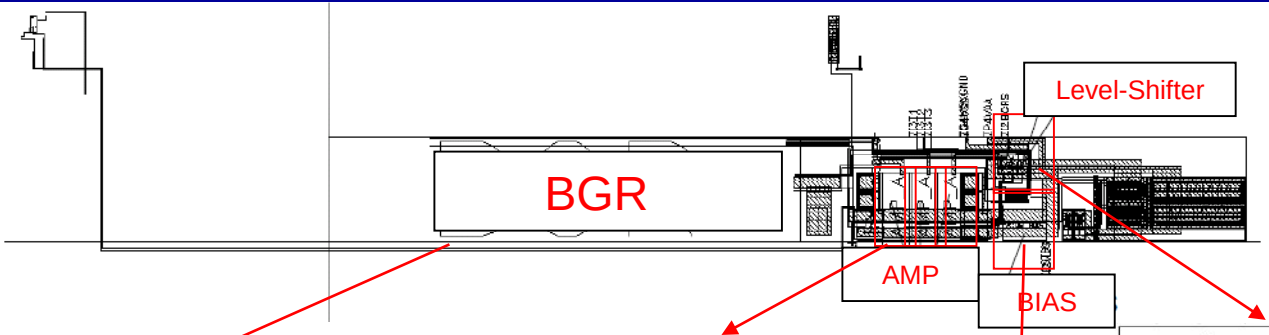
Objective and Optimization

- Objective: Area + Wirelength (HPWL or MST)
- Framework: Simulated Annealing
  - Moves
  - Feasibility Check
    - Topological Checking → sequence-pair conditions
    - Geometrical Checking → no positive cycle

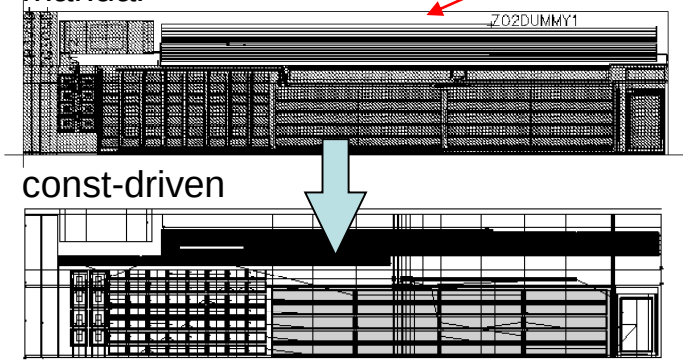
Design Flow for Analog Layout



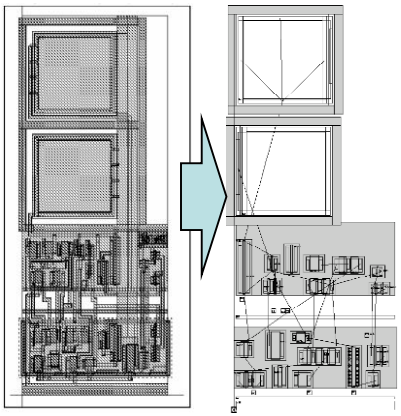
Design Case Study: LCD-Driver



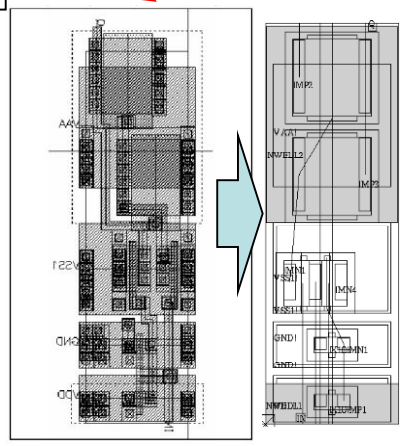
manual



const-driven

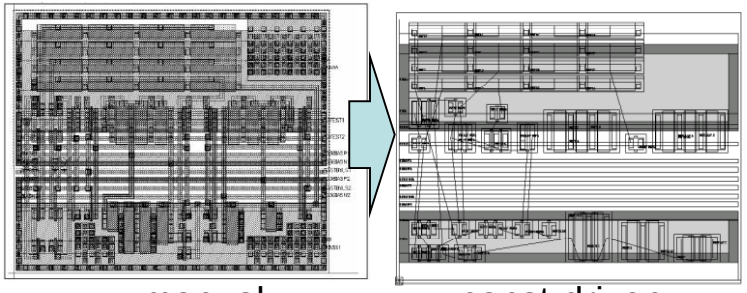


manual const-driven



manual const-driven

NOTE: Both ICs by '*manual*' and '*const-driven*' implemented on NECEL 0.35um, both of them could work.
(Collaboration with NEC micro systems.)



manual const-driven

Today's Talk

1) **Rect. packing-base analog placement**
   - ➔**Sequence-pair Packing**
   - ➔**Constraint-driven Optimization**

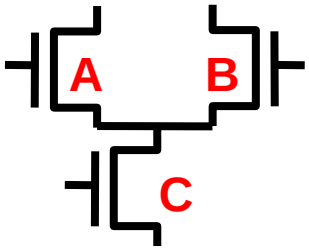
2) **With or without packing scenario,**

how do we develop analog placement?

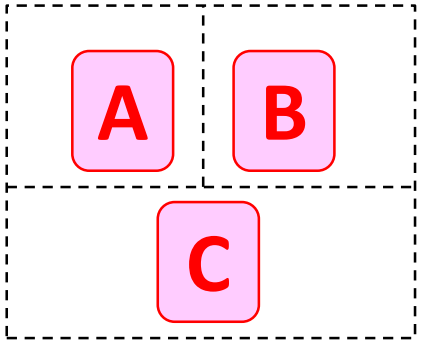
- ➔ **Analytical Analog placement with proximity constraints**

➔ **Comparison : w/ and w/o topological packing technique**

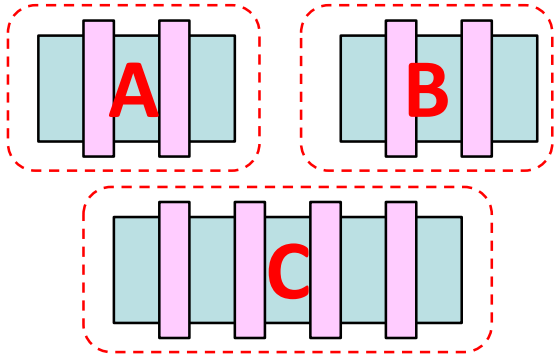
Representation of Placement (1)



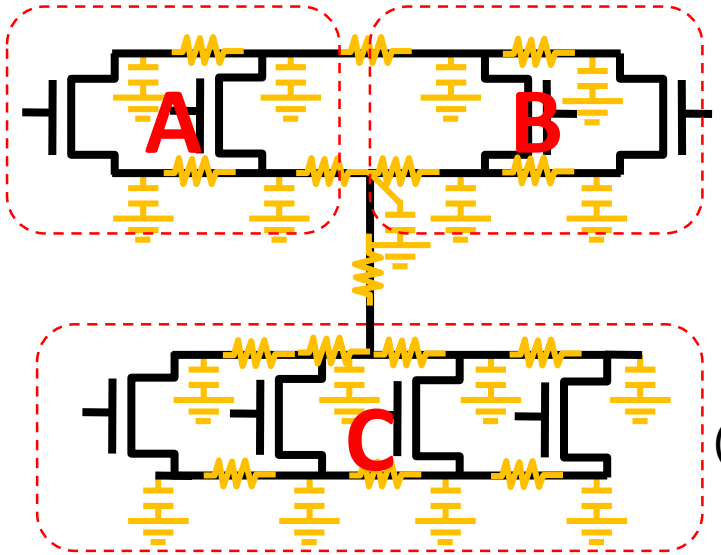
(1) Schematic



(2) Symbolic/Topological Placement

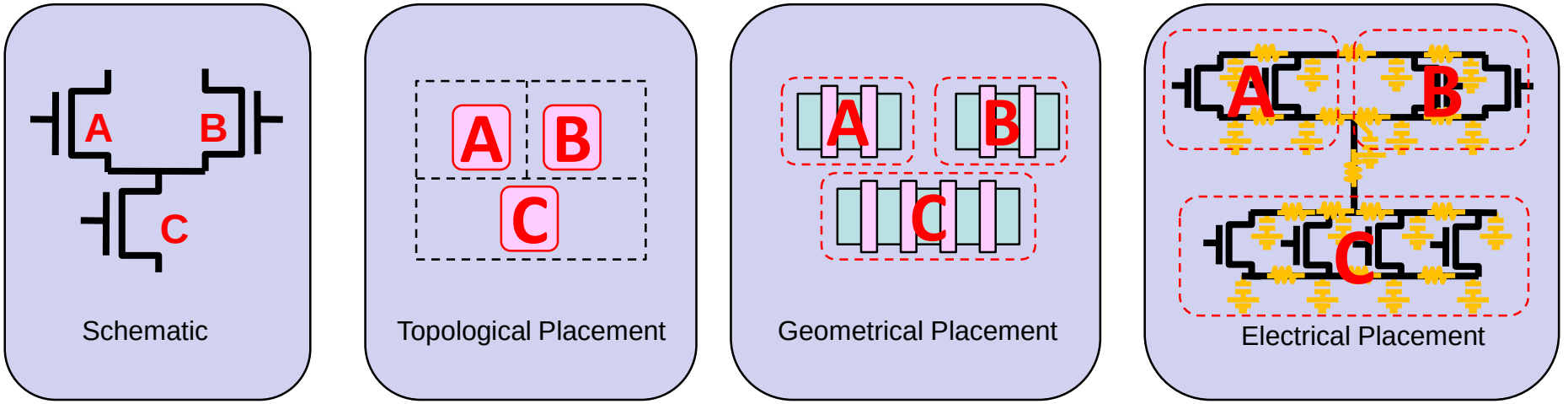


(3) Physical/Geometrical Placement



(4) Electrical Placement

Representation of Placement (2)



Outputs

Outline
I/O pin
Device size

Layers
Design rules

Parasitics

Steps

Device sizing

Floorplanning

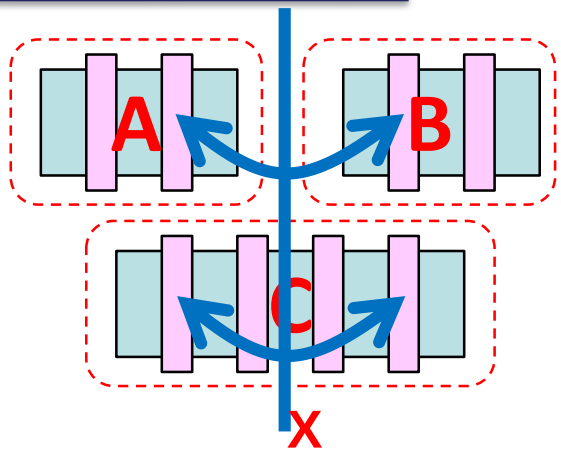
Device Generation (PDK)

Layout(Placement/Routing/Compaction)

LPE

Optimization of Placement

Constraint-driven

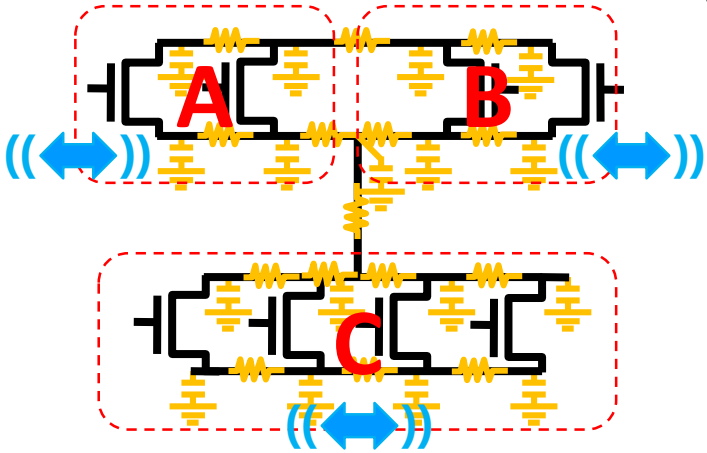


1. Spec.: Voff < 1mV
2. Extract diff. pair (A, B)
3. Symm. Const.: A and B is x-symmetry for X

Input is up to here

4. Represent placement and constraint topologically
5. Search optimal placement under constraints

Sensitivity-driven



1. Spec.: Voff < 1mV

Input is up to here

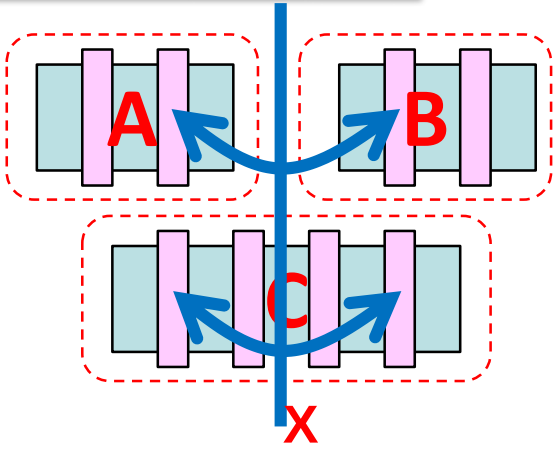
2. Generate parasitic network
3. Sensitivity analysis

$$\min\left(\frac{\partial V_{offset}}{\partial X_A}+\frac{\partial V_{offset}}{\partial X_B}+\frac{\partial V_{offset}}{\partial X_C}\right)$$

4. Perturb placement of A, B, C and optimize placement

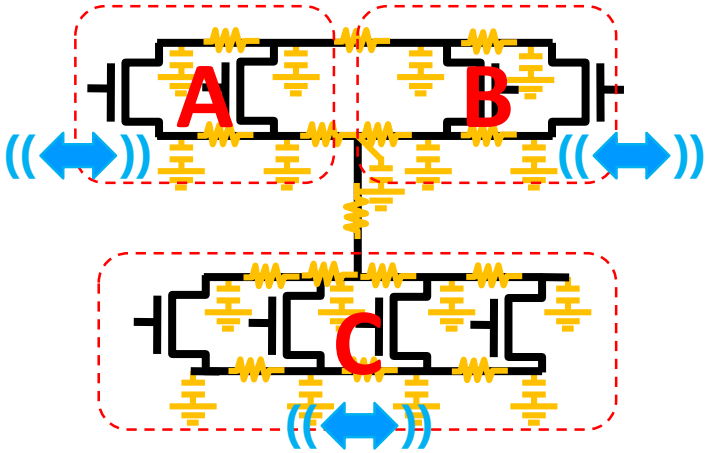
Constraint-driven v.s. Sensitivity-driven

Constraint-driven



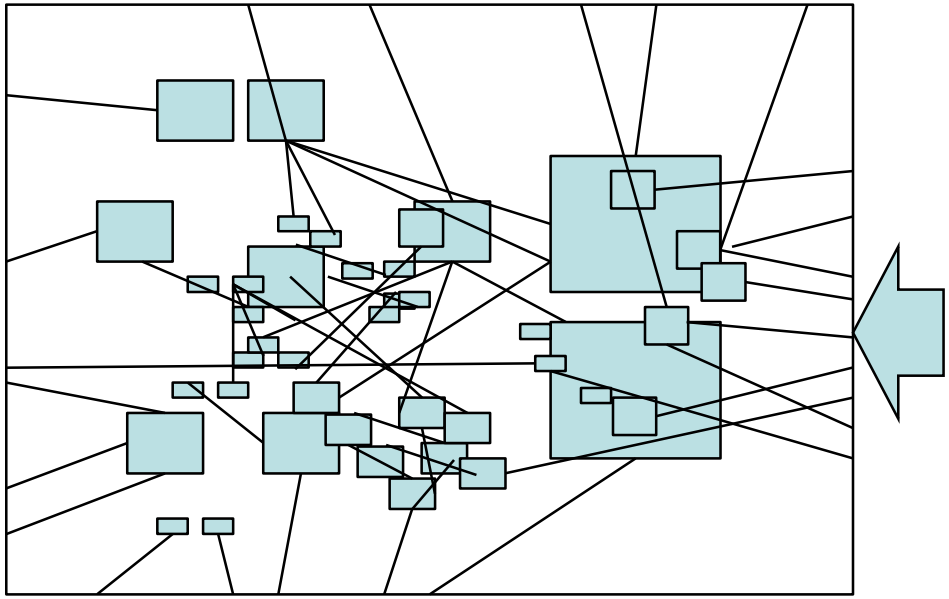
- Need to substitute objective and constraints
- Available to use general optimizer like SA
- Rapid computation and global optimization
- EDA and users can have explicit consensus by means of constraints

Sensitivity-driven

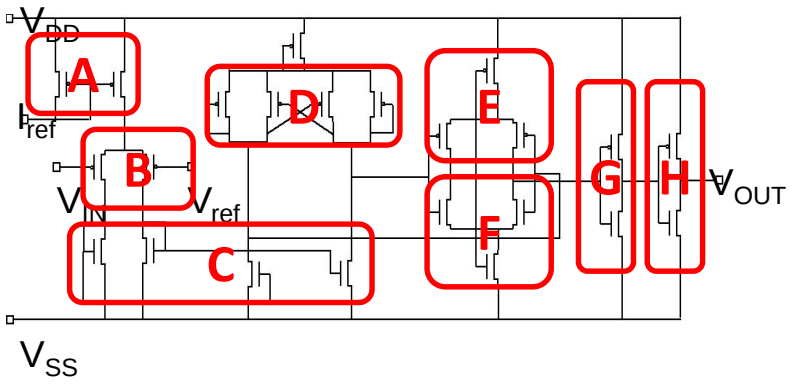


- Directly optimize specification without substituting objective and constraints
- Huge computation and local optimization
- All can be don in EDA
- Need routing information for accuracy

Preliminary of Sensitivity-driven: Analytical Analog Placement



Analytical Placement
Pros: high speed, good scalability
Cons: many overlaps, messy



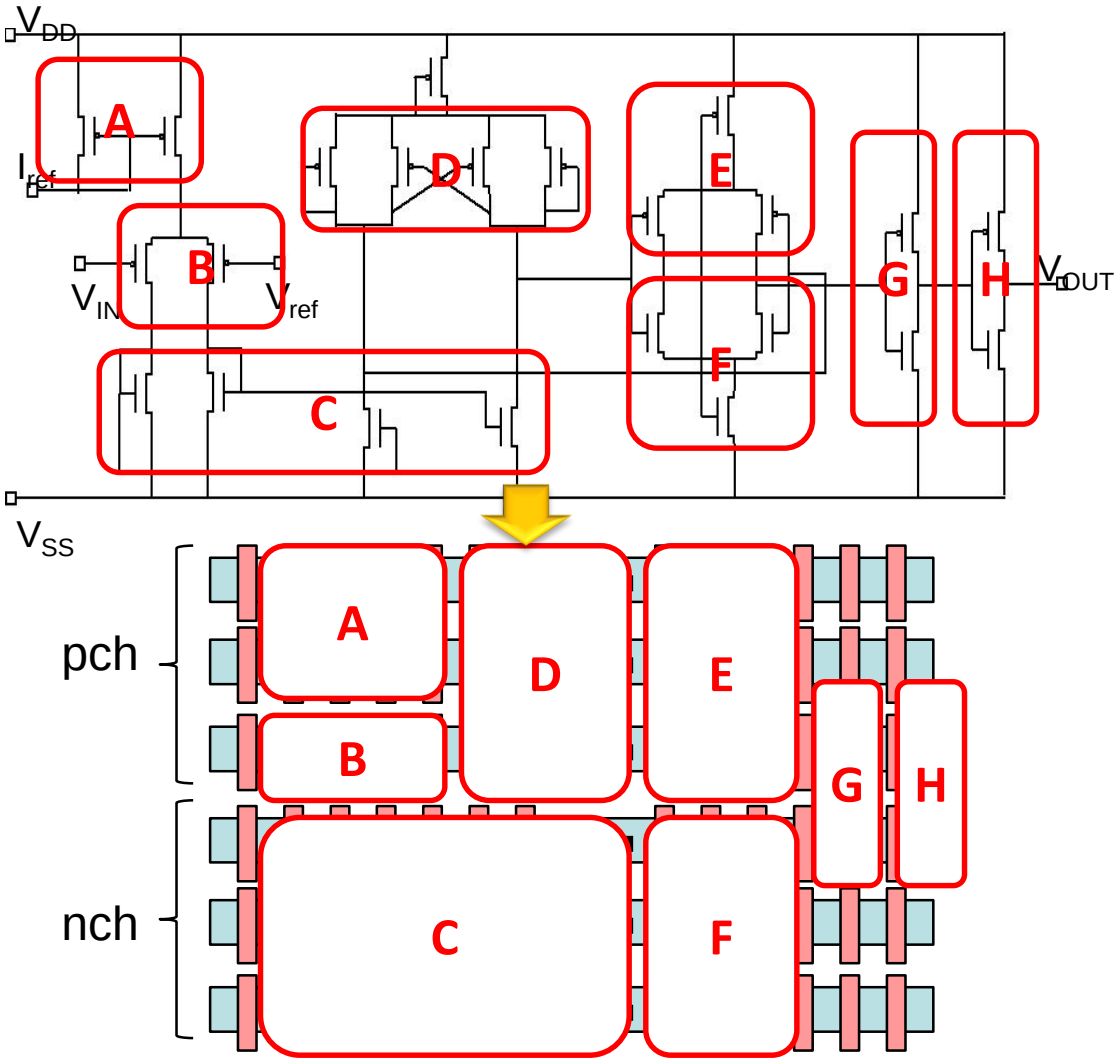
Proximity function induced by group information

Analytical analog placement w/ proximity constraints

Group Extraction from Schematic

1. Extract sub-netlist corresponding to current mirror, differential pair, logic primitive…

2. Place blocks corresponding to sub-netlists.



w/o Rect. Packing: Analytical Formulation

Min: CostOfHPWL + CostOfOverlap + CostOfGroupProximity

Variables: x and y-coordinates of each cell

CostOfHPWL → LogSumExp.

CostOfHPWL → Overlap Removal Length, Takashima, et. al. SASIMI 2010.

CostOfGroupProximity → like an HPWL formulation.

Well Group : P-well, N-well with same potential

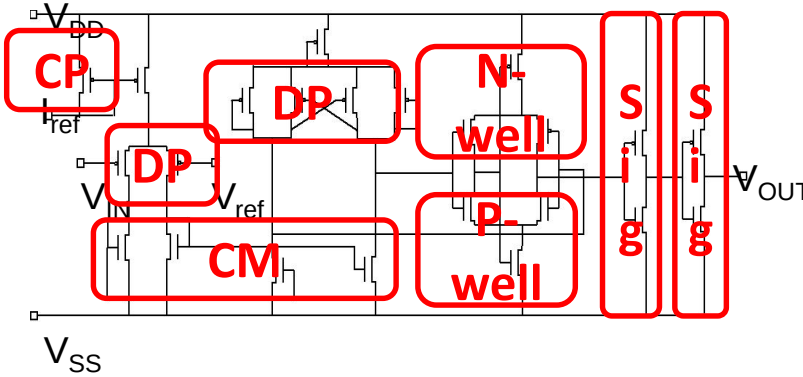
CM. Group : current mirrors

DP. Group : differential pairs

Signal Group : path from VDD to GND

Cap. Group : capacitances with same size

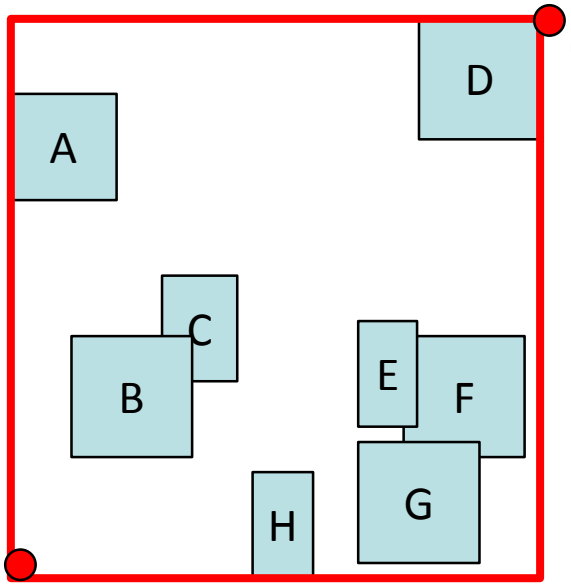
Res. Group : resisters connected in parallel or serial.



Group Proximity Cost Formulation

GroupCost = Max(AreaOfBoundBox, SumOfCellArea)

Group : { A, B, C, D, E, F, G, H }

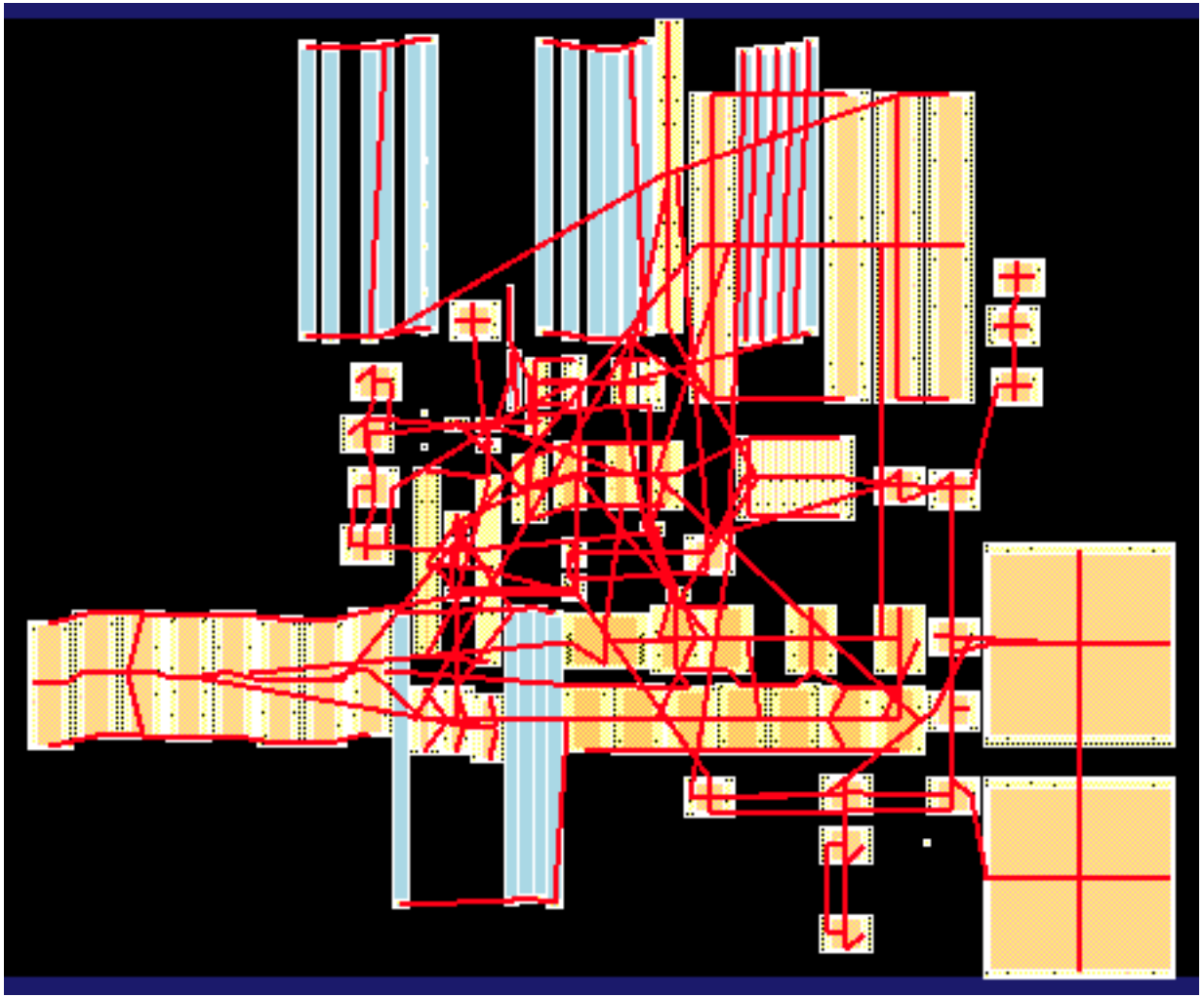


$$x\min = -t \times \log \sum_{i \in \{A, \cdots, H\}} \exp(-l(i)/t)$$

$$x\max = t \times \log \sum_{i \in \{A, \cdots, H\}} \exp(r(i)/t)$$

$$t \times \log\{\exp((x\max - x\min) * (y\max - y\min)/t) + \exp(\sum_{i \in \{A, \cdots, H\}} a(i)/t)\}$$

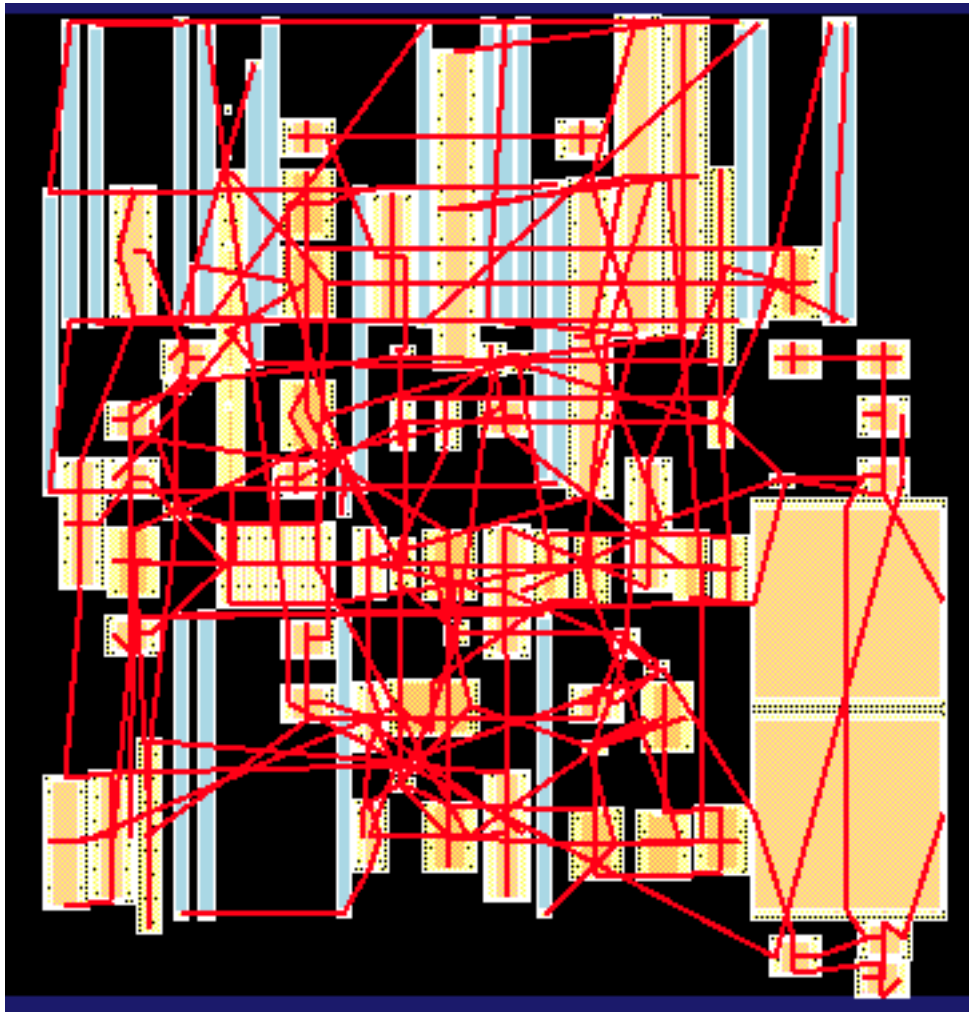
Example: Analytical Analog Placement w/ proximity constraints



TIME : 1.0 sec.
AREA : 29,793 (100%)
HPWL : 2,998 (100%)

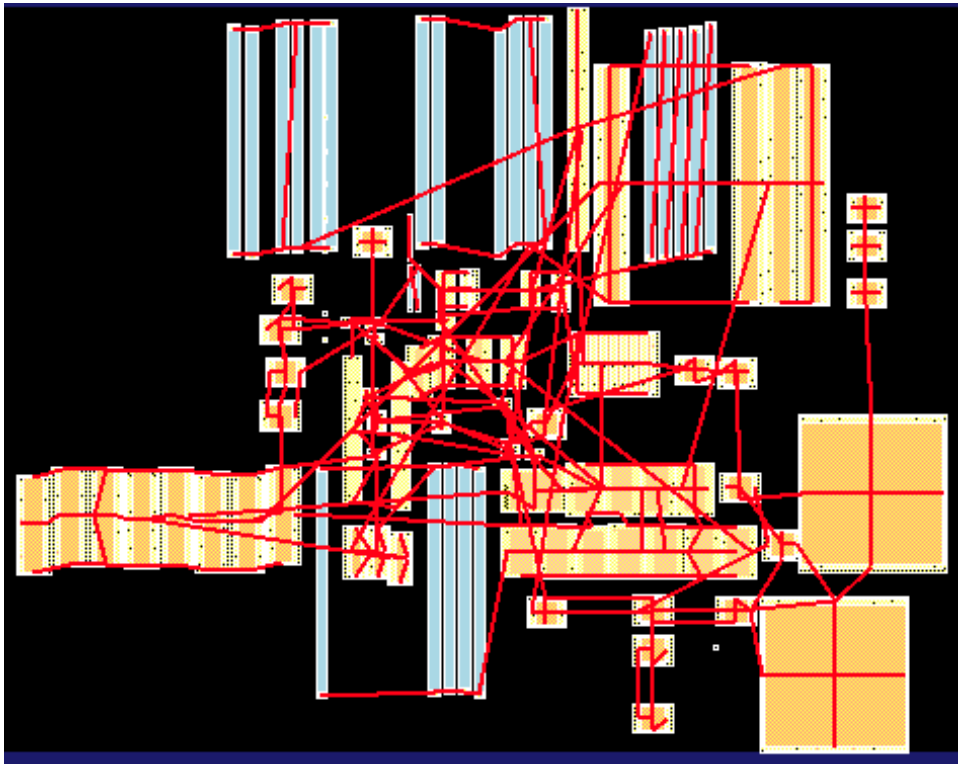
But, many DR-errors.

Analytical Analog Placement w/o Proximity Constraints

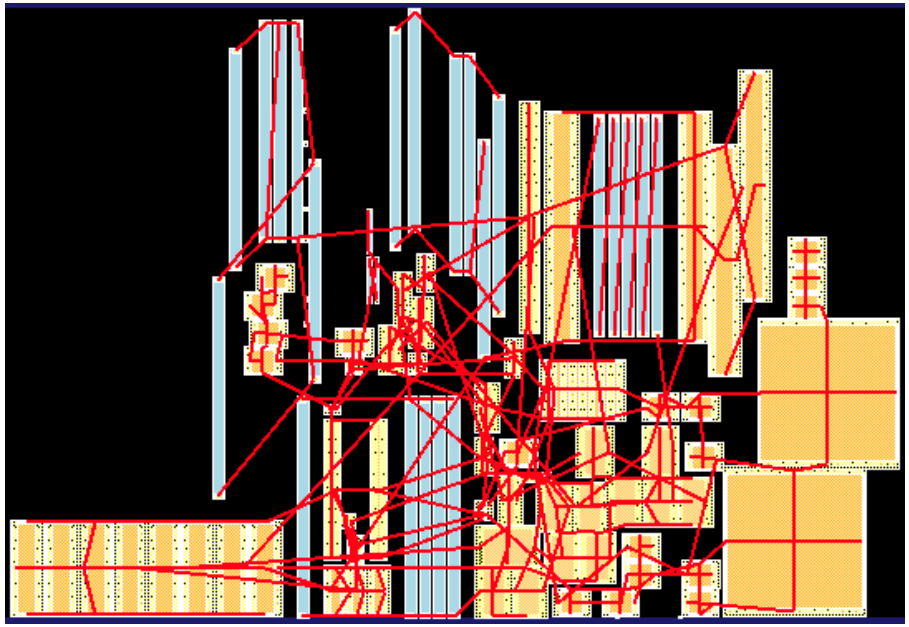


TIME : 1.0 sec.
AREA : 22,637 (76%)
HPWL : 4,259 (142%)

Eliminating DR-errors

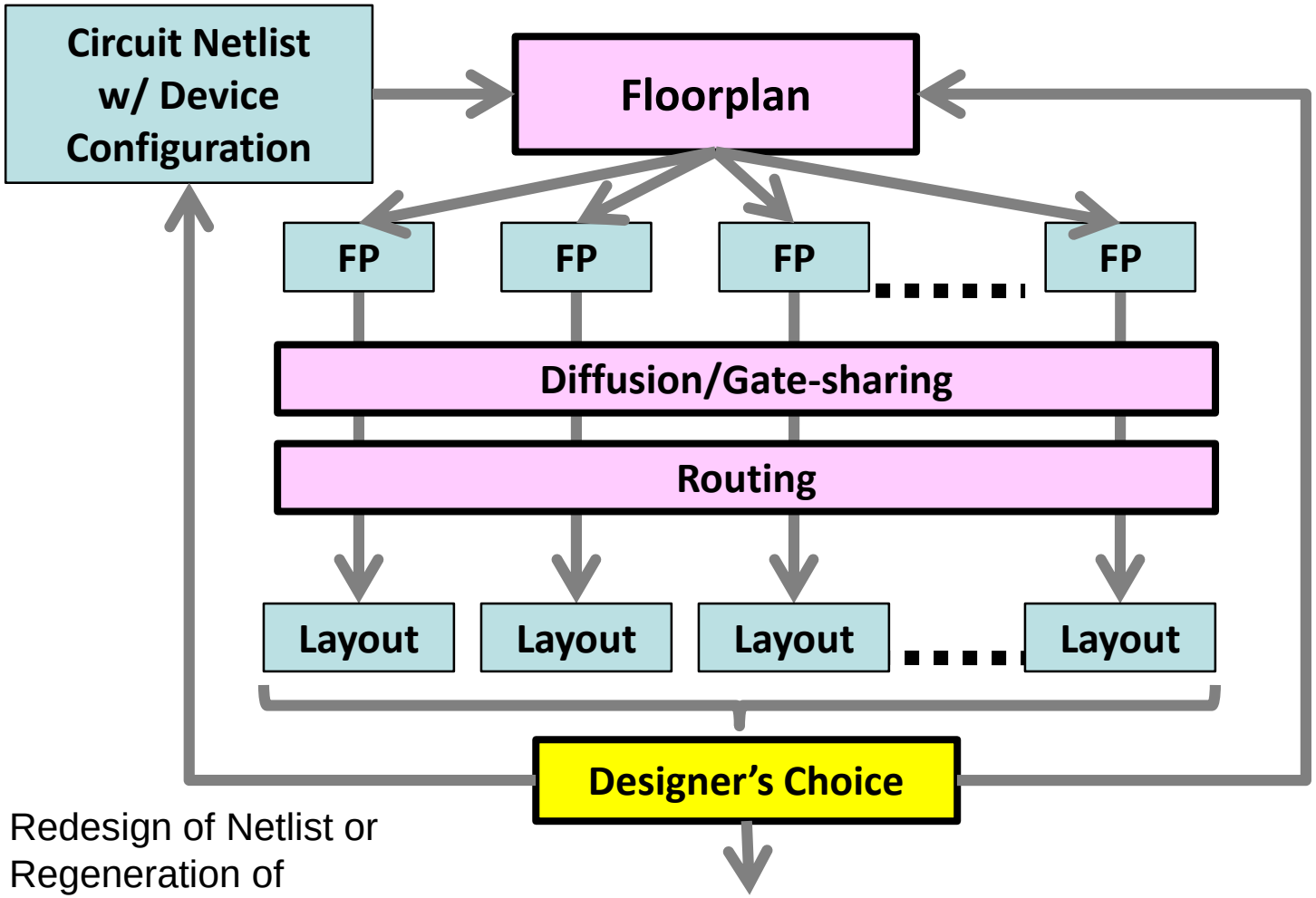


De-compaction
No DR-errors.

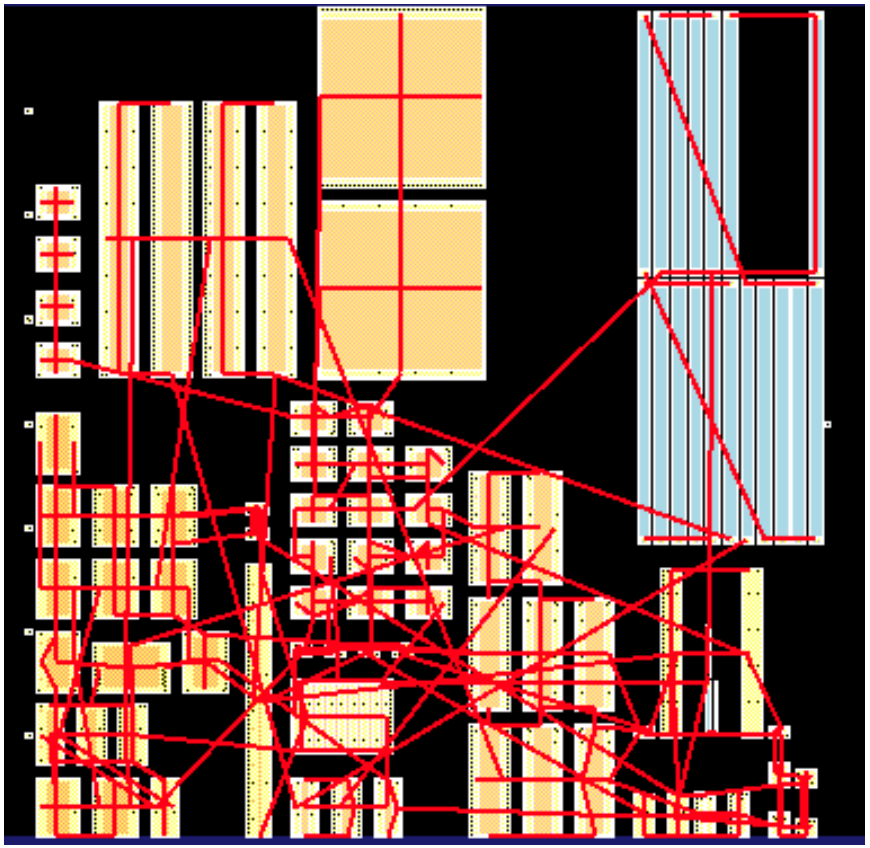


1D-Compaction
No DR-errors.

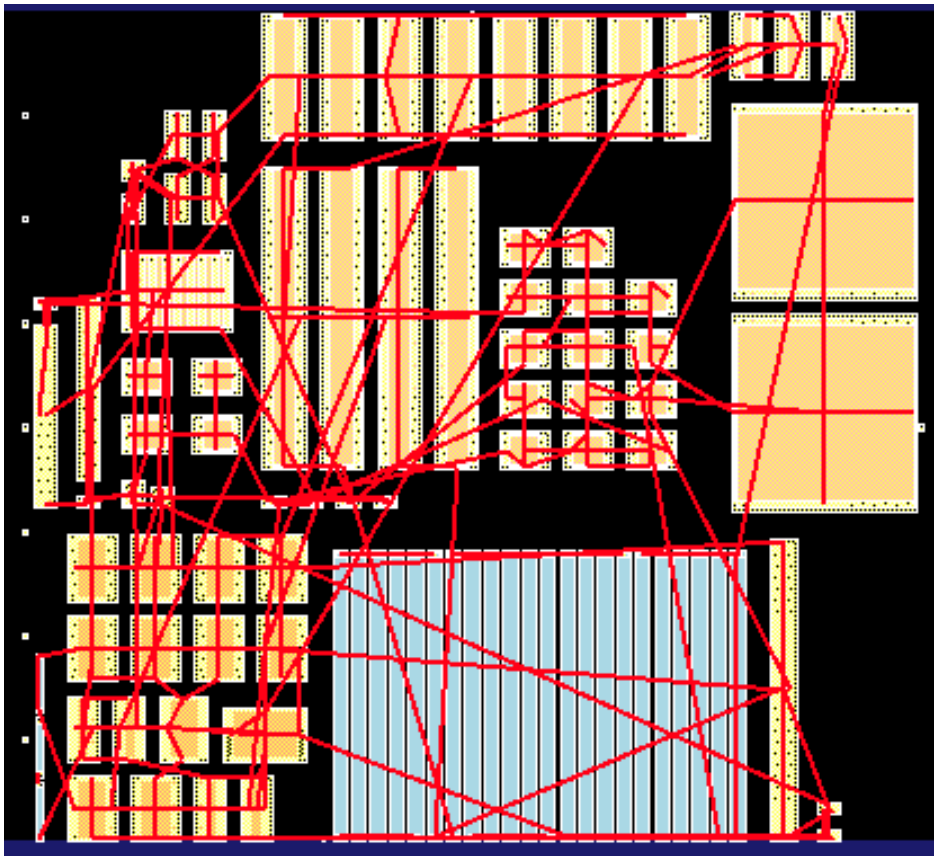
w/ Rect. Packing: Multi-output Floorplan



Comparison: Rect. Packing-base Placement (1)



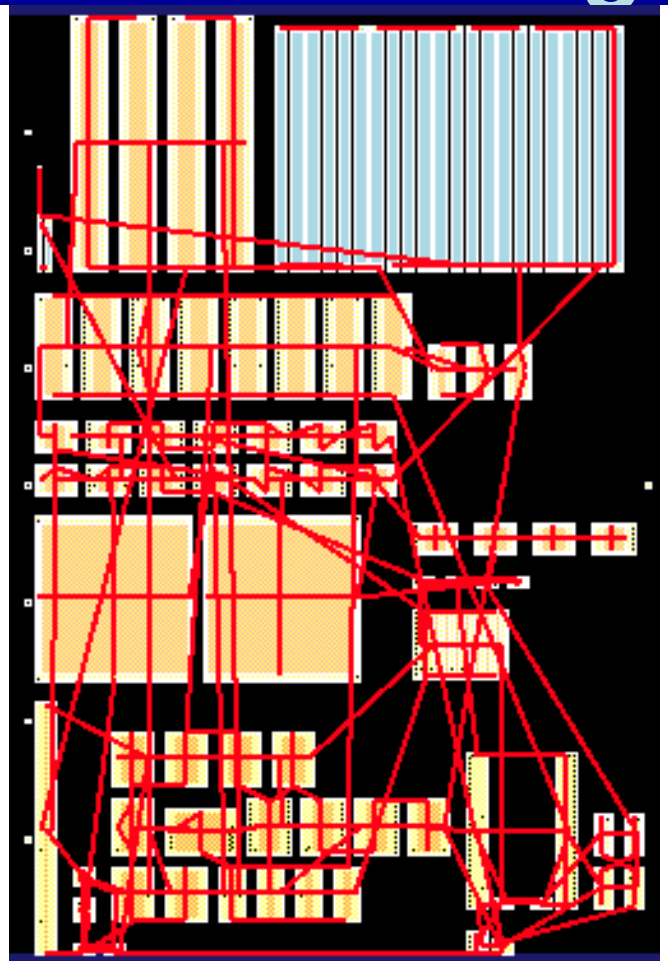
AREA : 23,212 (78%)
HPWL : 3,443 (115%)
No DR-errors.



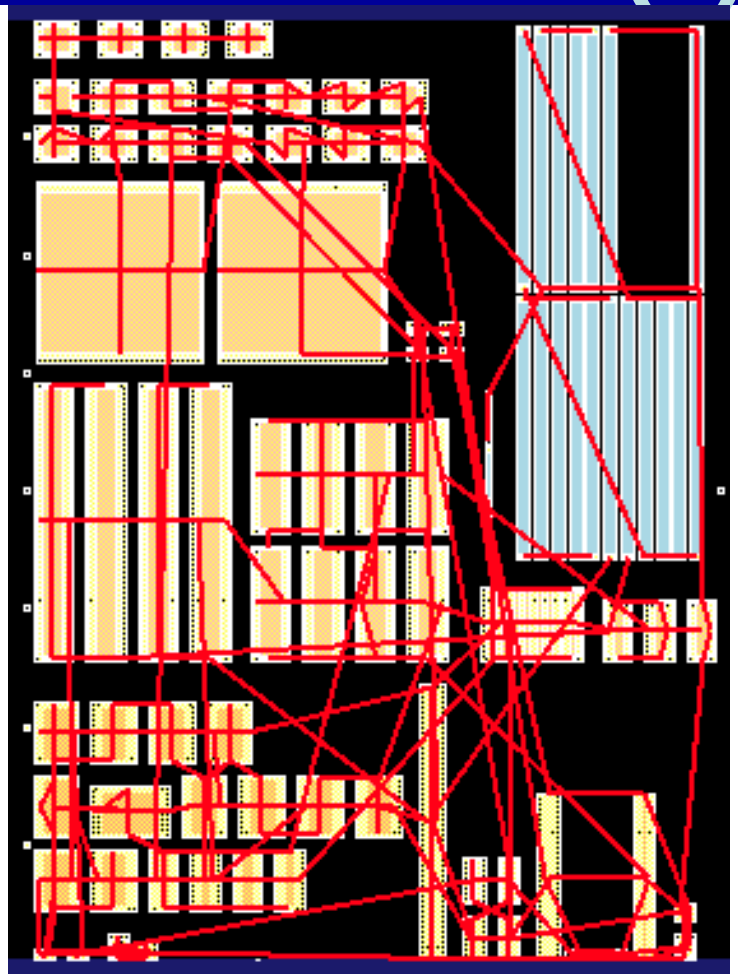
AREA: 25,405 (85%)
HPWL: 4,010 (134%)
No DR-errors.

Total time for 10 placements: 7.0 sec.

Comparison: Rect. Packing-base Placement (2)



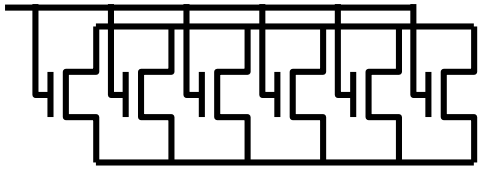
AREA : 27,070 (91%)
HPWL : 3,814 (127%)
No DR-errors.



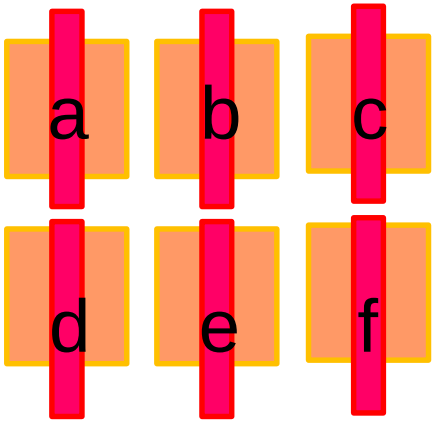
AREA : 26,798 (90%)
HWPL : 4,083 (136%)
No DR-errors.

w/ Rect. Packing: Dynamic Diffusion/Gate Sharing

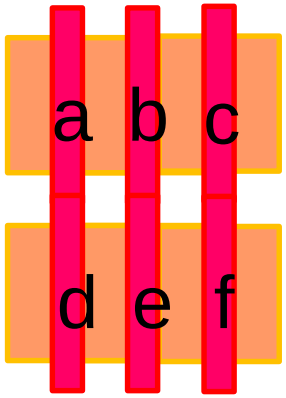
Diffusions (gates) can save area if they have the same net



circuit schematic



not sharing

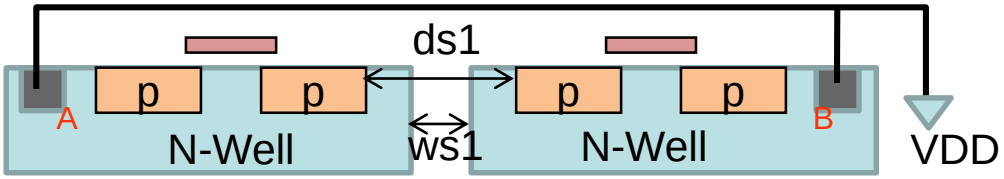


diffusion and gate sharing

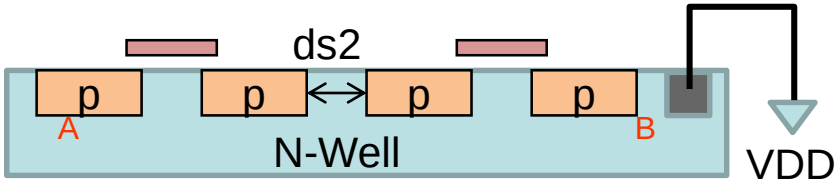
possible gate/diffusion sharing:
a set of blocks forming a topological row and array

w/ Rect. Packing: Dynamic Well Island Generation

Different rules for separation between wells

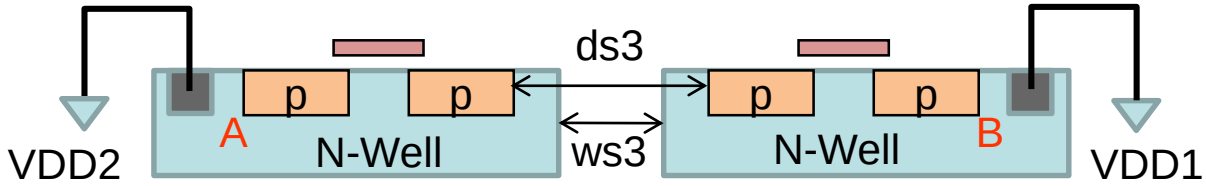


A and B have the same potential → separation = ws1



NOTE: ds2 < ws1 < ws2

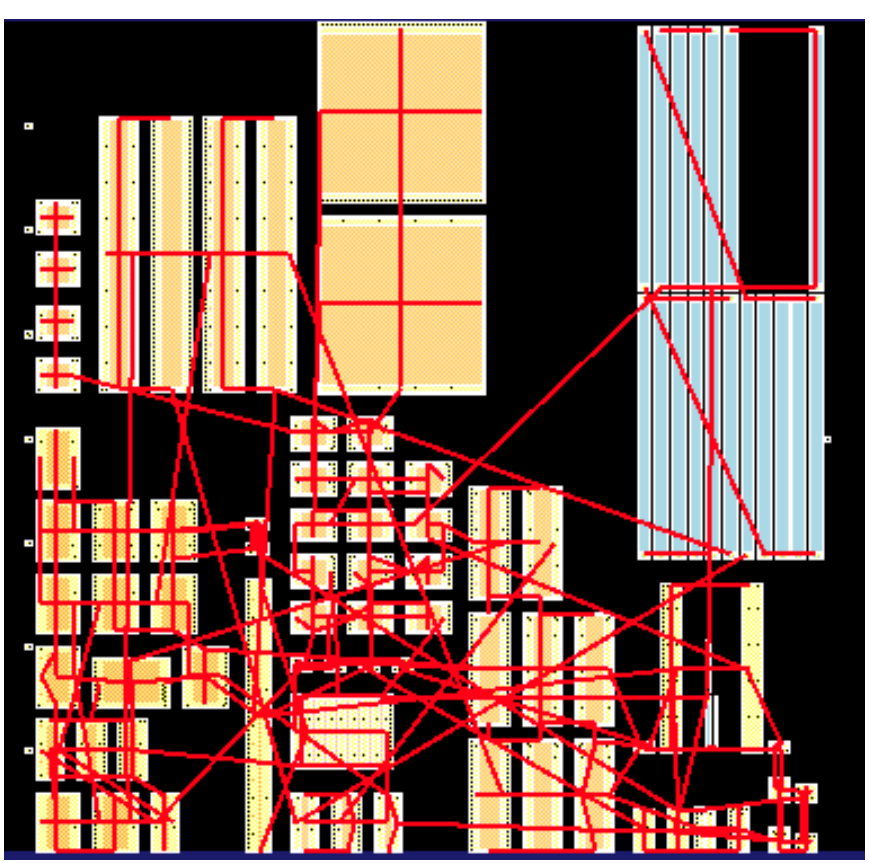
A and B have the same well island → separation = ds2 not for wells but diffusion



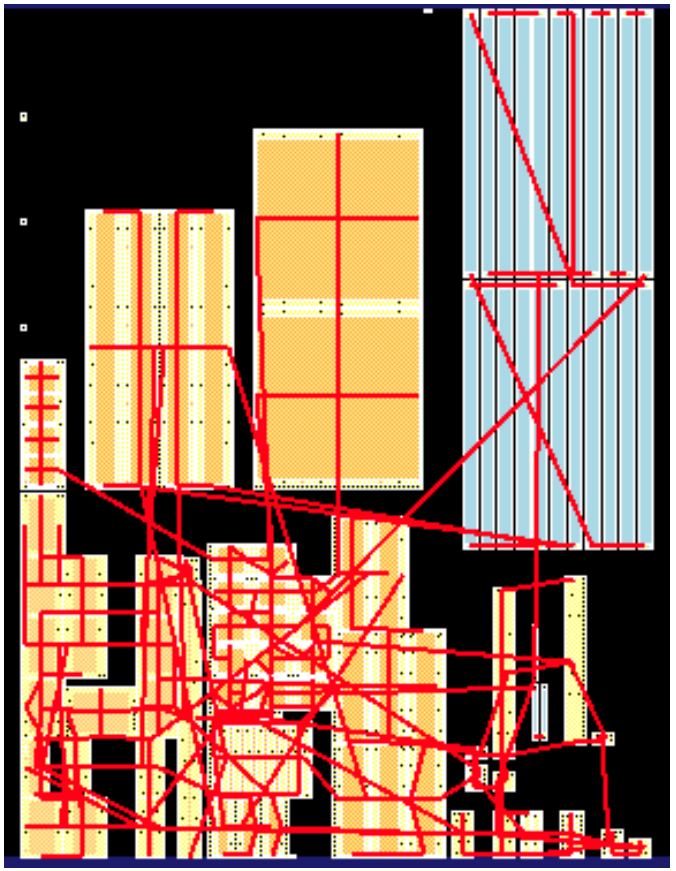
A and B have different potential wells → separation = ws3

possible well-island :
a set of blocks which are rectangular extractable

Control of Adjacency: Diffusion Sharing



w/o diffusion sharing



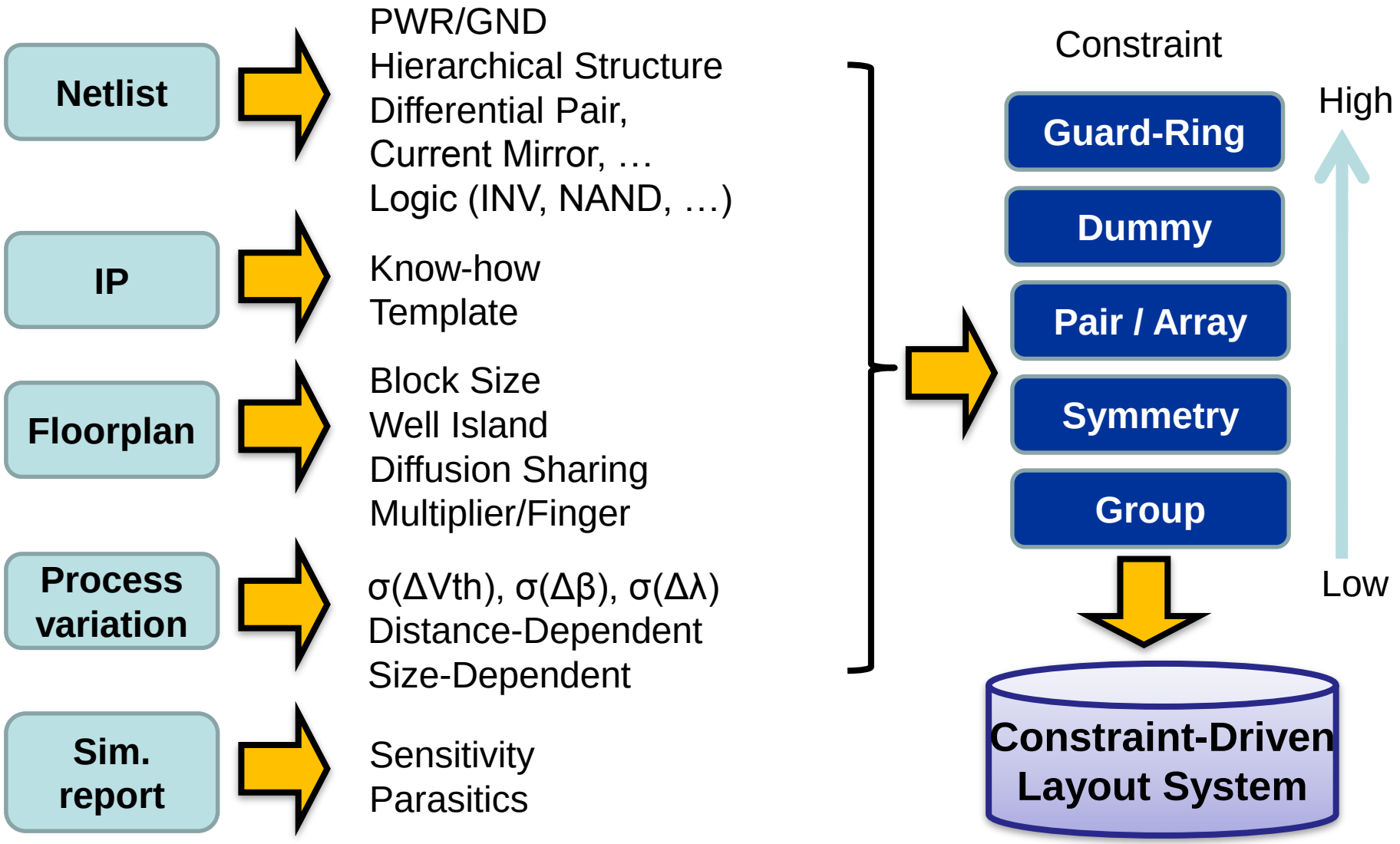
w/ diffusion sharing

Summary

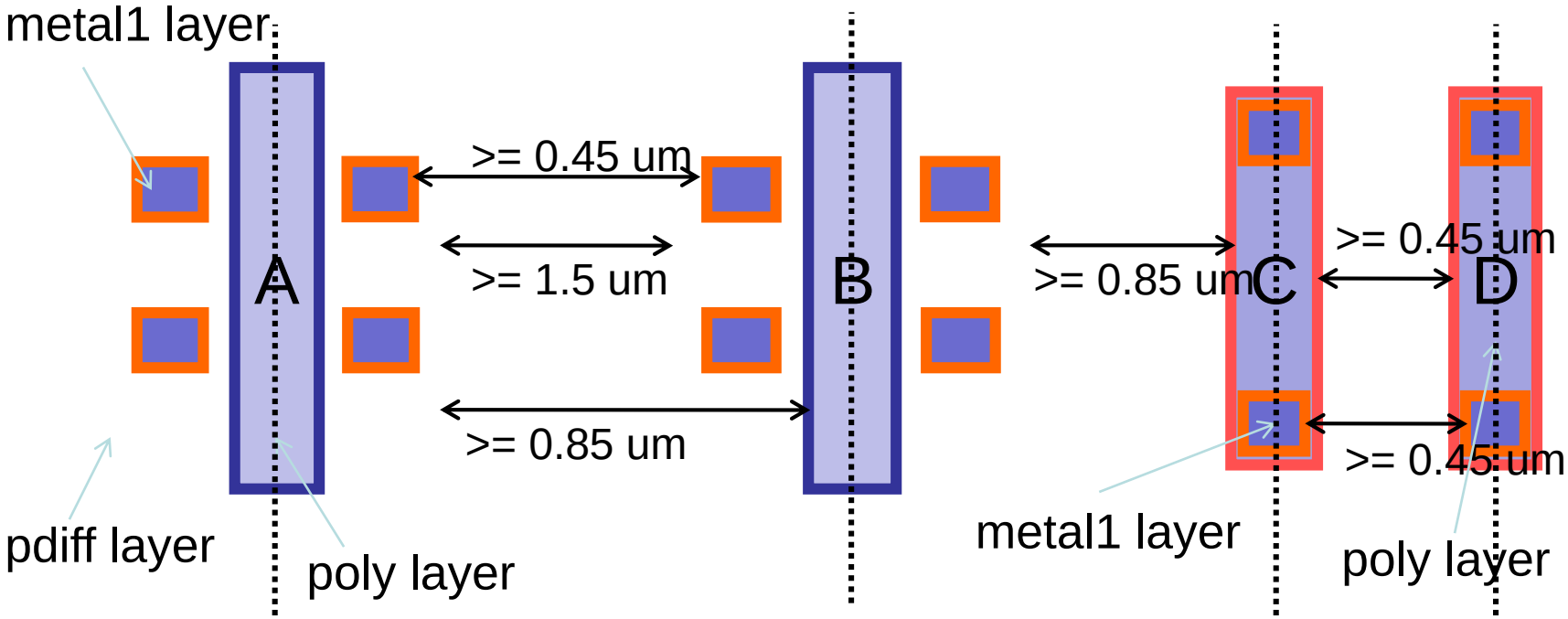
- Rect. Packing:
  - Compacted
  - Multi-output
  - Soft modules
  - No DR errors
  - Easy to take constraint-driven
  - **Easy to control adjacency (constraints)**
  - Floorplan to estimate area
- Analytical:
  - Less wire-length
  - Quick
  - Scalability
  - Potentially applicable to sensitivity-driven
  - Initial placement for manual designer

Thank you!

Analog Layout Constraint

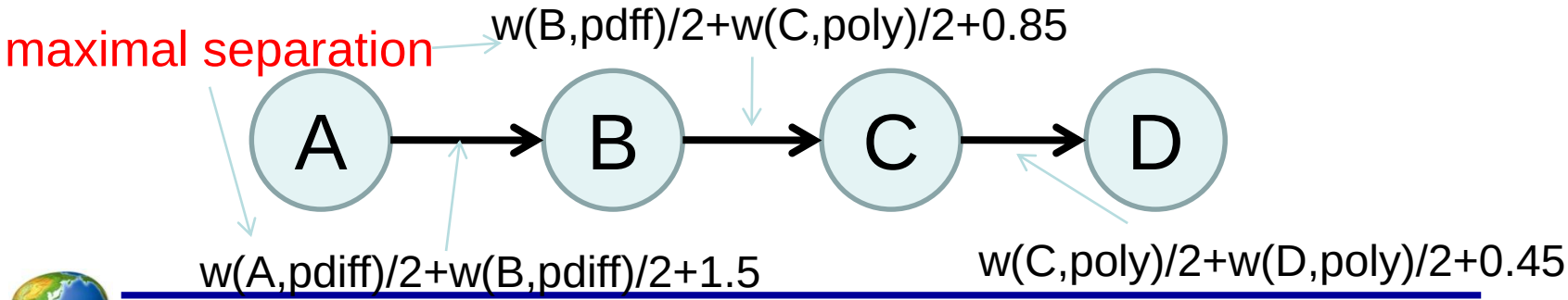


Separation Constraint

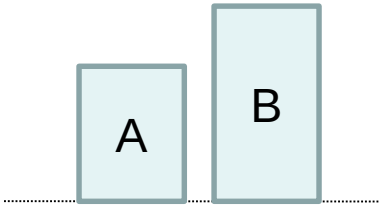


horizontal constraint graph:

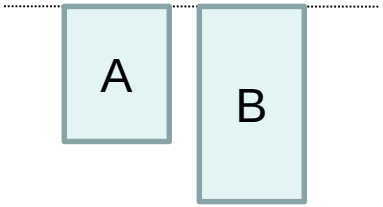
NOTE: w(X, L) = width of layer L of device X



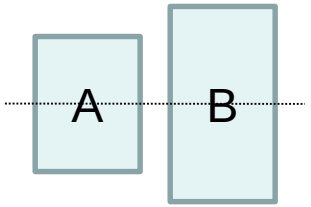
Alignment Constraint



bottom-alignment



top-alignment



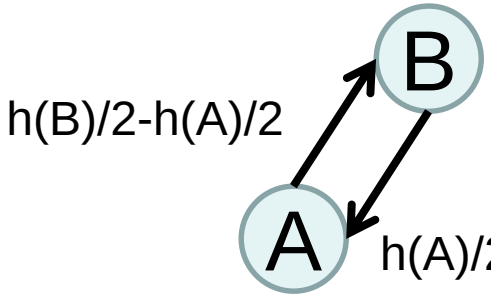
ycenter-alignment

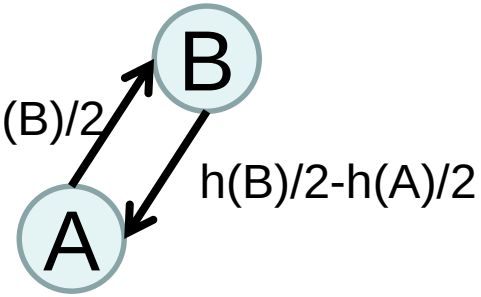
sequence-pair condition:

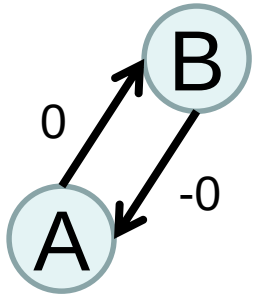
$\alpha^{-1}(A) < \alpha^{-1}(B), \beta^{-1}(A) < \beta^{-1}(B)$ or $\alpha^{-1}(B) < \alpha^{-1}(A), \beta^{-1}(B) < \beta^{-1}(A)$

SP=(…A…B…, …A…B…) SP= (…B…A…, …B…A…)

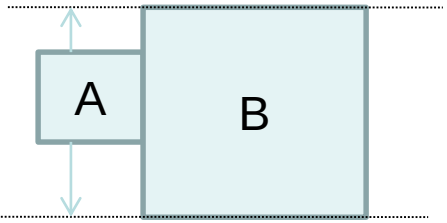
vertical constraint graph:



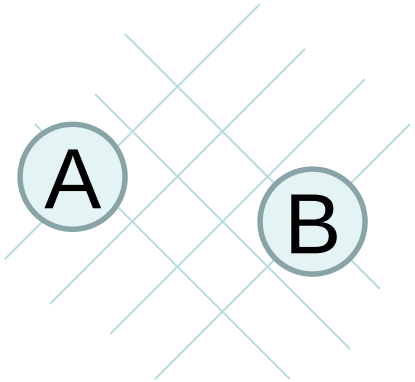




Abutment Constraint



horizontal-abutment



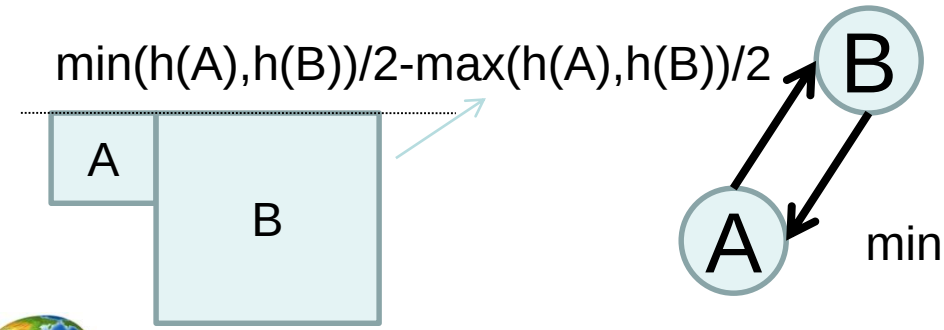
sequence-pair condition:

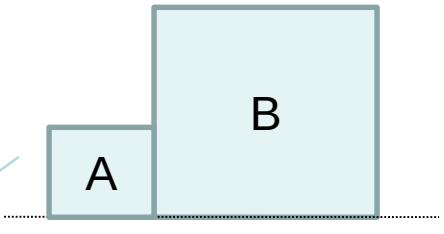
$\alpha^{-1}(A) < \alpha^{-1}(B), \beta^{-1}(A) < \beta^{-1}(B)$ and $\alpha^{-1}(X) < \alpha^{-1}(A)$ or $\alpha^{-1}(B) < \alpha^{-1}(X)$ or

$\beta^{-1}(X) < \beta^{-1}(A)$ or $\beta^{-1}(B) < \beta^{-1}(X)$

for $\forall X (\neq A, B)$

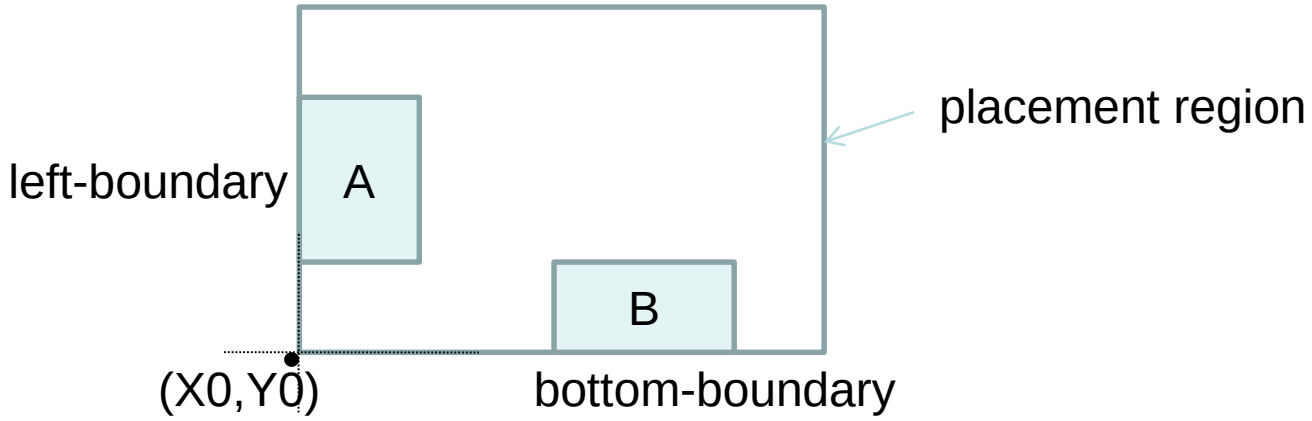
vertical constraint graph:





min(h(A),h(B))/2-max(h(A),h(B))/2

Boundary Constraint

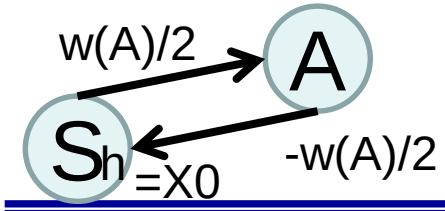


sequence-pair condition:

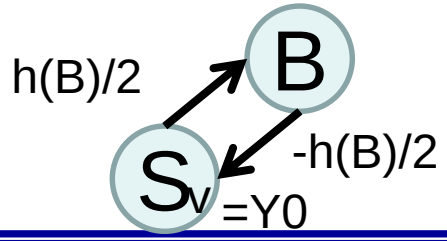
$$\alpha^{-1}(A) < \alpha^{-1}(X) \quad \text{or} \quad \beta^{-1}(A) < \beta^{-1}(X) \quad \text{for} \quad \forall X (\neq A)$$

$$\alpha^{-1}(X) < \alpha^{-1}(B) \quad \text{or} \quad \beta^{-1}(B) < \beta^{-1}(X) \quad \text{for} \quad \forall X (\neq B)$$

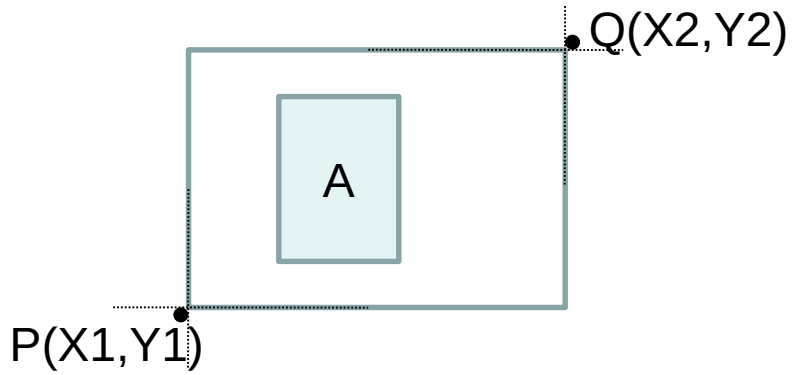
horizontal constraint graph:



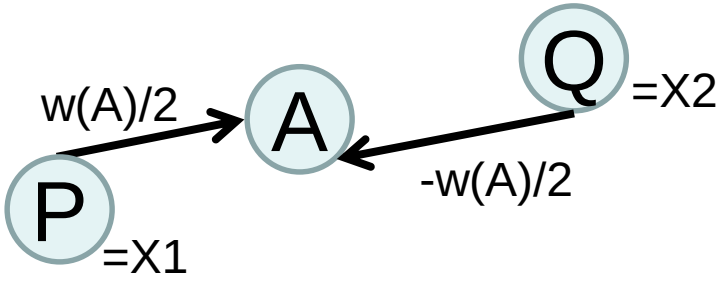
vertical constraint graph:



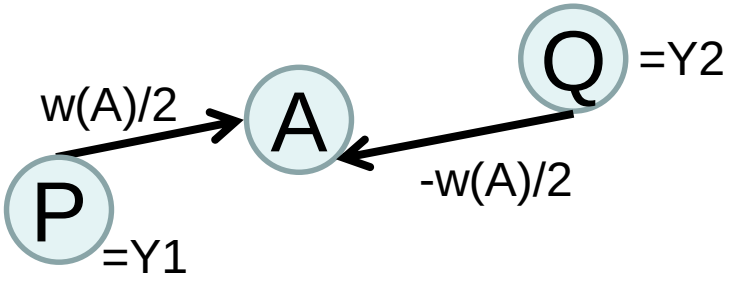
Range Constraint



horizontal constraint graph:

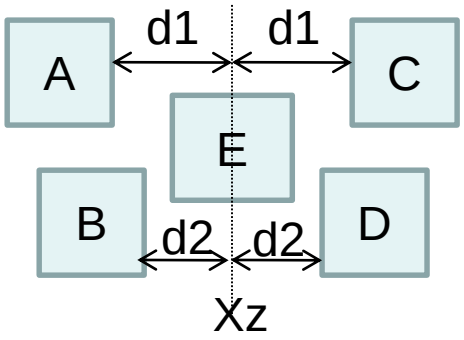


vertical constraint graph:



NOTE: P, Q are dummy blocks
range const. →preplaced const. if P and Q are the same as A

Symmetry Constraint



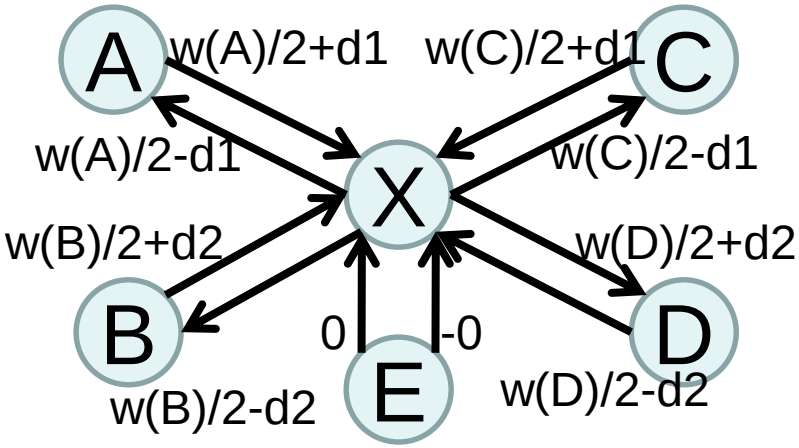
horizontal symmetry group
pair-symmetry: (A,C), (B,D)
self-symmetry: E

sequence-pair condition:

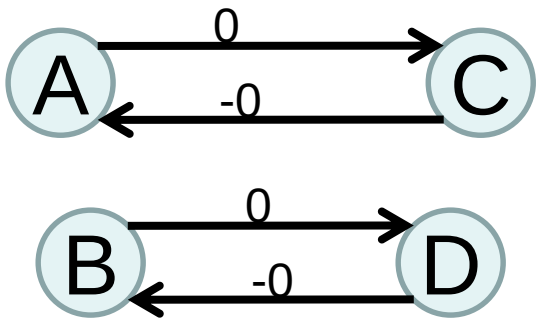
NOTE: sym(A)=C, sym(B)=D, sym(E)=E

$$\alpha^{-1}(A) < \alpha^{-1}(B) \Leftrightarrow \beta^{-1}(sym(B)) < \beta^{-1}(sym(A))$$

horizontal constraint graph:



vertical constraint graph:



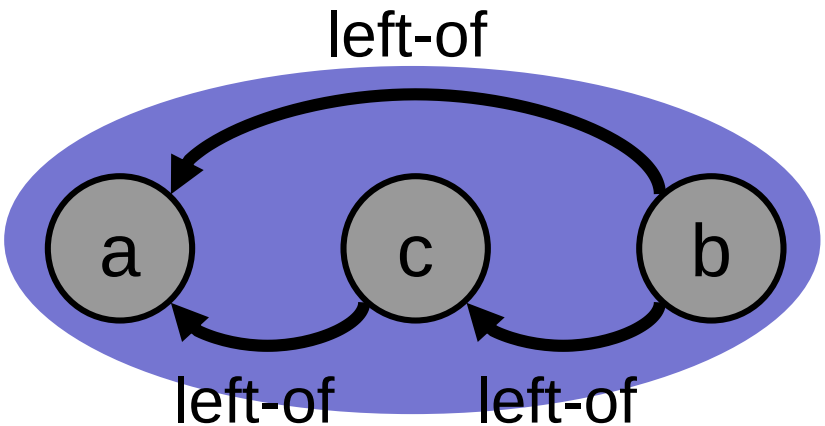
NOTE: ycenter-alignment

NOTE: X is dummy node, d1, d2 should be precalculated

Cluster Constraint(1)

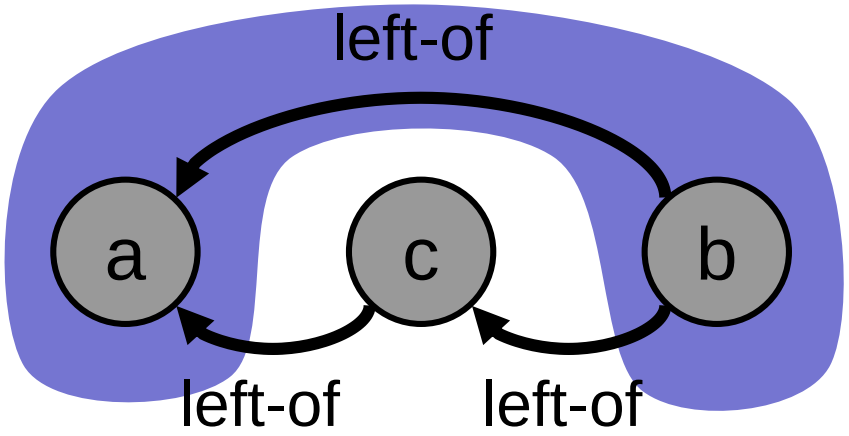
Horizontal-Convex:
For any pair (a, b) in X such that “a” is left-of “b”:
Any device “c” such that
“a” is left-of “c” and “c” is left-of “b” also belongs to X

Horizontal-convex



a, b, c ∈ X

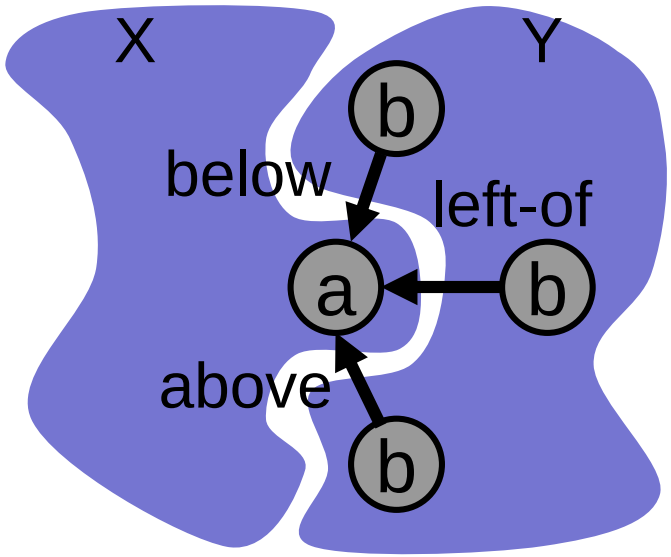
Not Horizontal-convex



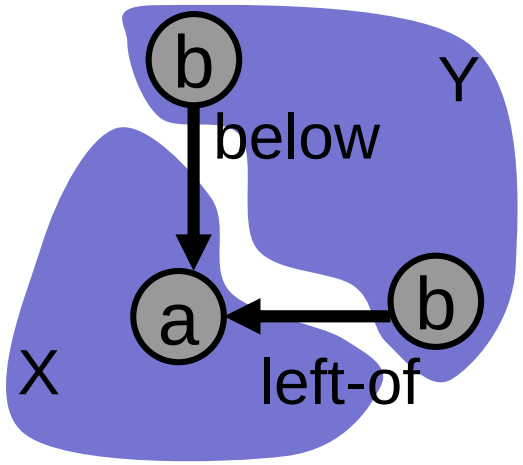
a, b ∈ X, c ∉ X

Cluster Constraint(2)

X is Convexly left-of Y:
- X and Y are horizontal-convex
- No pair (a, b) such that a $\in$ X is right-of b $\in$ Y



X is convexly left-below Y:
- X is convexly left-of and convexly below Y
- No pair (a, b) such that a $\in$ X is right-of and above b $\in$ Y



Cluster Constraint(4)

sequence-pair condition for all convex relation

X is convexly ... Y	Sequence-Pair ∀a ∈ X and ∀b ∈ Y
left-of	$\{\alpha^{-1}(a) < \alpha^{-1}(b)\} \cup \{\beta^{-1}(a) < \beta^{-1}(b)\}$
below	$\{\alpha^{-1}(a) > \alpha^{-1}(b)\} \cup \{\beta^{-1}(a) < \beta^{-1}(b)\}$
right-of	$\{\alpha^{-1}(a) > \alpha^{-1}(b)\} \cup \{\beta^{-1}(a) > \beta^{-1}(b)\}$
above	$\{\alpha^{-1}(a) < \alpha^{-1}(b)\} \cup \{\beta^{-1}(a) > \beta^{-1}(b)\}$
left-below	$\beta^{-1}(a) < \beta^{-1}(b)$
right-below	$\alpha^{-1}(a) > \alpha^{-1}(b)$
right-above	$\beta^{-1}(a) > \beta^{-1}(b)$
left-above	$\alpha^{-1}(a) < \alpha^{-1}(b)$