工業技術研究院
Industrial Technology
Research Institute

Benchmarking for Research in Power Delivery Networks of Three-Dimensional Integrated Circuits

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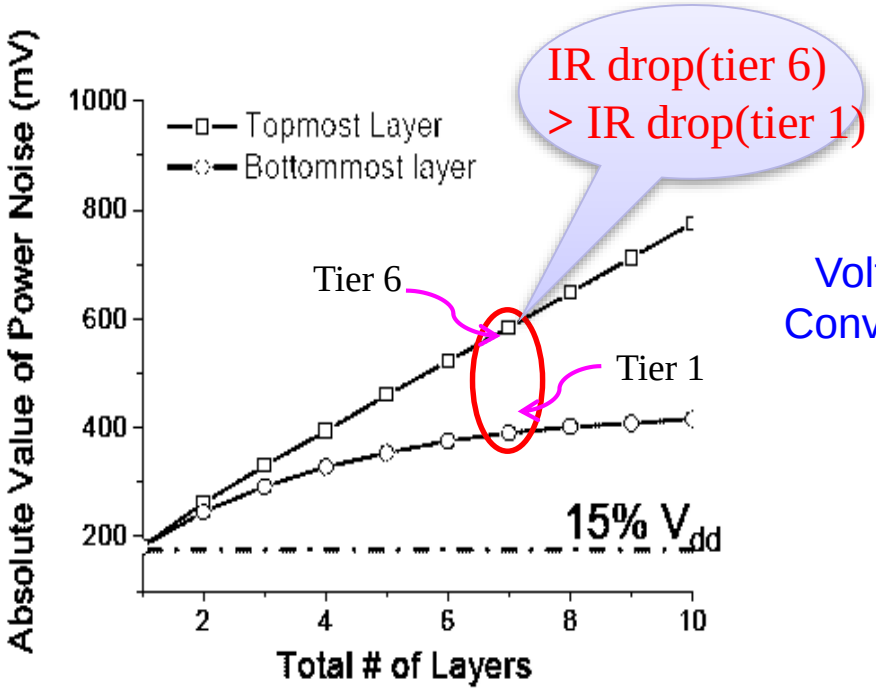
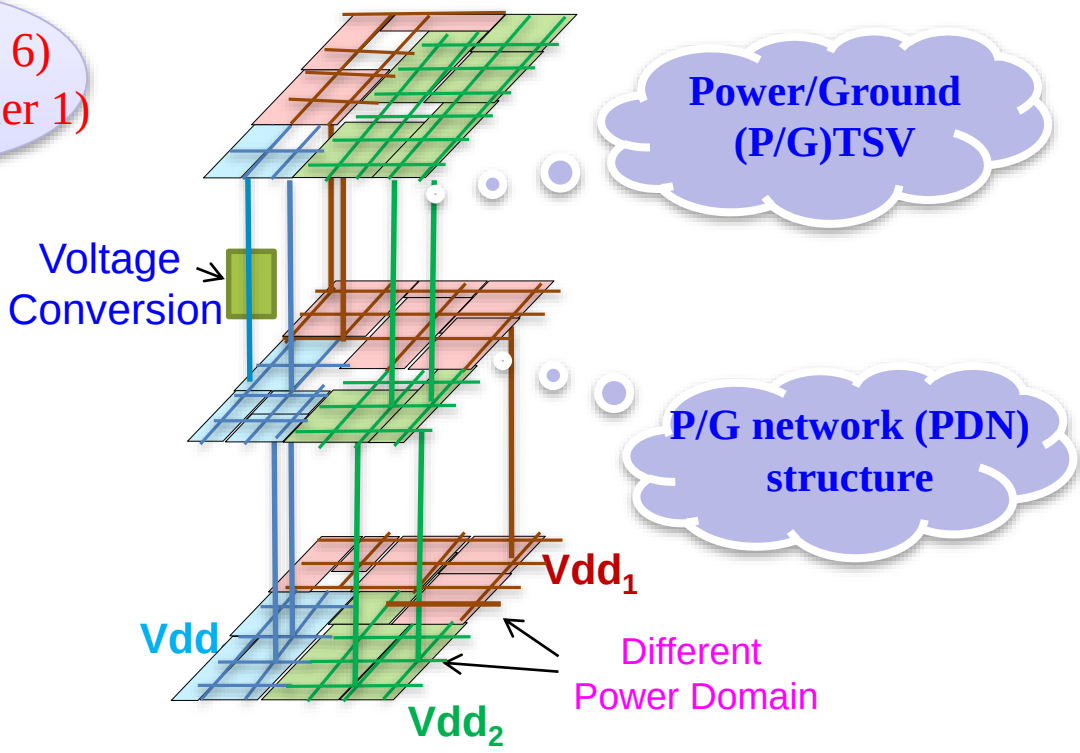
Power Delivery vs. IR Drop



Ref @ Joseph M. Pettit



IR drop in 3-D IC will be more serious!!

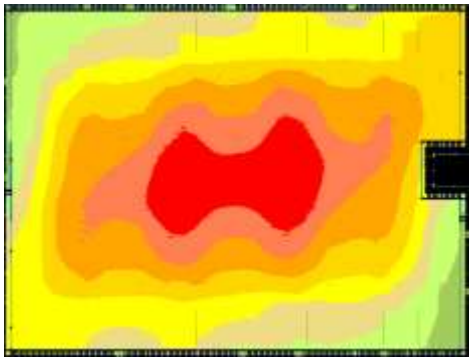
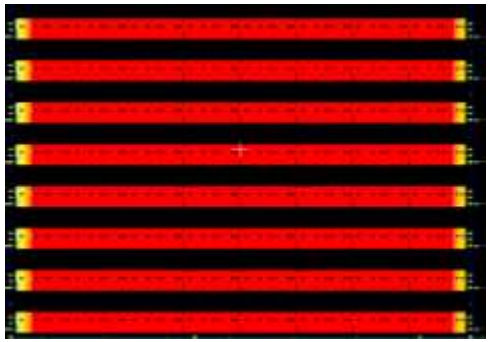
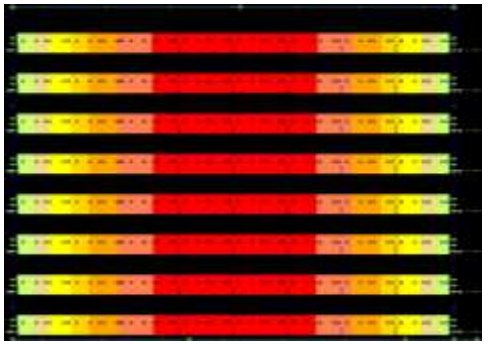
Much more vulnerable to power analysis attacks

Time Complexity

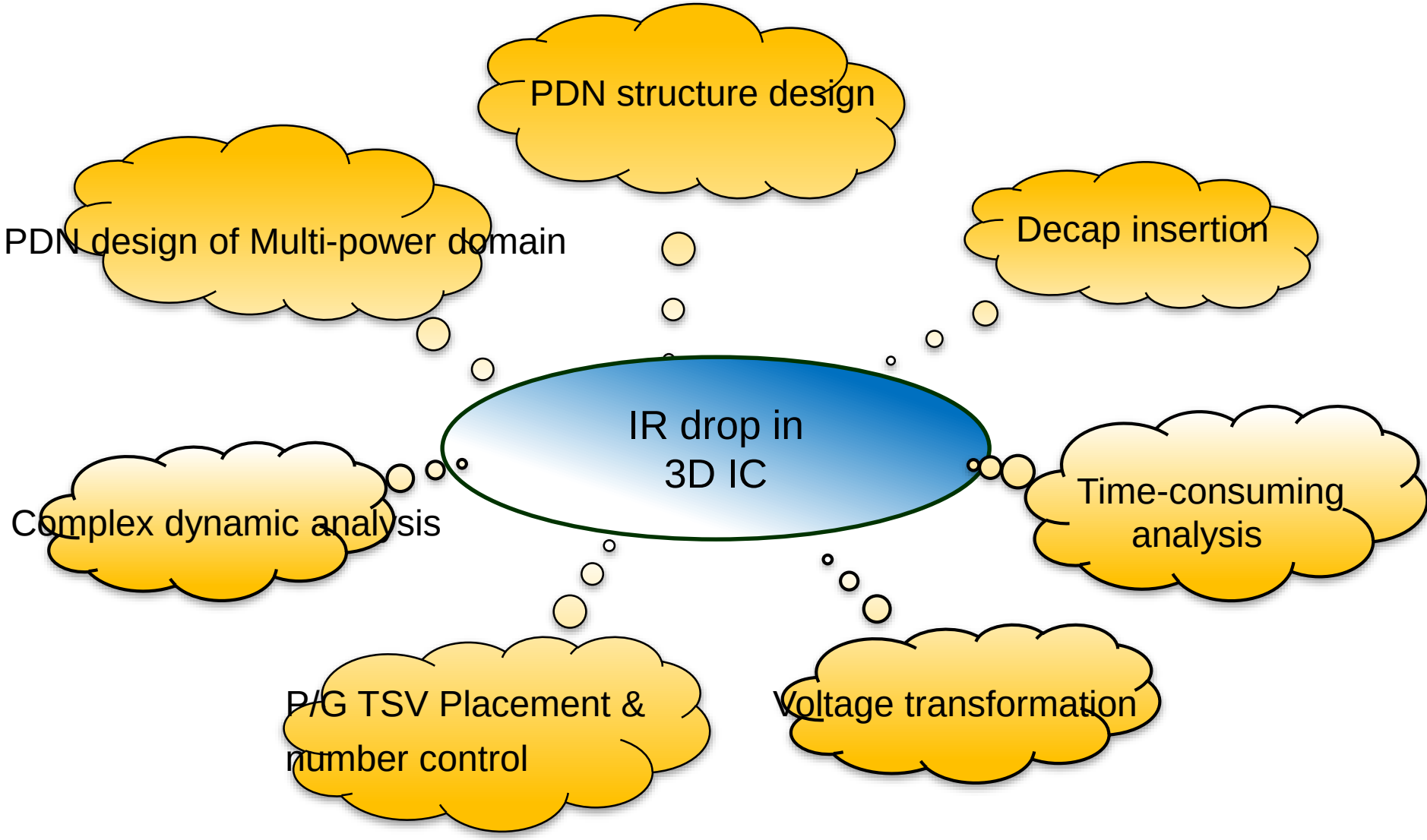
Time consuming

	Simulation Time	
	Stacked-die	Signal die
Tier0	7.4hr	1.1hr
Tier1		0.6hr

Serious IR drop

	Stacked-die	Signal die
Tier0		
Tier1		

3D IC PDN Design Challenge



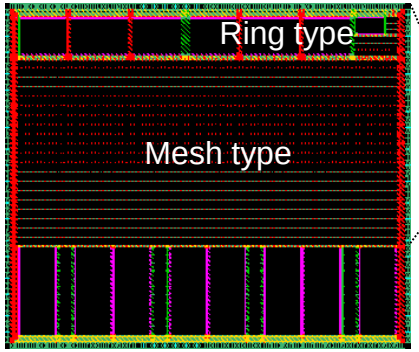
The Relative Research

- Active researches in 3D PDN
  - Spice-level 3D PDN modeling and simulation [Xu, et.al., 2011][Xie et.al., 2010]
  - Optimal 3D PDN design considering TSVs [Jung et.al., 2010][Singh et.al., 2010]
  - Decap insertion [Zhou et.al., 2009]
- The IBM 2D PDN benchmarks have stimulated the various researches in 2D PDN design, simulation and optimization.
  - However, no real 3D PDN benchmarks exist in the literature yet
- Researchers have to build their own ad-hoc 3D PDNs
  - Time consuming
  - Difficult to consider realistic design constraints
  - How to fairly compare different methods without identical benchmarks?

Outline

- Introduction
- TSV Modeling & Benchmark Circuit Description
- Released Data Description
- Conclusion

Power Integrity in Design Flow

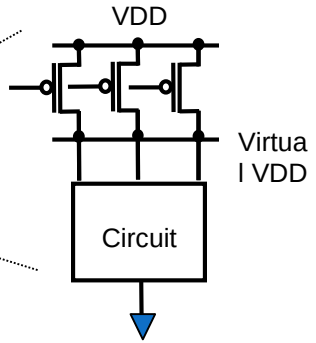


Power Planning

TSV location

Low power design

Using power gating



Placement

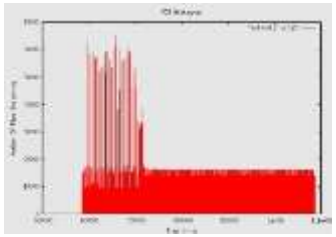
Routing

Decap insertion

TSV location refinement

PDN refinement

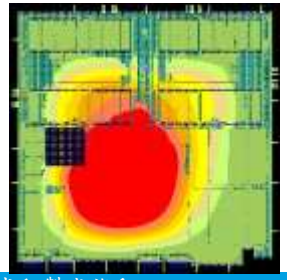
Rail Sign-off Analysis



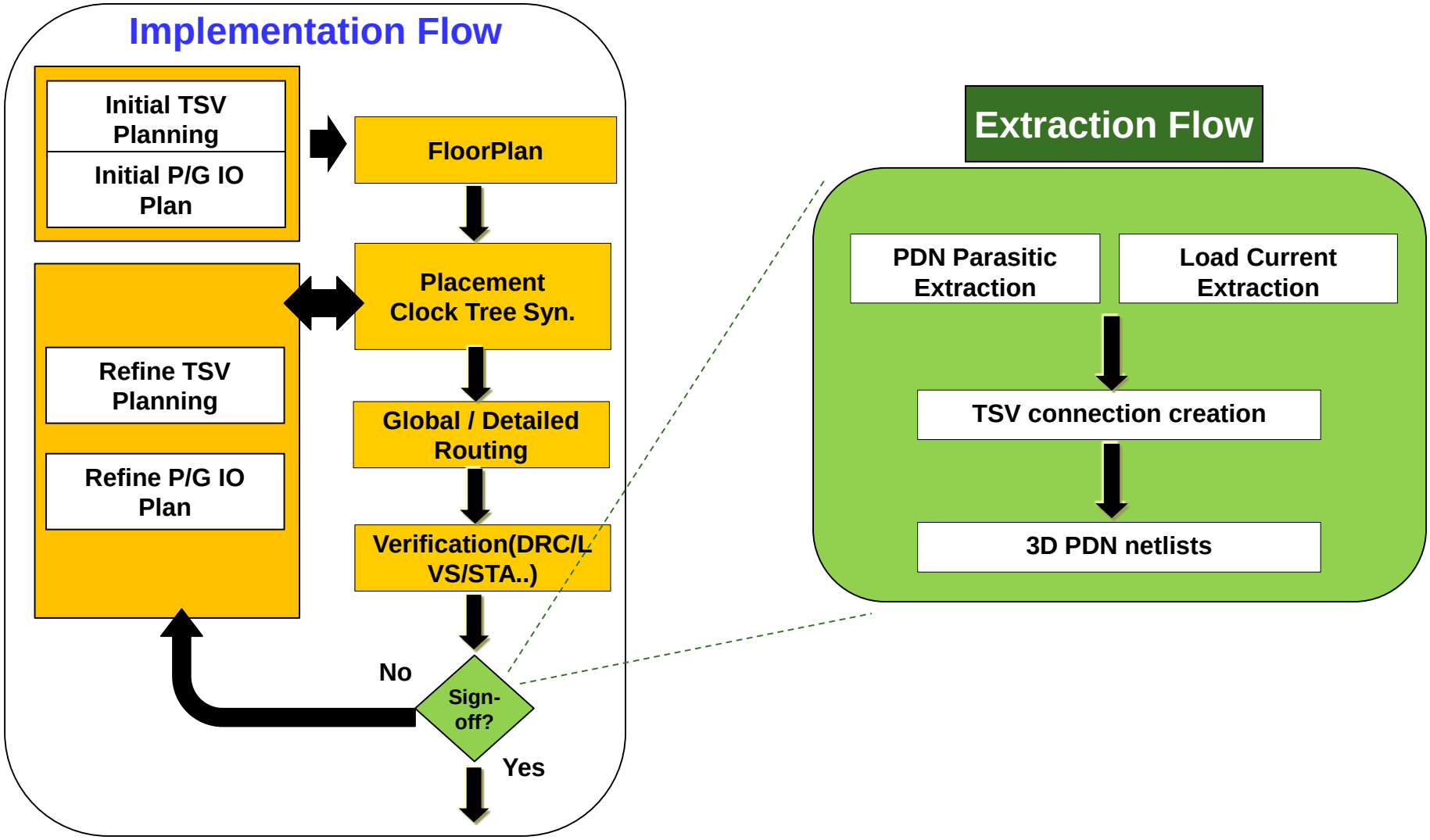
No

Satisfy?

Yes



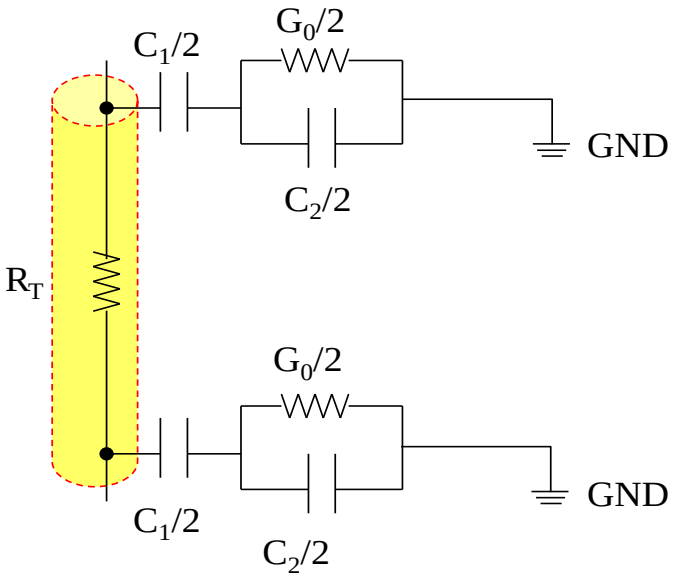
PDN Extraction in Design Flow



TSV Modeling

- Lumped circuit model for TSV parasitic parameters

Ref :H. Wang, J. Kim, Y. Shi and Jun Fan, "The Effects of Substrate Doping Density on the Electrical Performance of Through-SIlicon Vias," in Proc. of Asia-Pacific EMC Symposium, Jeju Island, Korea, 2011



- Simulated by ANSYS HFSS with
  - TSV height = 10*um*
  - TSV diameter = 10*um*
  - SiO_2 liner thickness = 0.5*um*

Parameter	Meaning
R_T	TSV resistance
C_1	TSV liner capacitance
C_2	Shunt capacitance of silicon substrate
G_0	Shunt conductance of silicon substrate

3D PDN Benchmarks Detail Information

P/G TSVs:279x

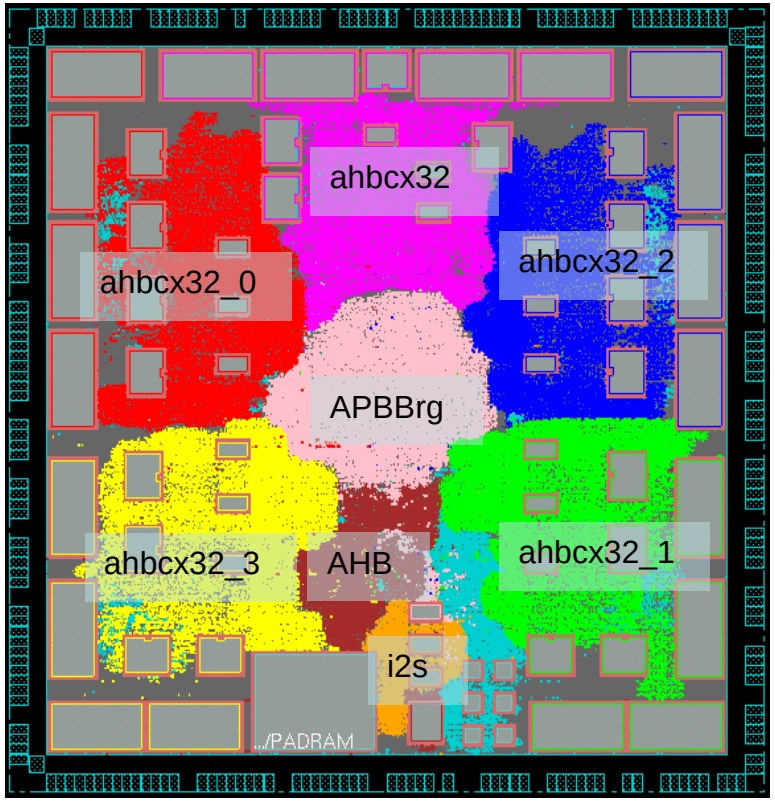
Chip name			3D-μP	3D-μPD	3D-TxRx	3D-SAP	3D-PAC
Chip information	VDD		1.8V	1.8V	1.8V	1.8V	1.0V
	VSS		0.0V	0.0V	0.0V	0.0V	0.0V
	Tier #		2	2	3	2	2
	P/G TSV #		8	8	16	268	2,234
	Tier-0 die area (um^2)		4,832x4,832	4,832x4,832	1,900x1,950	9,000x7,000	7,880x7,880
	Tier-1 die area (um^2)		4,832x4,832	4,832x4,832	1,900x1,950	7,280x5,390	3,880x3,880
	Tier-2 die area (um^2)		--	--	1900x1950	--	--
	Instance #		125,388	551,889	110,657	1,032,275	2,044,743
	Pad #		304	304	232	412	500
PDN Information	General	Metal layers #	7	7	7	7	10
		Current source #	239,530	239,530	218,066	2,902,474	3,364,314
		Voltage source #	28	28	16	36	51
	DC only	Node #	826,524	1,021,185	244,651	4,588,540	8,983,606
		Resistor #	913,154	1,178,081	312,251	7,638,905	13,234,026
	Tran. only	Node #	826,542	1,021,203	244,683	4,589,076	8,988,071
		Resistor #	913,170	1,178,097	312,283	7,639,442	13,238,494
		Capacitor #	762,239	967,057	235,189	4,147,603	6,067,910
		Current source step #[1]	200	140	140	160	100
Static noise (DC only)	Max(mV)		61	44	19	58	36
	Average(mV)		37	33	10	27	25

Dynamic noise can be reduced by 120mV

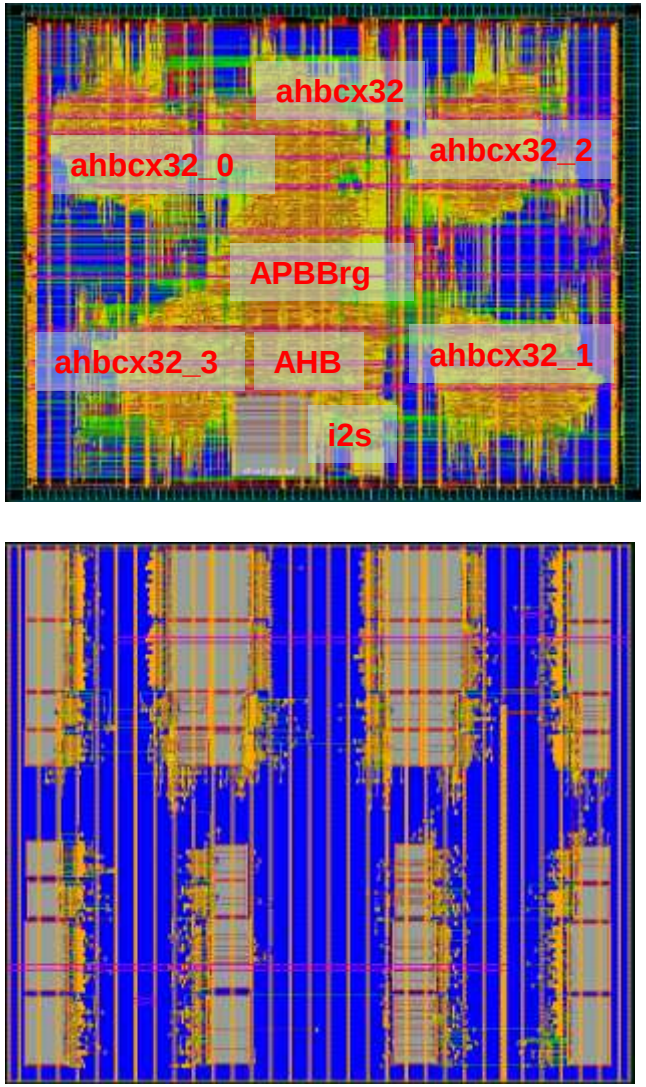
36x

Bechmark-3D_μp(1/2)

Original design:



3D IC:



tier0

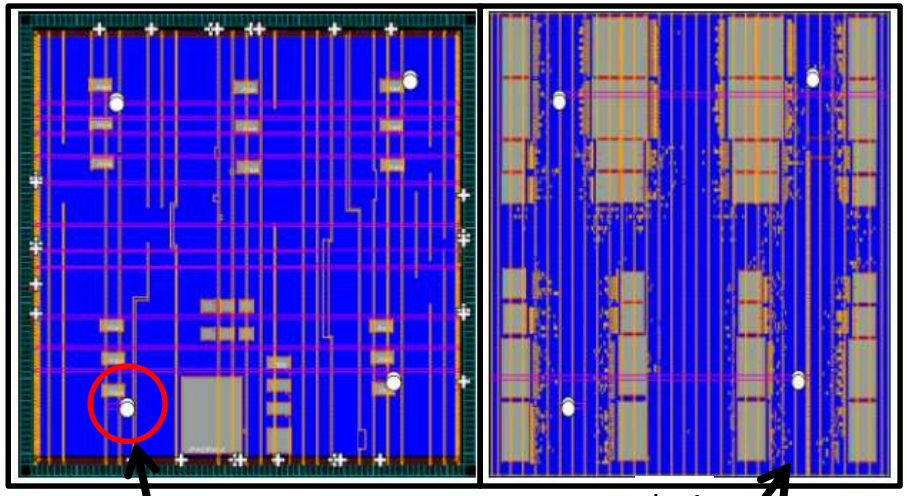
tier1

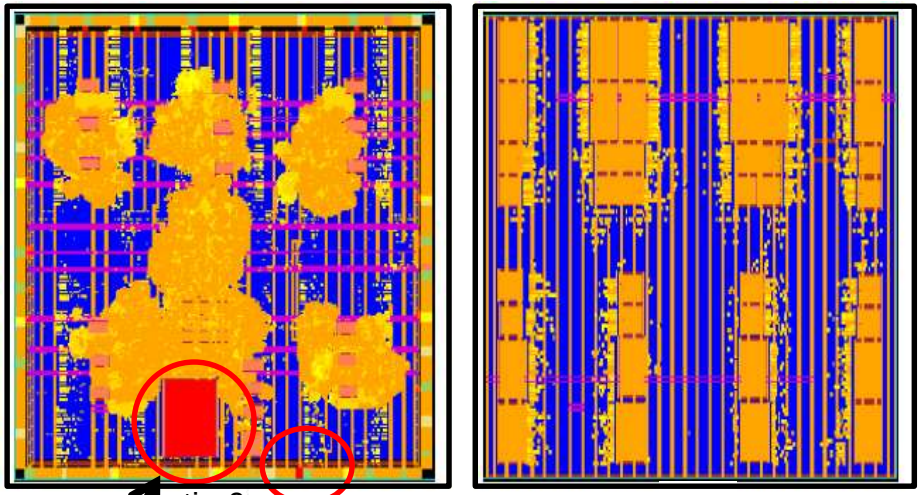
Tier0: five 32-bit microprocessors
AMBA High-performance Bus (AHB)
Tier1: SRAM banks

Bechmark-3D_μp(2/2)

PDN designs

Power maps





P/G TSVs pair

Blue region:
Follow pins

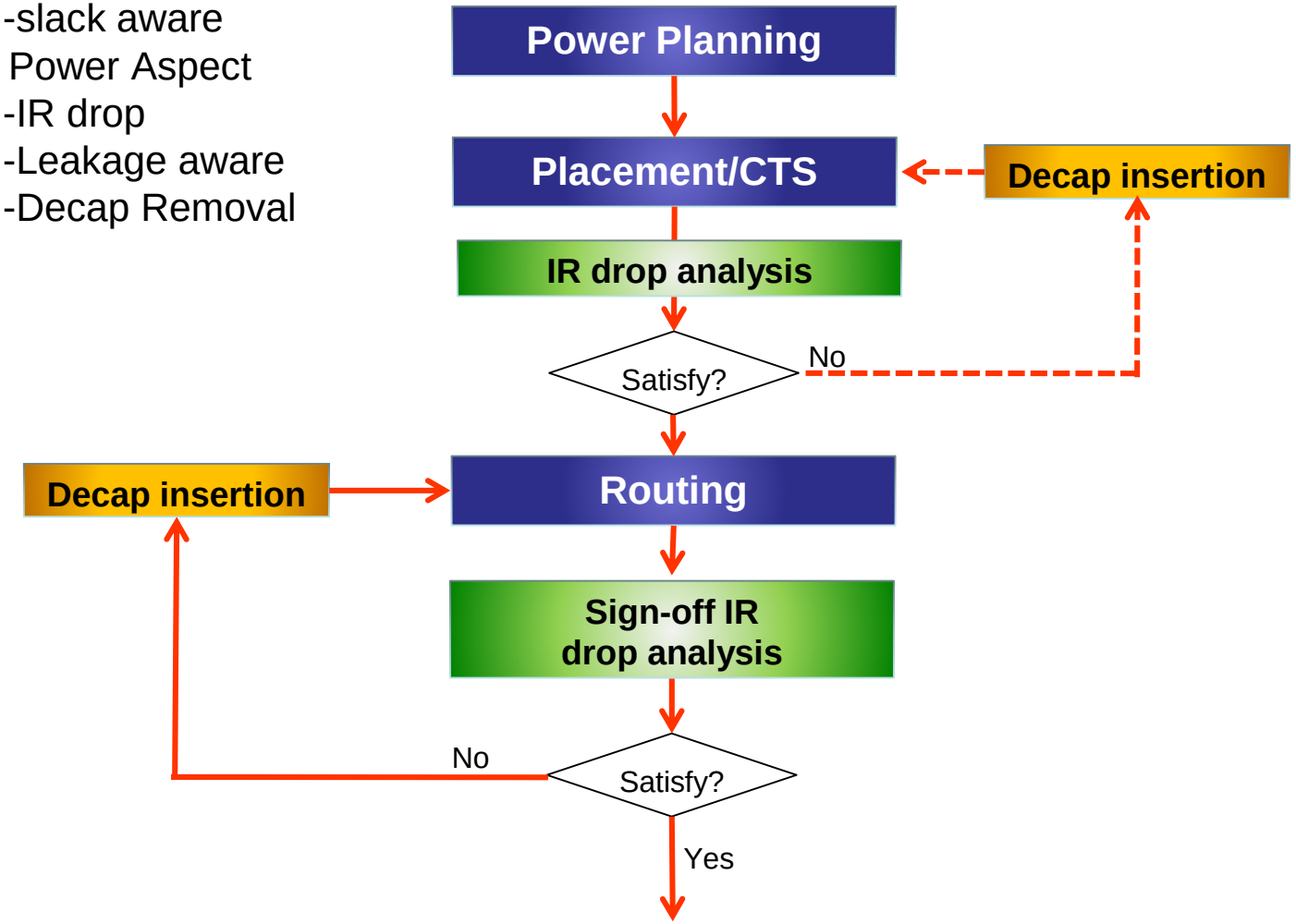
Memory & clock IO

Range(mW)	Cell Count	%
14.516~28.0321	2	0.00%
1~14.516	21	0.02%
0.001~1	24.771K	19.76%
0.0001~0.001	71.546K	57.07%
1e-05~0.0001	24.916K	19.88%
1e-06~1e-05	2.731K	2.18%
1e-07~1e-06	737	0.59%
0~1e-07	639	0.51%

- Choose to uniformly distribute the P/G TSVs
- Use 4 P/G TSVs pair

Decap Insertion Consideration

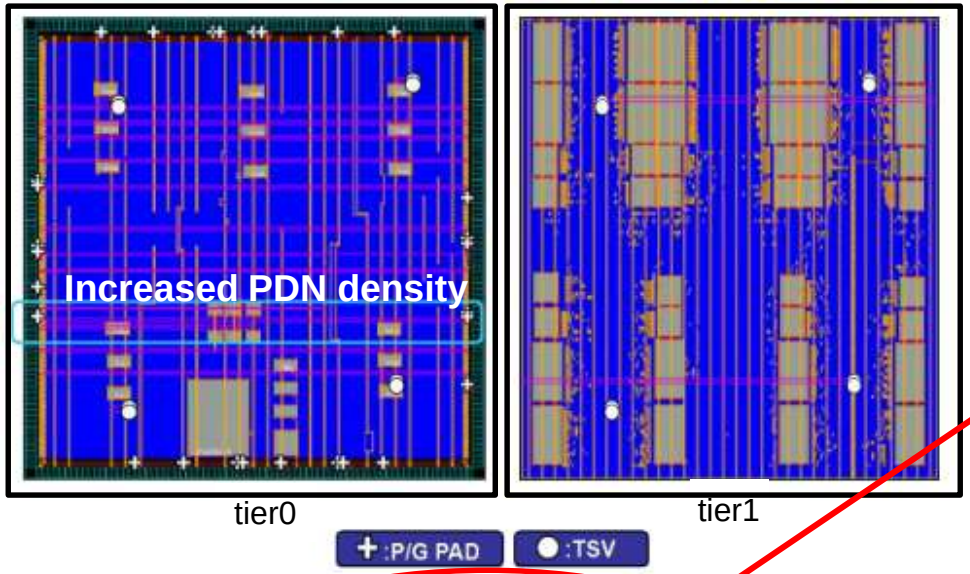
- Timing Aspect
  - -slack aware
- Power Aspect
  - -IR drop
  - -Leakage aware
  - -Decap Removal



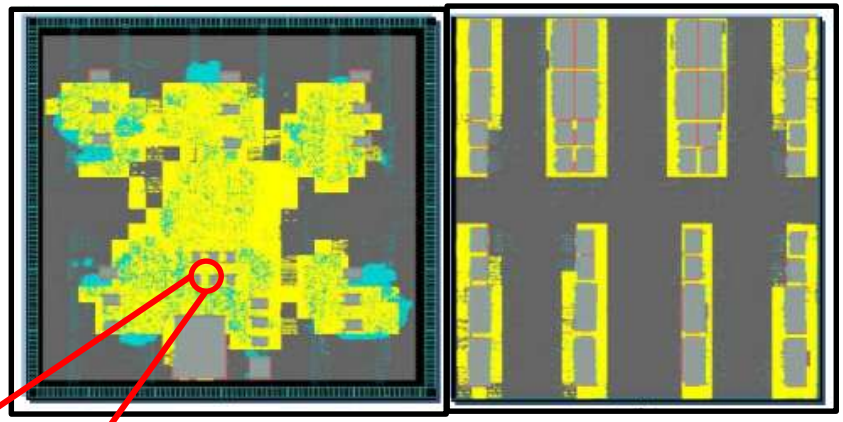
Ref: S.H. Chen, etc, "Experiences of low power design implementation and verification,*"2008 ASP-DAC Slide.*

Bechmark-3D_μpD

PDN designs



Decap requested maps



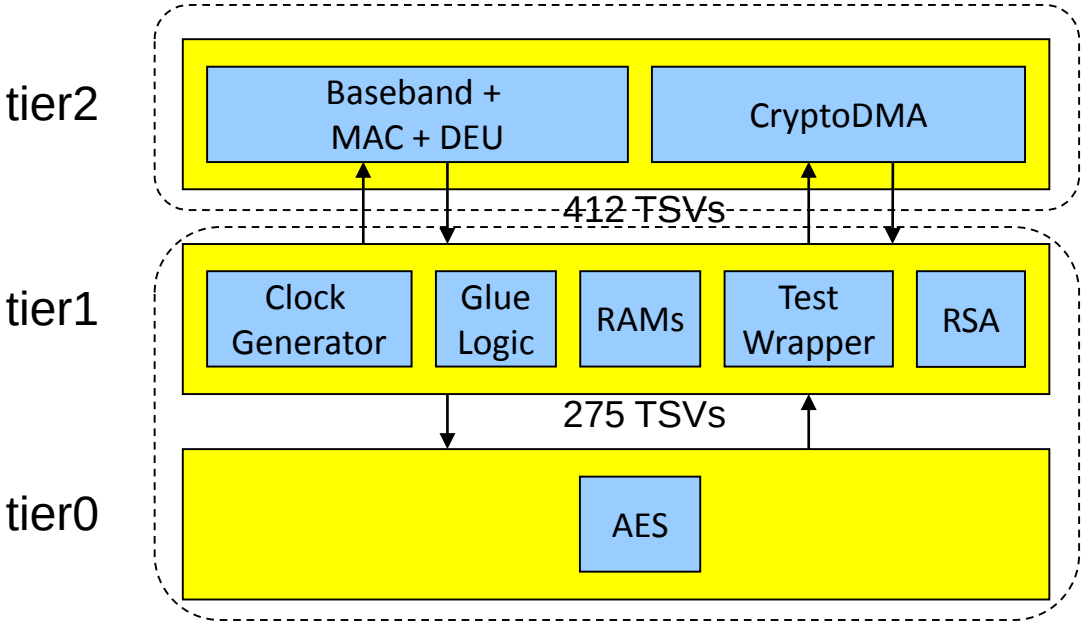

```
Data filtering results for decoupling cap requested for IR fix:
      Overall data minimum:        0F
      Overall data average: 3.15623e-14F
      Overall data maximum: 6.70113e-12F

Filter 1:  595483  of  595483  data values fell into this filter.
      filtered data range:          0F - 6.70113e-12F
      filtered data average: 3.15623e-14F
            8 values were in range 1:    5e-12F -    1e-09F
          111 values were in range 2:    3e-12F -    5e-12F
          276 values were in range 3:    2e-12F -    3e-12F
         1705 values were in range 4:    1e-12F -    2e-12F
         6087 values were in range 5:    5e-13F -    1e-12F
        16548 values were in range 6:    2e-13F -    5e-13F
         8526 values were in range 7:    1e-13F -    2e-13F
       562222 values were in range 8:        0F -    1e-13F
```

requested number of decaps

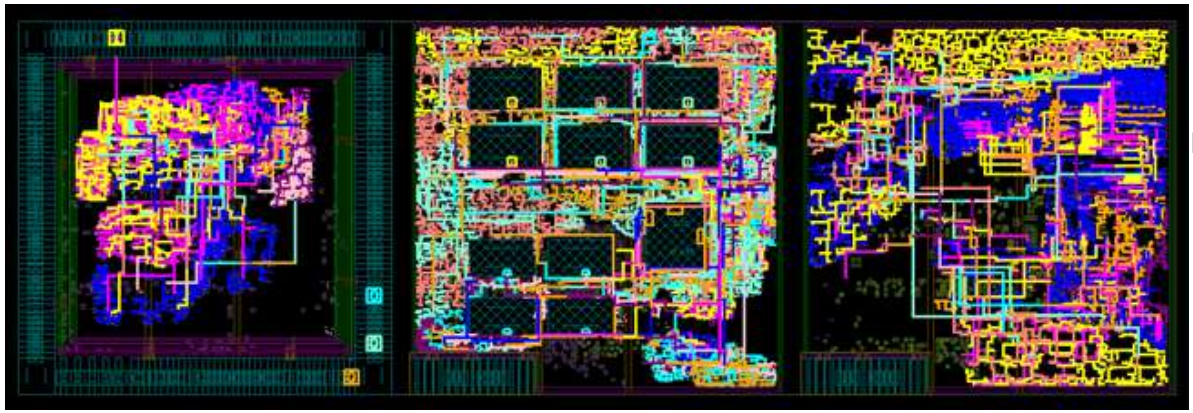
Dynamic noise can be reduced by 120mV

Bechmark-3D_TxRx(1/2)

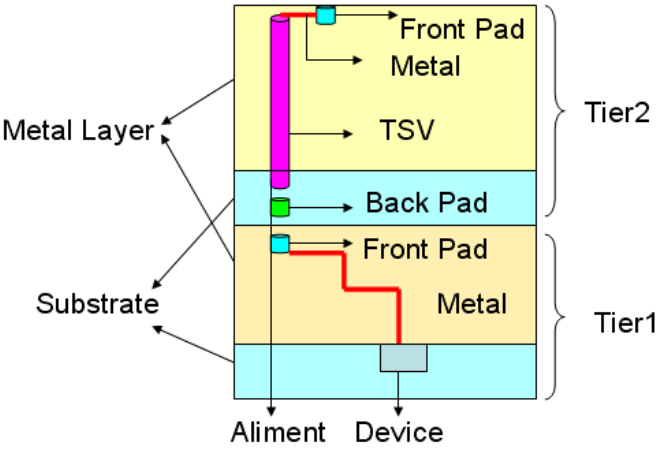


Communication logic
(baseband、MAC、DEU and TX/RX)

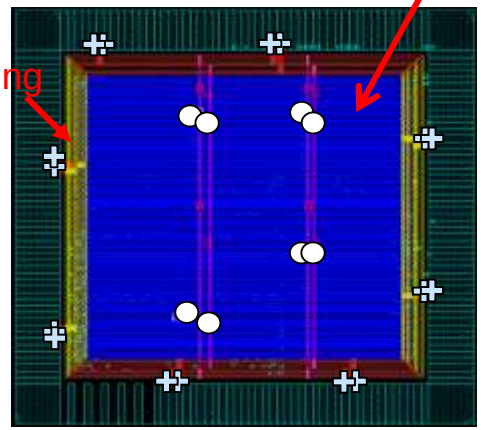
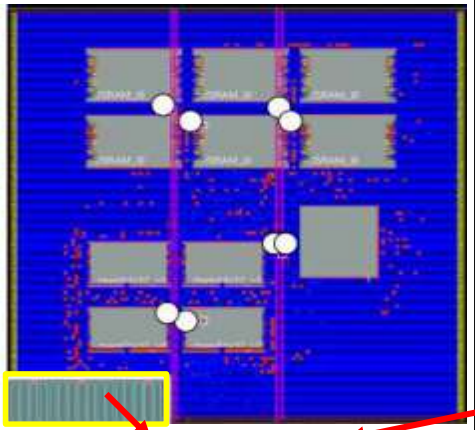
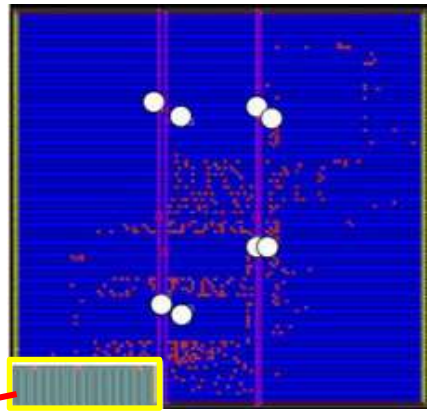
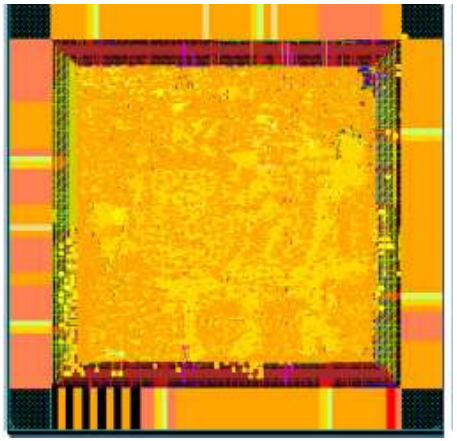
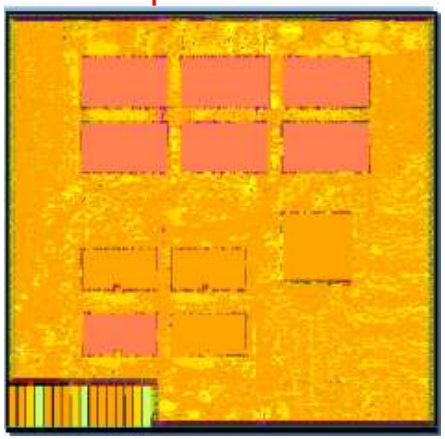
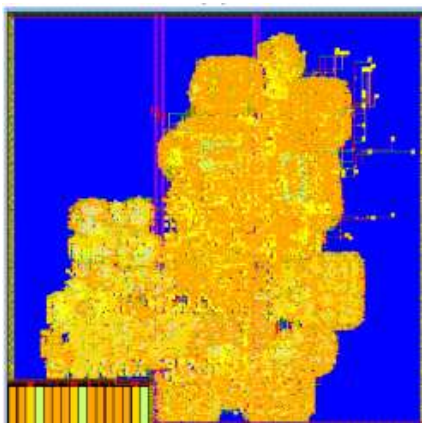
Logic/Testing function



◆TSV interconnection

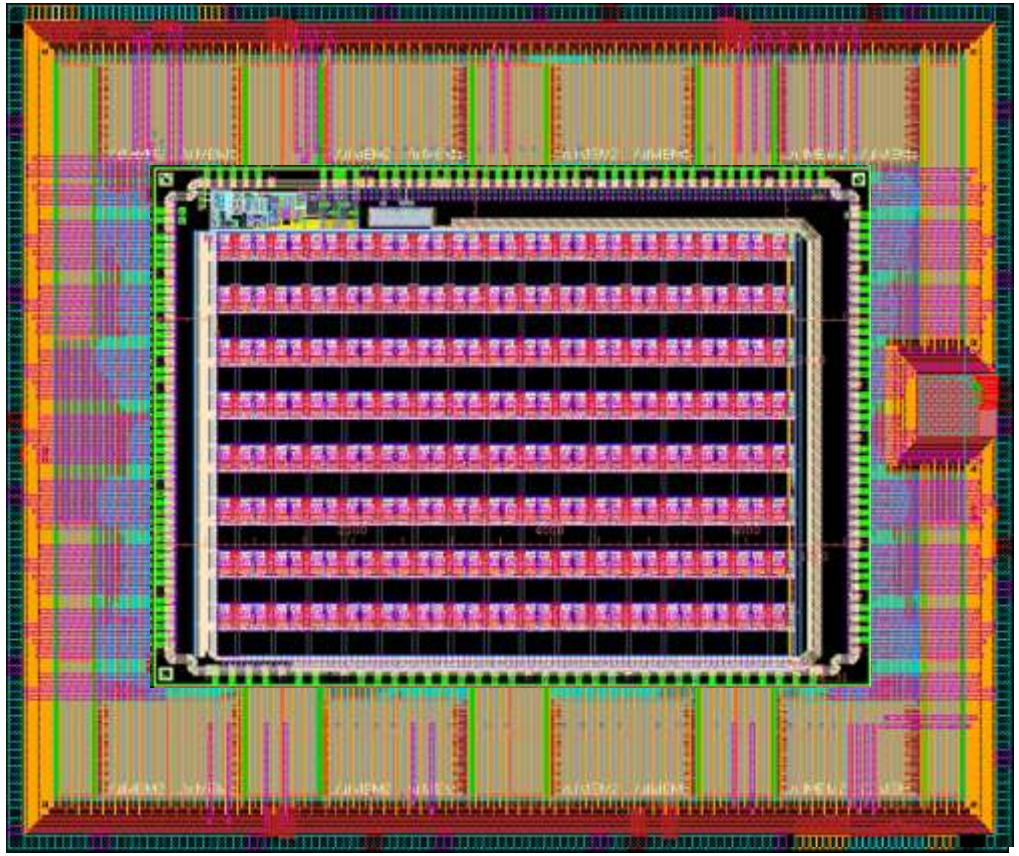


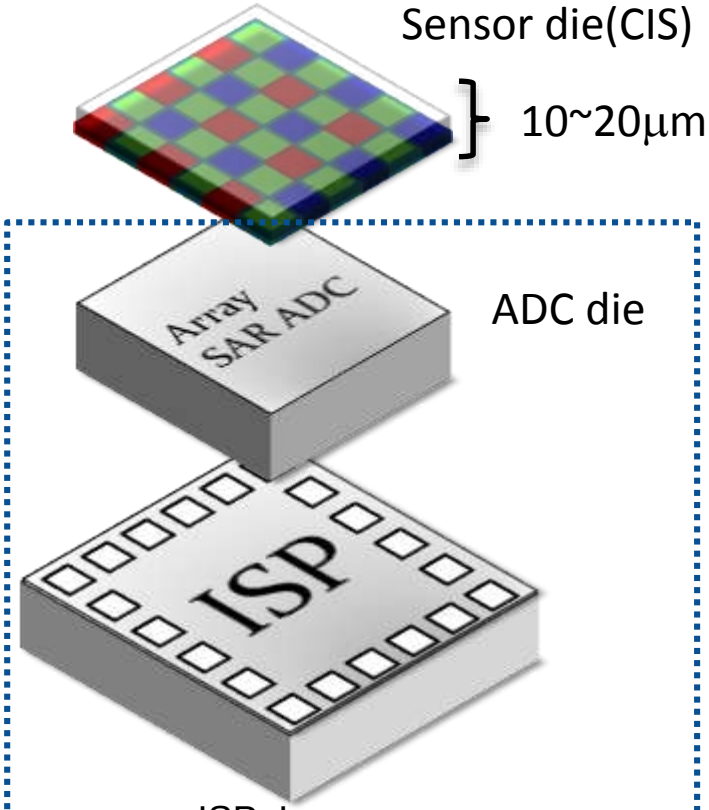
Bechmark-3D_TxRx(2/2)

	tier0	tier1	tier2
PDN Design			
Power Map			

Bechmark-3D_SAP(1/2)

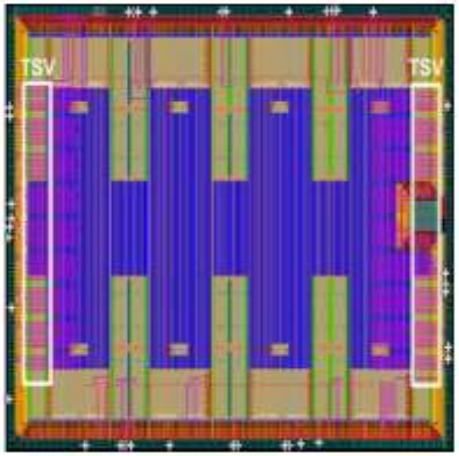
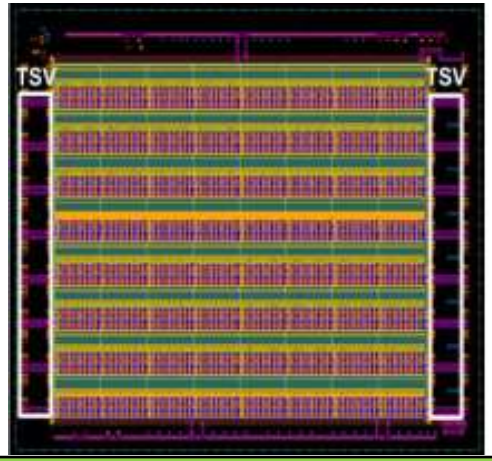
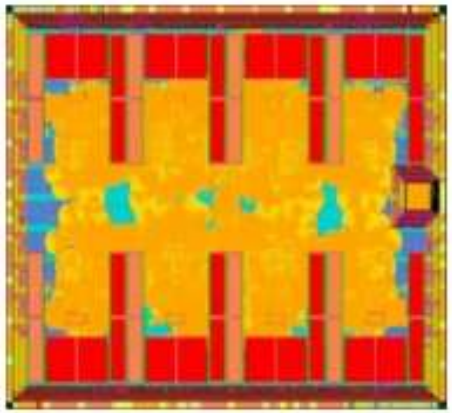
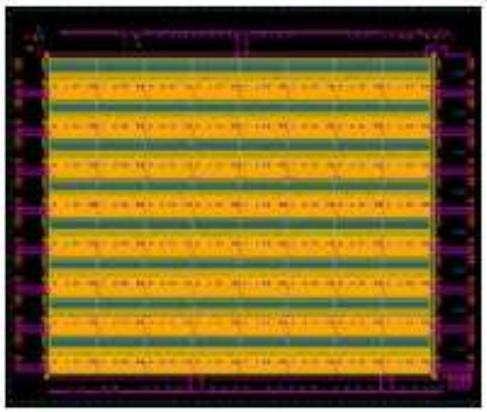
Pixel : 2048x1536, clock >100MHz



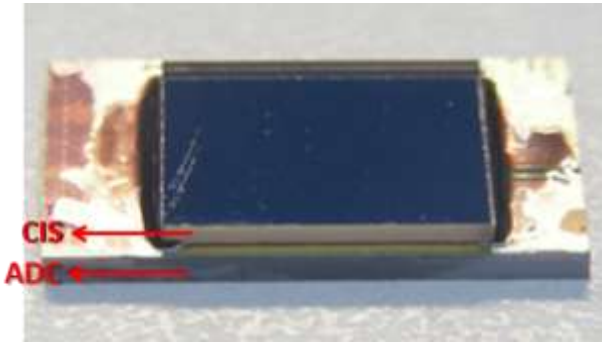


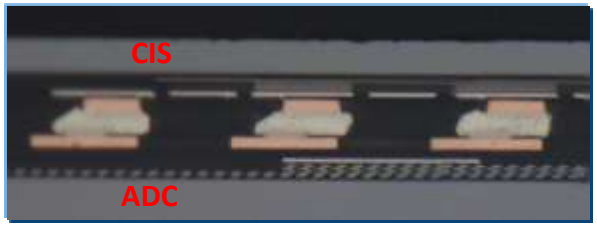
Benchmark-3D_SAP

Bechmark-3D_SAP(2/2)

tier0	tier1
PDN Design	
	
Power Map	
	

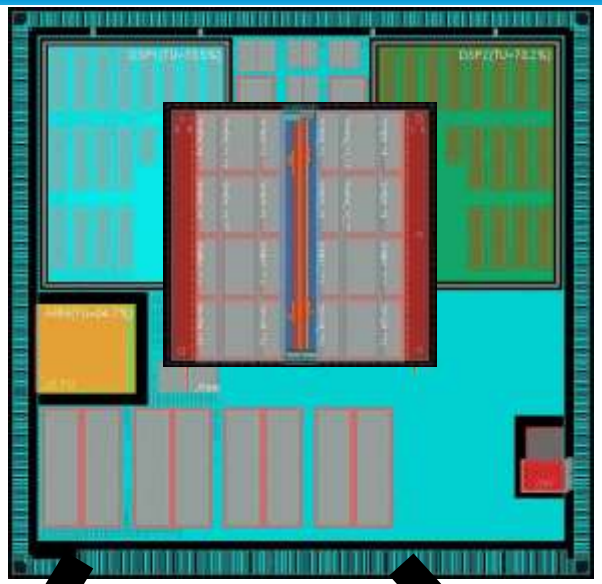
Die Photo





Bechmark-3D PAC(1/2)

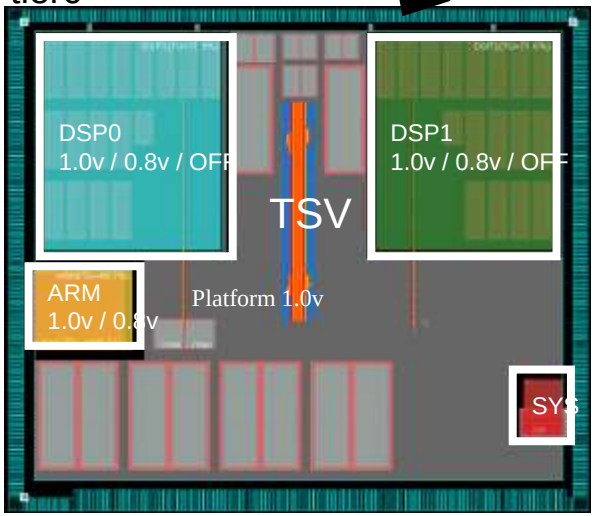
3D-stacked



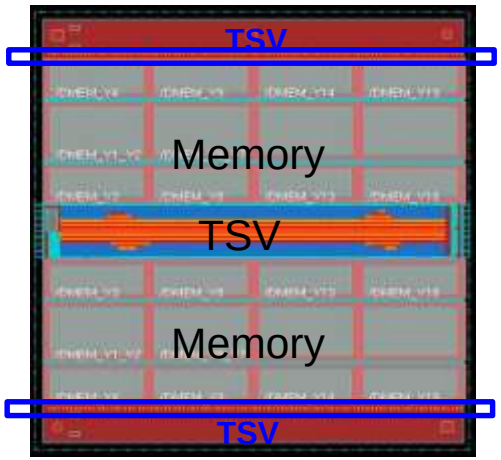
5umTSV,
Backside ViaLast

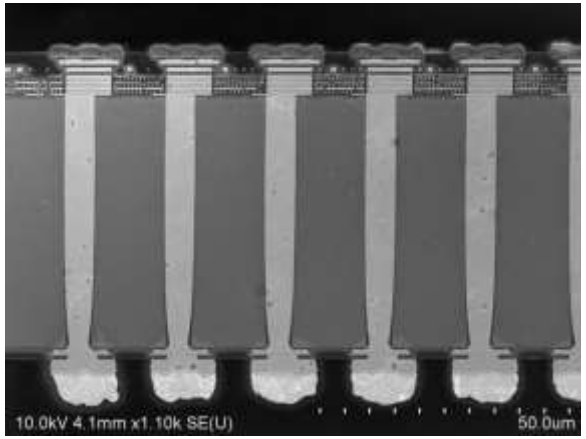
Design Specification	
Process	TSMC 90nm-G, 1P9M
Operating Frequency	150MHz AHB 300MHz PACDSP / AXI / ARM 600MHz DDR2
Operating Voltage	Internal core: 0.8V & 1.0V IO: 3.3V

tier0

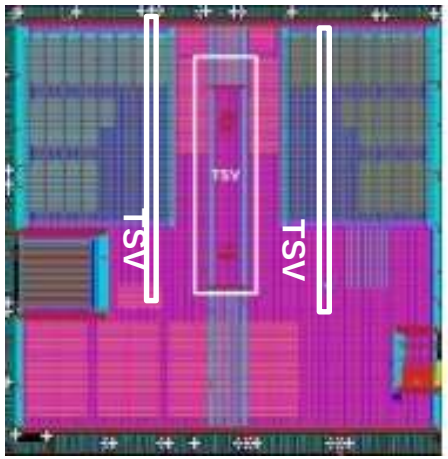
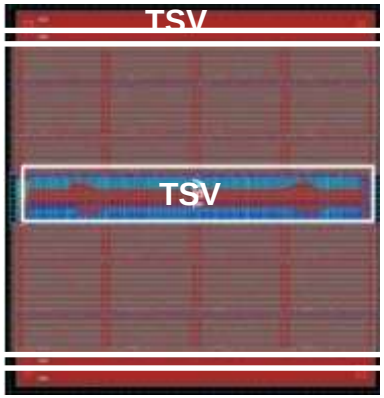
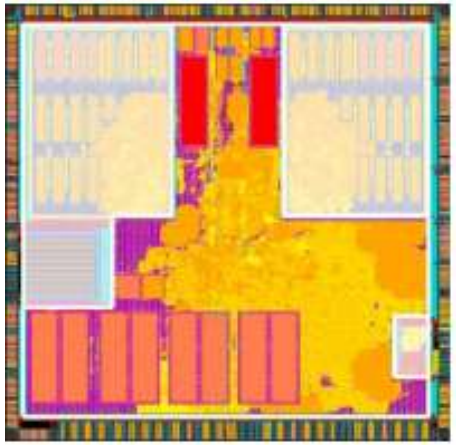
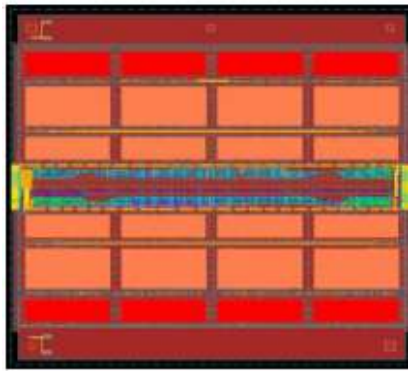


tier1

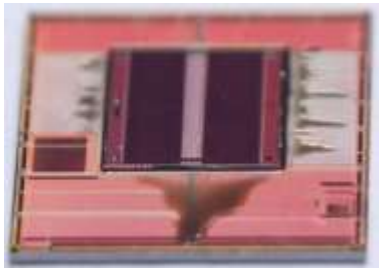


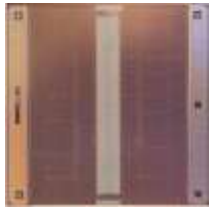


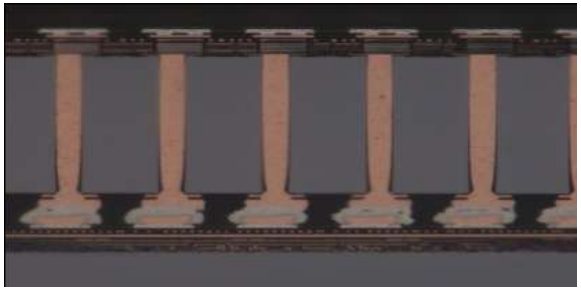
Bechmark-3D PAC(2/2)

tier0	tier1
PDN Design	
	
Power Map	
	

Die Photo







PDN Netlist Structure

Instance description

*|I (node_name instance_name p/g_mesh_name X Y)

R/RC netlist

R<number> <node1> <node2> value
C<number> <node1> <node2> value

DC/AC Current Loading

IVSS<number> 0 <node> value
IVDD<number> <node> 0 value

TSV Modeling

Rtsv<number> <node1> <node2> value
Ctsv<number> <node1> <node2> value

Power Source

V<number> <node> 0 value

Operation command

.op
.trans step_time stop_time
.print node1 node2…..

Example for DC analysis

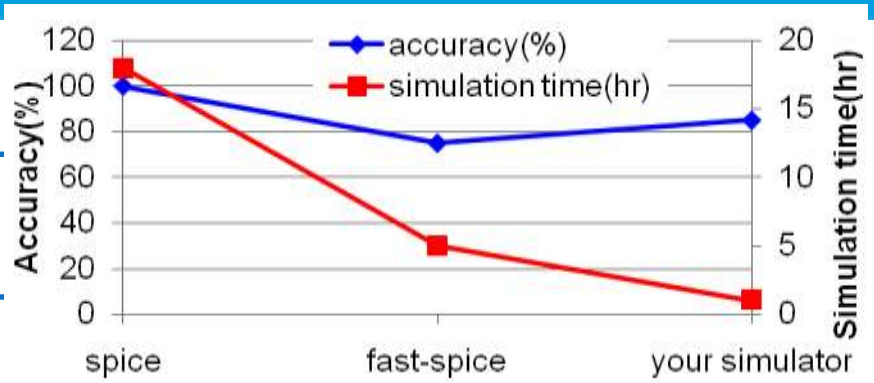
```
*|I (node_name  instance_name  p/g_mesh_name  X  Y)
*parasitic R for VSS/VDD
R<number>       <node1>       <node2>          value
*current source for VSS/VDD
IVSS<number>    0             <node>           value
IVDD<number>    <node>        0                value
*TSV parasitic R
Rtsv<number>    <node1>       <node2>          value
*voltage source
V<number>       <node>        0                value
*simulation command
.op
.print    <all_node>
.end
```

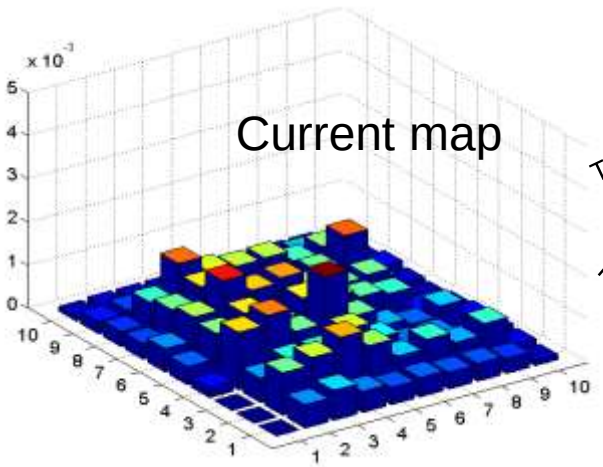
Example for dynamic analysis

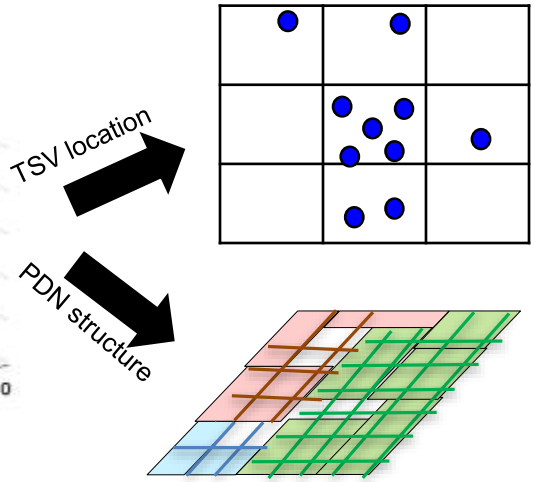
```
*|I (node_name  instance_name  p/g_mesh_name  X  Y)
*parasitic RC for VSS/VDD
R<number>       <node1>       <node2>          value
C<number>       <node1>       <node2>          value
*current source for VSS/VDD
IVSS<number>    0             <node>
                PWL  t1  value1  t2  v2  .....
IVDD<number>    <node>        0
                PWL  t1  value1  t2  v2  .....
*TSV parasitic RC
Rtsv<number>    <node1>       <node2>          value
Ctsv<number>    <node1>       <node2>          value
*voltage source
V<number>       <node>        0                value
*simulation command
.op
.trans step_time  stop_time
.print node1 node2.....
.end
```

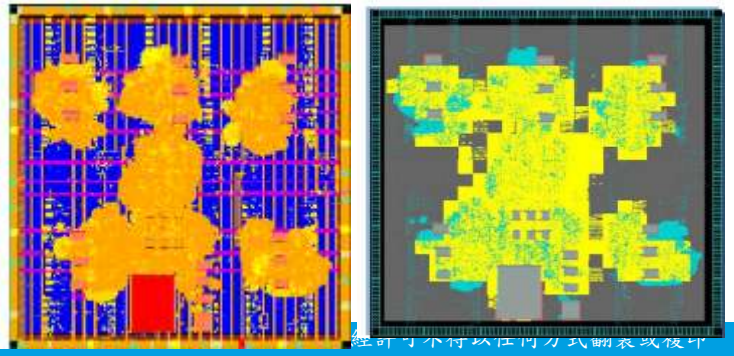
How to use these Benchmarks

- Simulator Test
- P/G TSV Location Investigation
- PDN Structure determination
- Decap Insertion









Delivery Website

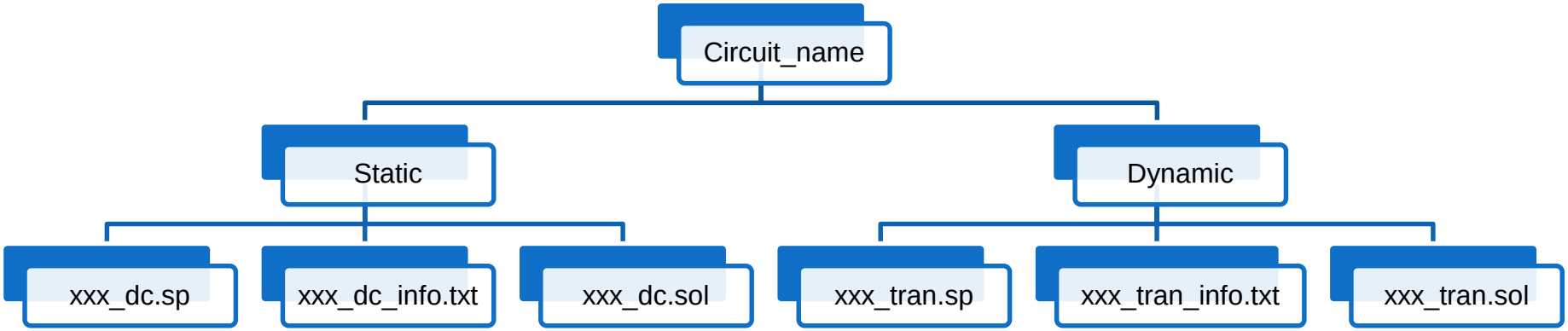
In Google, key word: *3D PDN Benchmark*

Website: http://web.mst.edu/~yshi/3D-PDN.html

Benchmark database

Table I. Benchark information

Benchmark Name			3D-μP	3D-μPD	3D-TxRx	3D-SAP	3D-PAC
Chip Information	VDD (V)		1.8	1.8	1.8	1.8	1.0
	VSS (V)		0.0	0.0	0.0	0.0	0.0
	Tier #		2	2	3	2	2
	P/G TSV #		8	8	16	268	2,234
	Tier-0 die area (μm²)		4,832 × 4,832	4,832 × 4,832	1,900 × 1,950	9,000 × 7,000	7,880 × 7,880
	Tier-1 die area (μm²)		4,832 × 4,832	4,832 × 4,832	1,900 × 1,950	7,280 × 5,390	3,880 × 3,880
	Tier-2 die area (μm²)		--	--	1,900 × 1,950	--	--
	Instance #		125,338	551,889	110,657	1,032,275	2,044,743
	Pad #		304	304	232	412	500
PDN Information	General	Metal layers #	7	7	7	7	10
		Current source #	239,530	239,530	218,066	2,902,474	3,364,314
		Voltage source #	28	28	16	36	51
	DC only	Node #	826,524	1,021,185	244,651	4,588,540	8,983,606
		Resistor #	913,154	1,178,081	312,251	7,638,905	13,234,026
	Transient only	Node #	826,542	1,021,203	244,683	4,589,076	8,988,071
		Resistor #	913,170	1,178,097	312,283	7,639,42	13,238,494
		Capacitor #	762,239	967,057	235,189	4,147,603	6,068,910
	Current source step #		200	140	140	160	100
	Max (mV)		61	44	19	58	36



Conclusion

- In this paper, we put forward a set of PDN benchmarks that are extracted from industrial 3D designs.
- These designs are carefully selected such that they cover a wide range of functionality, size, and TSV number.
- We hope that the released benchmarks can facilitate and promote the research in 3D PDNs.

Thank you