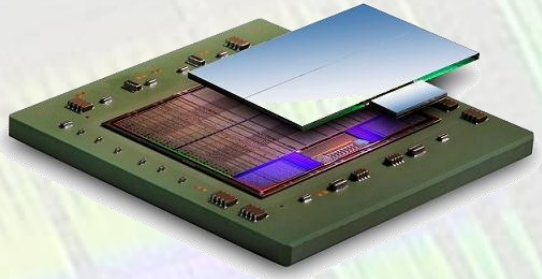
XILINX

ALL PROGRAMMABLE™

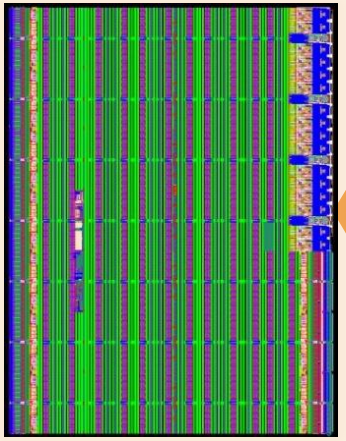
Heterogeneous 3-D stacking, can we have the best of both (technology) worlds



Liam Madden
Corporate Vice President
March 25th, 2013

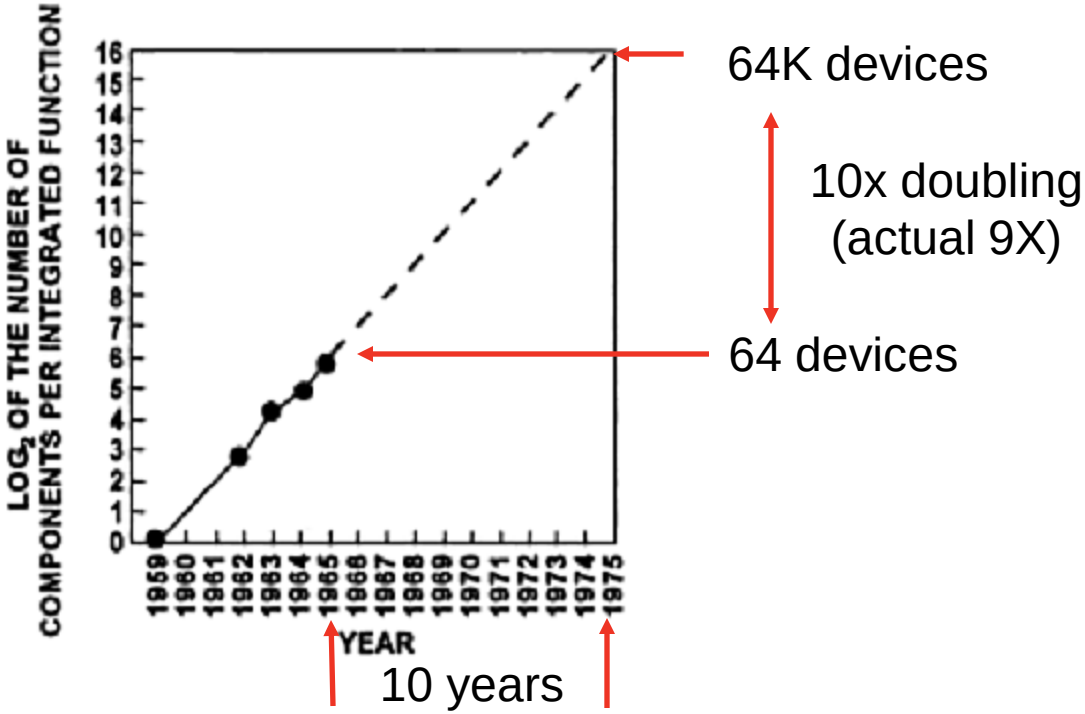
The ‘Chameleon’ Chip

Field Programmable Gate Array (FPGA)



Moore's Law

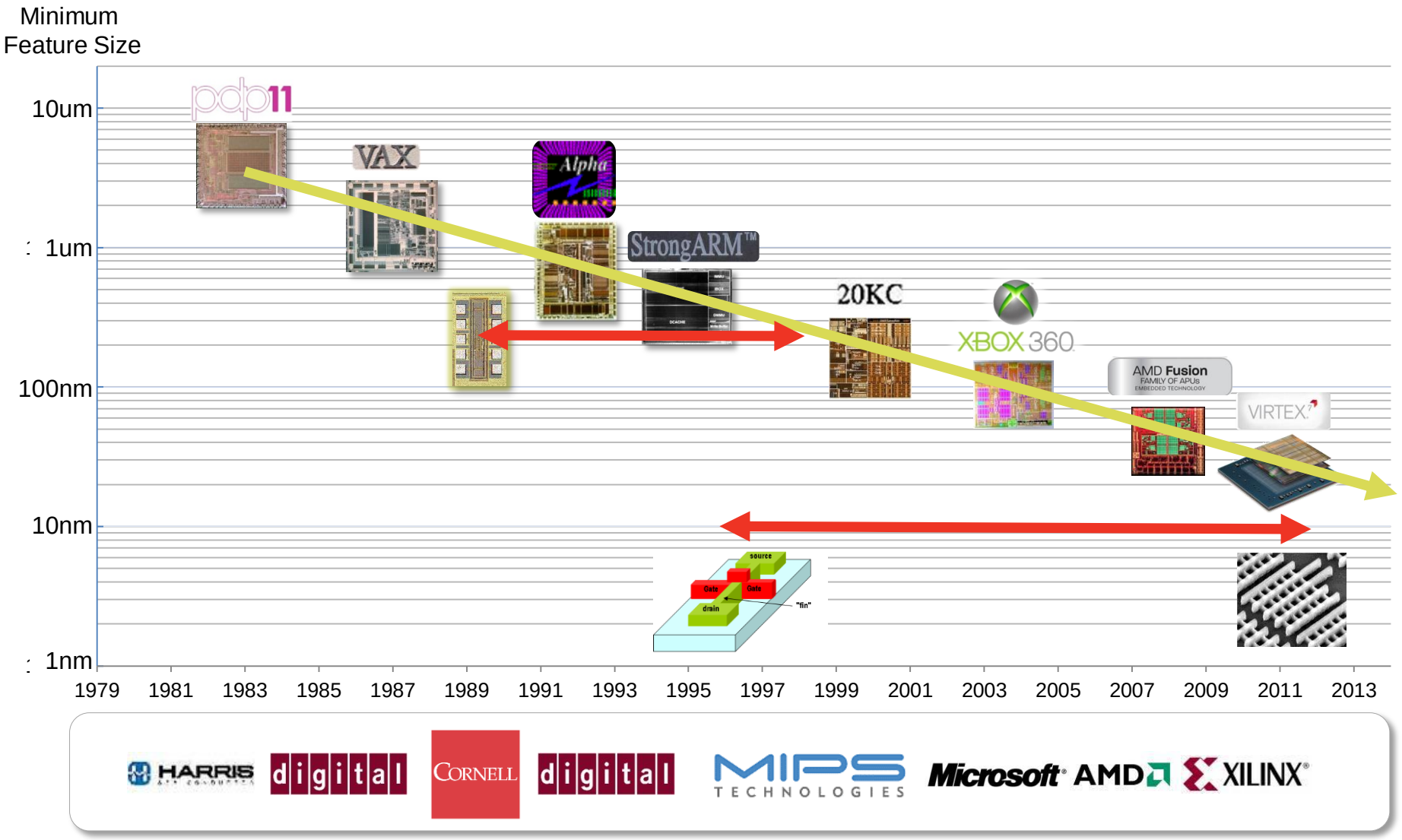
- 1965: Transistor density doubles every year



- Revised 1975: Transistor density doubles every two years

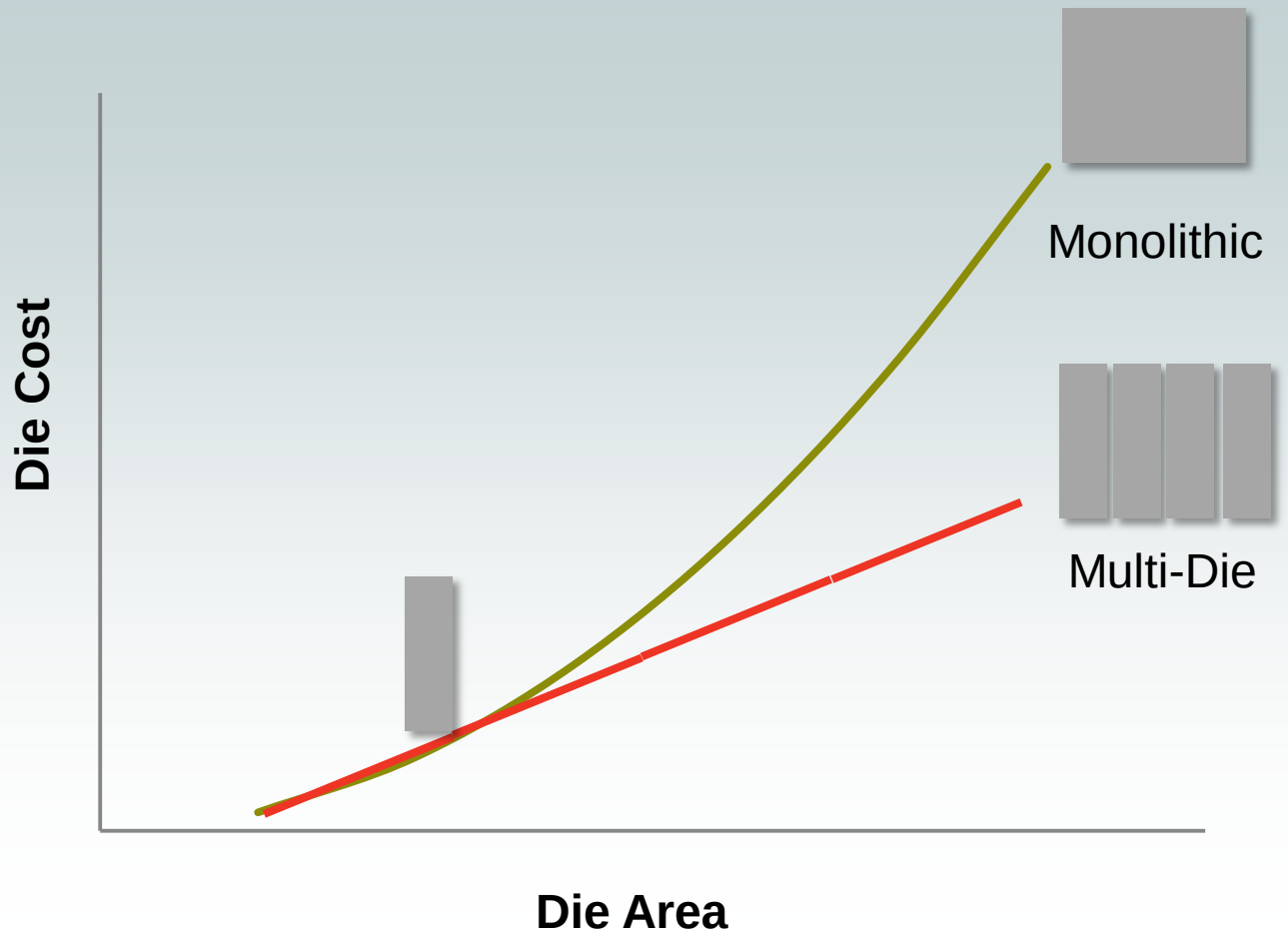
"Cramming more components onto integrated circuits" Gordon Moore, Electronics, Volume 38, Number 8, April 19th 1965

A Career in One Graph

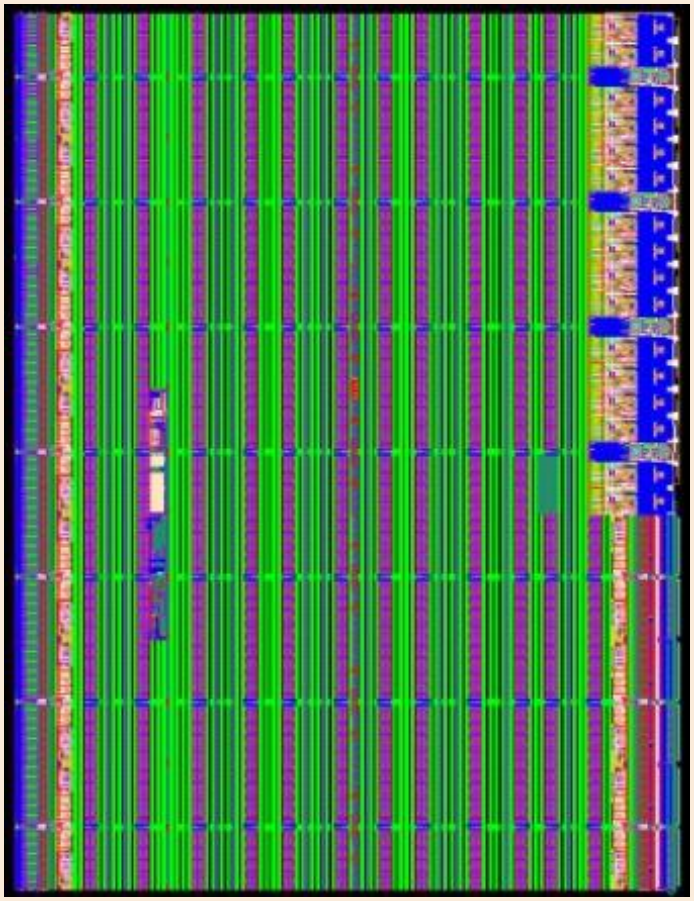


Cost Comparison: Monolithic vs Multi-Die

"Moore's Law is really about economics" *– Gordon Moore*

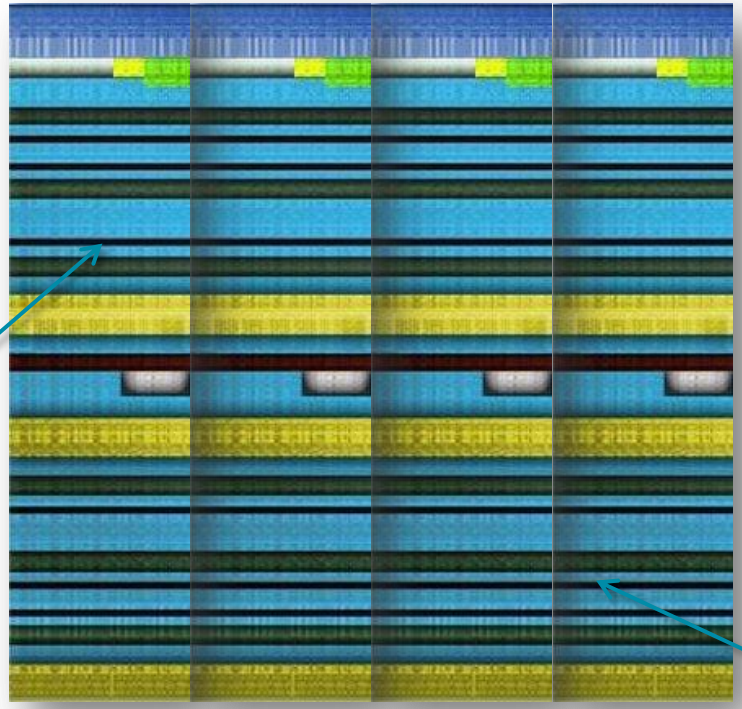


Why is First 3D Logic Product an FPGA?



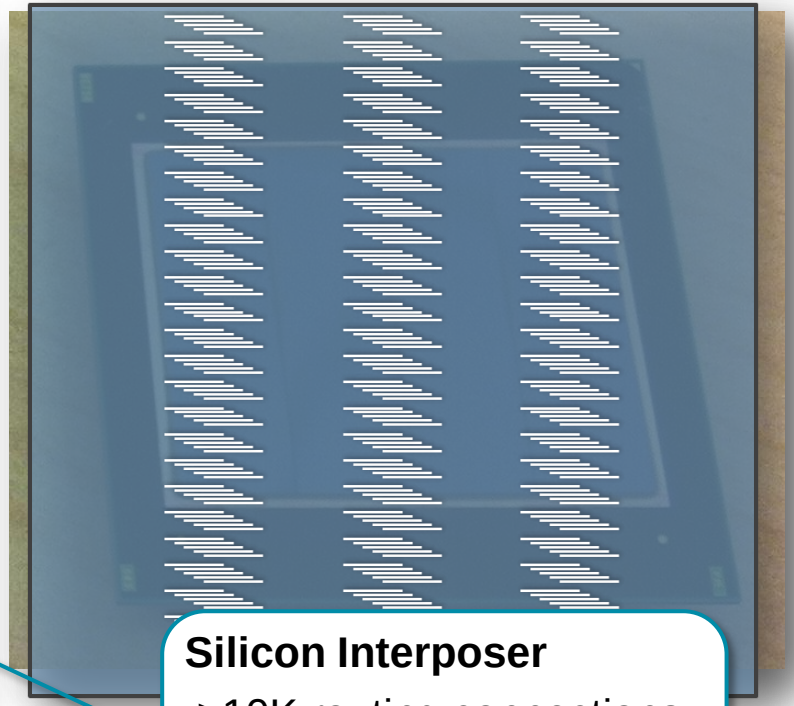
- Natural partition using "long lines"
- Very low "opportunity cost"
- No 3rd party dependence
- "Size matters" to customers
- Compelling value proposition "next generation density in this generation technology"

Virtex 2000T: Homogeneous Stacked Silicon Interconnect Technology (SSIT)



FPGA slice

FPGA Slices Side-by-Side

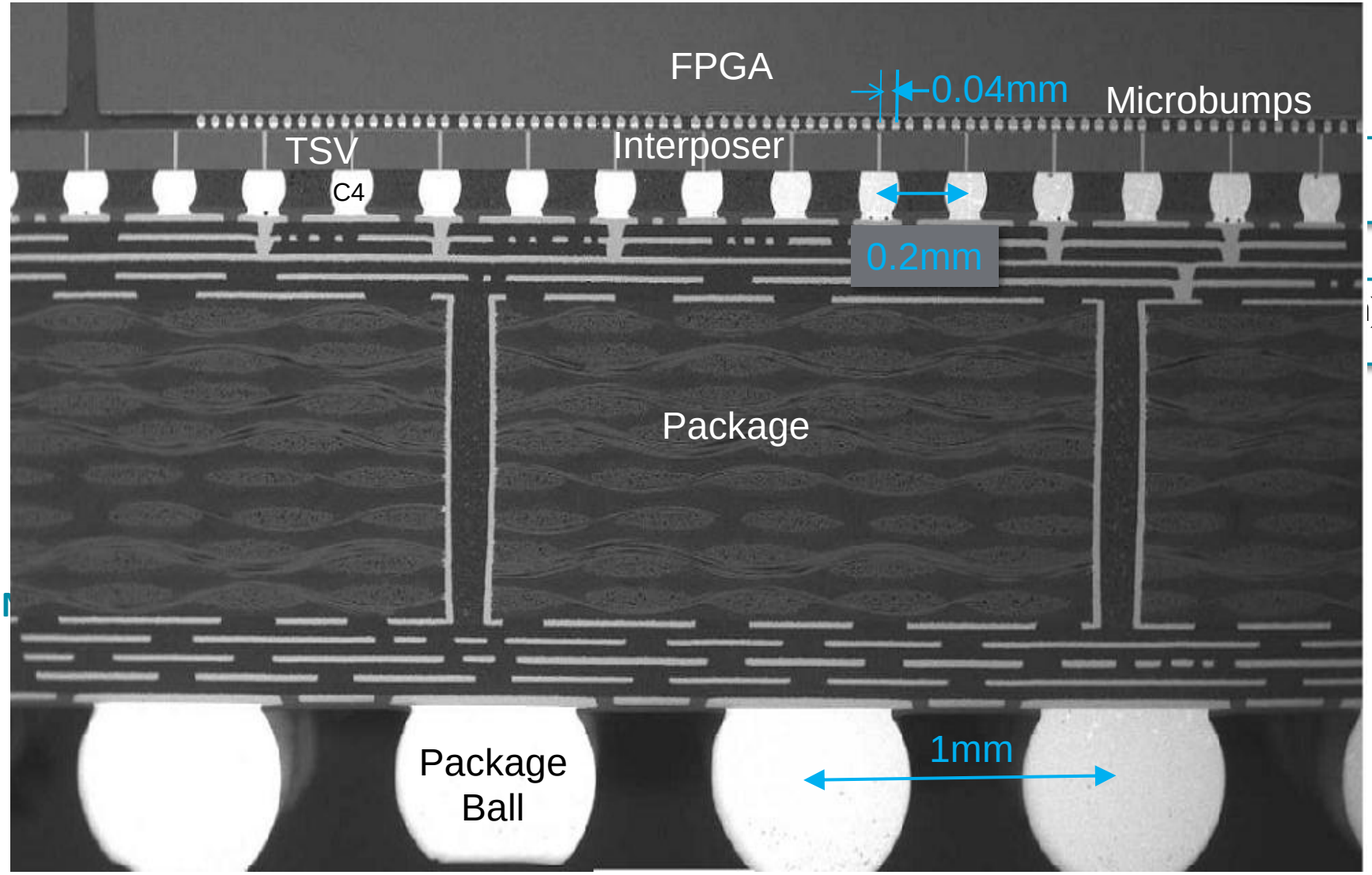


Silicon Interposer

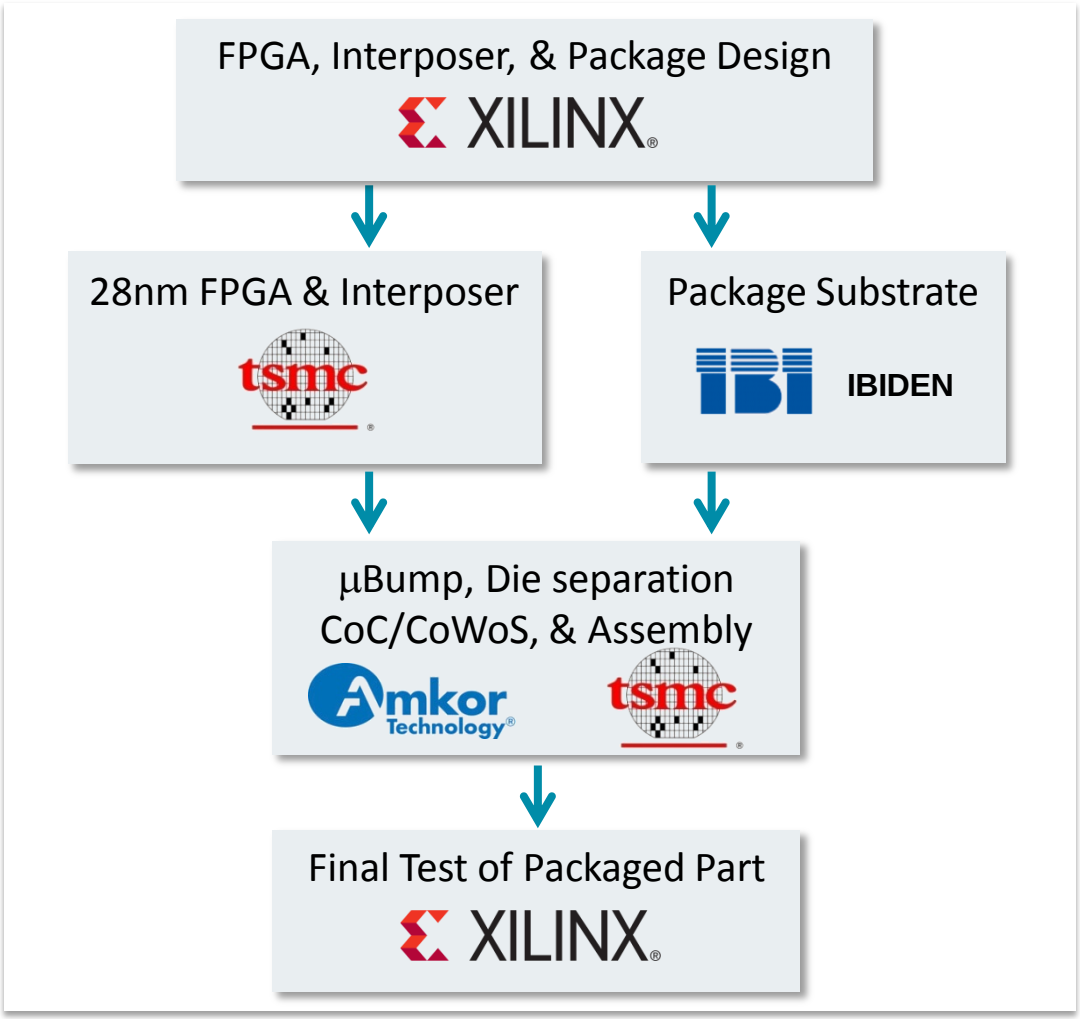
>10K routing connections between slices

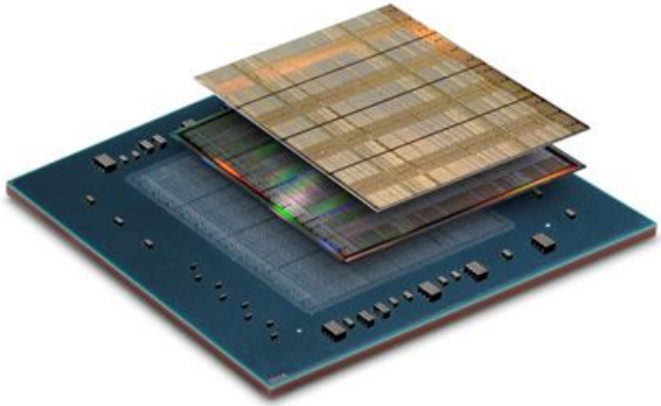
~1ns latency

Elements of SSIT

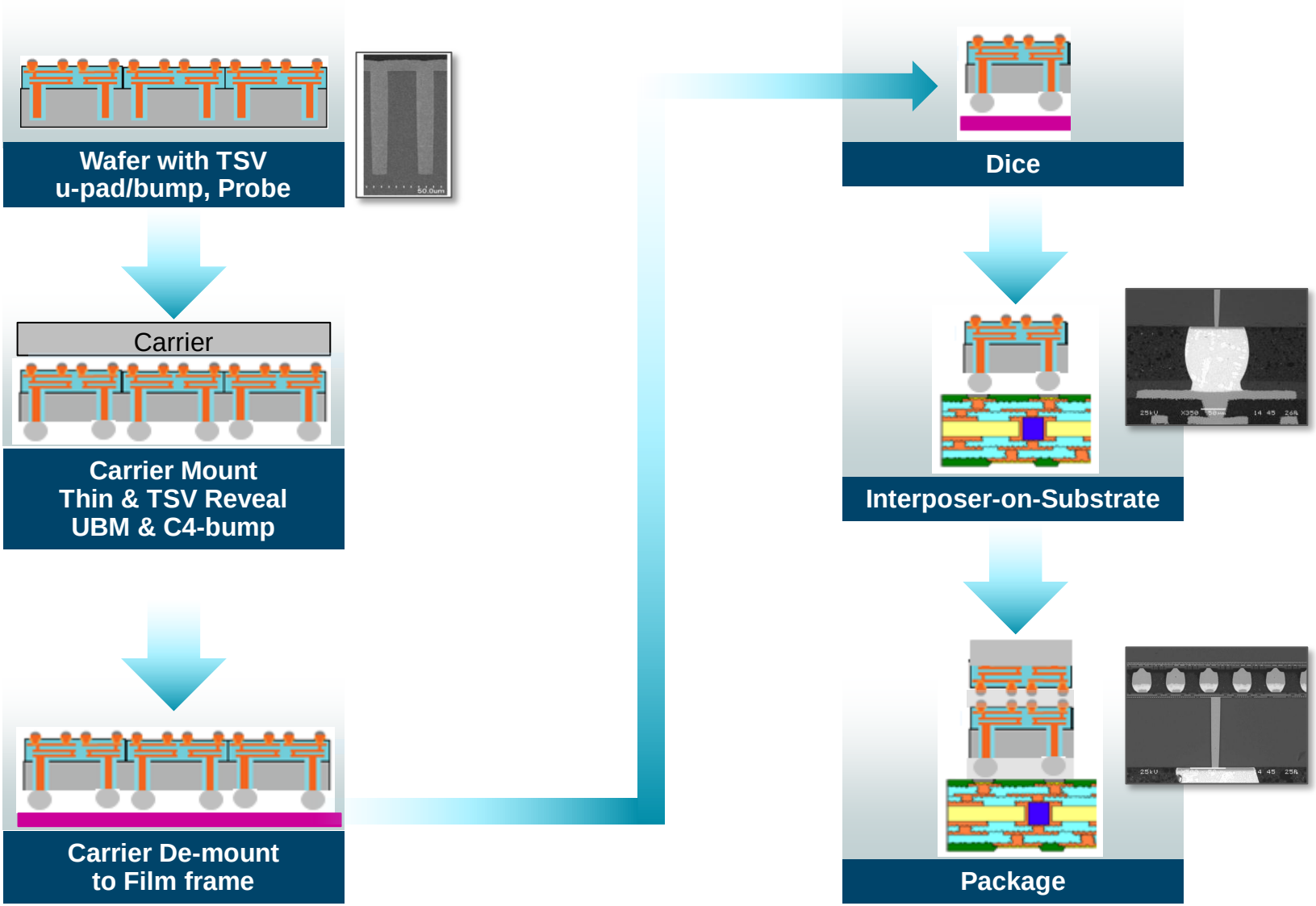


3D Supply Chain

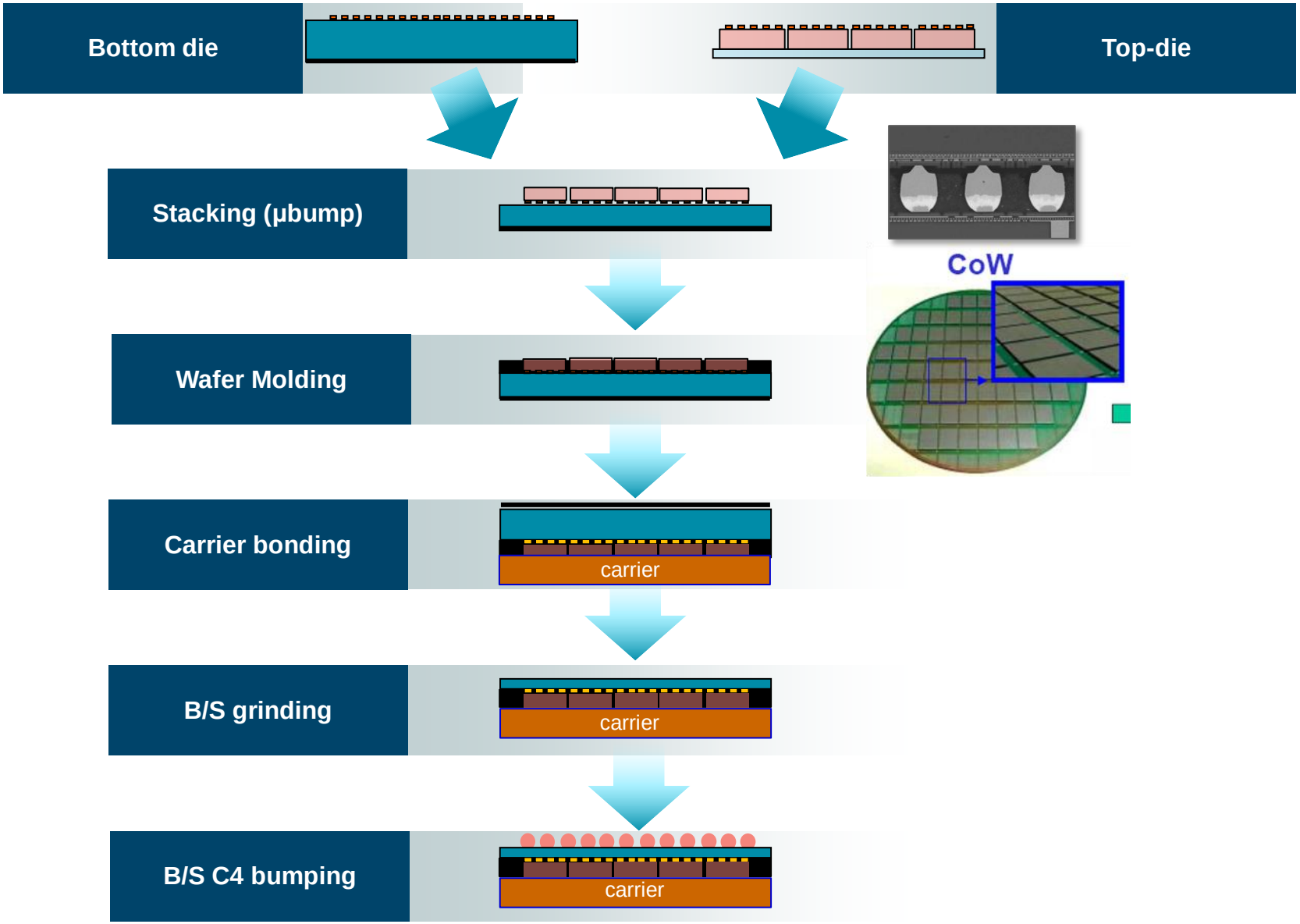




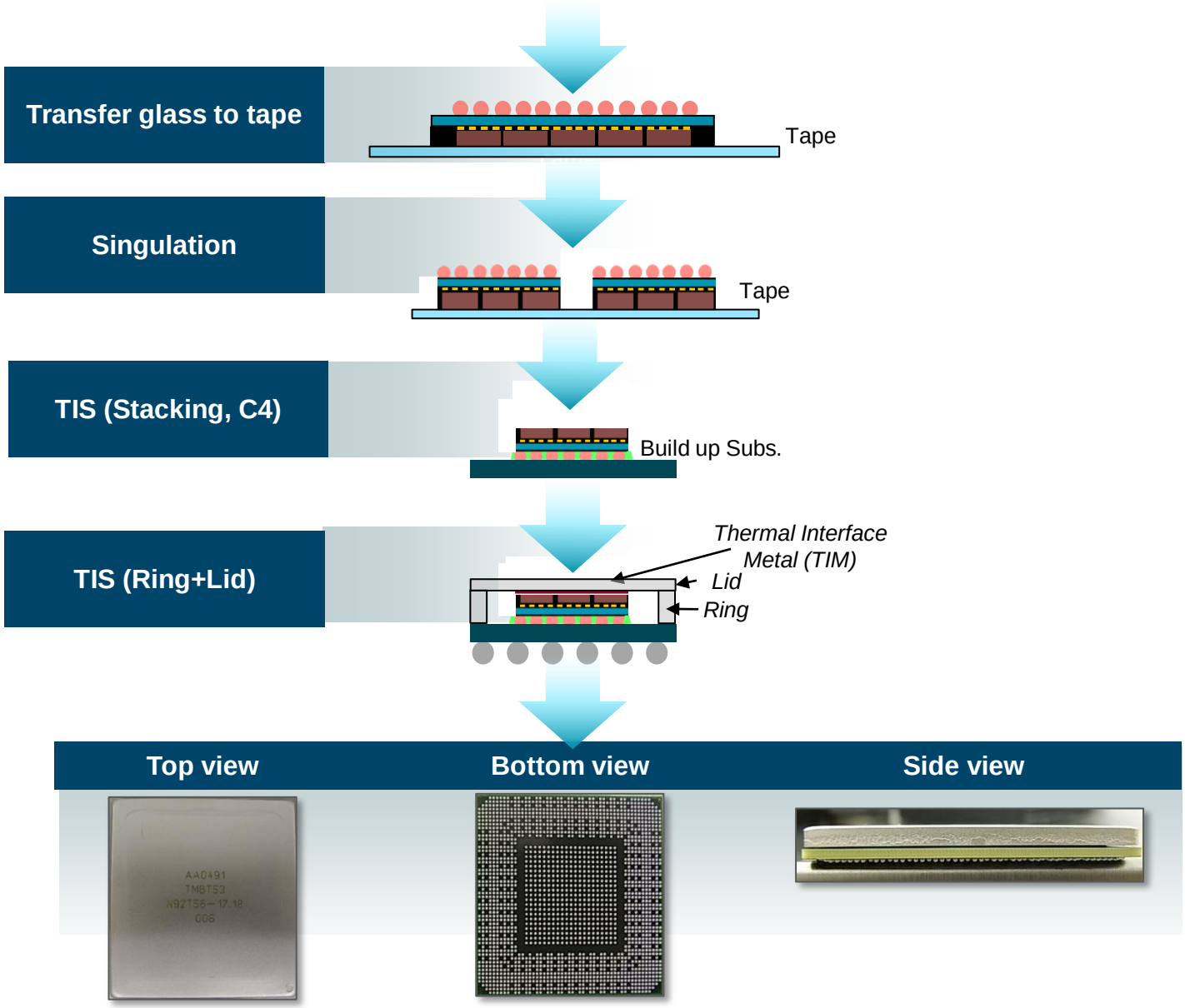
Co(CoS) Process Flow



(CoW)oS Process Flow-1 (Courtesy of TSMC)



(CoW)oS Process Flow-2 (Courtesy of TSMC)



3D Stacking: A world of difference

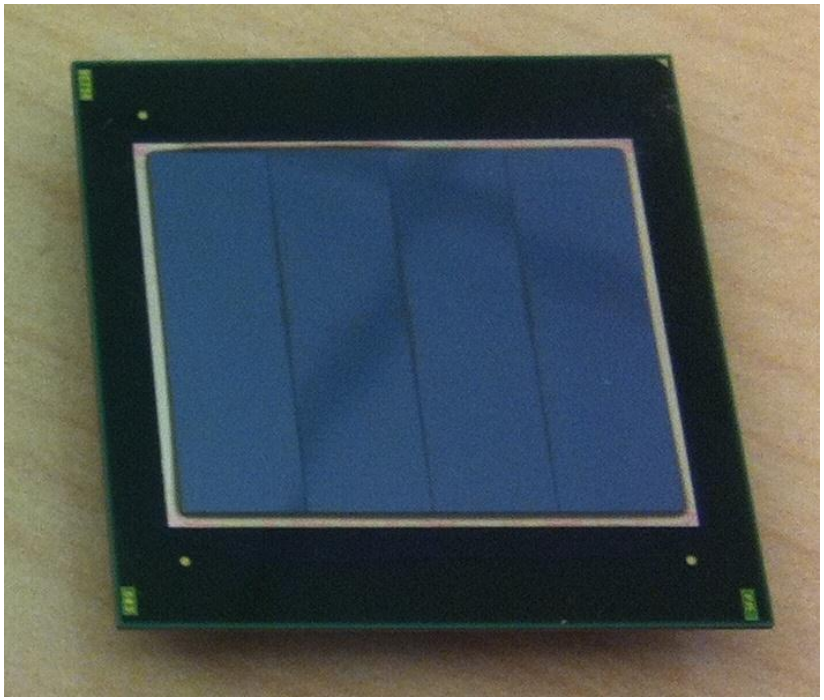
Earth

Area: ~500 Million km²

Population: ~6.8 Billion People

Oceans: 5

Age: ~4.5 Billion Years



Virtex-7 2000T

Interposer Area: ~775 mm²

Population: ~6.8 Billion Transistors

Sub-chips: 5

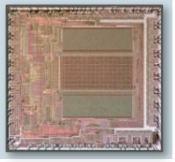
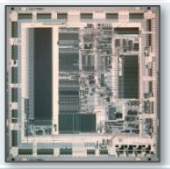
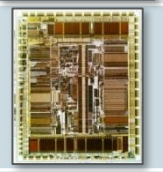
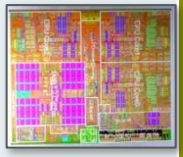
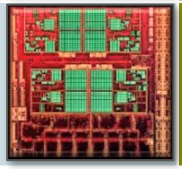
Age: ~45 weeks

Heterogeneous Integration

3 Decades of Microprocessor Integration

A Personal History

"Integrate or be integrated" – *Fred Weber, former CTO AMD*

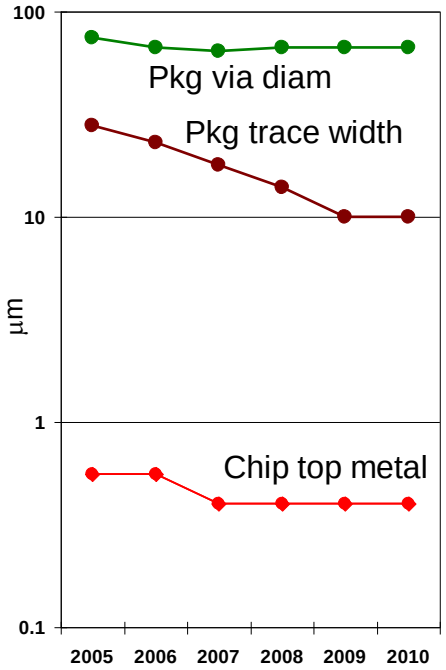
Year	Company	Product		Integration Level						
				Core				L2$	North Bridge	GPU
				DP	Ctl	L1 $	FPU			
1983	Harris	J11	4um 							
1989	DEC	Rigel	1.5um 							
1991	DEC	Alpha	0.75um 							
2005	Microsoft	Xenon	90nm 	3 Core						
2011	AMD	Fusion	40nm 	2 Core						

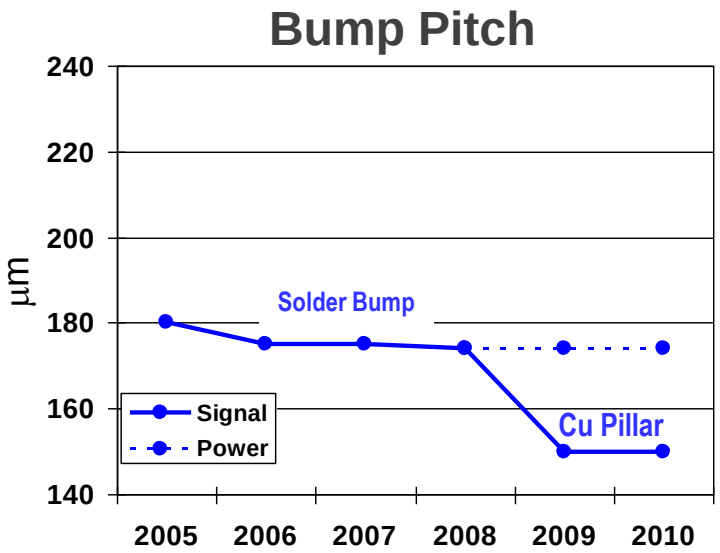
What Happened to System on a Chip?

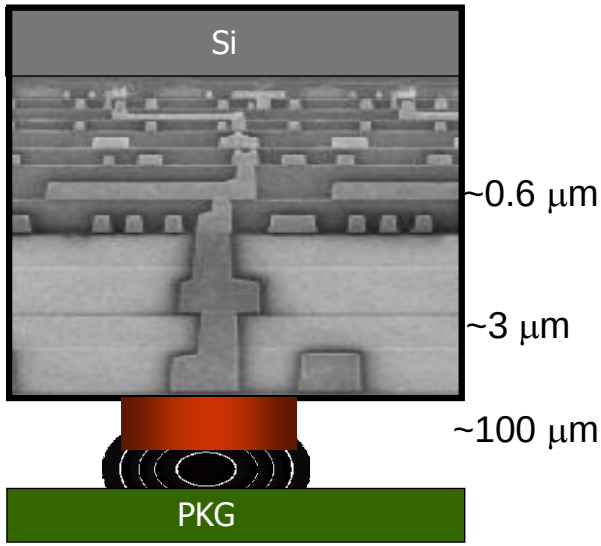
	Logic	Memory	Analog
Global Revenue 2011	$150B	$68B	$45B
Moore Scaling	Good	Good	Poor
Technology “Vintage”	28nm	28nm	180nm?
Transistor Characteristics	High performance/ Low leakage	Low leakage/ moderate performance	Stable with good voltage headroom
Metallization layers	>9	<5	<6
Differentiators	High density logic	Charge storage	Passives, Optical

What's the Problem with Multiple Packages?

- **The packaging chasm**
  - Two orders difference in package trace/width vs silicon metallization
  - I/O also isn't scaling due to bump pitch and chip to chip loading issues
  - Leads to increased area, power and complexity (SERDES)

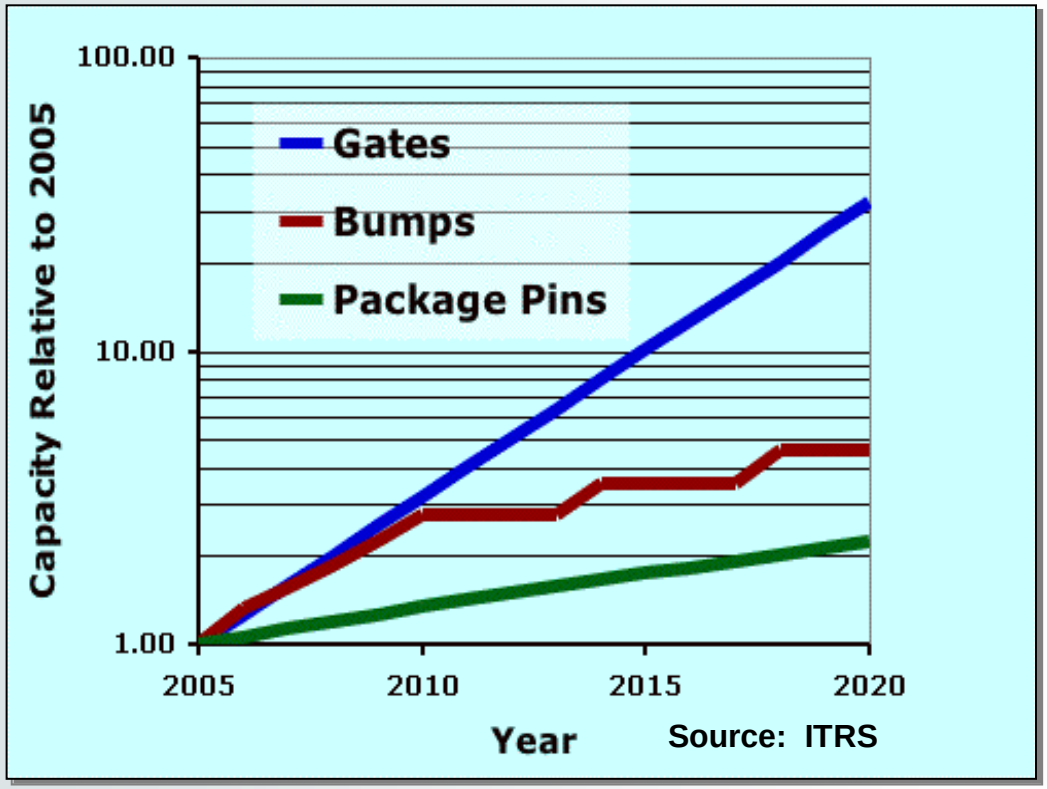






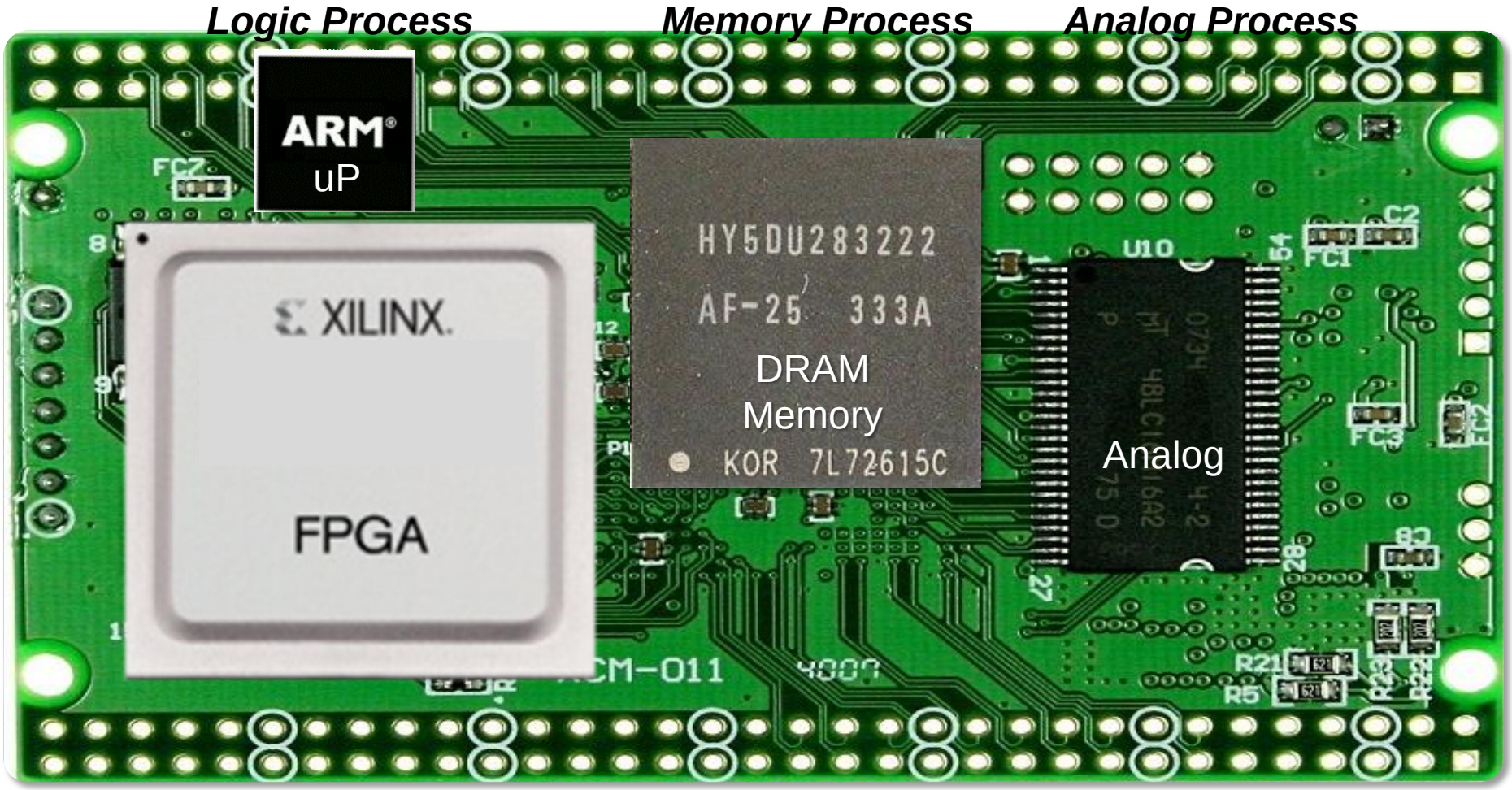
To scale in X dimension

Chip Input/Output Bottleneck



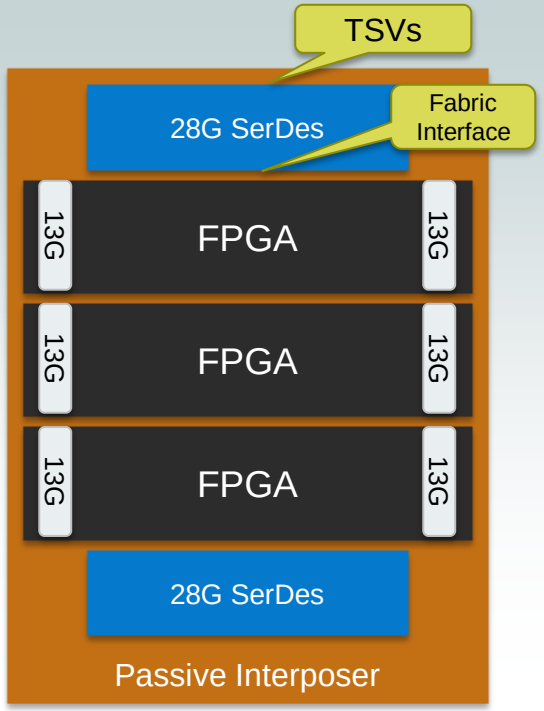
15x drop in I/O-to-logic ratio by 2020

Crossing the Packaging Chasm



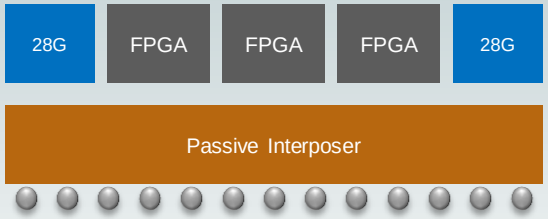
Virtex-7 HT: Heterogeneous SerDes

Top View



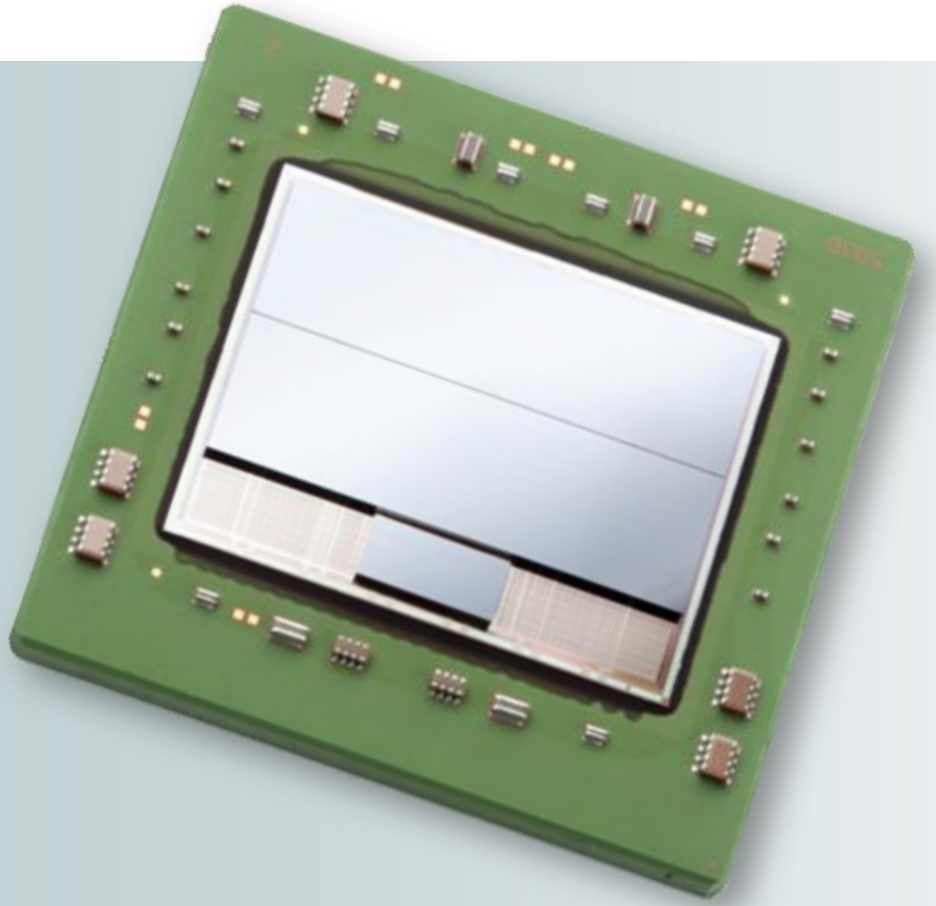
- 2.8Tb/s ~3X Monolithic
- 16 x 28G Transceivers
- 72 x 13G Transceivers
- 650 GPIO

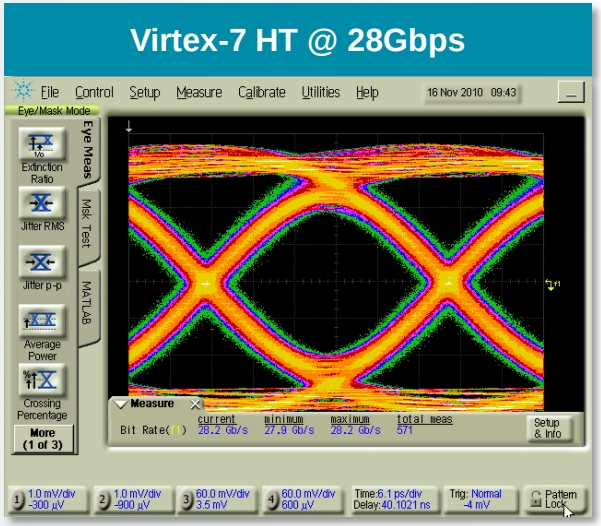
Cross Section



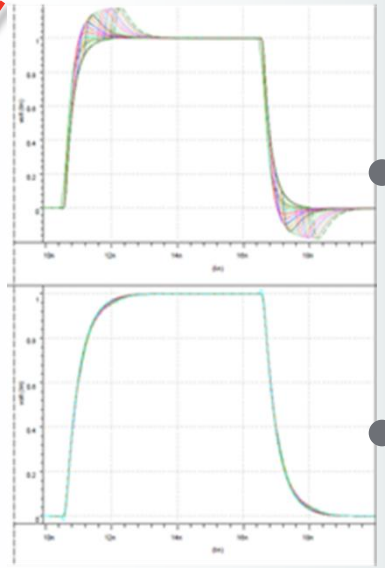
- Yield optimized
- Noise isolation
- 28G process optimized for performance
- FPGA process optimized for power

7V580T – Dual FPGA Slice with 8x28Gb/s SerDes Die



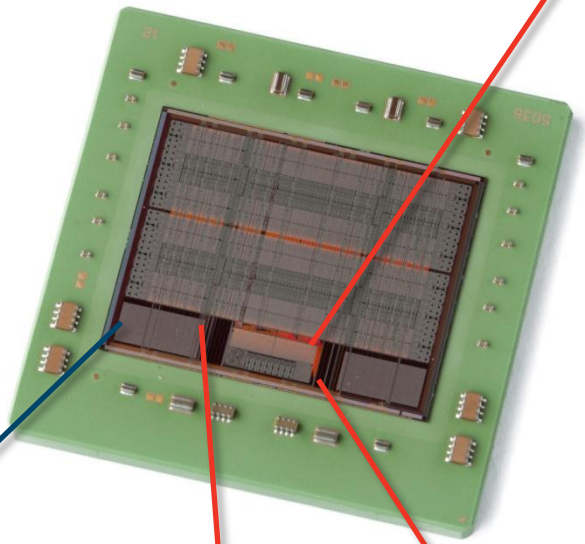


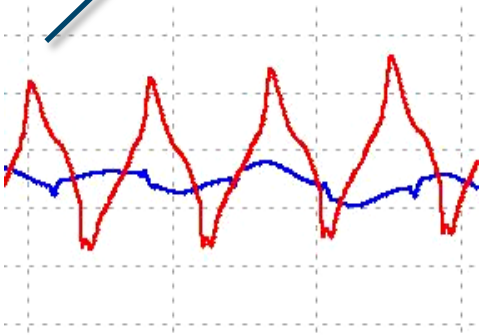
Interposer Routing and DCAP



Wire coupling, no shielding

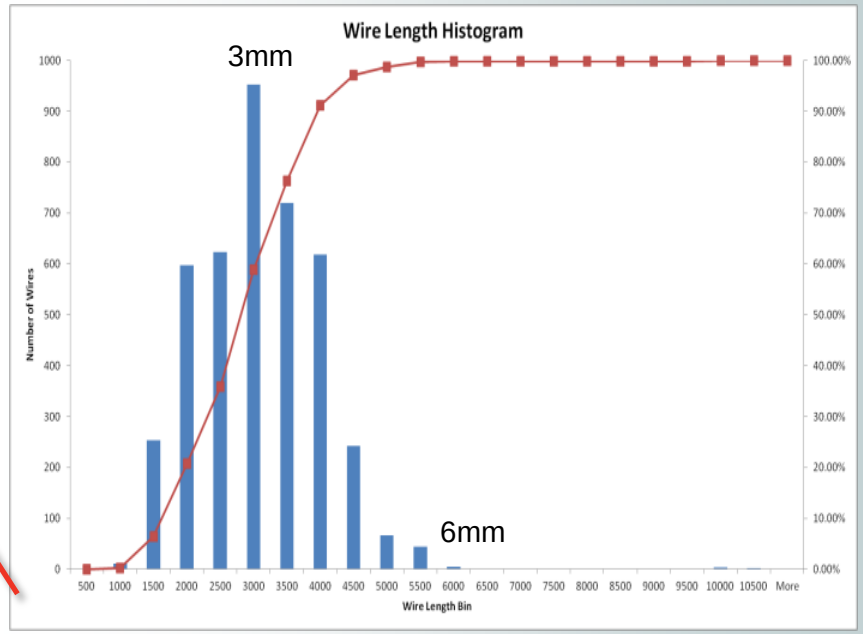
Wire coupling, with shielding



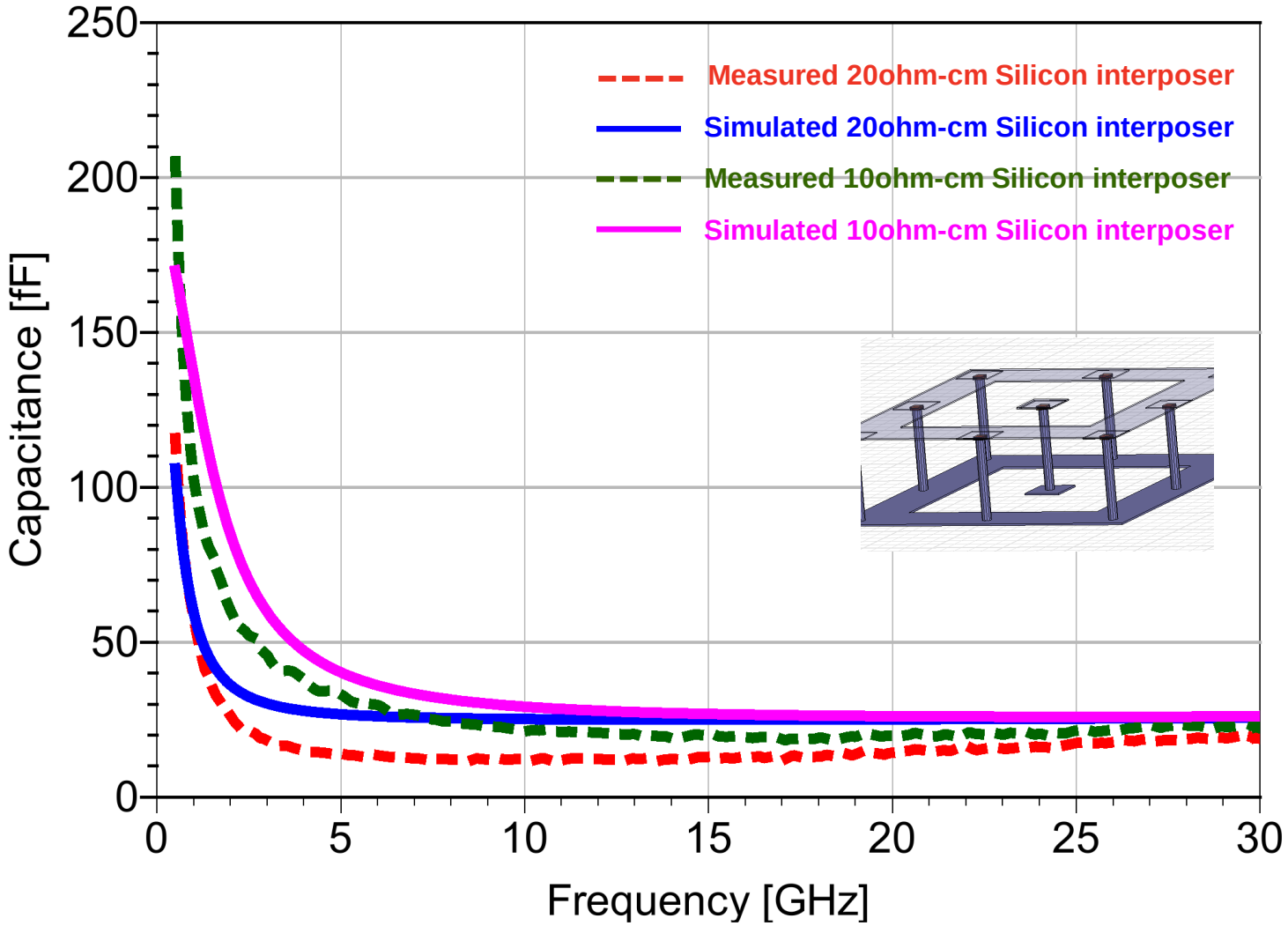


SSN, no DCAP

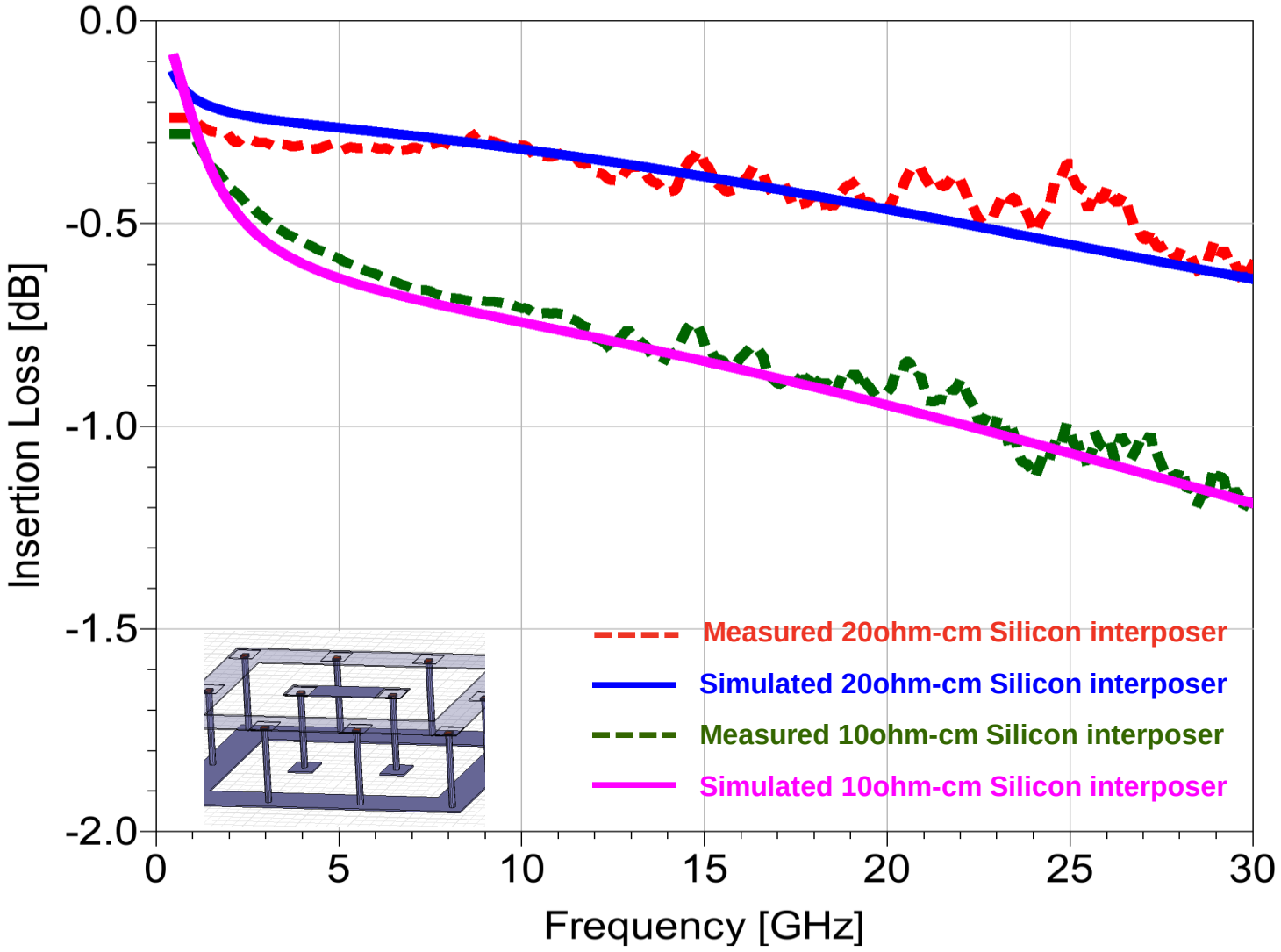
SSN, with DCAP



TSV Capacitance as Function of Substrate Resistivity

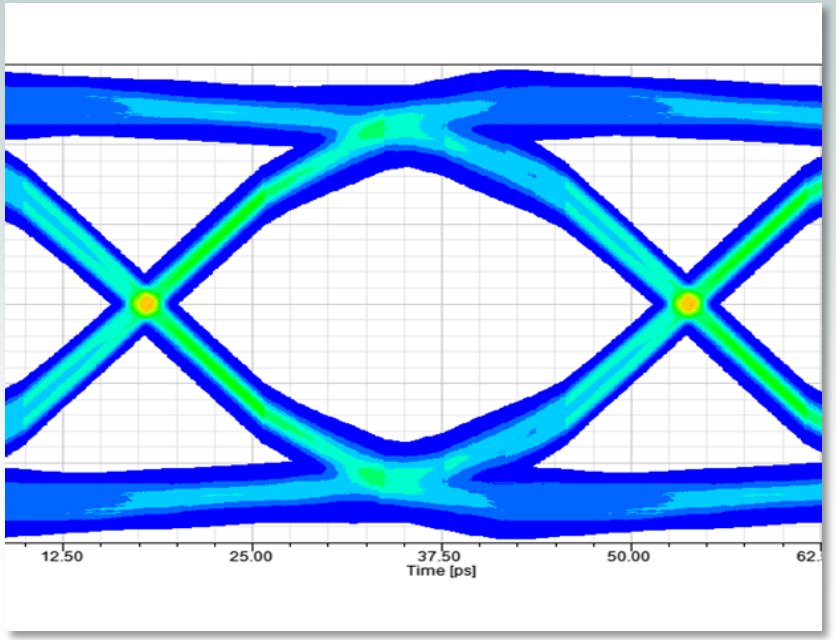


Insertion Loss as a Function of Interposer Resistivity

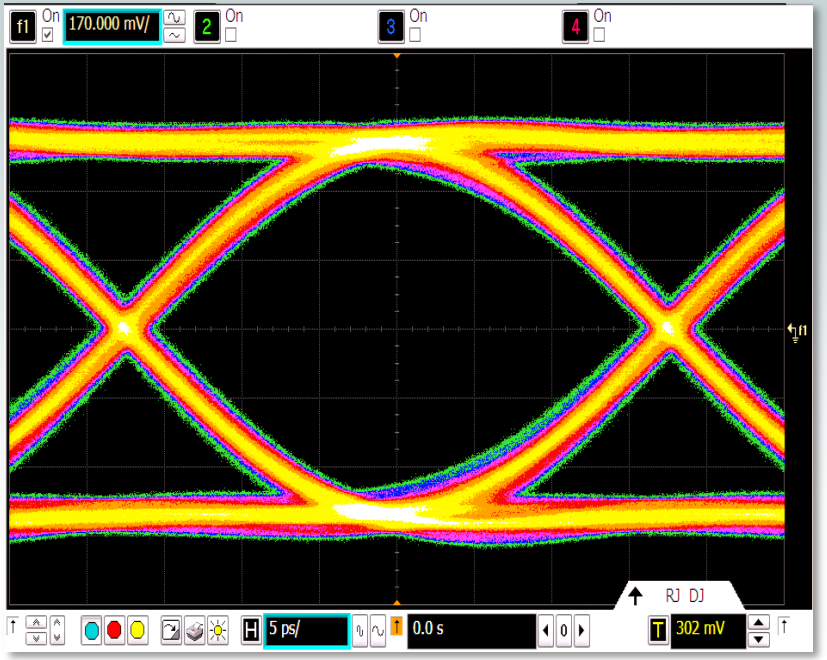


Simulated Eye Diagram and Measured Eye Diagram Comparison @ 28Gb/s

Simulation



Measurement



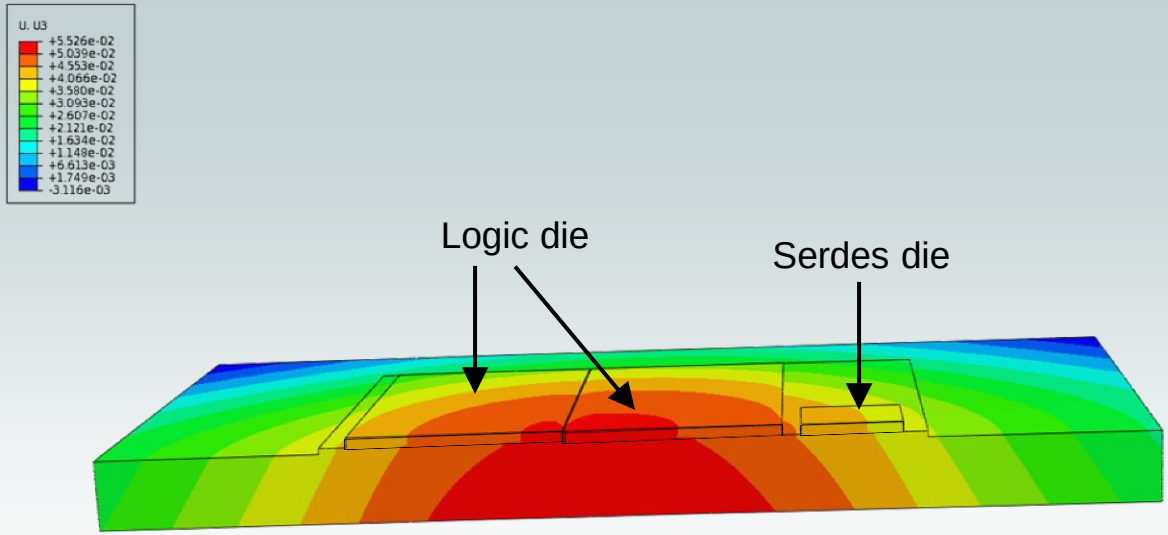
Measured Amplitude: **923mVp-p**

Measured Total Jitter: **6.25 ps @ BER 10E-12.**

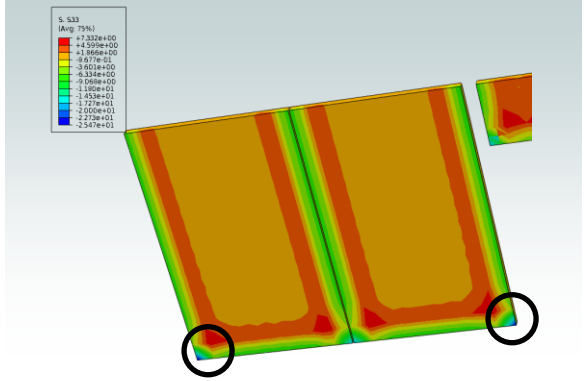
Measured Random Jitter: **230 fs (0.175UI of total jitter)**

3D Thermo-Mechanical Simulations at 25C

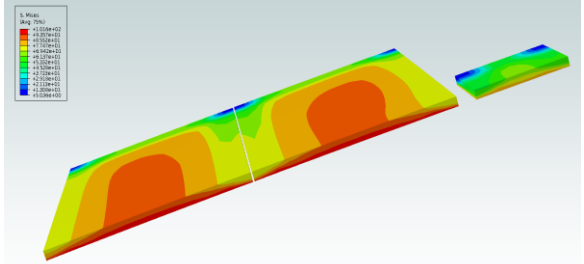
Warpage



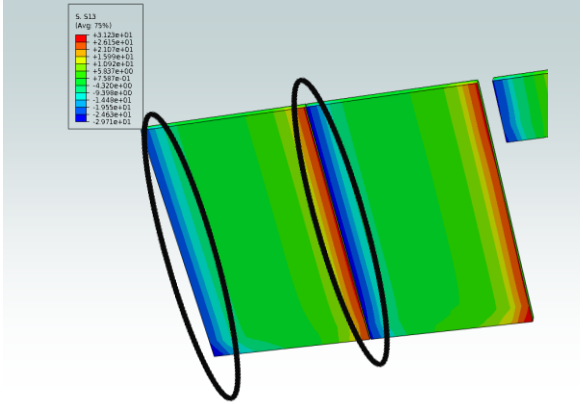
S33 Peel Stress



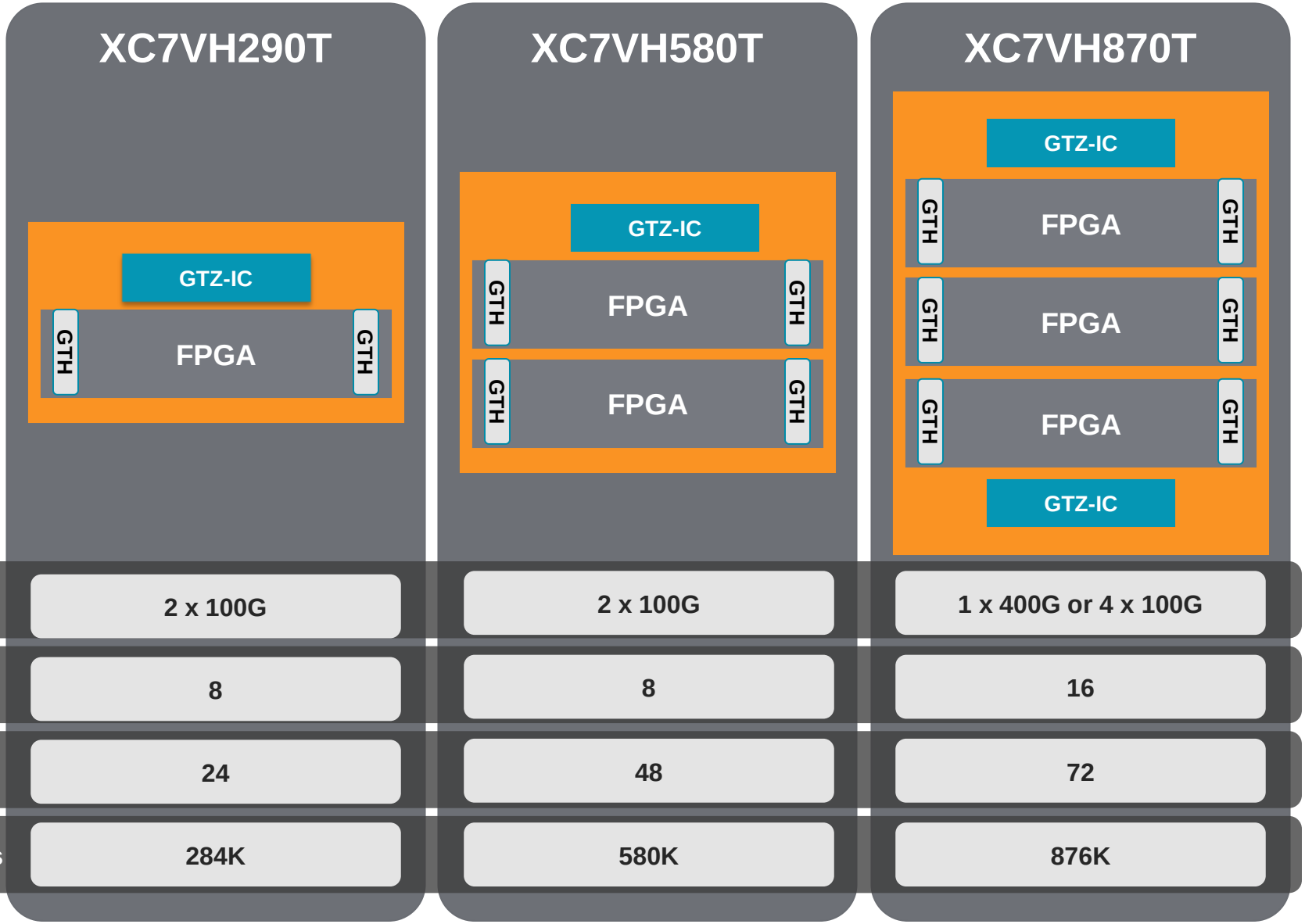
Von Mises Stress



S13 Shear Stress



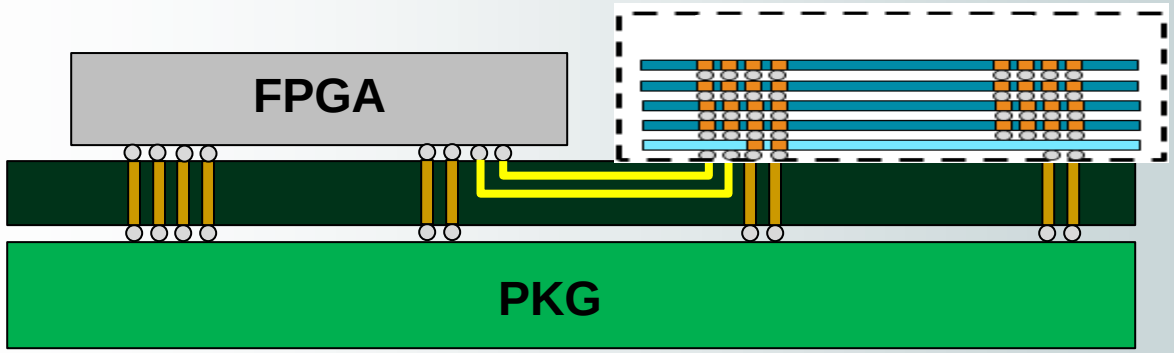
SSIT Enables Scalable FPGAs



	XC7VH290T	XC7VH580T	XC7VH870T
Network	2 x 100G	2 x 100G	1 x 400G or 4 x 100G
GTZ (28G)	8	8	16
GTH (13G)	24	48	72
Logic Cells	284K	580K	876K

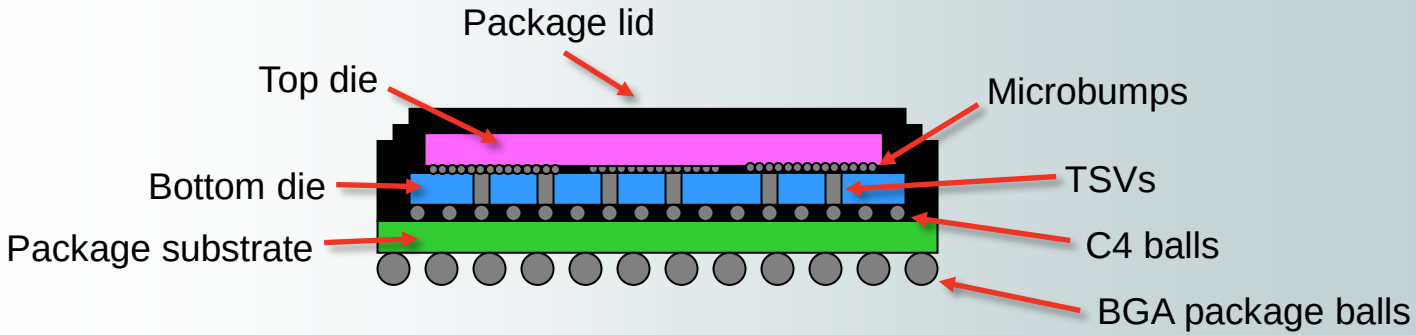
High Bandwidth Integrated Memory

- **Higher memory bandwidth at lower power**
  - 1Tbps – 2Tbps
  - ~1Gb/s per interposer wire
  - Simple extension of existing work



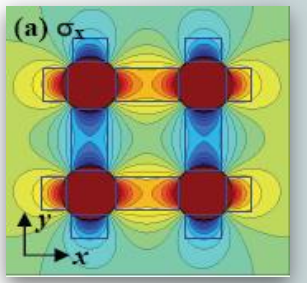
3D Active on Active: The Next Frontier

- **Who's on top?**



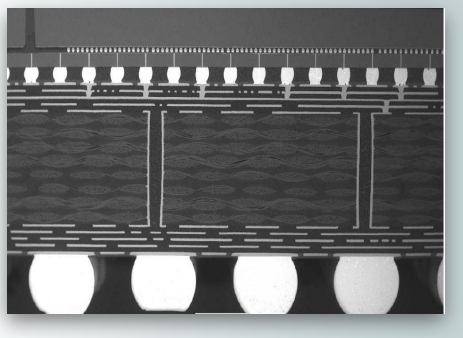
- **High performance chip on top for thermal and TSV process availability**
- **Bottom die supports power TSV's for top die**
- **Floor-planning critical**
  - Thermal concerns
  - TSV keep out zones

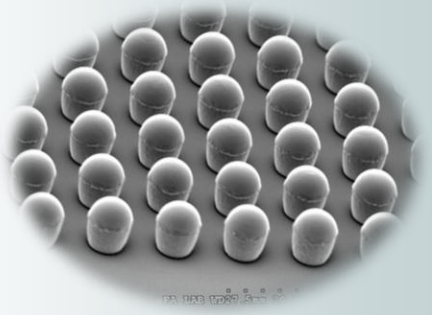
TSV-Induced Device Stress

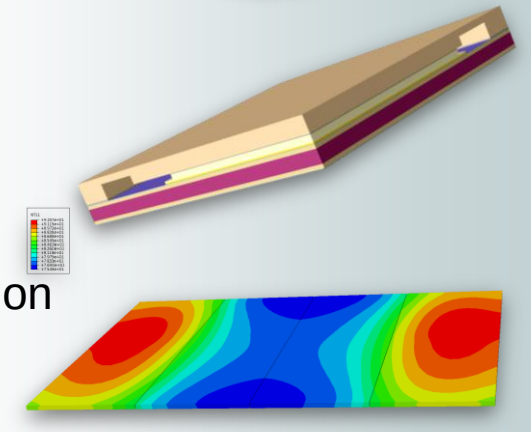


Challenges

- **Cost**
  - Wafer backside processing is complicated
  - “Device quality” wafers used for interposers
  - KGD methodologies still emerging
- **Scalability**
  - Micro-bump scaling is limited
  - Super-sized interposers (>30mm x 30mm)
  - Improve TSV aspect ratio
- **Design Support**
  - Multi-die analysis without Multi-mode Multi-corner explosion
  - Thermal modeling based on vertical hotspots



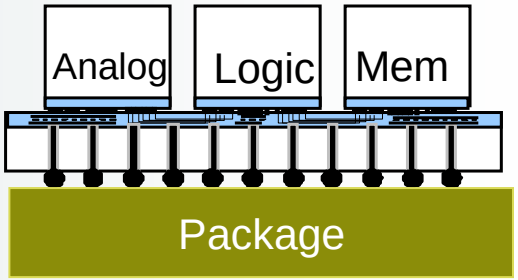




Summary

- Economic and technology forces are aligned to enable 3-D stacking

- The “end game” will see three distinct technologies: Logic, Memory, Analog



- Heterogeneous integration is already here

Thank You

Questions?

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