國立交通大學電子工程學系

Optimal Wiring Topology for Electromigration Avoidance Considering Multiple Layers and Obstacles

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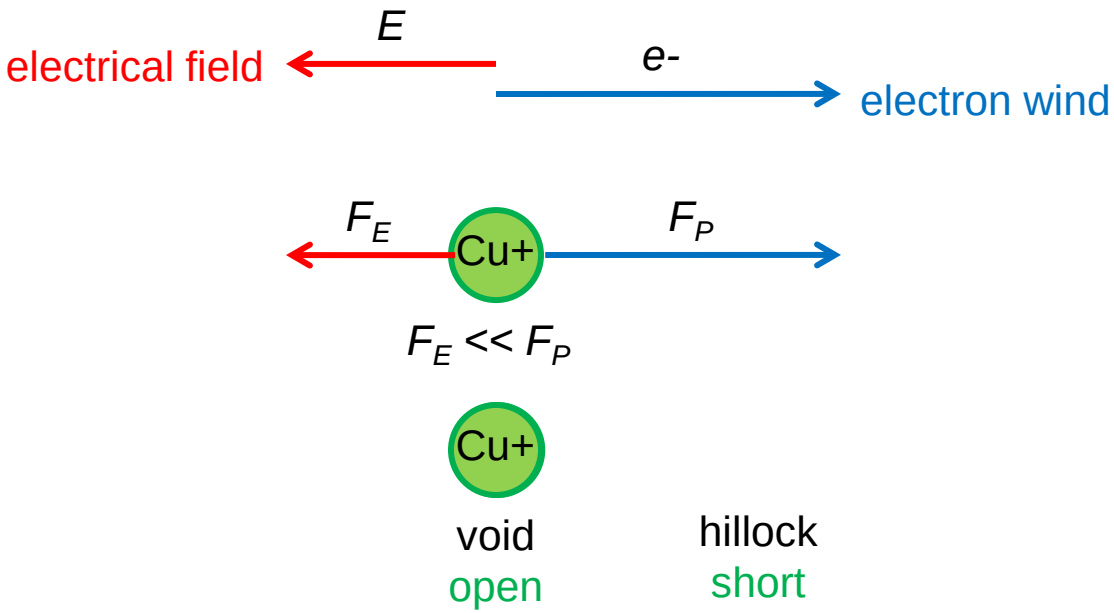
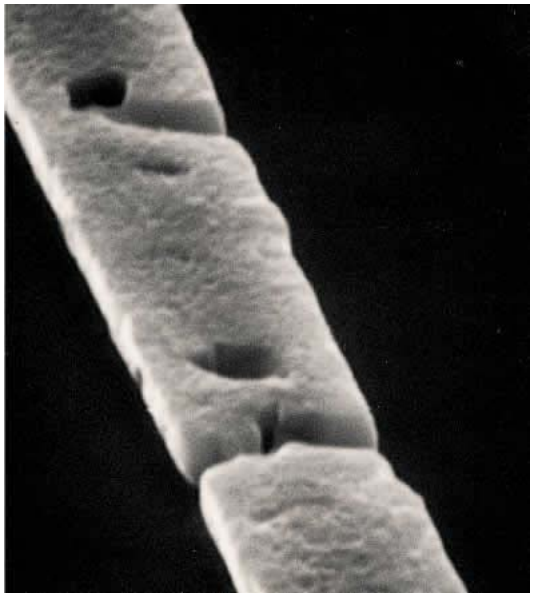
Outline

- **Introduction to EM**
- Problem & properties
- Our approach
- Experimental results
- Conclusion

Electromigration

- **Electromigration (EM)**
  - An extremely dense electron flow (electron wind) knocks off atoms within the wire and moves them away
  - This transport leaves a gap at one end and increase the stress at the other
    - Possible failures: open-circuit / short-circuit

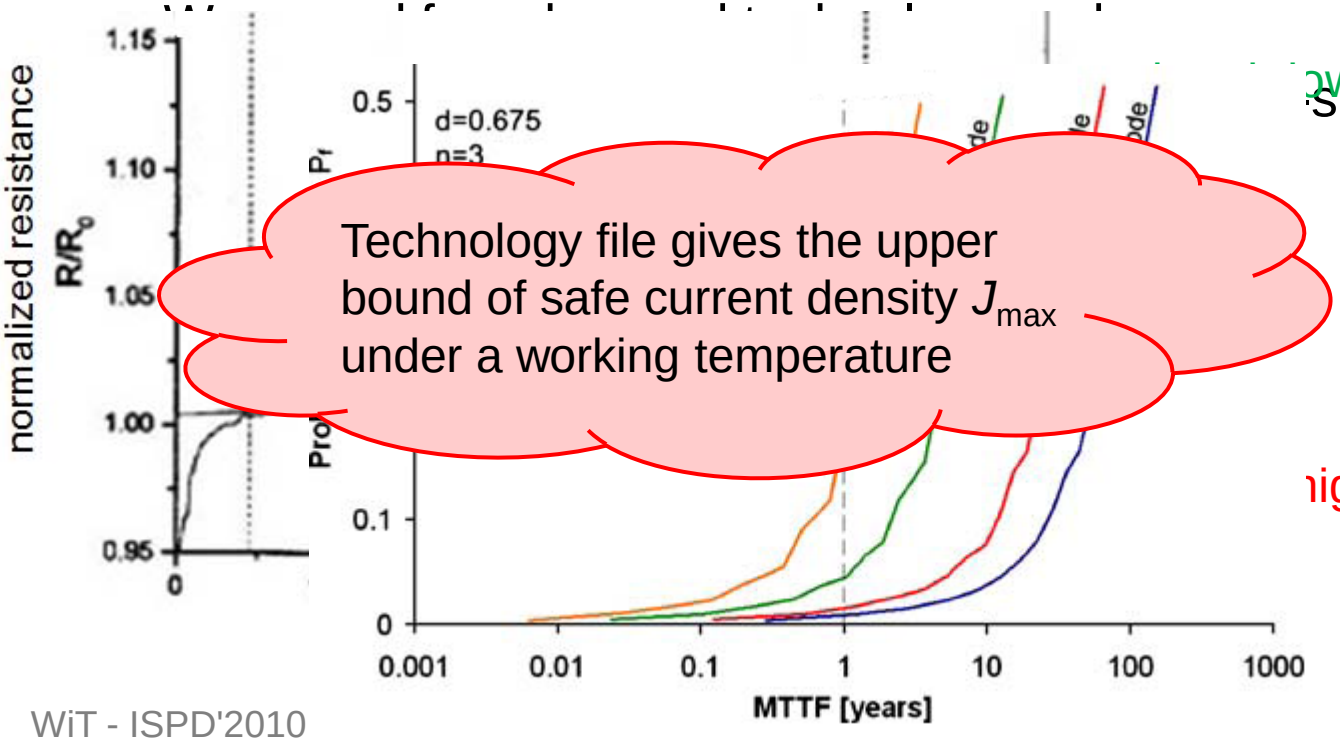




SANYO Semiconductor Co., Ltd.

Electromigration Is a Reliability Issue

- **EM is a wear-out failure**
  - Triggered after being used for a period of time
  - Measured in terms of mean time to failure (MTTF)
    - Black's equation, TED-1969
      - Current density and working temperature



Technology file gives the upper bound of safe current density J_{max} under a working temperature

-signal designs

ıigh current densities

J Electron Test, 2009

EM Reliability (1/2)

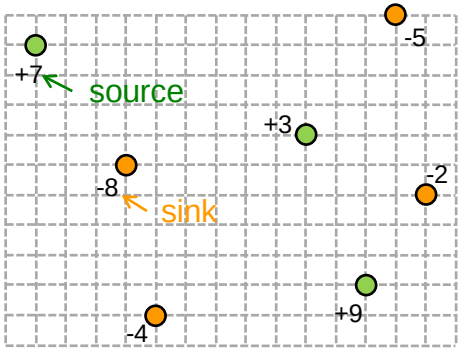
- **EM simulation/analysis**
  - Because EM occurs only after a circuit has been used for a period of time, the defect chips cannot be filtered out during product testing.
  - It is desired to characterize the realistic current values for each terminal/wire and to identify the wires that are potentially threatened by EM.
- **Wiring topology for EM**

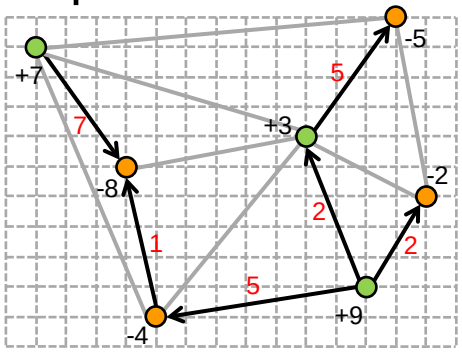
EM Reliability (2/2)

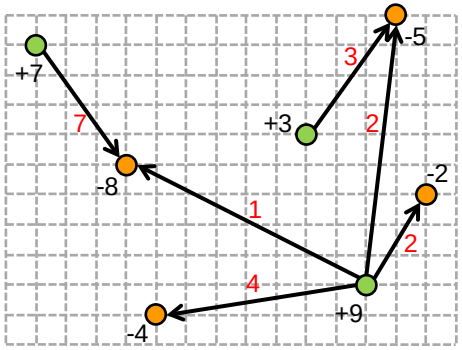
- **EM analysis/estimation**
- **Wiring topology for EM**
  - A thin wire should be widened for EM safety.
  - Conventional EM fixing is applied at post-layout, which may use many routing resources and layout changes.
  - If a good wiring topology considering EM is applied to a router, we may immune EM with much fewer routing resources.
  - e.g.,
    - Adler & Barke, DATE-2000
    - Adler et. al, DAC-2000
    - Lienig & Jerke, ASPDAC-2003
    - Yan & Chen, APCCAS-2008

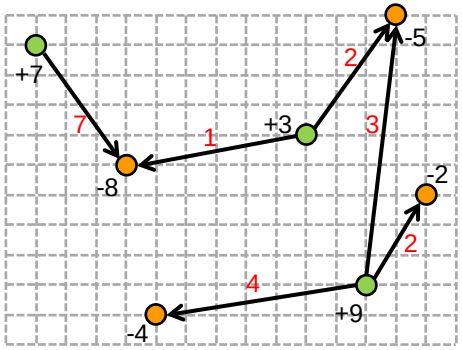
EM Routing

- **The routing resource is measured by the total wire area.**
  - The wire width is determined by EM-safe current density instead of minimum printable width.

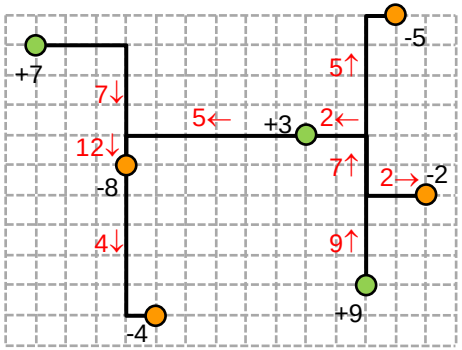


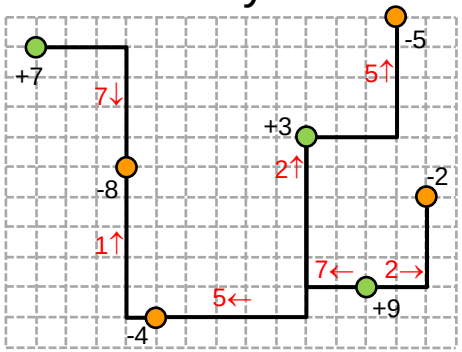


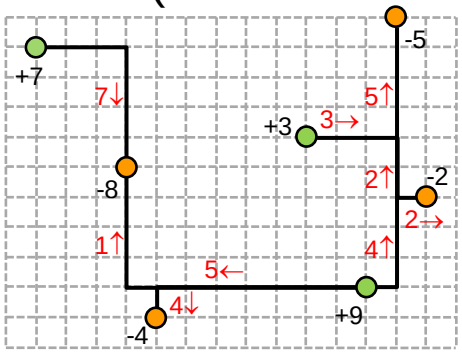


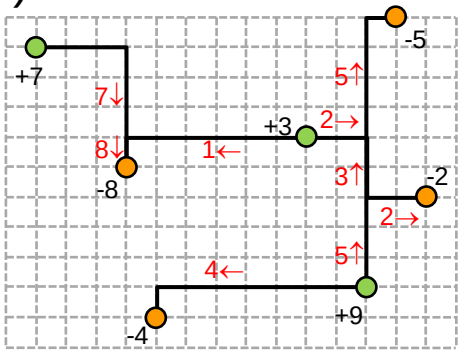


Assume a unit width wire can carry one-unit current (normalized to 1)









Minimum WL = 33
Area = 182

ASPDAC-2003
Area = 154

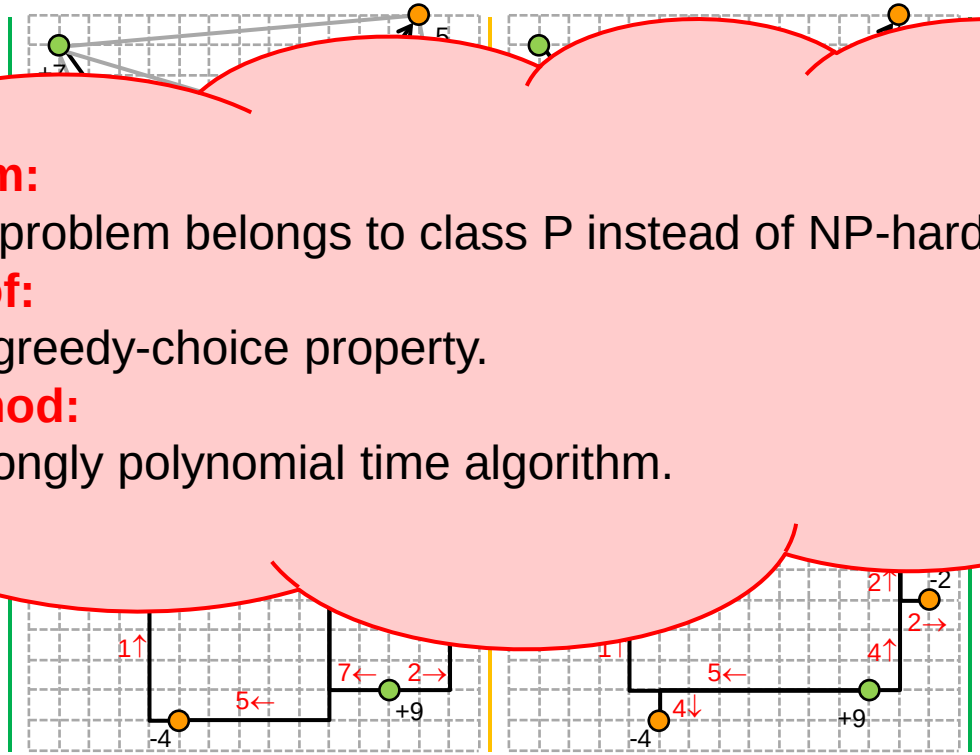
APCCAS-2008
Area = 144

Ours
Area = 142 (optimal)

Our Contribution

- **Prior works tended towards heuristics**
  - State-of-the-art results

Claim:
This problem belongs to class P instead of NP-hard.
Proof:
The greedy-choice property.
Method:
A strongly polynomial time algorithm.



ASPDAC-2003
DT-based
Area = 154

APCCAS-2008
Greedy
Area = 144

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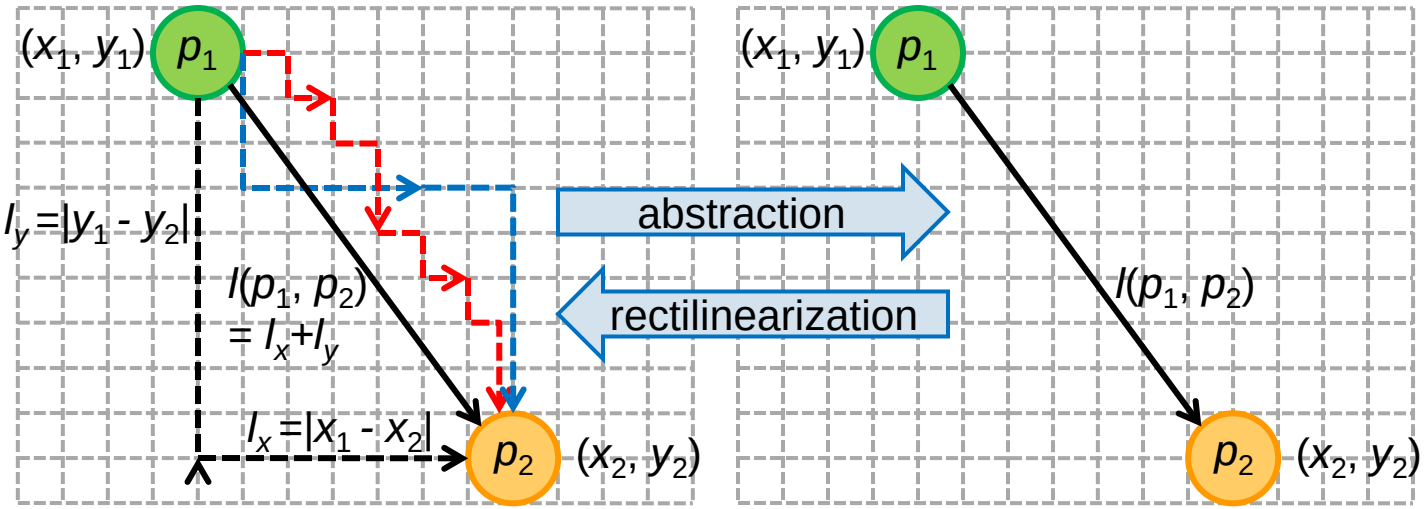
Wiring Topology for EM Avoidance (TEA)

- **Input**
  - A set $S = \{s_1, s_2, \ldots, s_m\}$ of m current sources
  - A set $T = \{t_1, t_2, \ldots, t_n\}$ of n current sinks
    - Each current source i (sink j) is associated with its flow
  - The maximum tolerable current density J_{max}
  - The minimum feasible wire width w_{min} for each routing layer/via
- **Output**
  - A wiring topology to connect all current sources and sinks in $S+T$
    - Minimum total wire area of its detailed routing tree
    - Sufficient current for each wire segment: $f \propto w$
    - Kirchhoff's current conservation law
- **Remarks:**
  - $f \propto w$: The wire width offering one unit current is a layer-specific constant.
  - The current values can be DC, RMS, peak, average currents under different EM conditions and for various signal types.
  - Feasibility: $\sum f_{si} + \sum f_{tj} = 0$

Wirelength: Abstraction

- **2D**

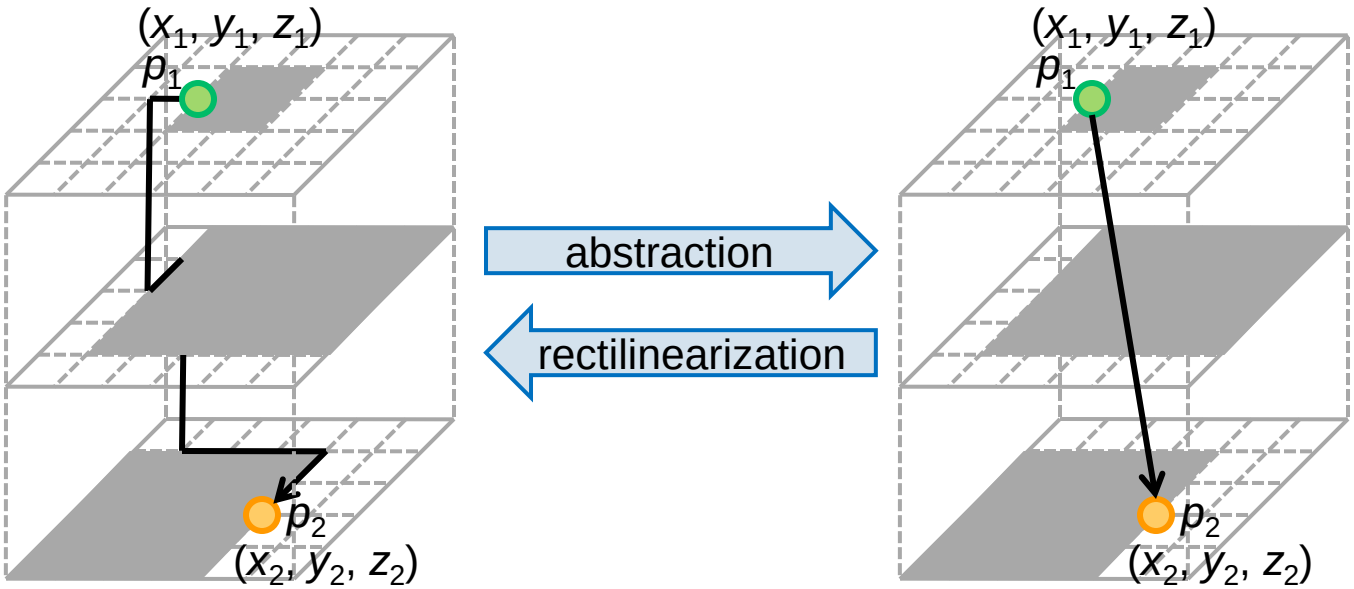
No obstacles



- **3D**

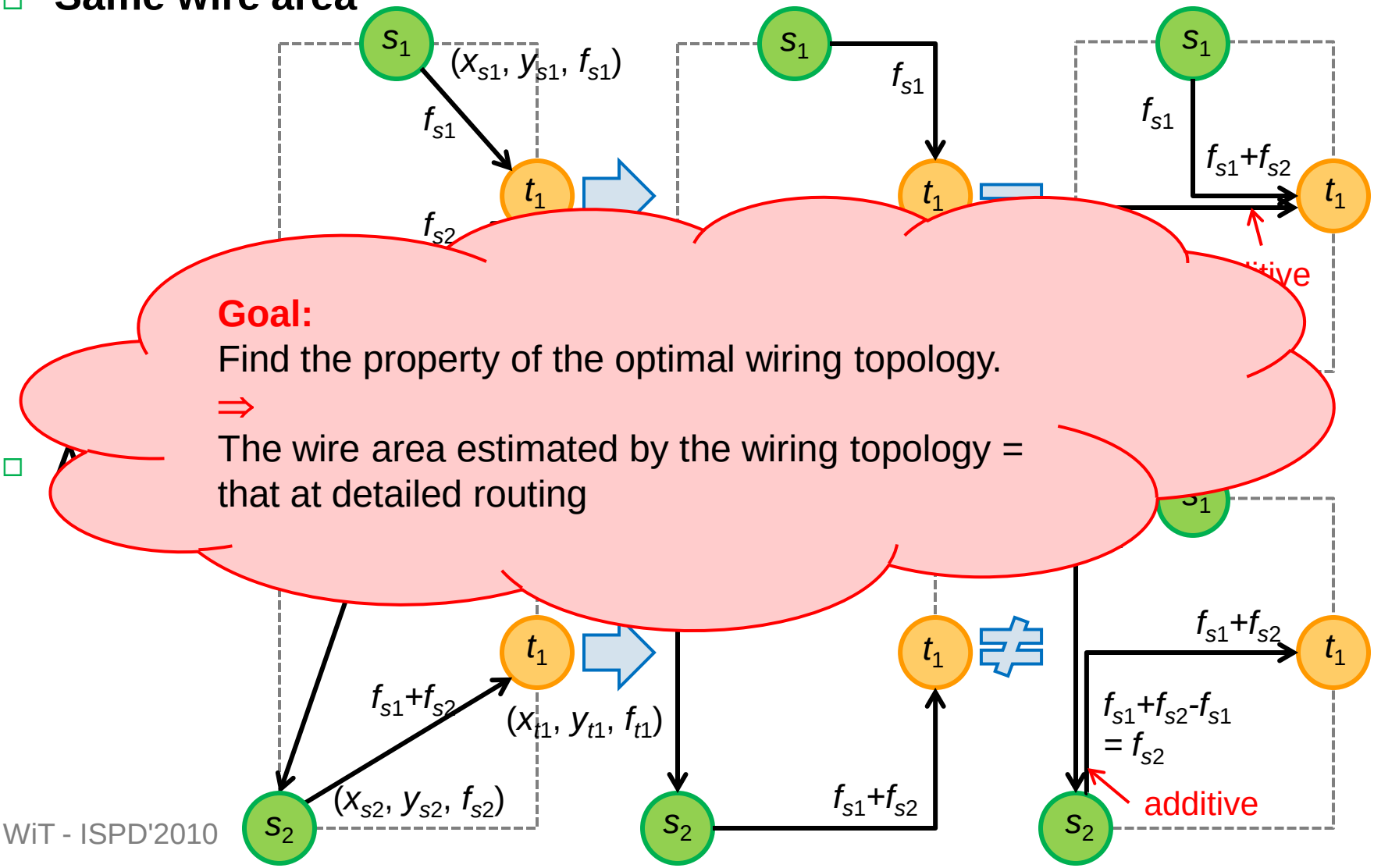
With obstacles

the minimum accumulated area cost for one unit current



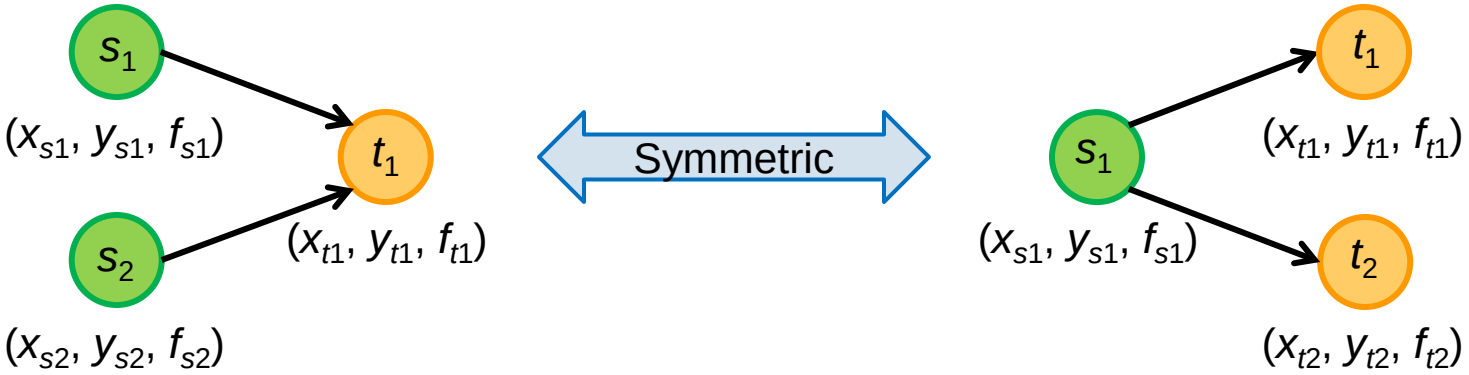
Wire Area: Superposition

- **Same wire area**



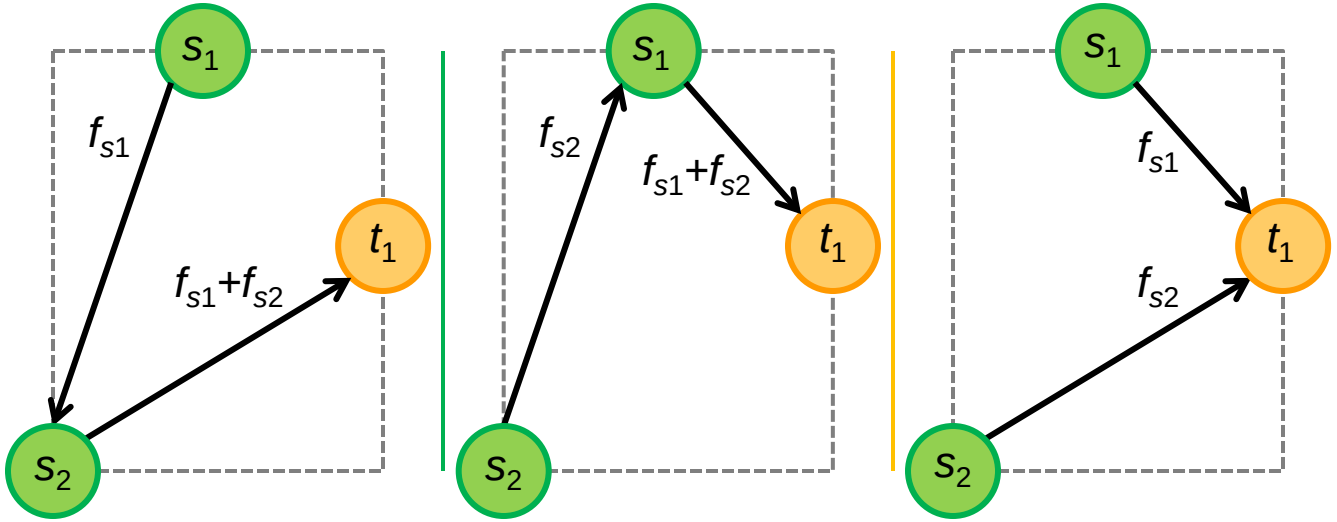
The Greedy-Choice Property (1/3)

- **The generic form: 2 sources s_1, s_2 and 1 sink t_1.**
  - $f_{s1} + f_{s2} + f_{t1} = 0$
- **We prove the greedy-choice property**



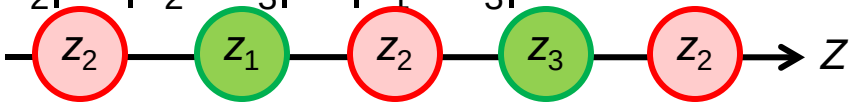
The Greedy-Choice Property (2/3)

- **Prove by exchange argument.**



$A\{s_1 \to s_2 \to t_1\}$ $A\{s_2 \to s_1 \to t_1\}$ $A\{s_1 \to t_1\} + A\{s_2 \to t_1\}$

- Axes are independent.
- Consider 3 points z_1, z_2 and z_3 on an axis: fix z_1 and z_3, move z_2
  $\Rightarrow |z_1 - z_2| + |z_2 - z_3| \geq |z_1 - z_3|$



- $A\{s_1 \to s_2 \to t_1\}$ or $A\{s_2 \to s_1 \to t_1\} \geq A\{s_1 \to t_1\} + A\{s_2 \to t_1\}$

The Greedy-Choice Property (3/3)

- **Corollary: The greedy-choice property holds at a general multi-layer space with obstacles.**

The greedy-choice property
⇒
1. We can consider wire connections only from sources to sinks.
2. The wire area keeps the same after the slant edges of the greedy-choice property are rectilinearized.

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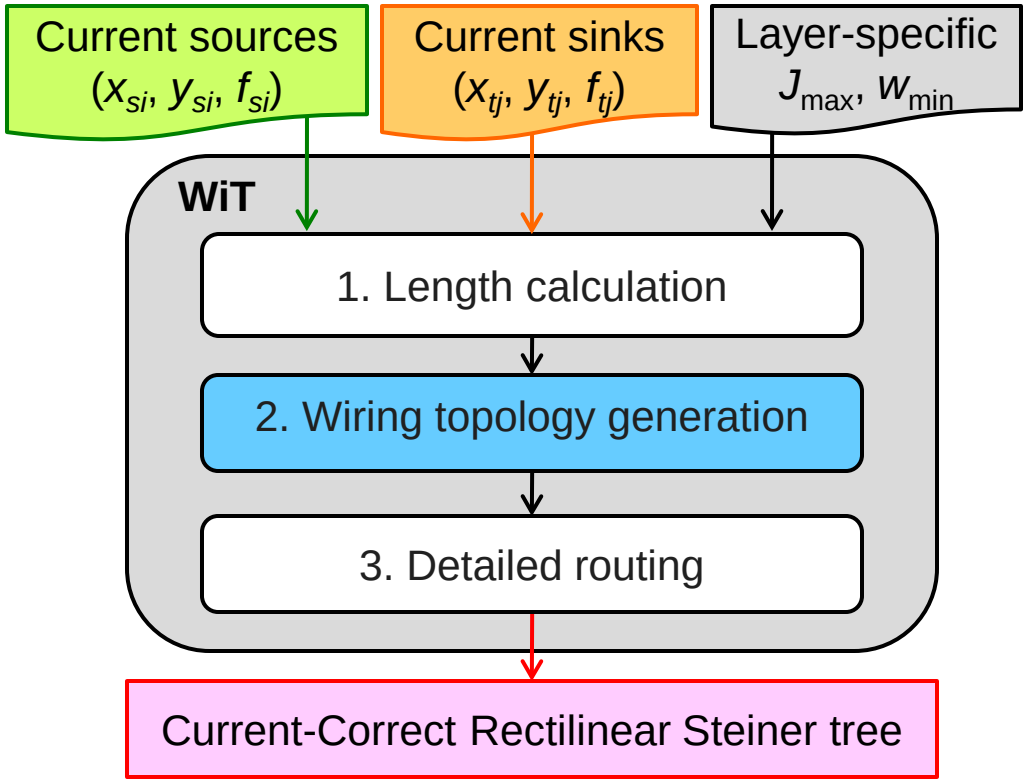
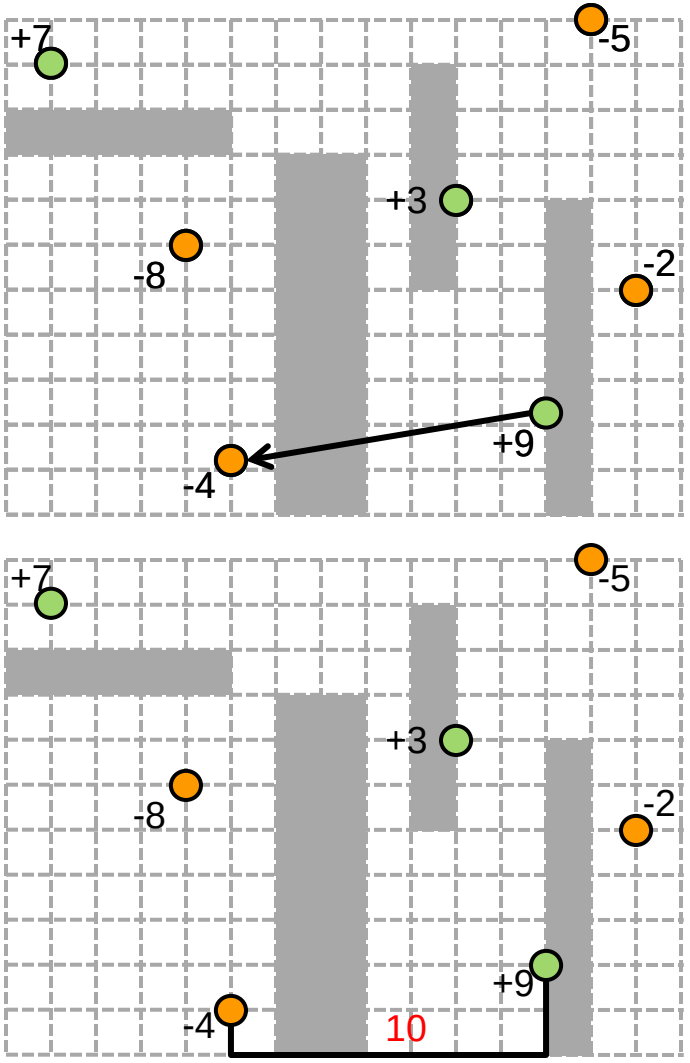
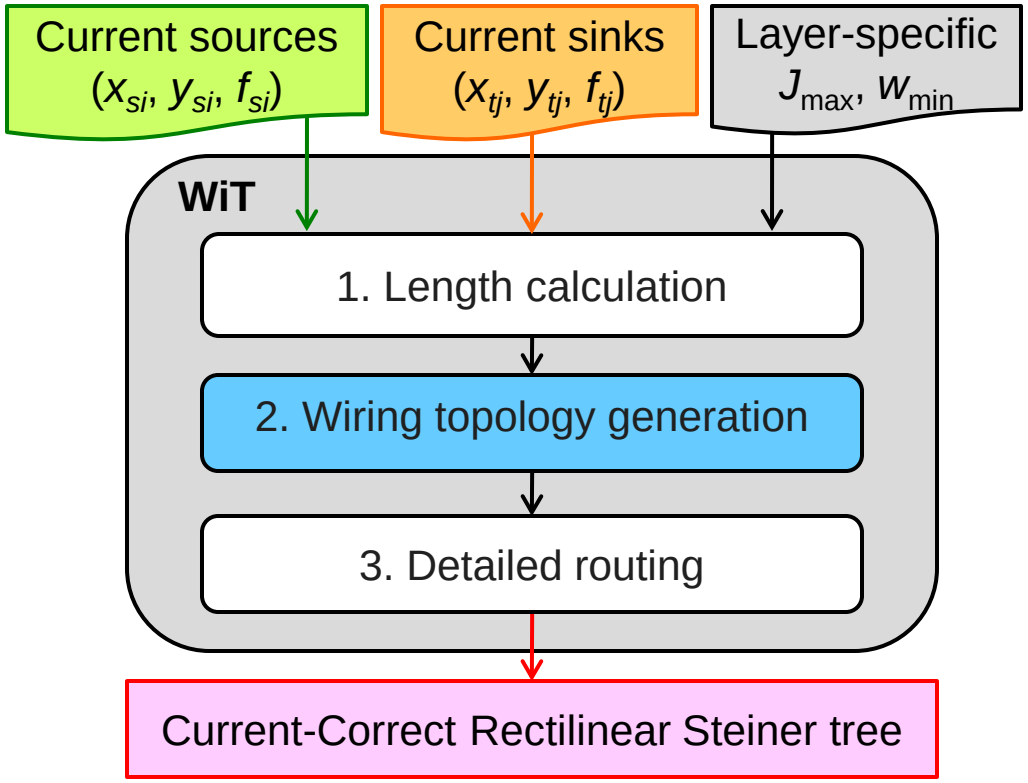
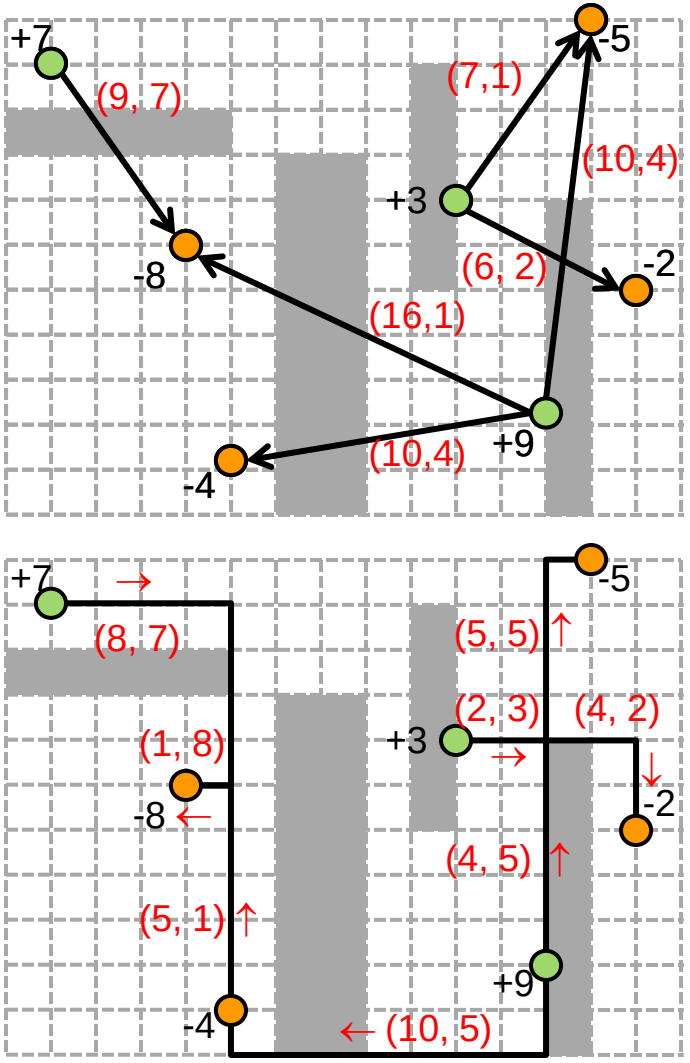
Overview of WiT (1/2)





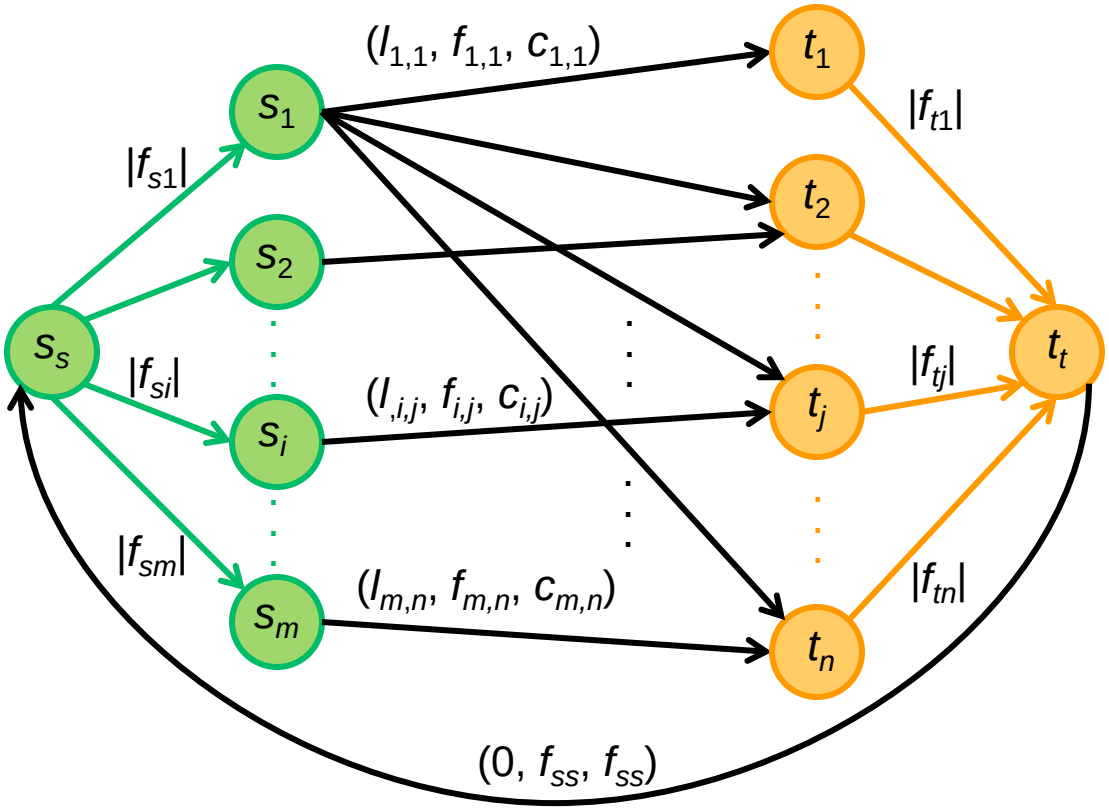
Overview of WiT (2/2)





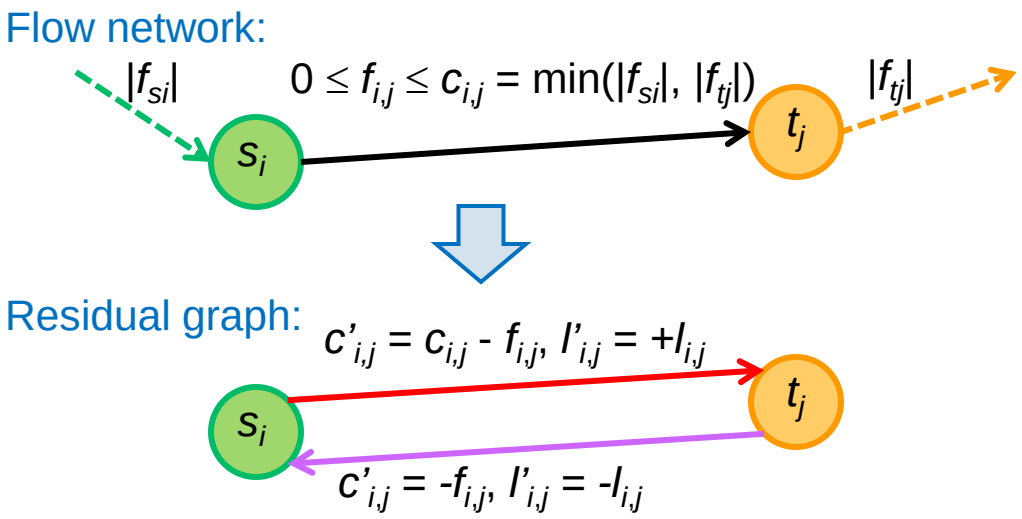
Flow Network

- **Triple: (wirelength, flow, capacity)**
  - Feasible flow: $0 \le f_{i,j} \le c_{i,j} = \min(|f_{si}|, |f_{tj}|)$



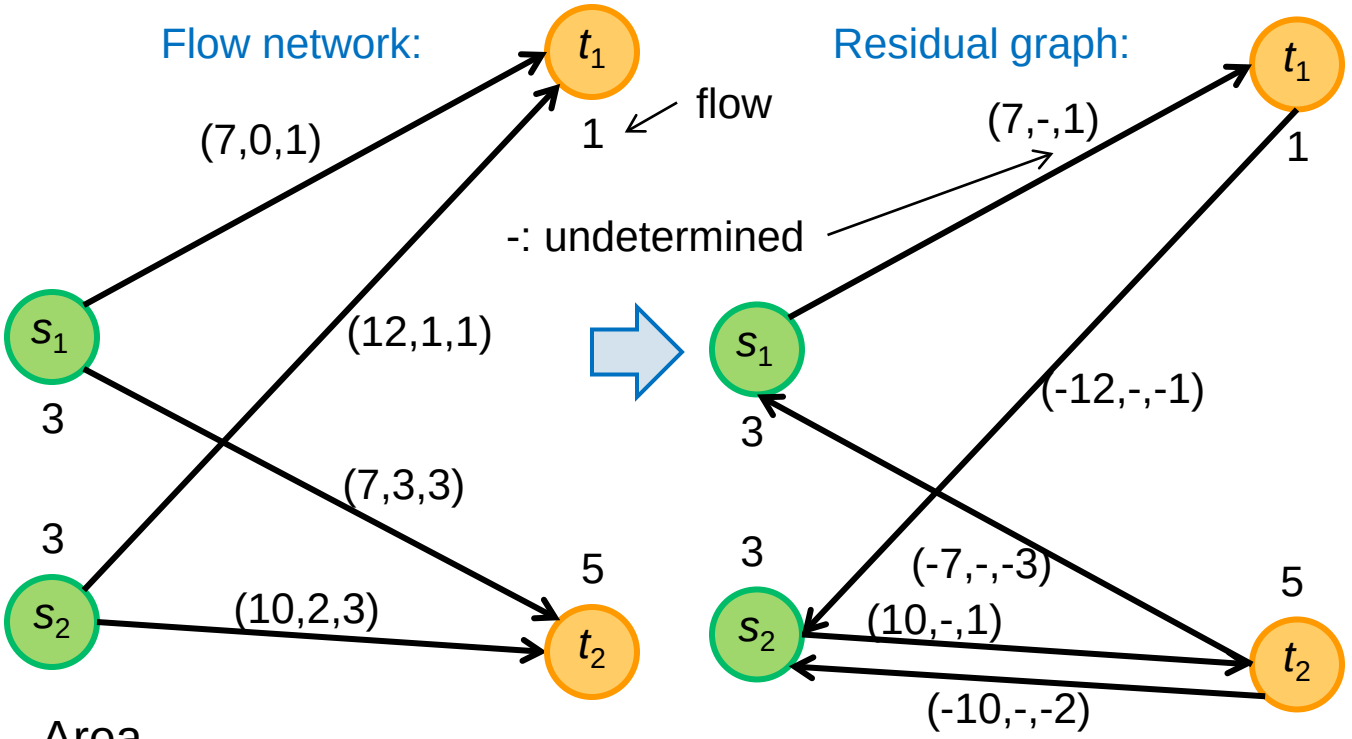
Residual Graph

- **Forward edge: push flow**
- **Backward edge: return flow**



Wire Area Optimization

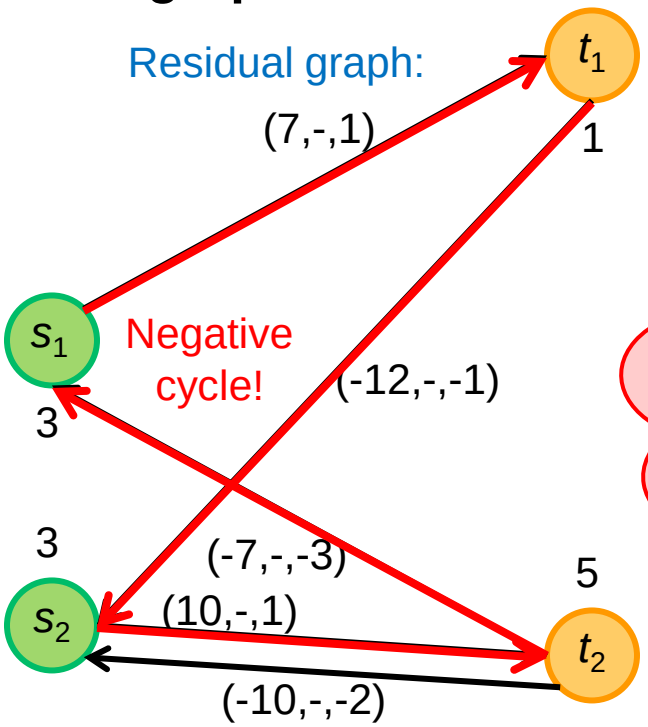
- **Triple: (wirelength, flow, capacity)**



Area
= 7*0 + 7*3 + 12*1 +10*2
= 53

Negative Cycle Detection (1/2)

- **Theorem: Negative-Cycle Removal: If the flow assignment of a flow network is optimal, there exists no negative cycles in its residual graph.**



7 + (-12) + 10 + (-7) = -2

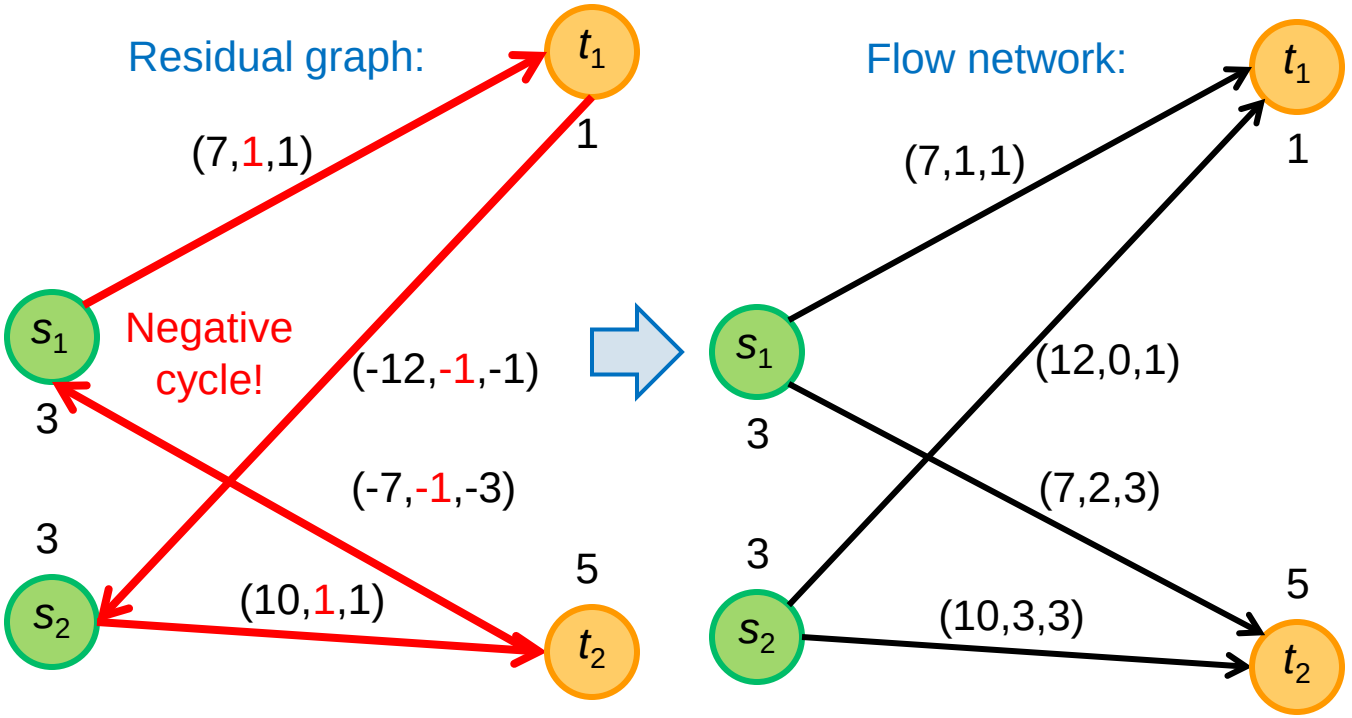
Push a flow along the negative cycle

⇒

1. Reduce the area cost
2. Flow = min residual cap

Negative Cycle Detection (2/2)

- **Theorem: Negative-Cycle Removal: If the flow assignment of a flow network is optimal, there exists no negative cycles in its residual graph.**



Area
= 7*1 + 7*2 + 12*0 +10*3
= 51

The WiT Algorithm

WiT(*S*, *T*)
1. construct the flow network and calculate paths and lengths
2. **if** the given flow at sources/sinks is legal **then**
3. find an initial flow assignment
4. **while** there exists a negative cycle in the residual graph **do**
5. remove the negative cycle
6. update the flow network
7. update the residual graph
8. rectilinearize the wiring topology by stored paths

- **Initial solution:**
  - For efficiency, we select the greedy method.
  - For effectiveness, we choose the minimum wirelength as the greedy rule.

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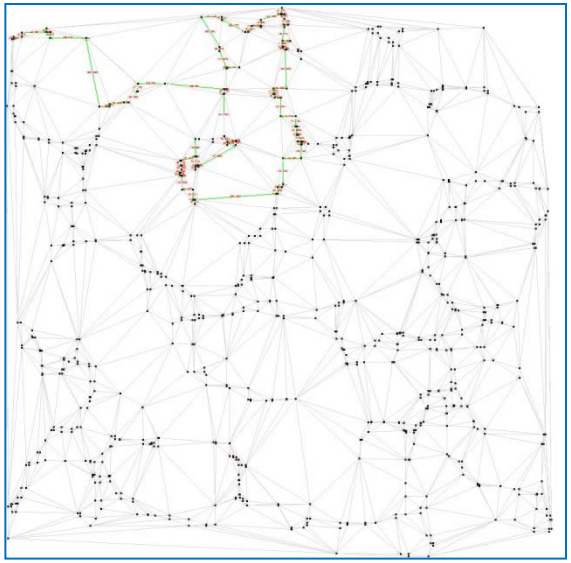
Results

- **Implementation:**
  - C++ language with LEDA package
  - NB with an Intel® Core™2 CPU T9400 of 2.53 GHz frequency and 4 GB memory under Windows Vista™ Business 64 bit Service Pack 1 OS.

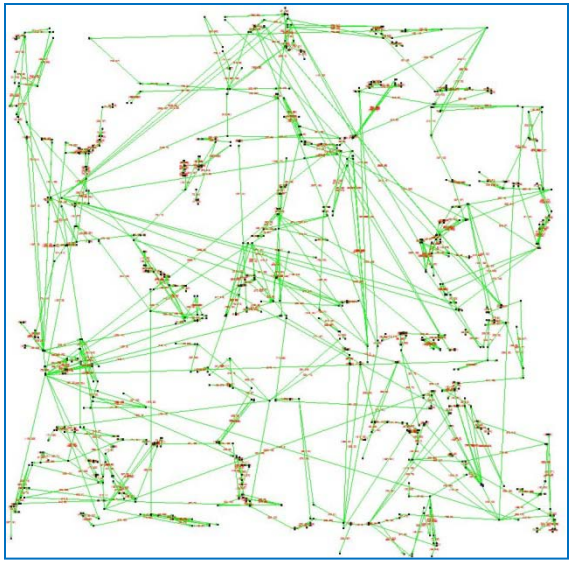
Testcase		INP1	INP2	INP3	INP4	IND1	IND2	IND3	IND4	IND5	RT01	RT02	RT03	RT04	RT05
#Terminals		7	16	10	16	10	10	10	25	33	75	180	303	475	850
ASPDAC-2003	Area	154	122	210	32	6,661	79,400	FAIL	23,112	31,466	FAIL	FAIL	FAIL	FAIL	FAIL
	Runtime (s)	0.001	0.002	0.001	0.002	0.038	0.016	-	0.016	0.040	-	-	-	-	-
APCCAS-2008	Area	144	98	128	40	5,319	79,000	6,181	16,000	20,814	189,437	10,638,884	3,360,716	6,475,941	59,207,240
	Runtime (s)	0.001	0.002	0.001	0.002	0.001	0.001	0.001	0.003	0.005	0.120	4.958	45.553	297.806	8,573.453
	Refined area	**142**	**90**	**116**	**32**	**5,301**	**74,200**	**5,513**	**13,728**	**17,044**	**144,071**	**7,151,286**	**2,325,806**	**4,205,757**	**37,318,054**
	Gain	2	8	12	8	18	4,800	668	2,272	3,770	45,366	3,487,598	1,034,910	2,270,184	21,889,186
	#Iterations	**1**	**2**	**1**	**1**	**1**	**3**	**15**	**20**	**29**	**147**	**622**	**1,938**	**4,288**	**9,238**
	Refine runtime (s)	0.000	0.000	0.001	0.000	0.000	0.001	0.001	0.002	0.003	0.028	0.496	4.741	28.883	440.429
WiT	Initial area	142	94	116	32	5,301	78,200	5,629	15,092	19,624	156,489	8,139,250	2,840,420	4,831,845	45,677,120
	Initial runtime (s)	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.015	0.042	0.109	0.425
	Final area	**142**	**90**	**116**	**32**	**5,301**	**74,200**	**5,513**	**13,728**	**17,044**	**144,071**	**7,151,286**	**2,325,806**	**4,205,757**	**37,318,054**
	Gain	0	4	0	0	0	4,000	116	1,364	2,580	12,418	987,964	514,614	626,088	8,359,066
	#Iterations	**0**	**1**	**0**	**0**	**0**	**3**	**2**	**17**	**37**	**78**	**415**	**949**	**1,197**	**3,487**
	Total runtime (s)	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.016	0.297	1.794	6.489	89.497

- **Efficient initial solution.**
- **We can refine any initial solution to the optimal.**

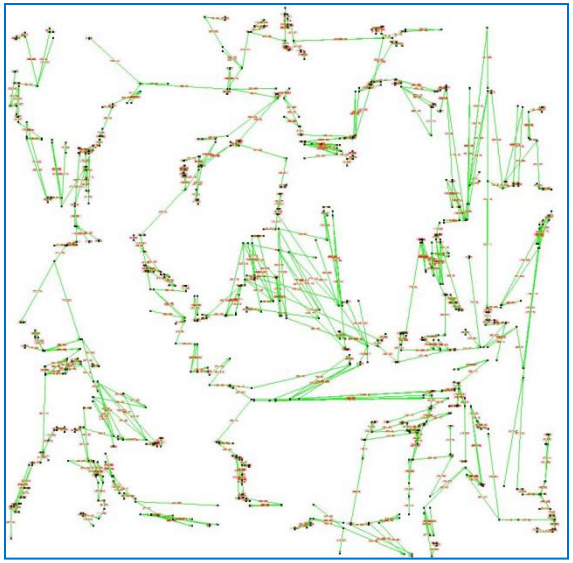
RT05: 850 Terminals



ASPDAC-2003
FAILED



APCCAS-2008
Area = 59,207,240



Ours
Area = 37,318,054

Conclusion

- **In this paper, we focus on wiring topology generation for avoiding electromigration for power networks or signal nets in analog and mixed-signal designs.**
- **The major contribution is that we claim this problem belongs to class P instead of class NP-hard.**
- **Based on the proof of the greedy-choice property, we successfully model this problem on a multi-source multi-sink flow network and then can solve it in a strongly polynomial time.**
- **Experimental results prove the efficiency and effectiveness of our algorithm.**

Thank You!

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Backup slides

Multi-Source Multi-Sink Circuits?

- **Q: What kind of design has multiple sources and sinks?**
- **A: Usual in analog or mixed signal designs, power network, etc.**

Non-uniform Temperature Distribution

- **Q: What if non-uniform temperature distribution within a chip?**
- **A: This abstraction still works with given temperature distribution map.**