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Skew Management of NBTI Impacted Gated Clock Trees

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Outline

- Background: Clock Gating & NBTI Effect
- Problem: Skew due to NBTI in gated clock
- Previous Works
- Proposed Solution
- Results

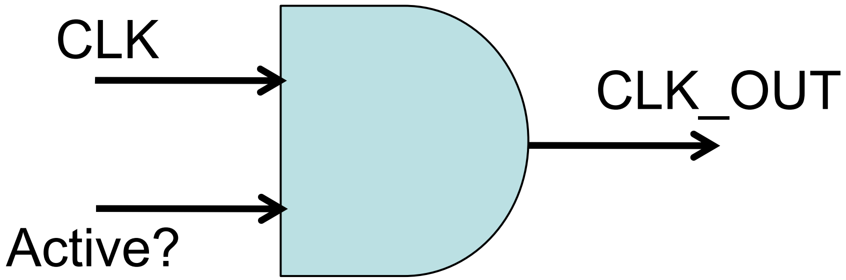
Clock Gating

- Very popular low power technique
- Freeze (“gate”) clock to inactive module
  - Needs: Signal informing if a module is inactive
  - Needs: Way to use this signal to freeze clock
- Inactivity deduced by checking input permutations
  - Example: OPCODE for adder? Freeze multiplier clock
  - RTL simulation and ON/OFF set manipulation helps

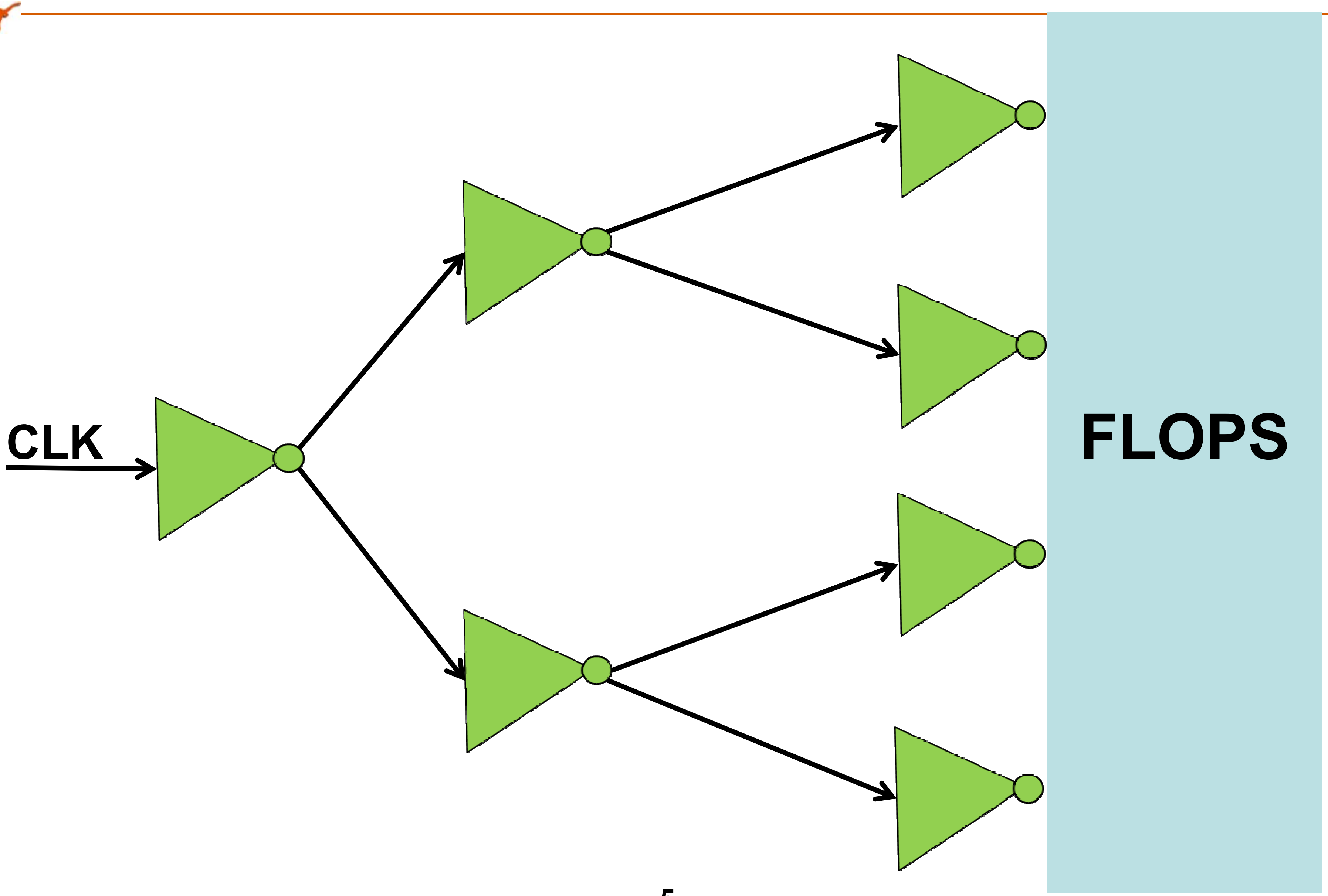
Clock Gating (2)

- Duration of gating determined by many factors
  - Gating aggressiveness, input data statistics

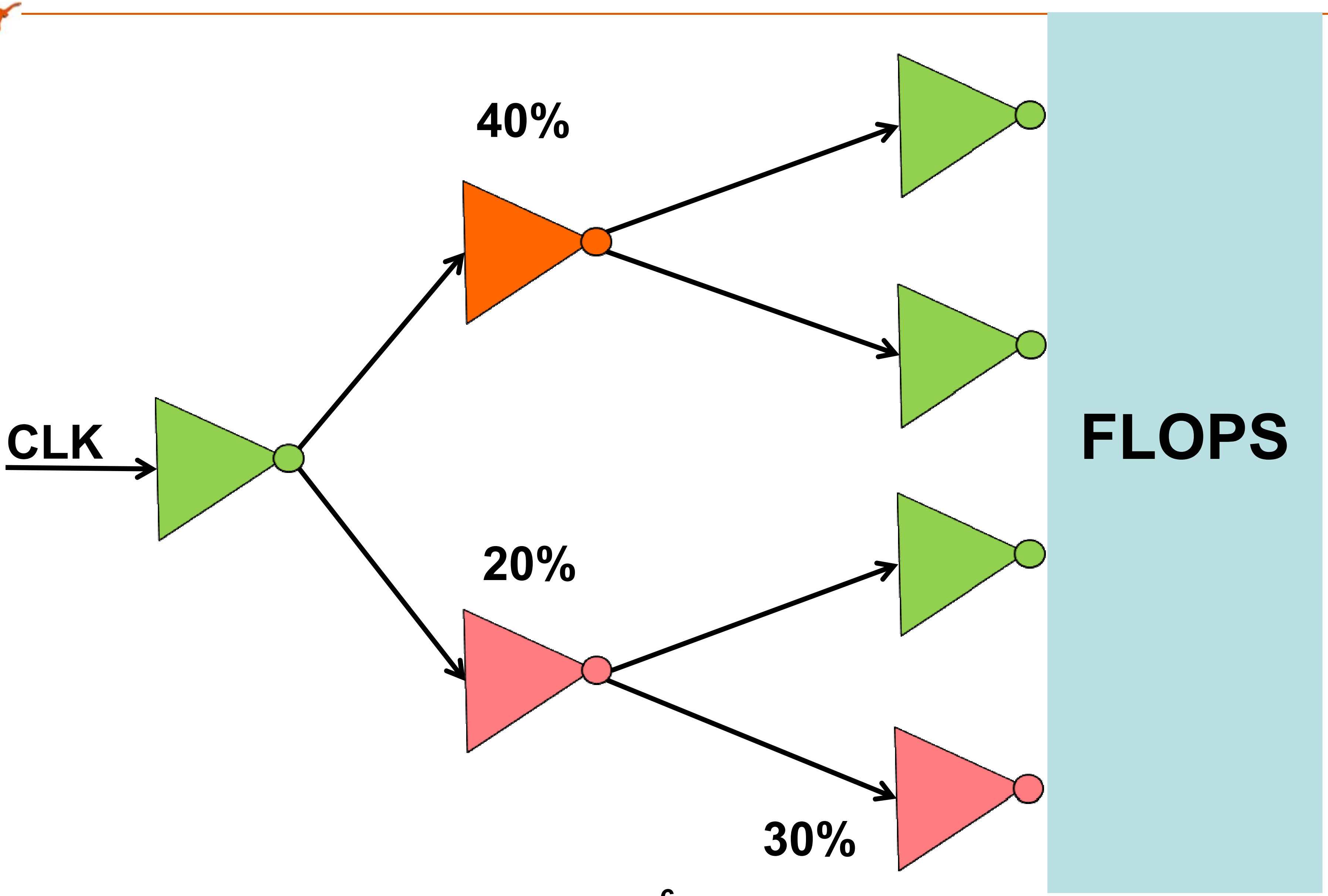
- How to stop clock signal?
  - Use NAND/NOR/AND/OR gate
  - One input: regular clock signal
  - Other input: Inactivity/Activity signal



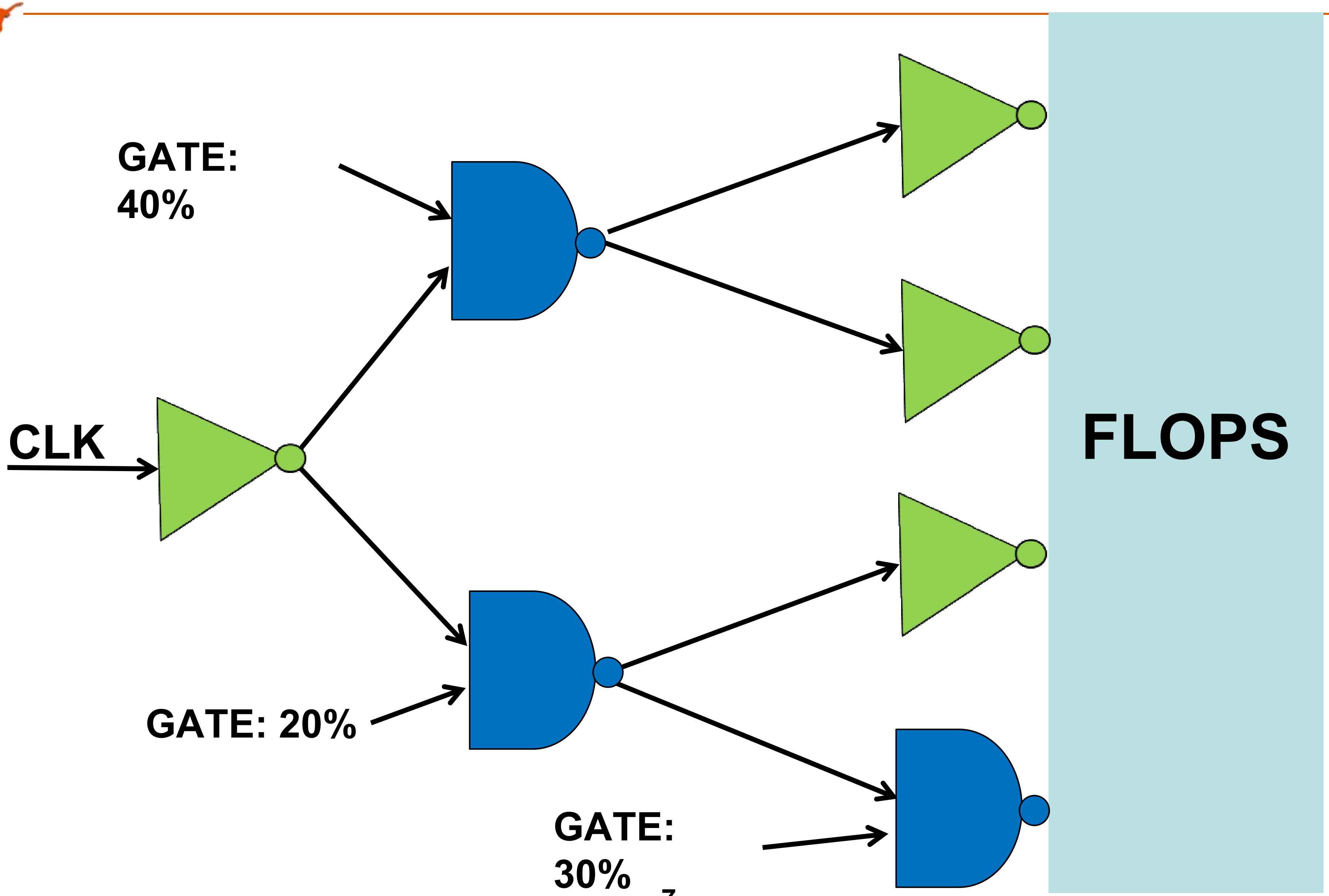
Example Clock Tree



Minimize Clock Gating Elements



Implementation using NANDs



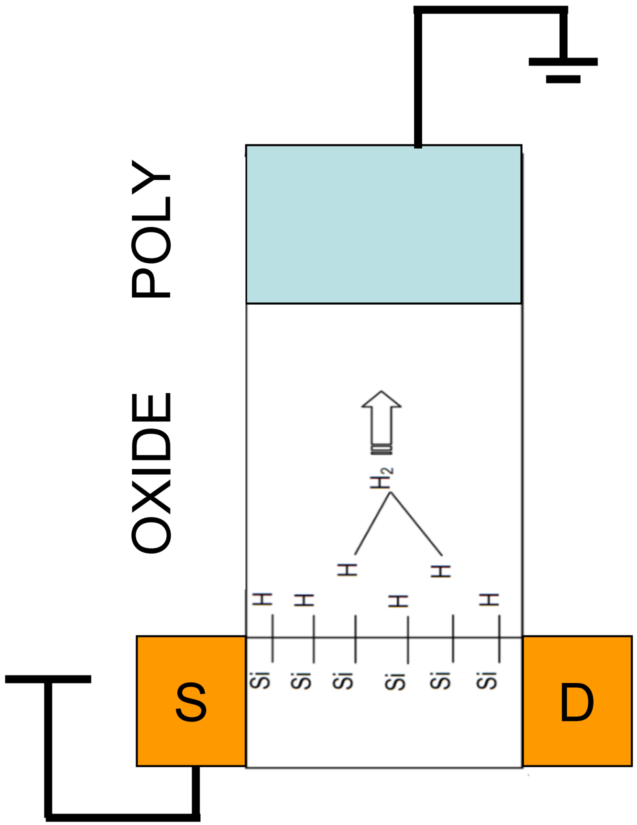
NBTI Effect

- **N**egative **B**ias **T**emperature **I**nstability
- Occurs when **PMOS** negatively biased (V_{GS}<0)

- Reason:
  - › V_{GS}<0 causes Si-H breaking
  - › Need higher V_G to invert channel

- Effects:
  - › ΔV_{TH} = +100mV 10 years
  - › 30% increase in inverter delay

    [Kumar et. al. DAC 2007]



[Alam et. al. 2005 Micro. Reliab.]

NBTI Effect (2)

- Proportional to negative bias duration ($\sim t^N$)

- For PMOS in standard cells,
  - $V_{GS} < 0$ ➔ $V_G < V_{DD}$ ➔ Input to cell = logic LOW
  - Thus, logic LOW feeding a cell causes NBTI
  - **Differing LOW probability ➔ different degradation**

- Define SP0 = Probability of signal to be LOW
  - Higher SP0 ➔ More NBTI Degradation

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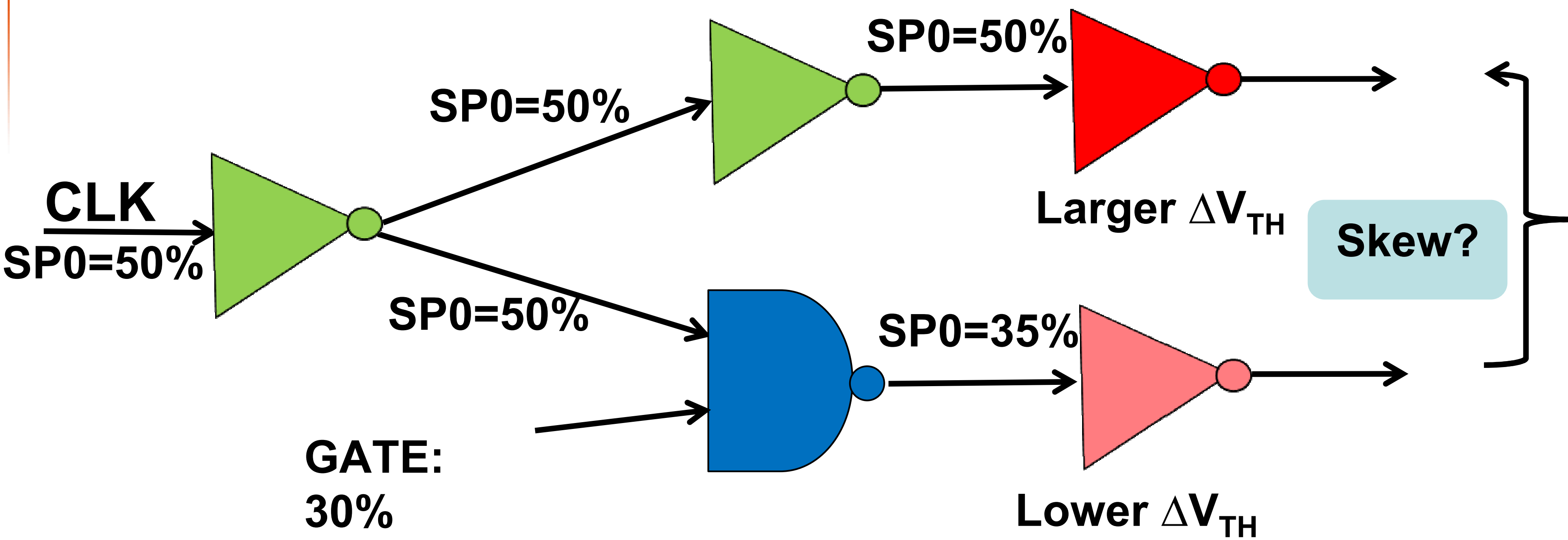
SP0 Difference due to Clock Gating



- Using NAND gate reduces SP0 at output
- Using NOR gate increases SP0 at output
- In both cases, $\Delta \mathbf{V}_{TH}$ mismatch will exist!

Problems due to ΔV_{TH} mismatch?

- Clock skew can degrade significantly!
- Up to 2.5X increase in skew [Chakraborty et al, DATE 2009]
  - Large variation due to difference in nominal values
  - Will lead to timing violation and circuit failure

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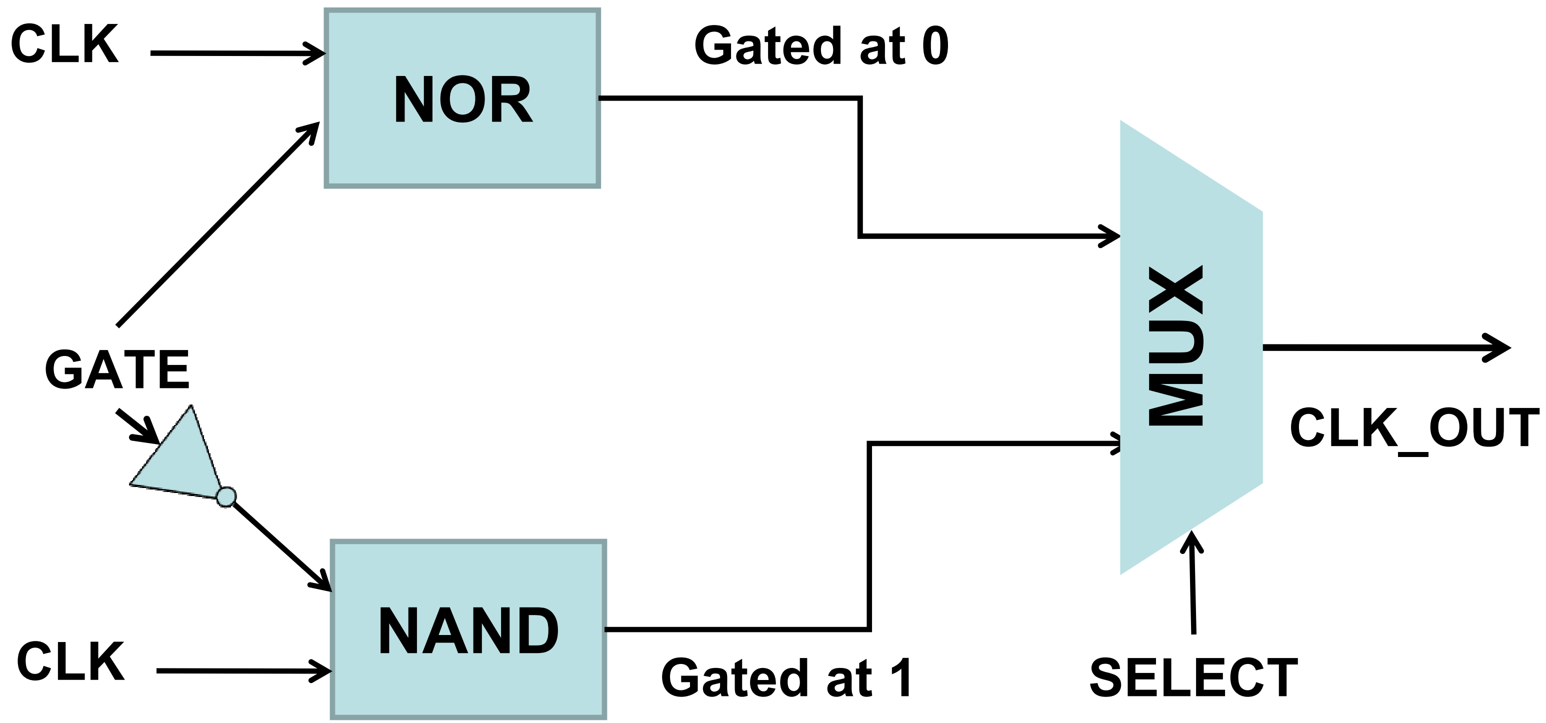
Previous Works

- 2003: US patent 6651230 [John Cohn et. al.]
  - Essentially overdesign by tightening skew bound.
  - **A limit to which skew constraint can be tightened.**
- 2009: DATE 09 [Chakraborty et. al.]
  - First runtime compensation for NBTI in clock trees
  - At runtime, choose NAND or NOR to drive
  - Aims to equalize all signal probabilities (of clock nets)
    - **Power Penalty? Routing?**

Previous Works (2)



If { GATE = FALSE }	CLK_OUT = CLK
Else If { SELECT = 0 }	CLK_OUT = 0
Else	CLK_OUT = 1

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Main Idea

- NAND Gate increases SP0 at output
- NOR Gate reduces SP0 at output
- SP0 impacts delay cell of the cell being driven
- Need to reduce **delay** difference at sinks

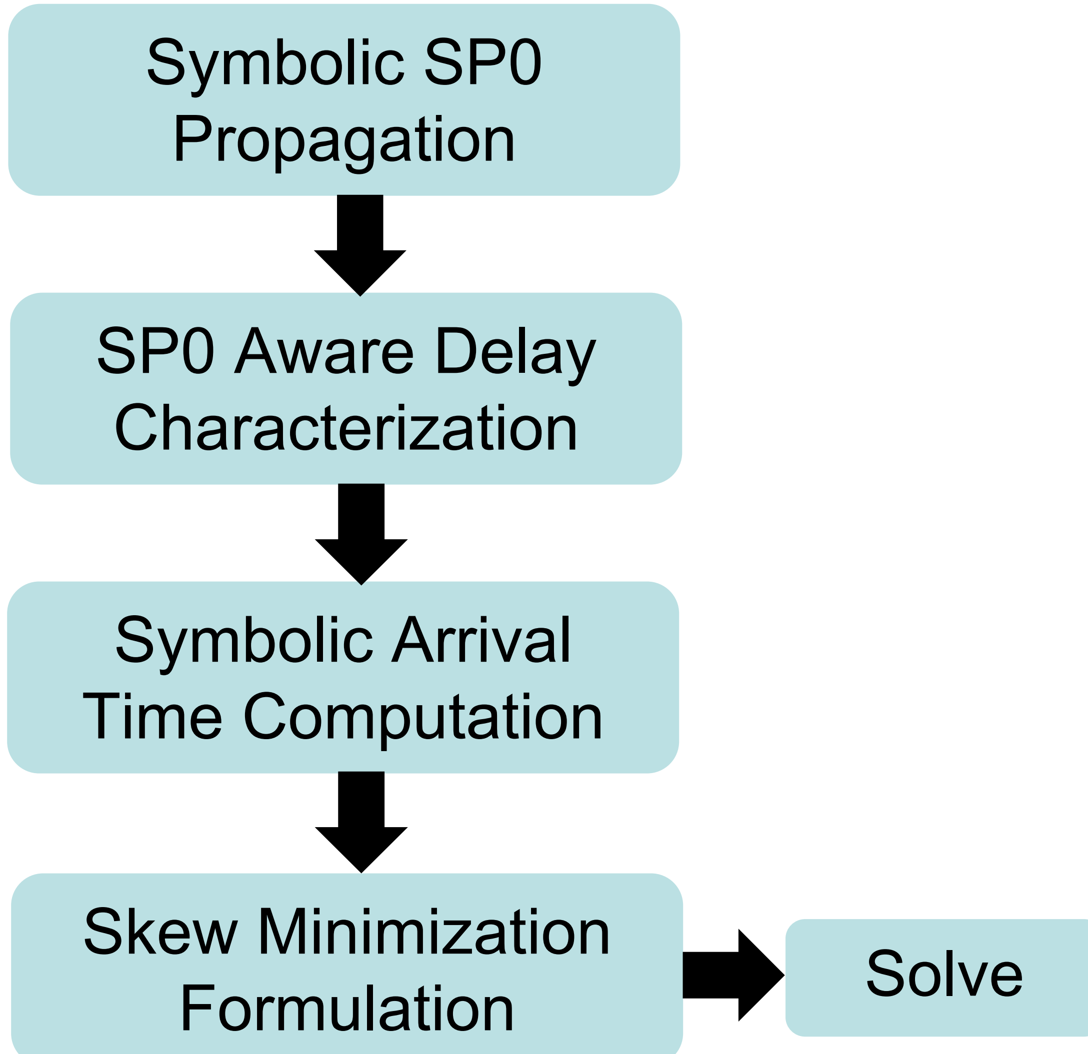
- Multiple levels of clock gating elements
  - Can we selectively choose NAND/NOR at the right places, so that even if SP0 is different within the tree, by the time sinks are reached, the **delay** difference is minimized?

Proposed Solution

- At design time (i.e. statically), determine NAND or NOR choice for each gating enabled buffer
  - Objective: Minimize skew after NBTI aging

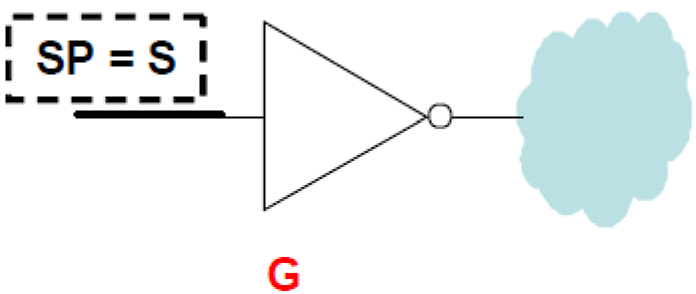
- Benefits:
  - No hardware penalty w.r.t. regular clock gating
  - No glitches due to SELECT signal switch
  - No extra routing overhead

Our Optimization Flow

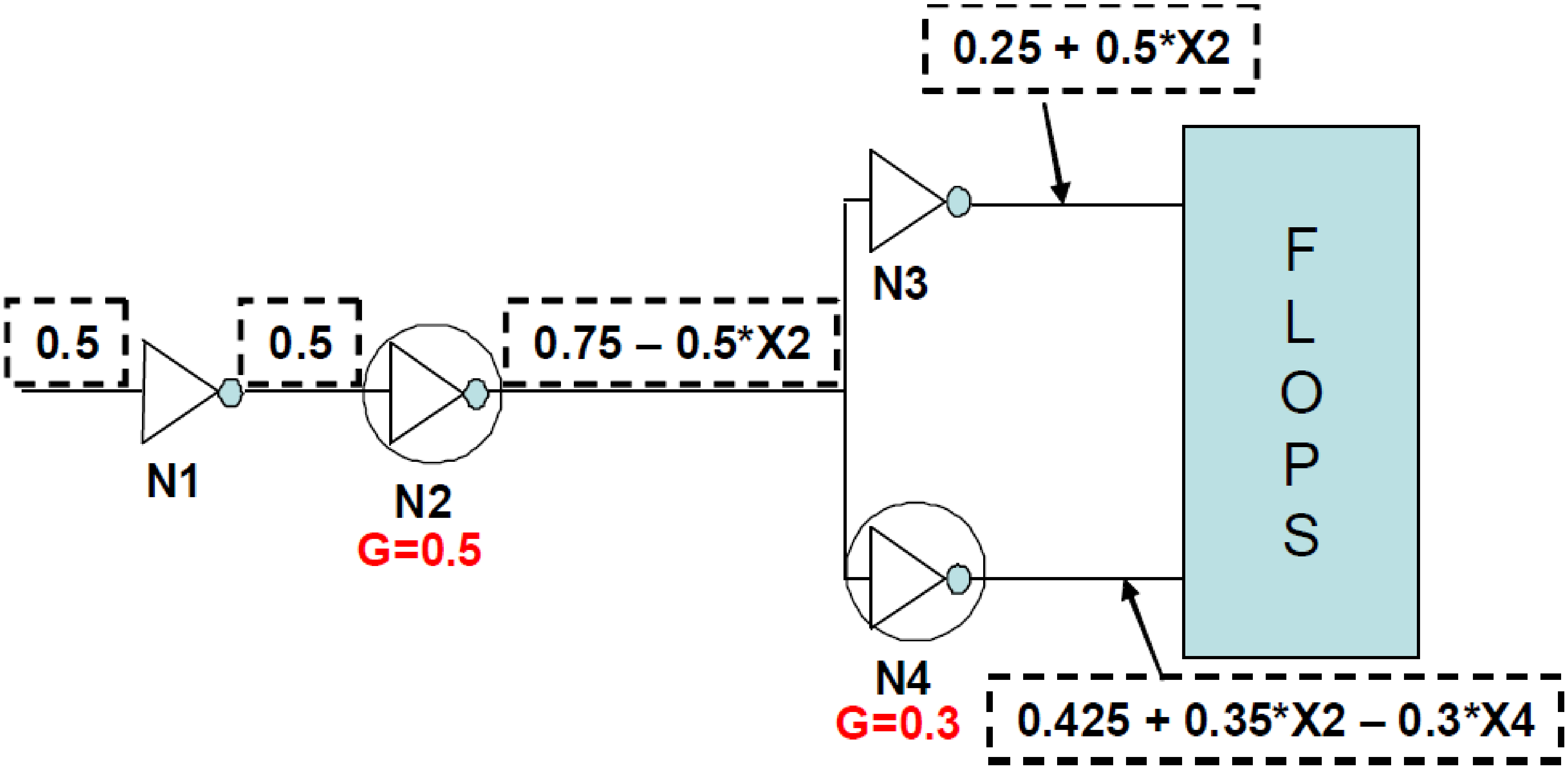


Propagate SP0 in Clock Tree

- For gating probability of G & input SP0 of S, output SP0 for NAND or NOR choice:

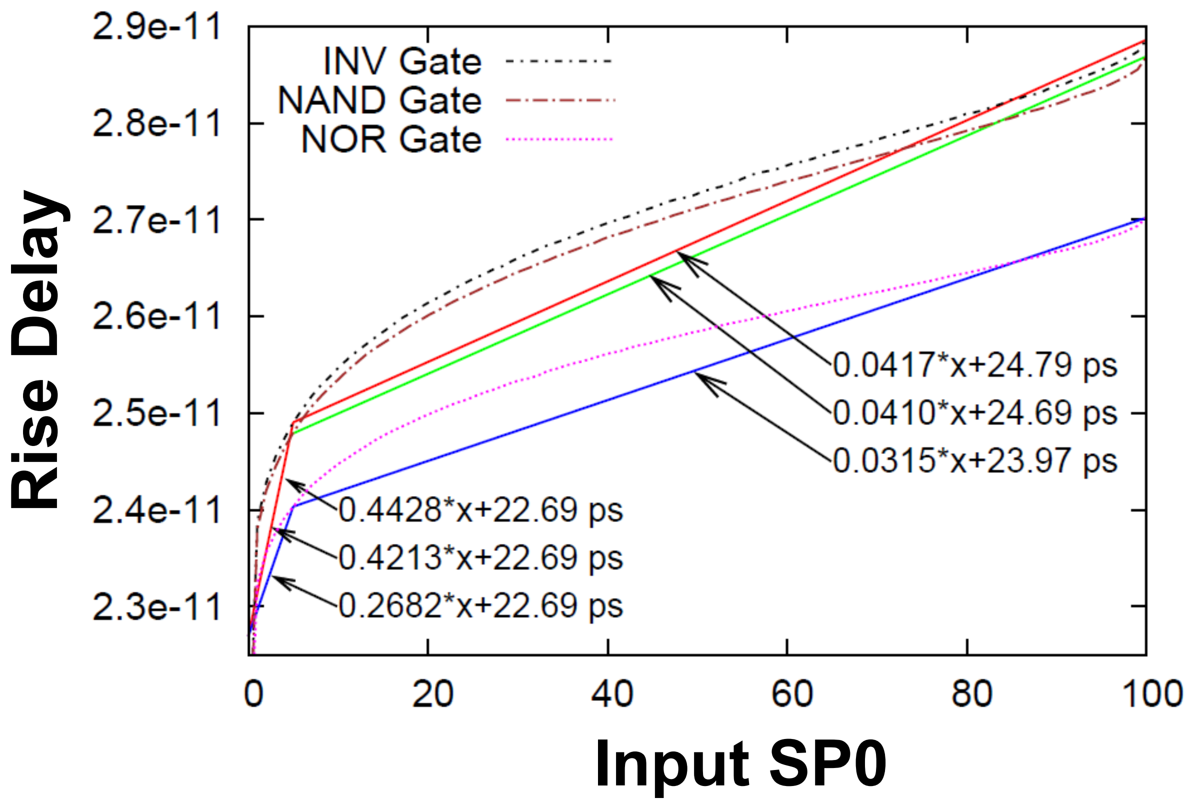


Example: SP0 Propagation

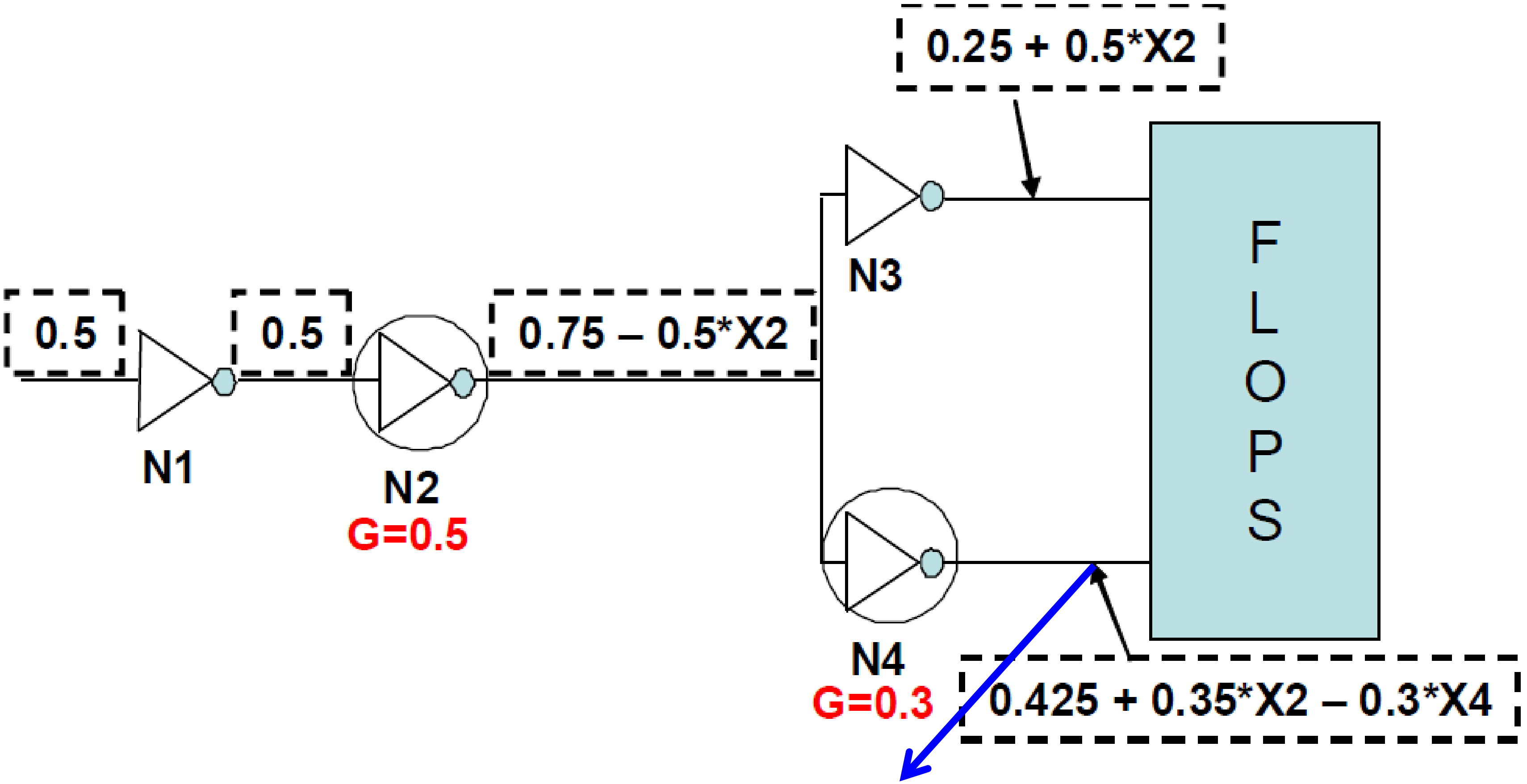


Delay Characterization

- NBTI impacts TRISE. TFALL unchanged
- TRISE characterization w.r.t. SP needed
- Conducted SPICE simulations to obtain



Example [Delay Expression]



DINV(0.5) +

X2 * DNAND(0.5) + X2’ * DNOR(0.5) +

(X4 * DNAND(0.72 - X2 * 0.5) + X4’ * DNOR(0.75 - X2 * 0.5))

Can the expressions of Delay and SP become unmanageable as we traverse down the clock tree?

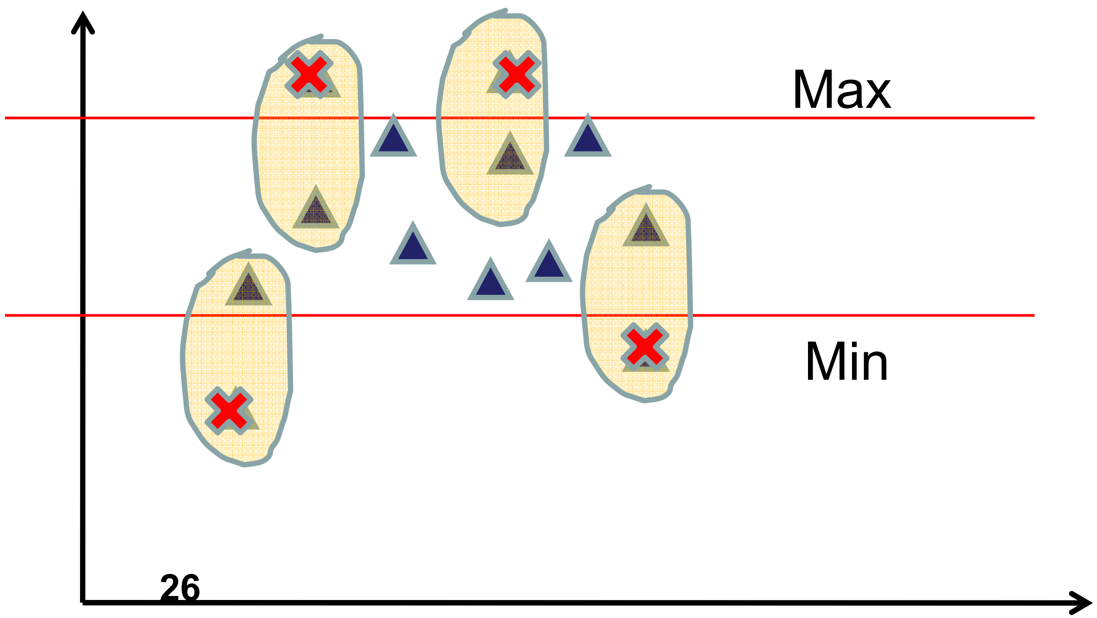
Like: X1*X2*X3'*X4*X6'…

Observations

- Lemma 1: SP0 of any gate is at most a linear function of Xi.
  - No multiplication of Xi in SP expression.
- Lemma 2: Delay expression is at most a quadratic function of Xi
  - X1*X2 possible. Not X1*X2*X3 etc.
- Thus, delay/SP0 expression remain only quadratic functions of Xi.
  - If Xi binary, quadratic => linear transformation

ILP Formulation

- Minimize: MAX – MIN   // Both dummy variables
- Subject To:
  - Arrival Time(Sink i) <= MAX for all i;
  - Arrival Time(Sink i) >= MIN for all i;
  - MAX >= 0;
  - MIN >= 0;
  - Xi = {0, 1}

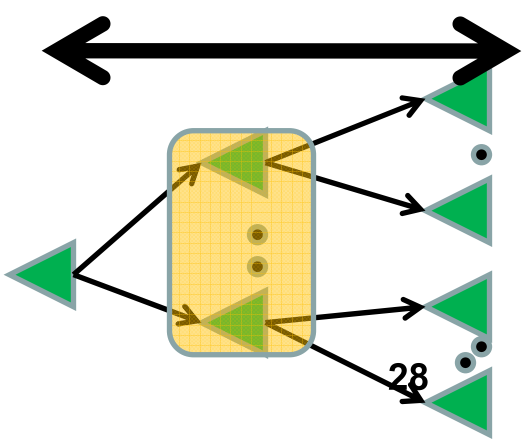


Experimental Setup

- Generated balanced clock trees (skew=0)
  - 9K to 350K sinks.
  - Buffers at all branching points
- Picked 2% of buffers as gating enabled
- Assign 20% ⇔ 70% gating probability
- Clock source input SP=0.5
- Spice netlist from 45nm Nangate library
- C++ for SP propagation & ILP writing
- Mathematica to reduce. CPLEX to solve.

Benchmarks

Name	Depth	Fanout	# Buffers	# Sinks	# Gated
A	7	4	22k	87k	331
B	8	3	10k	8k	144
C	9	3	29k	26k	426
D	8	4	88k	349k	1251
E	9	3	29k	26k	430
F	8	3	10k	9k	138
G	8	4	87k	349k	1267
H	7	4	22k	87k	326



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Results

- Age the circuit to 10 years

- Calculated skew for four cases
  - Choose NAND/NOR based on our formulation
  - Choosing all NAND gates
  - Choosing all NOR gates
  - Try 10 random assignment, pick best

Results (contd)

Name	Solver Time (s)	OUR Skew (ps)	All NAND (ps)	All NOR (ps)	10 Rand. (ps)
A	0.14	**2.80**	4.41	9.02	7.24
B	0.06	**2.18**	3.23	5.84	4.96
C	1.41	**4.13**	6.4	9.28	7.05
D	0.81	**3.03**	5.04	9.74	6.21
E	0.12	**2.76**	5.46	10.21	7.04
F	0.09	**3.94**	6.21	12.23	11.82
G	0.47	**3.88**	6.75	13.07	10.58
H	0.09	**2.59**	3.91	8.44	5.38
Avg:		1	**1.56X**	**2.19X**	**1.33X**

- Significantly tightens the skew budget

Conclusions

- Proposed choosing NAND/NOR gating at design time minimize skew degradation.
- Optimal (ILP) results show 55% and 120% lower skew than all NAND/all NOR cases.
- Random + pick best results reduce 20% and 80% over all NAND/all NOR cases.
- Fast. Log(n) binary variables.
- Future Works:
  - ILP is NP complete. Some other formulation.
  - How ICGs can be handled.

Thank you.

Questions?