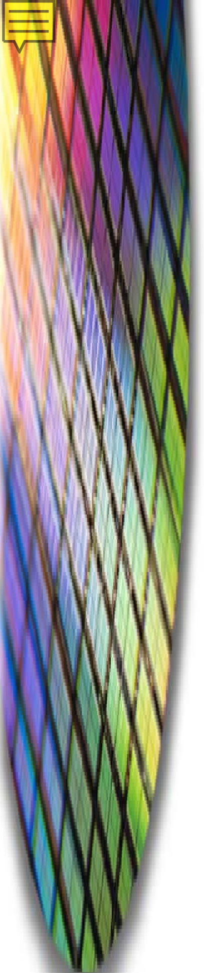

Total Sensitivity Based DFM Optimization of Standard Library Cells

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Outline

- Motivation
- Our Contribution
- Total Sensitivity
  - Device criticality based sensitivity
  - Lithography proximity induced sensitivity
  - Process variation induced sensitivity
- Total Sensitivity Based Layout Optimization
- Experimental Results
- Conclusions

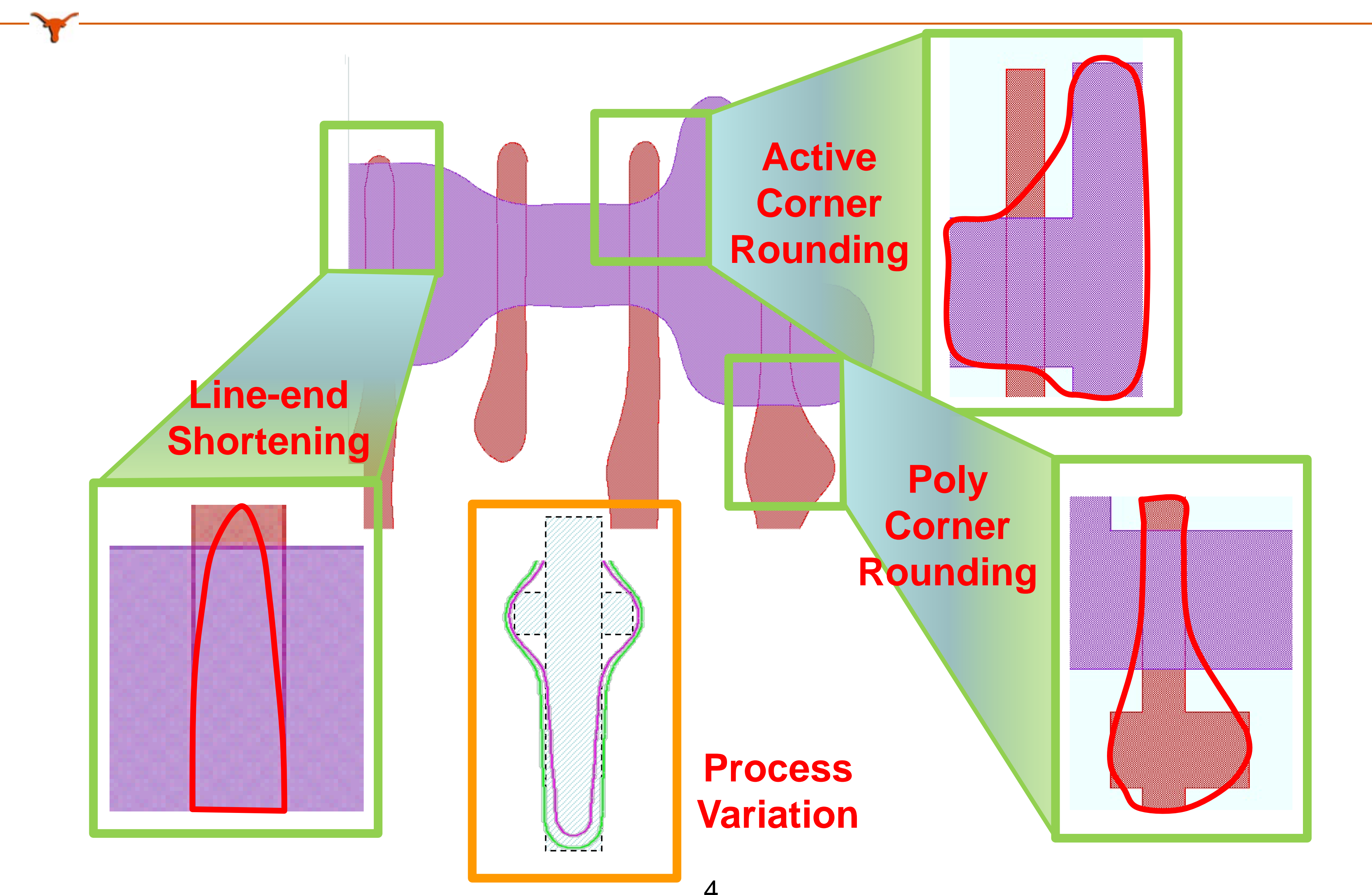
Current Lithography Challenges

10
[Courtesy Intel]
Lithography
Wavelength
365nm
248nm
1
193nm
um
0.1
Gap
130nm
90nm
65nm
Feature
Size
13nm
EUV
[Courtesy Intel, 2006]
1980 1990 2000 2010 2020

Rounding
Disappeara
-nce
Pinch,
Pullback

- Optical lithography (193nm) will continue for several years.
  - Immersion, RET (Resolution Enhancement Technique, e.g. OPC)
  - DPL (Double Patterning Lithography)
- Next Generation Lithography (e.g. EUV)
  - Economical/material/technical challenges

Gate Variation @Standard Cell



Impact of Gate Length Variation

- ΔL_{gate} is up to 10% @45nm node.

- The small improvement of ΔL_{gate} reduction can leads to significant decrease of delay and leakage variations.

Standard Cell Layout Optimization

- Since a lot of identical cells will be used repeatedly, any small changes can result in significant improvements.
- Restricted design-rules in industry [Choi'07 SPIE,Liebmann'09 SPIE]
  - Rule based and simple
  - Large number of rules and expensive rule checking
  - RDR is starting to fail in their attempt to use a discrete modeling approach on a continuous systems.
- Lithography model based optimization [Cote'04 ISQED,Tang'08 SPIE]
  - Robust layout for nominal lithography
  - No consider device criticality in circuit level
  - No single metric for both lithography proximity and process variation
- New model-based approach is needed.

Our Contributions

- Timing Criticality
  - The variation for a high sensitive device should be as small as possible.
- Process Criticality
  - Minimize the difference between fastest and slowest process corner
- Total Delay Sensitivity Modeling
  - Circuit Topological Delay Sensitivity
  - Lithography Proximity Induced Sensitivity
  - Process Variation Induced Sensitivity

➔ Delay, Leakage and Process Robust Layout

Device Criticality Based Sensitivity

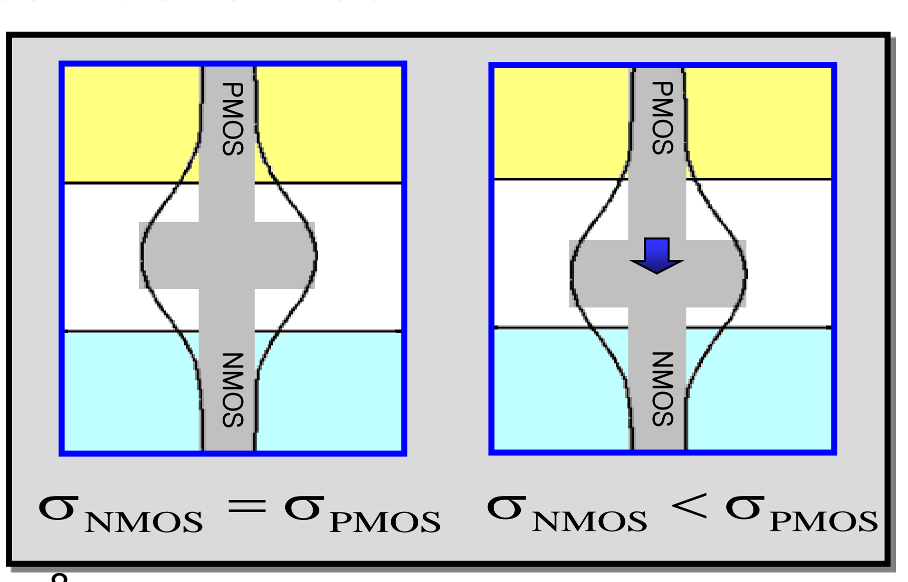
- Delay variation for the delay arc, α due to variation, ΔL_i :

$$\Delta d^{\alpha} = \sum_{i} \frac{\partial d^{\alpha}}{\partial L_i} \Delta L_i$$

- Total delay sensitivity index, Ψ:

$$\Psi = \sum_{\alpha} \omega^{\alpha} \cdot \Delta d^{\alpha} = \sum_{i} \sigma \cdot \Delta L_i$$

- The devices within the cell can be ranked.
- *Circuit induced sensitivity* ➔ *σ*



Lithography Proximity Sensitivity

- Transversal (ΔL_x) variation and Longitudinal (ΔL_y) variation
- ΔL_x: EPE as a function of Δe_x.

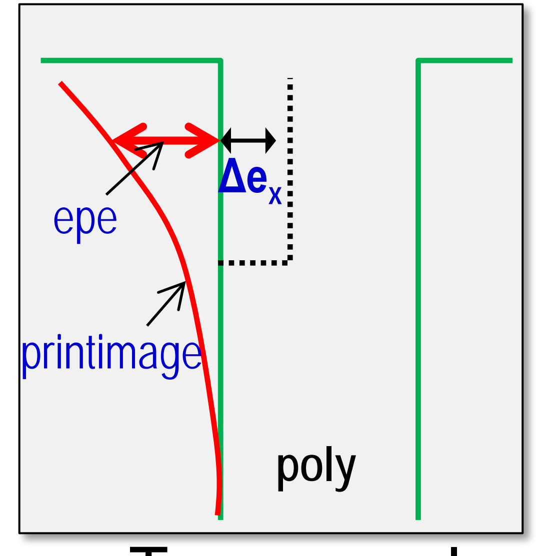
$$\Delta L_{x,i} = \frac{\partial L_{x,i}}{\partial e_{x,i}} \Delta e_{x,i}$$

- ΔL_y is changed from different conduction

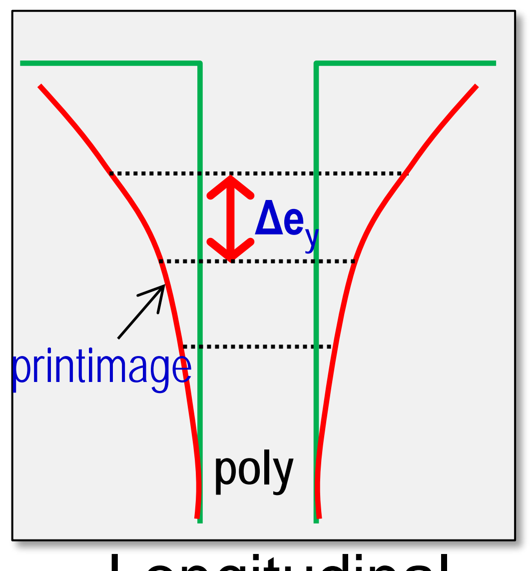
$$\Delta L_y = \frac{\partial L_y}{\partial e_y} \Delta e_y = \Delta L_i \quad \frac{\partial L_y}{\partial e_y} \propto f(\Delta L_x, \omega)$$

ω is a weighting factor of narrow width effect

- *Lithography proximity Induced sensitivity* ➔ γ



Transversal



Longitudinal

Process Variation Induced Sensitivity

- Dose and focus errors are the dominant sources

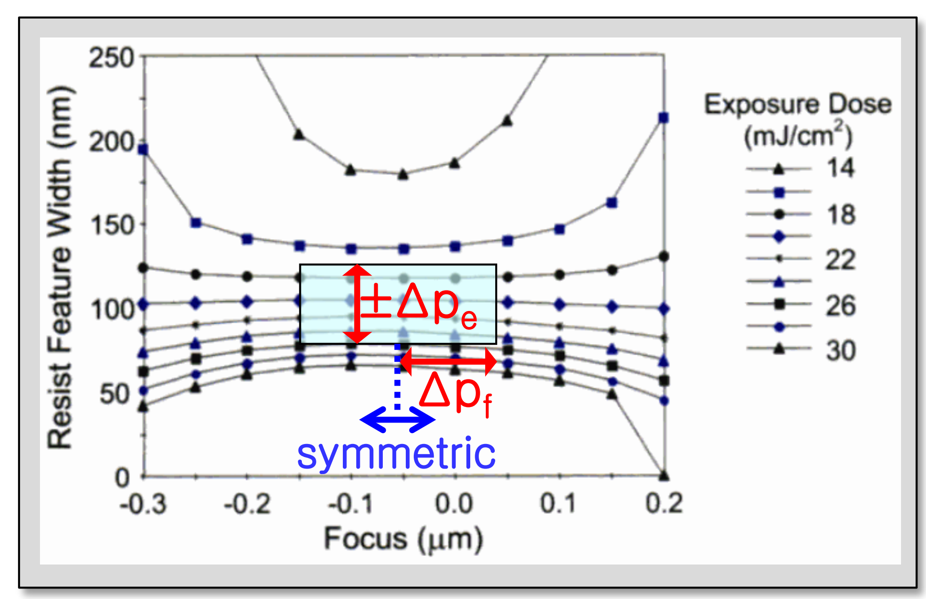
$$\Delta L = \frac{\partial L}{\partial \ln p_e} \% \Delta p_e + \frac{\partial^2 L}{\partial p_f^2} \Delta p_f^2$$

- Given focus level, Δp_f , ΔL can be simplified:

$$\Delta L = \left.\frac{\partial L}{\partial \ln p_e}\right|_{F_0} [1 + \alpha \cdot \Delta p_f^2] \cdot \% \Delta p_e$$

$$= \left.\frac{\partial L}{\partial \ln p_e}\right|_{\Delta p_f} \cdot \% \Delta p_e$$

- *Process induced sensitivity*
  η



Three Metrics of Sensitivity

- Device Criticality → σ

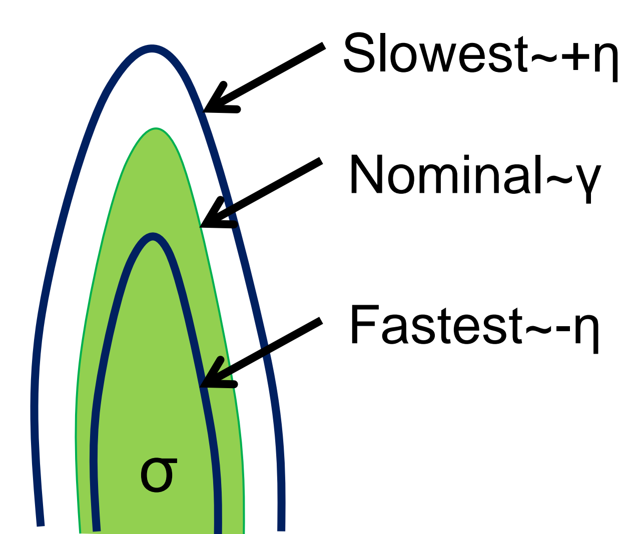
$$\Psi = \sum_i \sigma \cdot \Delta L_i$$

- Lithography Proximity Sensitivity → γ

$$\Delta L_i = \frac{\partial L_y}{\partial e_y} \Delta e_y$$

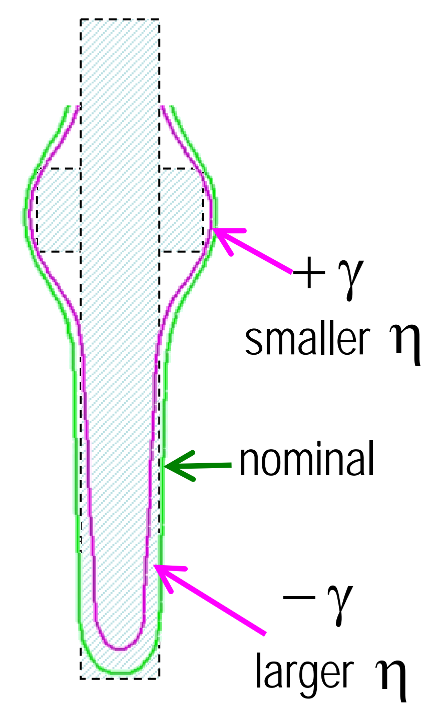
- Process induced sensitivity → η

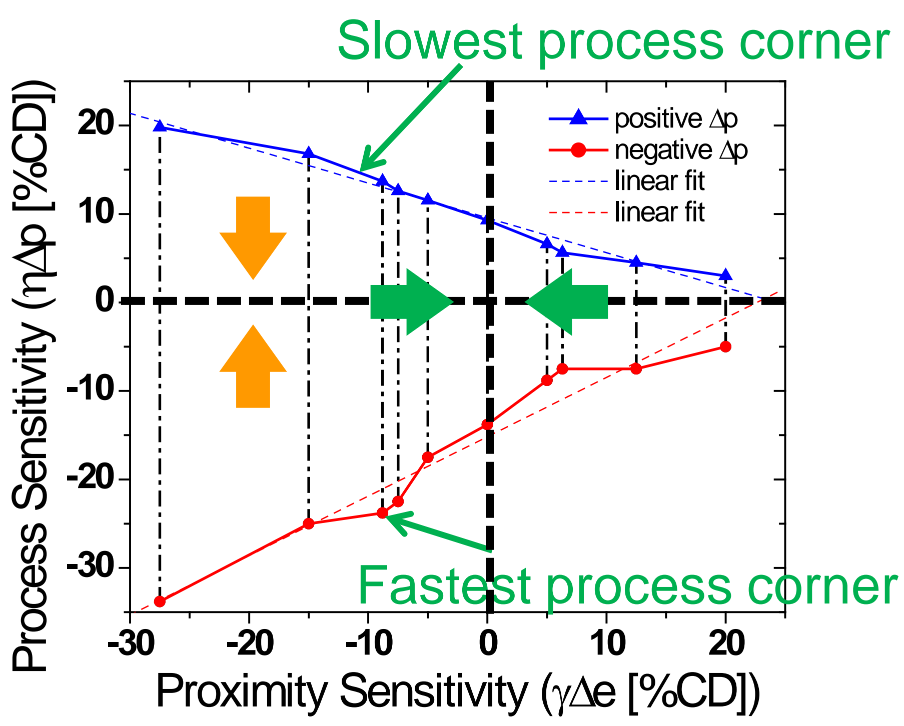
$$\Delta L_i = \left.\frac{\partial L}{\partial \ln p_e}\right|_{\Delta p_f} \cdot \pm\% \Delta p_e$$



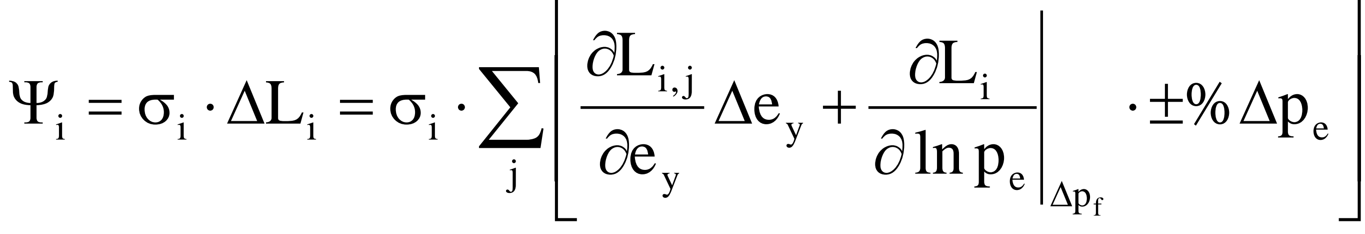
Correlation Between γ and η

- The process sensitivity (η) is highly correlated with the lithography proximity sensitivity (γ).
- Once γ is calculated, we can estimate η.
- We should minimize the process gap (Slowest - Fastest).





Total Sensitivity



$$\Psi_i = \sigma_i \cdot \Delta L_i = \sigma_i \cdot \sum_j \left[\frac{\partial L_{i,j}}{\partial e_y} \Delta e_y + \left. \frac{\partial L_i}{\partial \ln p_e} \right|_{\Delta p_f} \cdot \pm\% \Delta p_e \right]$$

$$= \sigma_i \cdot (\gamma_i + \eta_i)\Big|_{\Delta e_y, \pm\% \Delta p_e} \qquad \begin{cases} \sigma_i : device_criticality \\ \gamma_i : proximity_sensitivity \\ \eta_i : process_sensitivity \end{cases}$$

- Device criticality aware layout
- Process-robust layout

Poly / Active Layer Optimization

- Poly corner to active (**PCA**) → positive ΔL_{gate}
- Poly line-end (**PLE**) → negative ΔL_{gate}
- Active corner to poly (**ACP**) → positive ΔW_{gate}

PLE_P PCA_P PCA_N PLE_N PAct H_thk H_r NAct

PLE_P PCA_P PCA_N PLE_N H_thk H_ma

ACP_L ACP_R ΔWRL WRL

ACP_L ACP_R ΔWRL

Poly Layout Optimization

Active Layout Optimization

Poly Layer Optimization

- PCA shows a convex form (-1/√x) in our DRC range.
- PLE has a positive linear trend in a certain range.

$$\gamma_{ij} \geq a \cdot \sqrt{PCA_i} + b \cdot PLE_i + c \qquad \eta_{ij} \geq d \cdot \Delta p_i \cdot \gamma_{ij} + e$$

18
15
12
9
6
3
0
Normalized ΔL_{eff} [nm]
60
50
40
30
20
10
0
-10
Normalized Δd [%]
Normalized ΔL_{eff}
Convex fit
Normalized Δd
Convec fit
0 10 20 30 40 50 60 70
Distance (Poly PAD to Active) [nm]

PCA

-0.9
-1.2
-1.5
-1.8
Normalized ΔL_{eff} [nm]
-4
-5
-6
-7
-8
Normalized Δd [%]
Normalized ΔL_{eff}
Linear fit
Normalized Δd
Linear fit
6 9 12 15 18
Distance (Line-end to Active) [nm]

PLE

Poly Layer Optimization

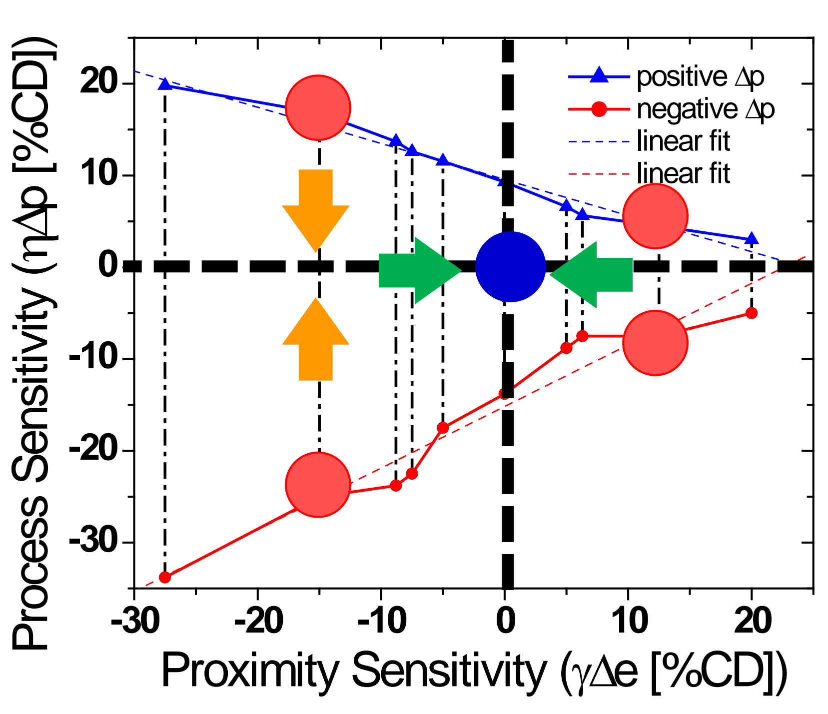
min: $\left|\Delta d_{ij,\max}\right| + \left|\Delta d_{ij,\min}\right|$

s.t.: $\Delta d_{ij,\max} \geq \sigma_i \sum_{j \in S(i)} (\gamma_{ij} + |\eta_{ij}|)\Big|_{\Delta e_y, \% \Delta p}$

$$\Delta d_{ij,\min} \leq \sigma_i \sum_{j \in S(i)} (\gamma_{ij} - |\eta_{ij}|)\Big|_{\Delta e_y, \% \Delta p}$$

$$\gamma_{ij} \geq a \cdot \sqrt{PCA_i} + b \cdot PLE_i + c$$

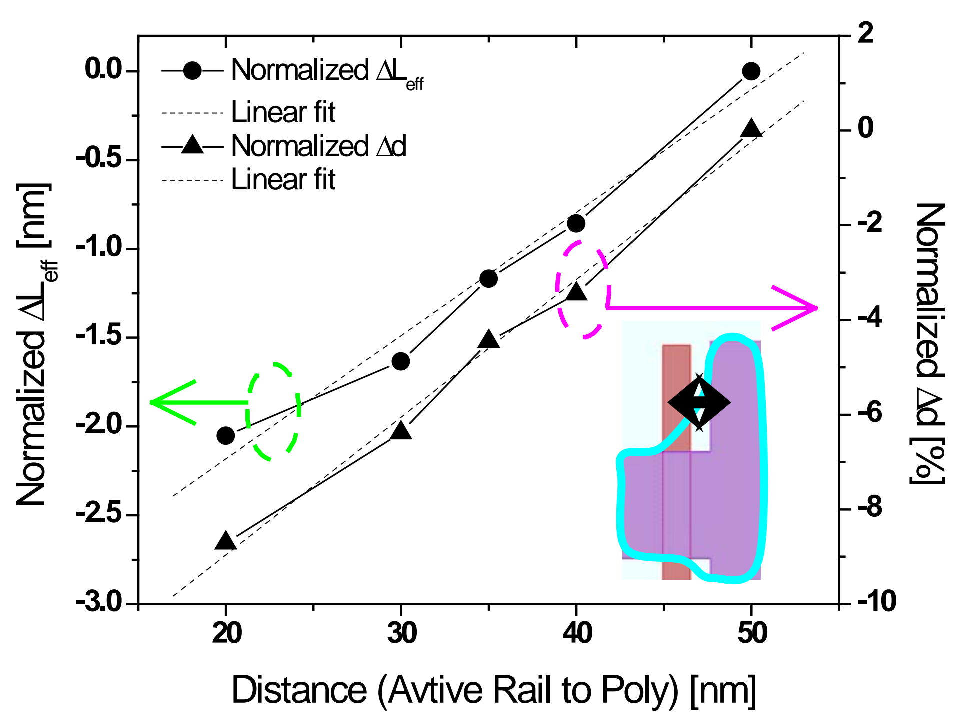
$$\eta_{ij} \geq d \cdot \Delta p_i \cdot \gamma_{ij} + e$$



- The objective is to minimize the maximal delay variation.
- Since γ_{ij} is convex, we can obtain optimal PCA and PLE.

Active Layer Optimization

- ACP has a positive linear trend with the distance of active corner to poly.



min: $\Delta d_{ij,\max} \geq \sigma_i \sum_{j \in S(i)} \gamma_{ij} \Big|_{\Delta e_y}$

s.t.: $\gamma_{ij} \geq a \cdot ACP_i + b$

- The objective is to minimize gate proximity.
- γ_{ij} is linear, we can obtain optimal ACP.

Overall Flow

Schematic

Statistical Characterization

Device Criticality σ_i,

Layout

OPC/Lithography

Total Sensitivity

$\sigma_i \cdot (\gamma_i + \eta_i)\big|_{\Delta e_y, \% \Delta p}$

Convex Formula

Poly Optimization

Linear Formula

Active Optimization

Layout Extraction

Cell Characterization

Experiment Results: Setup

- Impletemeted in Tcl/Perl
- Industrial 45nm ASIC designs
- Calibre-WB for model based OPC/Litho
- H-Spice for timing/characterization
- Two Layout Optimizations
  - Conventional restricted design rule (RDR) approach (CONV)
  - Total sensitivity based layout optimization (TSDFM)

Delay Variation

- Δdelay @best process is relatively low (around 3%)
- Up to 24% reduction in the delay difference between the fastest and the slowest process corner.

* Average delay for entire cells

Leakage Variation

- The local maximum leakage is decreased up to 91.9% in a cell and as much as 57.5% on average.
- Despite the small improvement of ΔL, we can see the huge amount of improvement on leakage current.

Cell	ΔL	Leakage	ΔL	Leakage	Improve
	CONV		TSDFM		%
C1	-2.26	2.289E-08	-1.27	5.407E-09	85.12
C2	-1.28	5.434E-09	-0.94	4.619E-09	26.45
C3	-1.83	6.747E-09	-1.19	5.203E-09	35.13
C4	-2.90	3.082E-08	-1.08	4.940E-09	90.91
C5	-1.43	5.789E-09	-1.33	5.546E-09	7.07
C6	-1.86	6.808E-09	-0.54	3.639E-09	71.12
C7	-2.03	2.002E-08	-1.78	6.630E-09	75.78
C8	-2.76	2.917E-08	-1.18	5.178E-09	89.46
C9	-2.29	2.332E-08	-1.54	6.046E-09	82.38
C10	-2.79	2.945E-08	-2.54	2.637E-08	11.37

Conclusions

- Total sensitivity (device criticality, nominal lithography proximity, process variation)
- The process sensitivity is highly correlated with the lithography induced sensitivity.
- Optimization is done by reducing the gap between the fastest and slowest delay corner. (up to 25% reduction of Δdelay and 92% decrease of leakage)
- Future works
  - Metal proximity & interconnect optimization
  - S/D contact optimization

Acknowledgments

- This work is supported in part by SRC, NSF CAREER Award, and equipment donations from Intel.

Back-up slide

- Delay variation for the delay arc, α due to variation, ΔL_i :

$$\Delta d_i = \frac{\partial d}{\partial L_i} \Delta L_i \quad \Rightarrow \quad \Delta d^{\alpha} = \sum_i \frac{\partial d^{\alpha}}{\partial L_i} \Delta L_i$$

- Total delay sensitivity index, Ψ:

$$\Psi = \sum_{\alpha} \omega^{\alpha} \cdot \Delta d^{\alpha} = \sum_i \sum_{\alpha} \omega^{\alpha} \cdot \frac{\partial d^{\alpha}}{\partial L_i} \Delta L_i = \sum_i \sigma \cdot \Delta L_i$$

- The devices within the cell can be ranked.
- *Circuit induced sensitivity* ➔ *σ*

Device → ↓ Delay Arc	N_1	N_2	P_1	P_2
$A(r) \rightarrow X(f)$	$\sigma^1_{N_1}$	$\sigma^1_{N_2}$	$\sigma^1_{P_1}$	$\sigma^1_{P_2}$
$B(r) \rightarrow X(f)$	$\sigma^2_{N_1}$	$\sigma^2_{N_2}$	$\sigma^2_{P_1}$	$\sigma^2_{P_2}$
$A(f) \rightarrow X(r)$	$\sigma^3_{N_1}$	$\sigma^3_{N_2}$	$\sigma^3_{P_1}$	$\sigma^3_{P_2}$
$B(f) \rightarrow X(r)$	$\sigma^4_{N_1}$	$\sigma^4_{N_2}$	$\sigma^4_{P_1}$	$\sigma^4_{P_2}$
Device Criticality Metric, γ_i	$\sum_\alpha \sigma^\alpha_{N_1}$	$\sum_\alpha \sigma^\alpha_{N_2}$	$\sum_\alpha \sigma^\alpha_{P_1}$	$\sum_\alpha \sigma^\alpha_{P_2}$

< NAND2 case study >