IBM Research

ITOP: Integrating Timing Optimization within Placement

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Timing-driven Placement

Timing closure – primary objective of an automated physical synthesis tool

- **Objective**
  - Minimize critical path delay and overall timing within a physical synthesis framework
- **How is it Done?**
  - Path delays dominated by interconnect delays
  - Minimize critical path delay by minimizing the critical net/path wire length

Previous Work

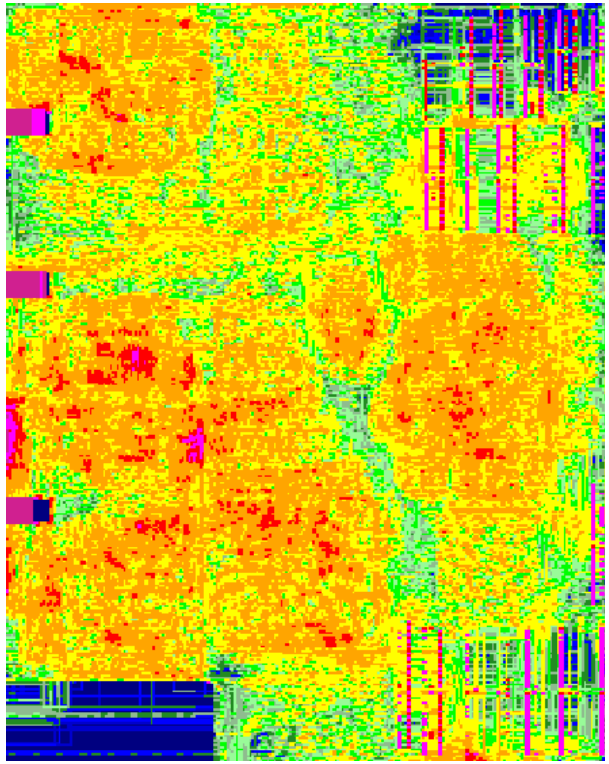
- **Global Timing-driven Placement**
- **Incremental Timing-driven Placement**

Global Timing-driven Placement

- **Global Placement using net constraints**
  - Minimize wire length of the “nets” on the critical paths
  - Implicit delay minimization via net length minimization

- **Key Approaches:**
  - Net-weights
    - Weight nets on critical paths for placement
  - Net-length Constraints
    - Constrain net lengths during placement

Global TDP: Key Drawbacks

Initial Placement	Coarse Timing Optimization	Timing-driven Placement
		
Wire Length (xe6)		
140.29 (1.00)	**146.94 (1.05)**	**160.10 (1.14)**

Global TDP: Key Drawbacks

No interaction with timing optimization transforms (buffering, gate sizing, etc.,)

Net Constraints

- **How much / how many?**
- **Remain static during placement**
- **Invalidated due to placement changes**
- **Dynamic regeneration may lead to oscillations**

Incremental Timing-driven Placement

- **Incremental Placement Using Path Smoothing**
  - Directly optimize critical paths in the design

- **Key Approach:**
  - Model the physical properties during placement
    - gate delay, interconnect delay, etc.,
  - Use mathematical programming to perform placement
  - Mostly use Linear Programming

Incremental TDP: Key Drawbacks

Inaccurate or crude delay models

Computationally intensive mathematical programming

Limited scope in terms of the number of paths

Ignore module overlap constraints when solving the mathematical program

Do not explicitly model placement blockages

Cannot handle other issues like placement congestion

ITOP: **I**ntegrating **T**iming **O**ptimization within **P**lacement

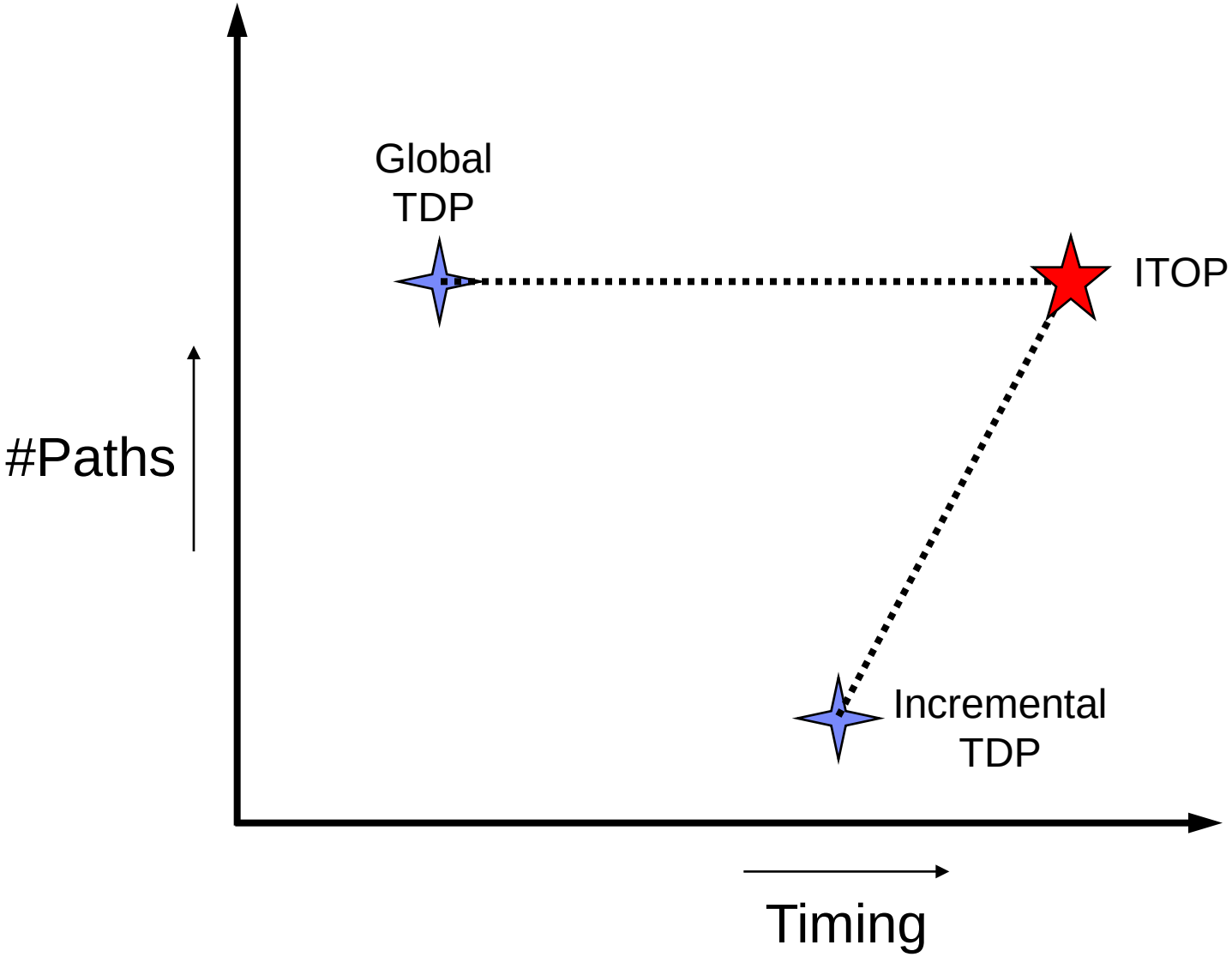
Effectively integrates timing optimization
and static timing analysis into placement

Incremental Timing-driven Placement

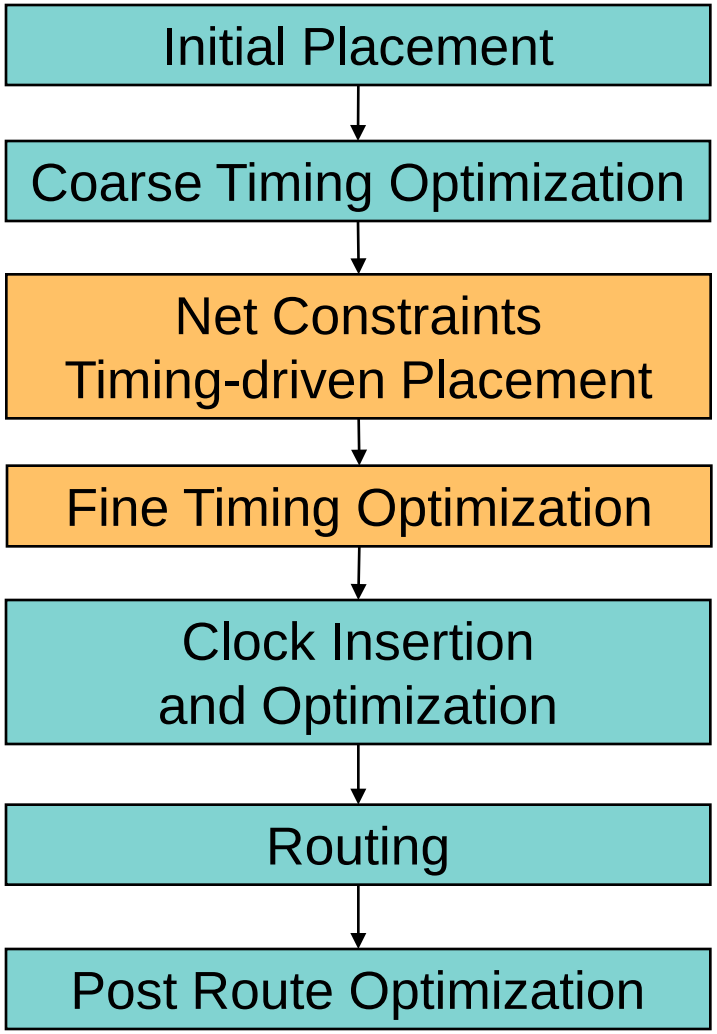
- Incremental blockage-aware critical path smoothing
- Incremental timing optimization (buffer insertion, gate sizing)
- Congestion mitigation and wire length recovery
- Slack Histogram Compression

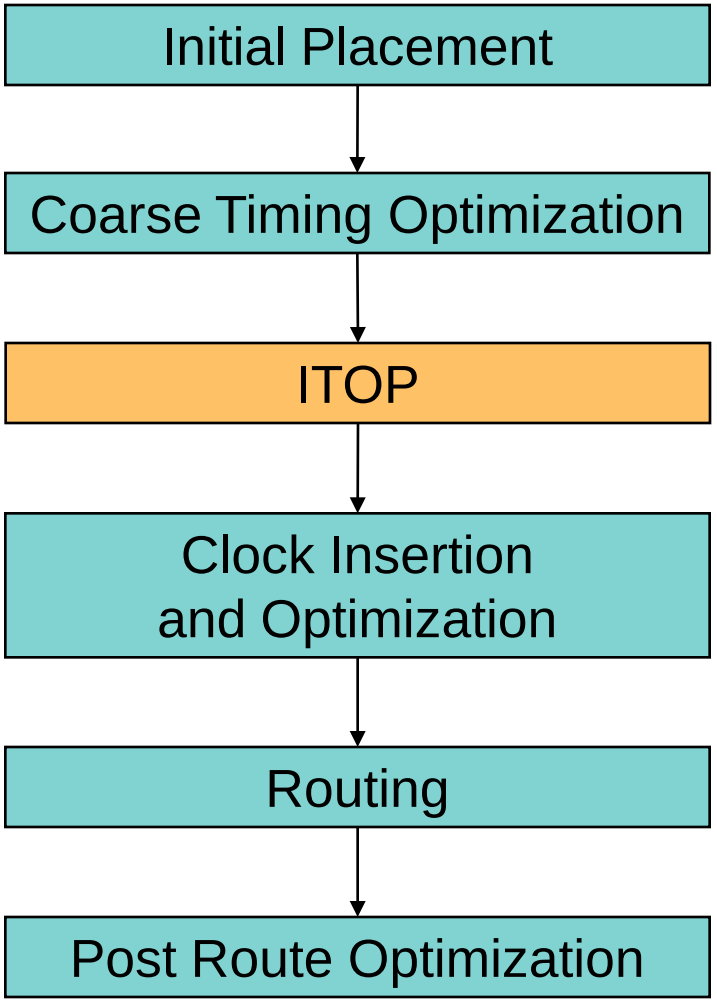
Gradually improve circuit timing without
degrading wire length and routability

Scope vs. Solution Quality

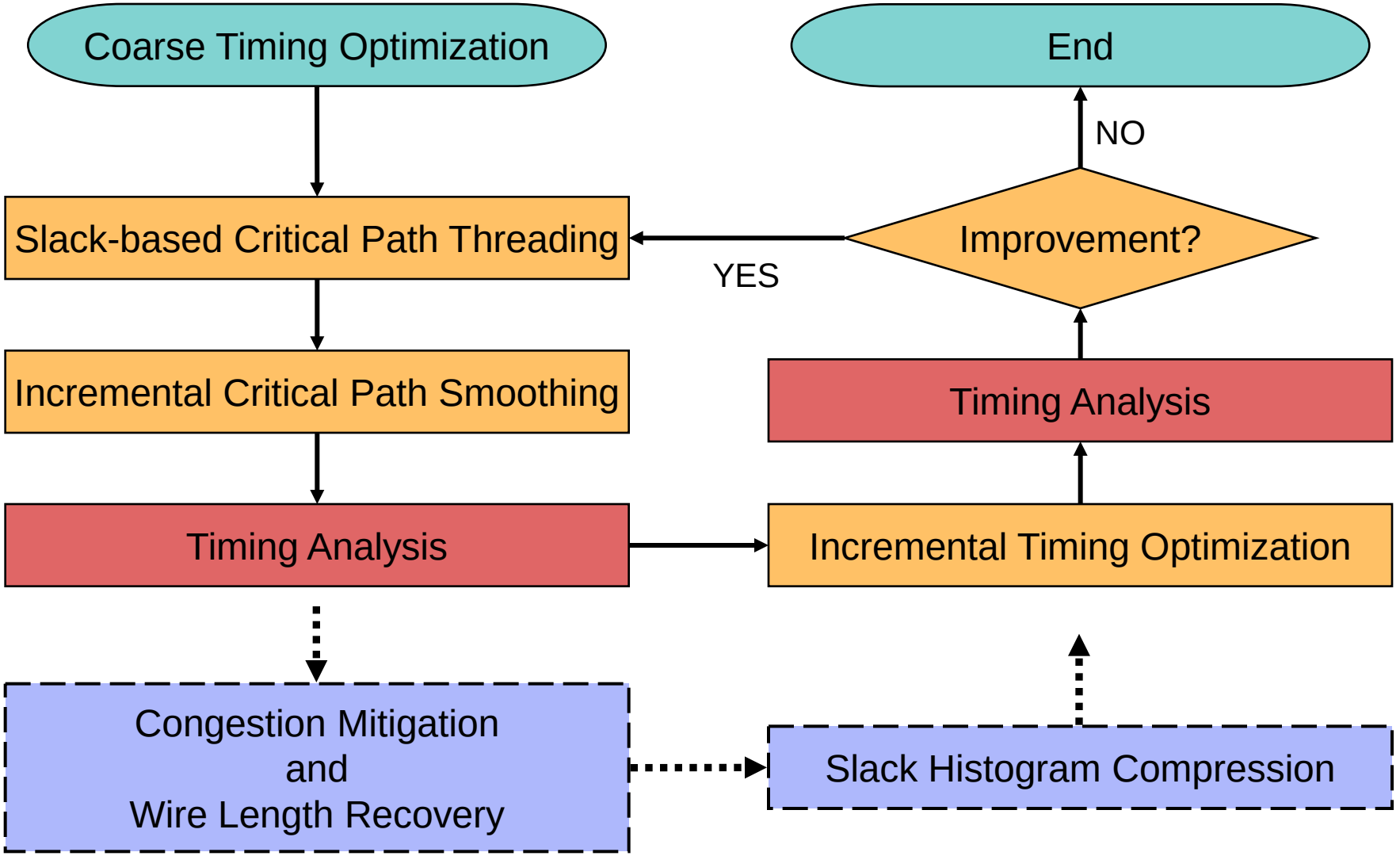


Physical Synthesis Flow: Traditional vs. ITOP

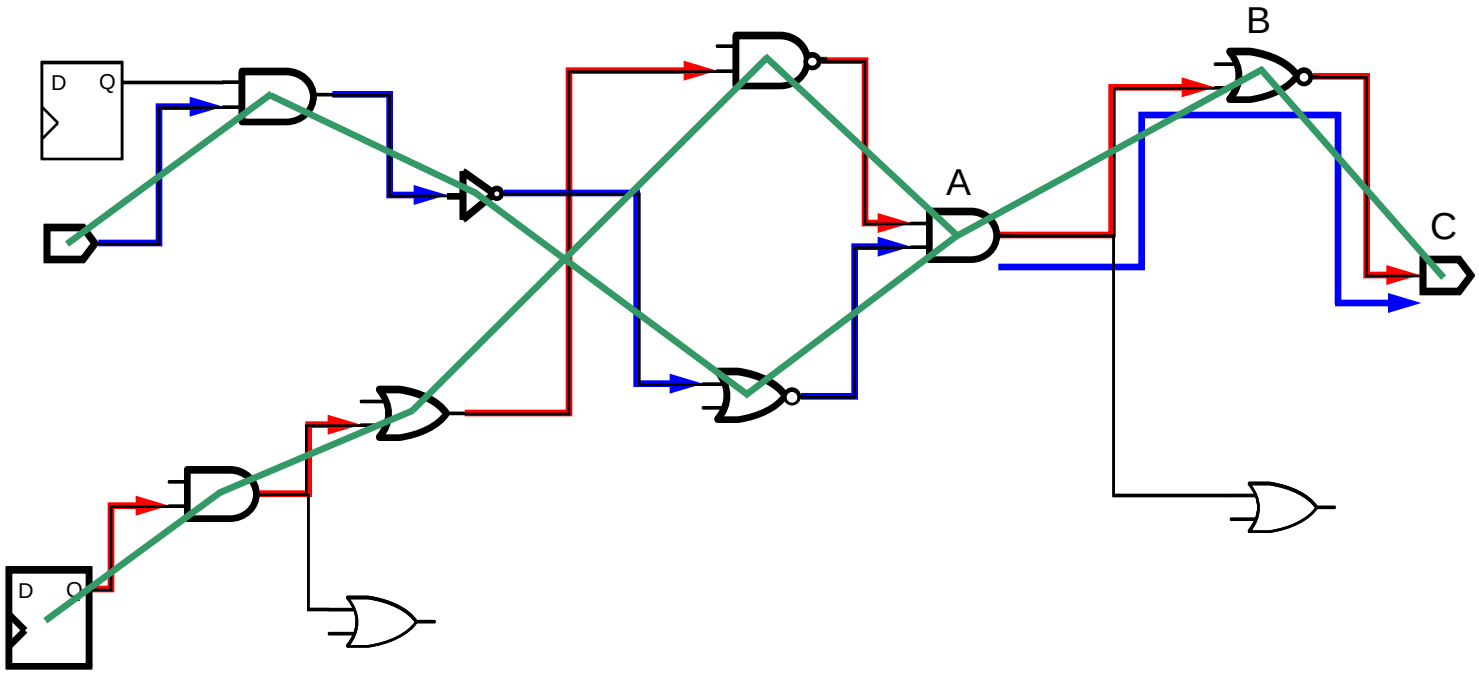




ITOP: High-level Flow



Slack-based Critical Path Threading



- **Components and interconnects in bold represent critical paths**
- **Create additional two-pin nets linking the components on the critical paths**
- **Assign a “high” net-weight on these two-pin nets**

Incremental Critical Path Smoothing

Move the top-most timing critical modules

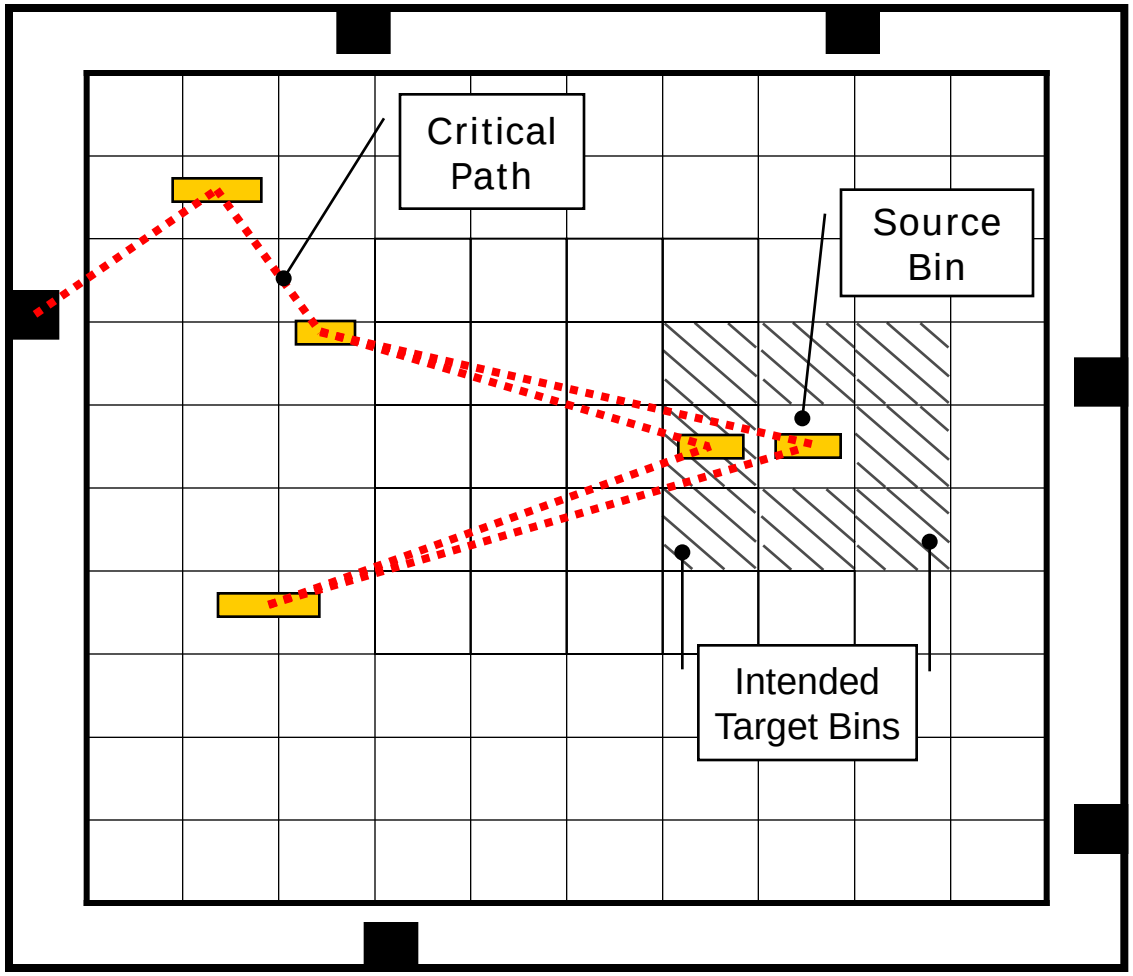
Greedy heuristic for module movement
- **Local iterative movement of the modules**

Movement score: Weighted quadratic wire length

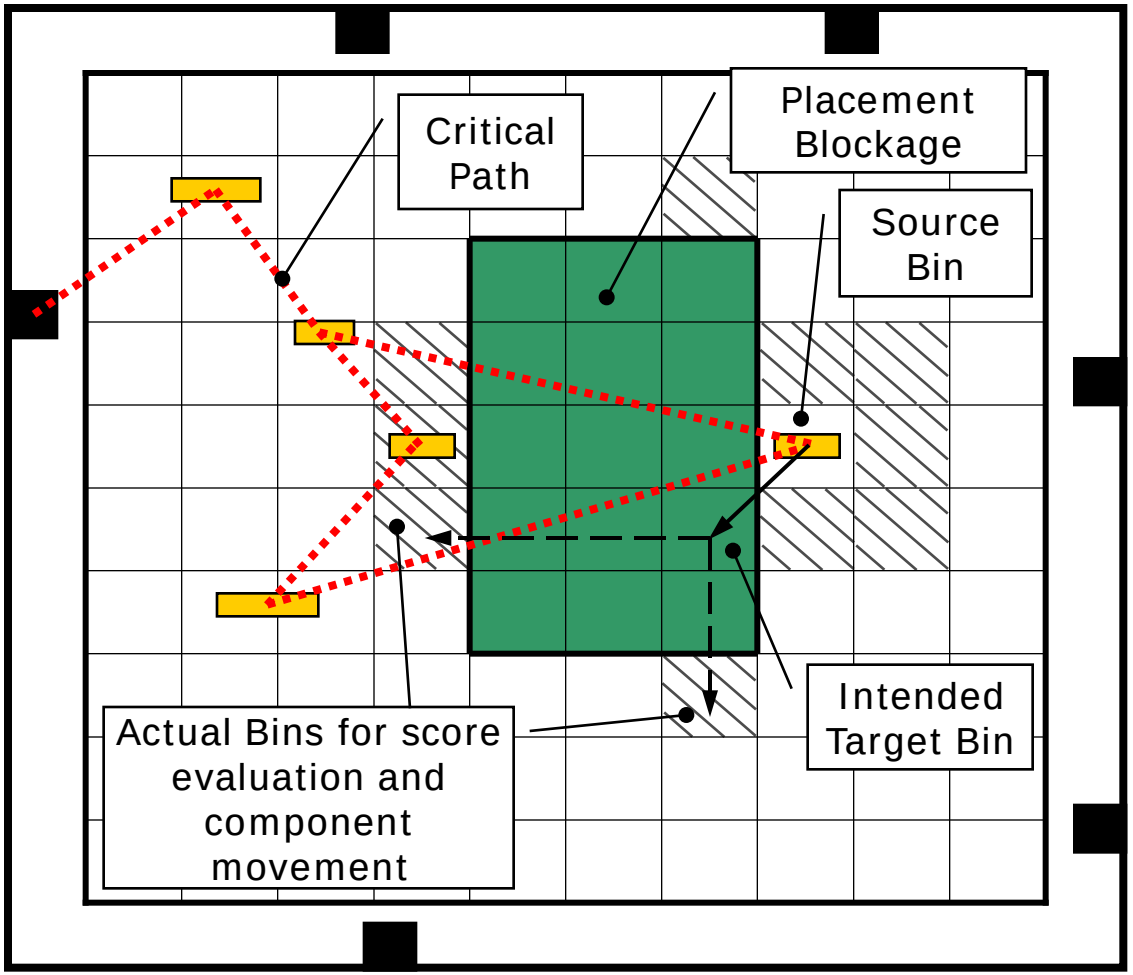
Displacement threshold to limit module movement

Consider blockages during movement (tunneling)

Incremental Critical Path Smoothing: Example

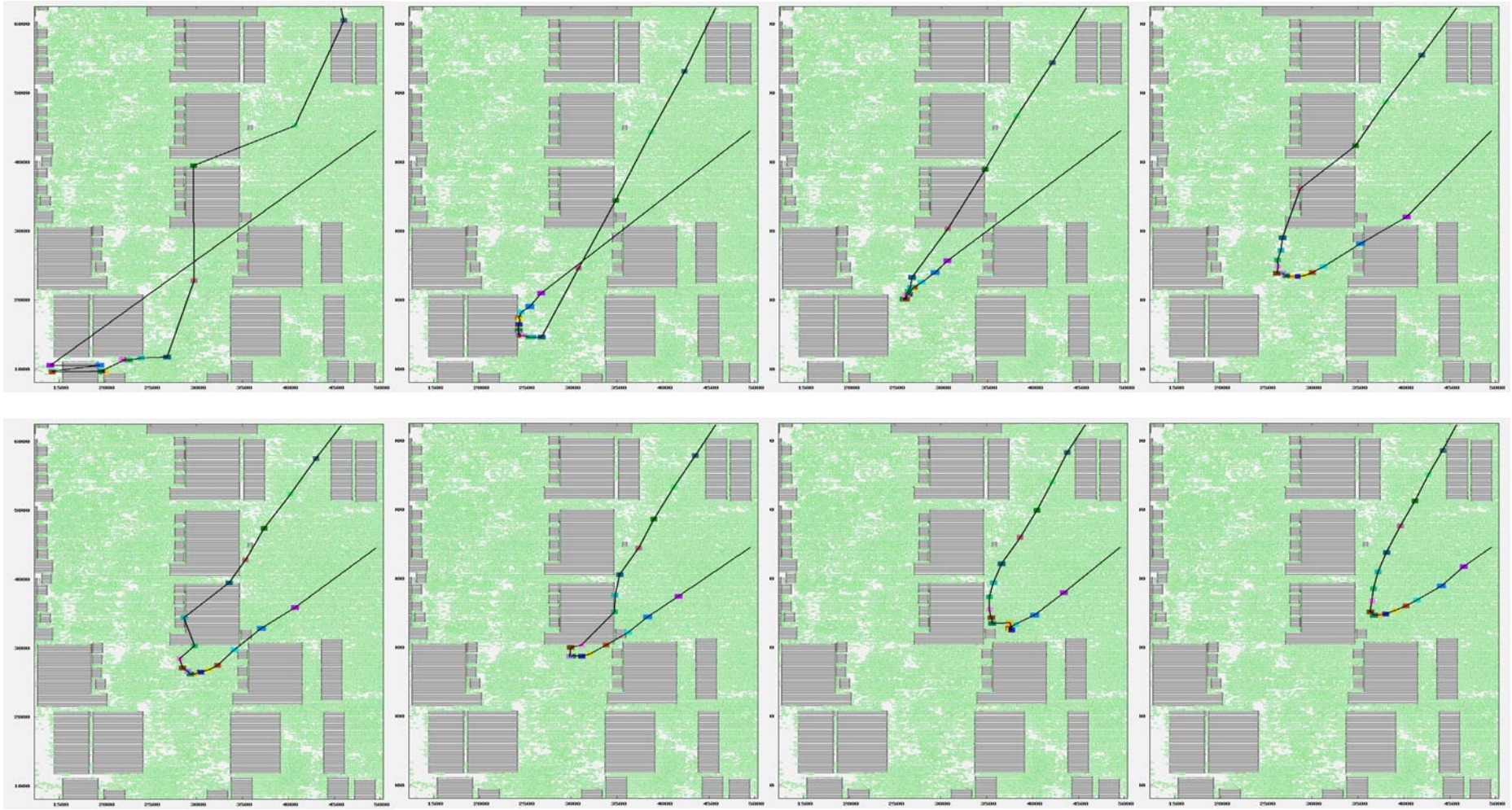


Tunneling to Handle Placement Blockages



Incremental Critical Path Smoothing

Initial

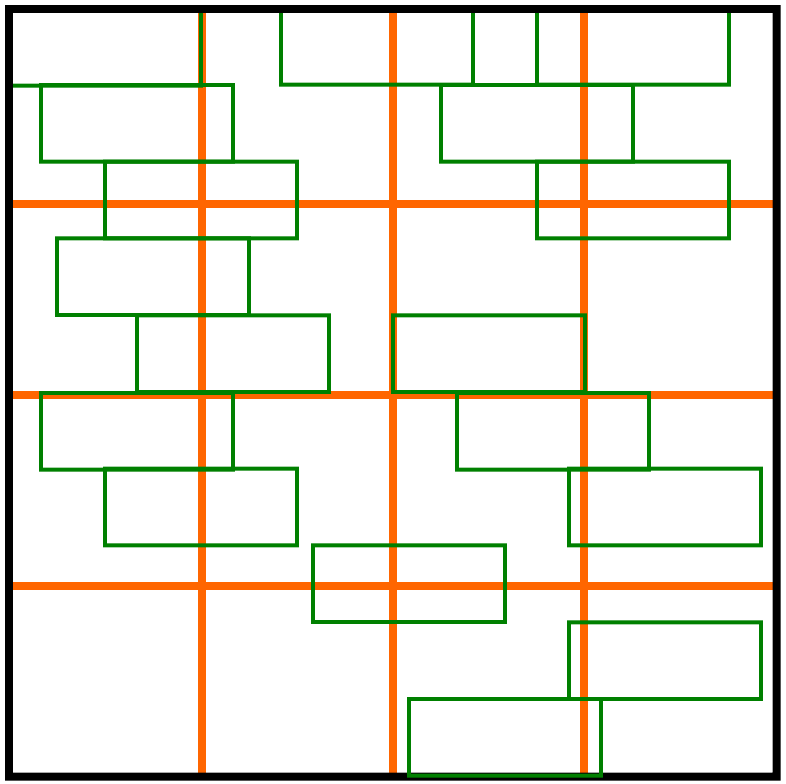


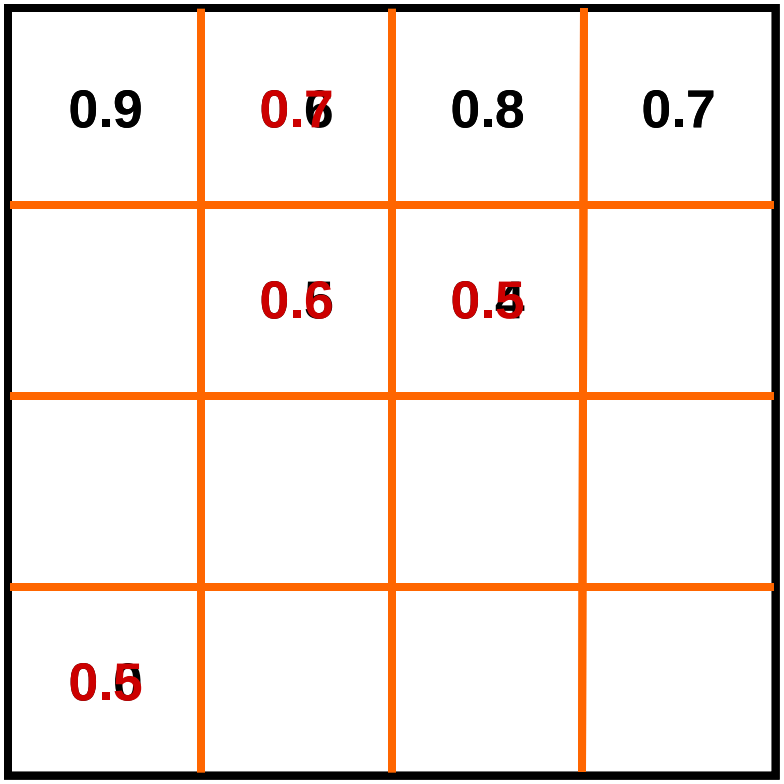
Final

Incremental Timing Optimization

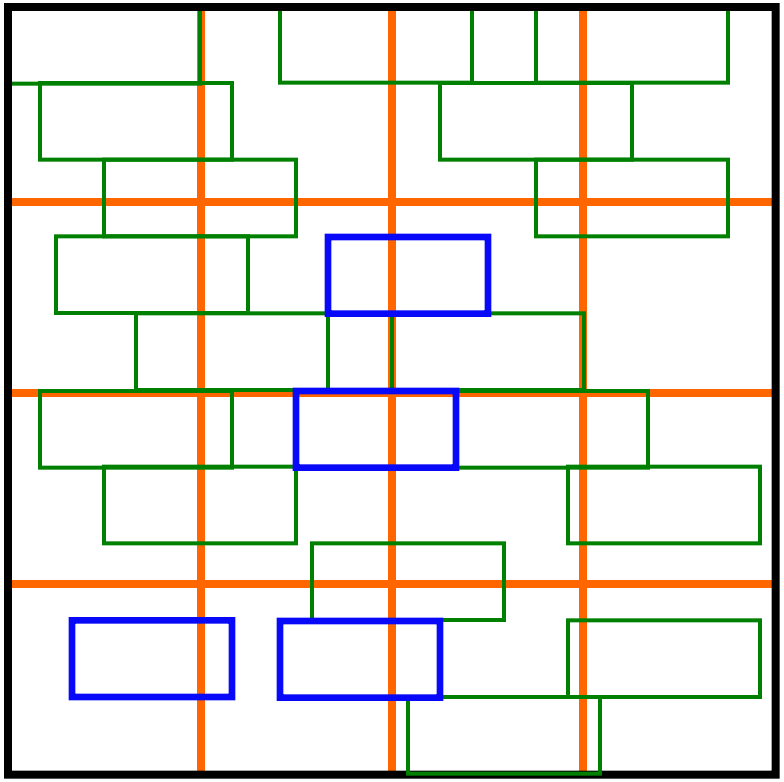
- **Timing analysis to determine the negative paths after placement**
- **Consider only a subset of the negative paths in the design (critical paths)**
- **Quick buffer insertion and gate sizing to improve timing on the critical paths**
- **Flexible to use other transforms**
  - multi-threshold vt tuning, wire sizing, layer assignment

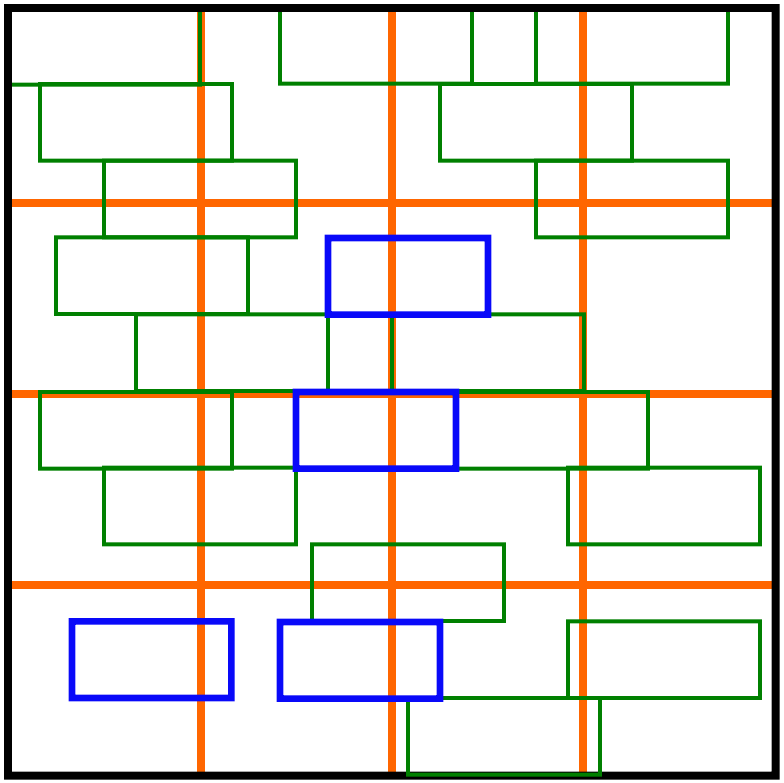
Congestion Mitigation





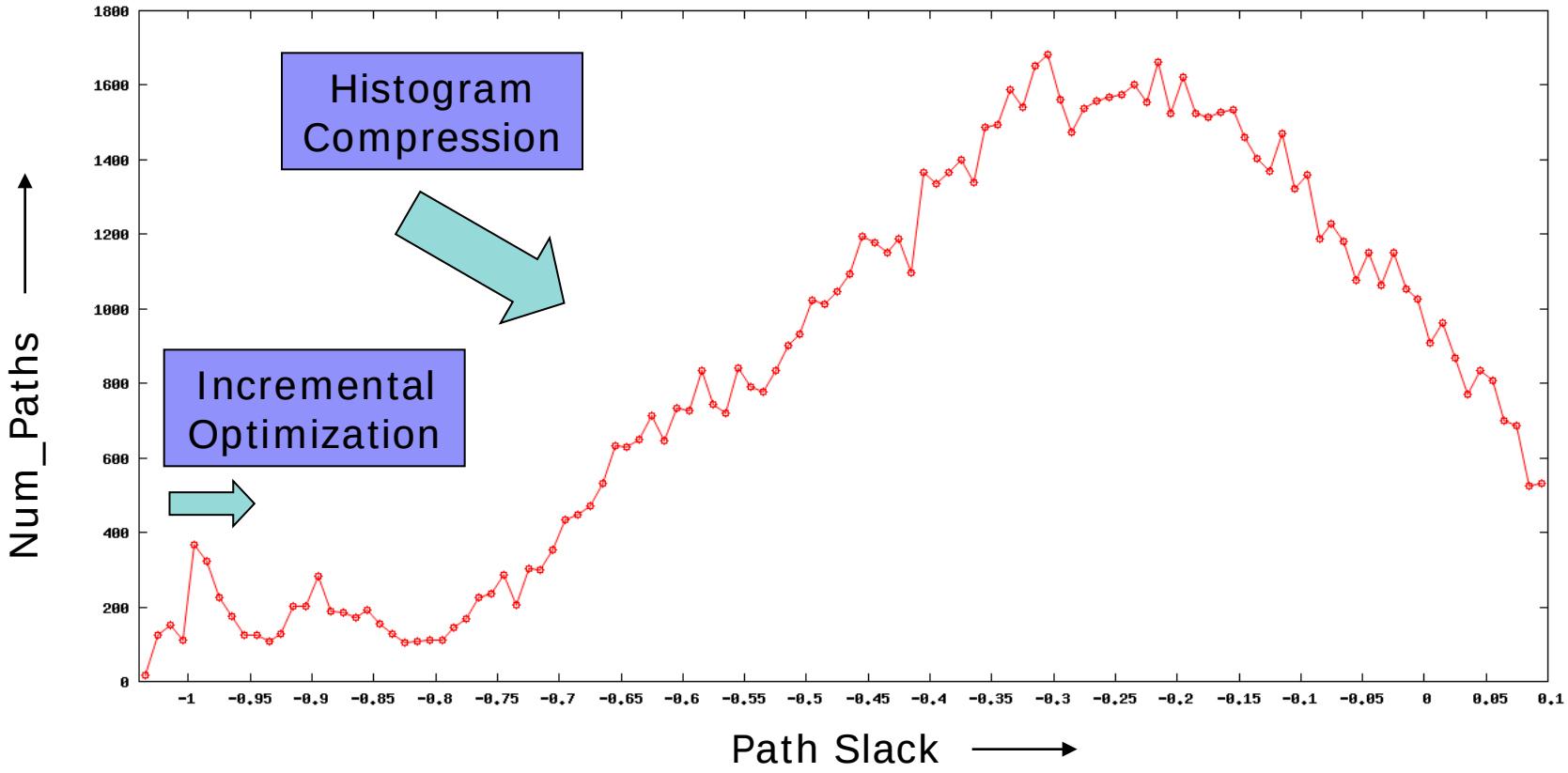
Congestion Mitigation





Slack Histogram Compression

- **Timing optimization on a larger set of paths in the design**



Experimental Setup

- **Implemented within the IBM Placement Driven Synthesis tool**
- **Benchmark Designs: High performance 65nm and 45nm industrial designs**

Circuit	Modules	Nets
ckt_1	77K	61K
ckt_2	102K	104K
ckt_3	142K	145K
ckt_4	171K	176K
ckt_5	260K	269K
ckt_6	298K	313K
ckt_7	433K	441K
ckt_8	451K	465K
ckt_9	476K	490K
ckt_10	554K	562K
ckt_11	951K	961K
ckt_12	1034K	1056K

Effect of Placement During ITOP

Worst-Slack vs. Iteration

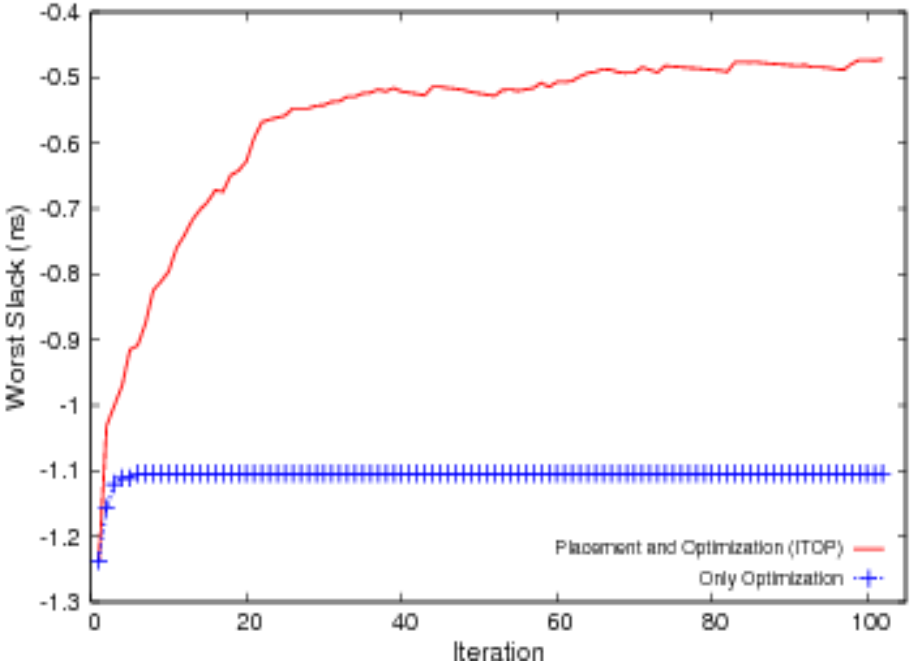
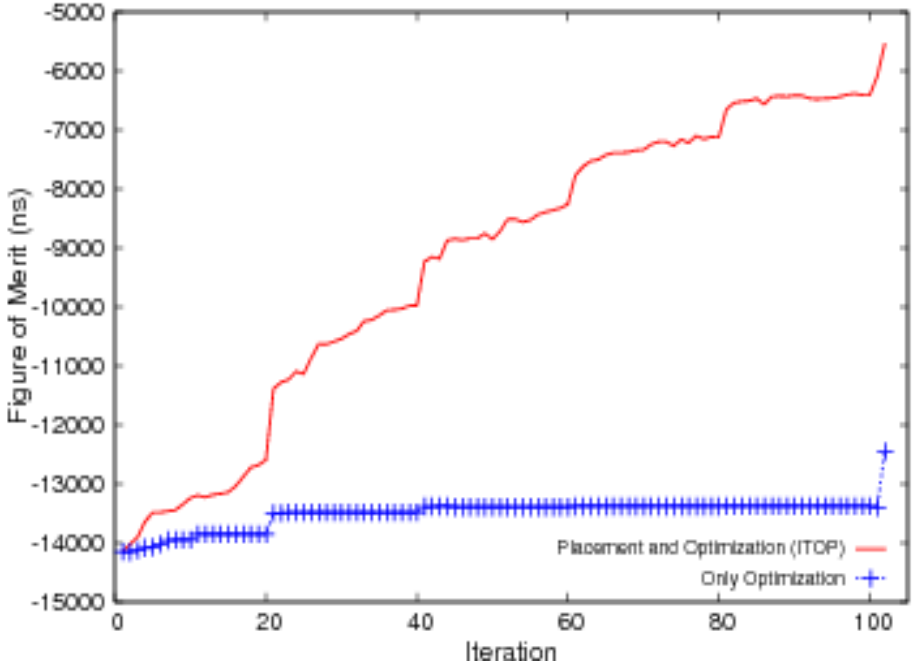


Figure of Merit vs. Iteration



- **Incremental placement is essential**
  - To improve overall timing
  - Prevent optimization from getting stuck in a local minima

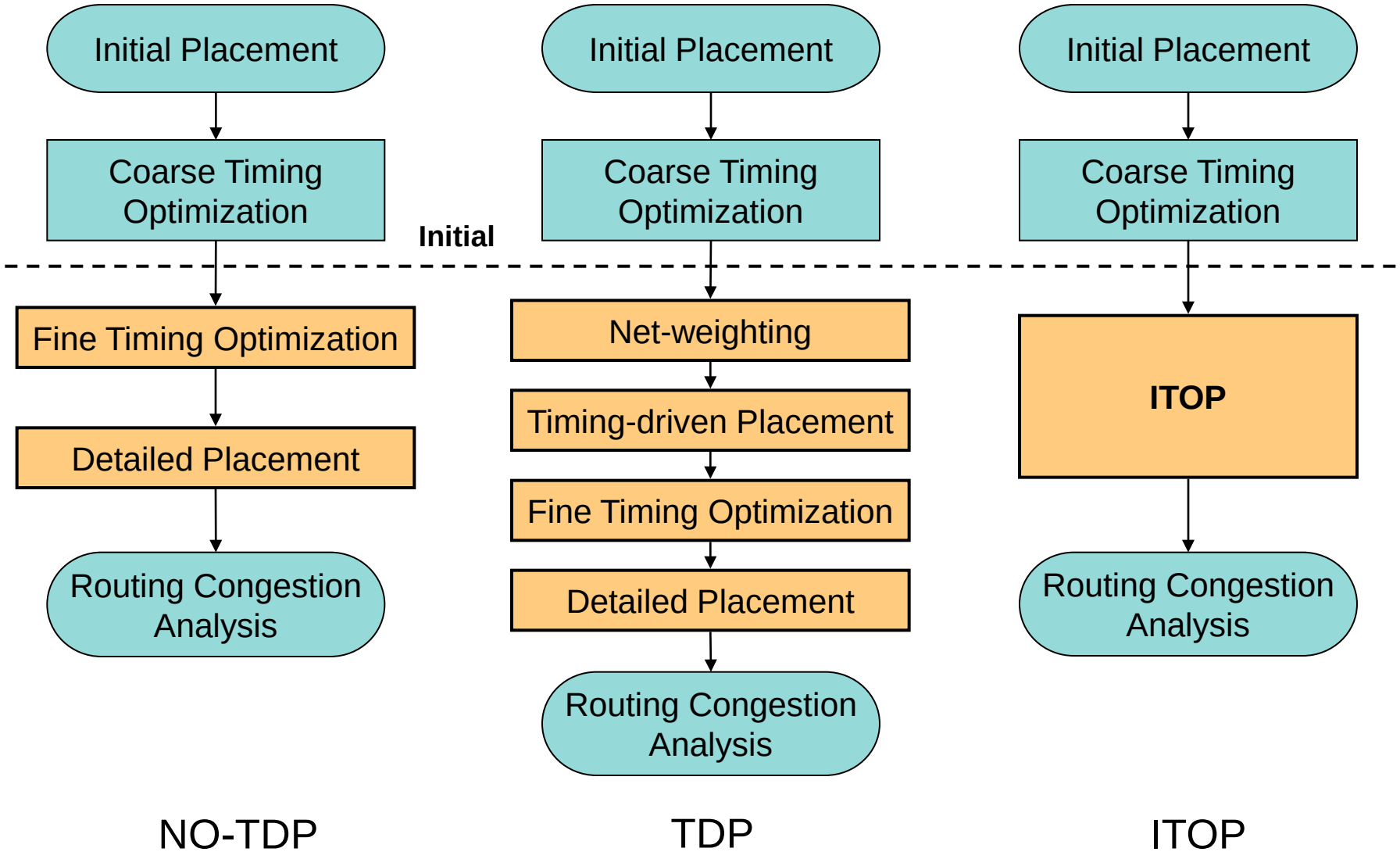
Effect of Tunneling During Placement

	Worst Slack (ns)			Figure of Merit (ns)		
	No Tunneling	With Tunneling	%Improv	No Tunneling	With Tunneling	%Improv
ckt_5	-0.44	-0.31	29.55	-2902	-2636	9.17
ckt_6	-1.65	-1.07	35.15	-7083	-6298	11.08
ckt_9	-0.32	-0.06	81.25	-116	-48	58.62

Effect of Slack Histogram Compression

	Figure of Merit (ns)			Number of Negative Paths		
	No Compression	With Compression	%Improv	No Compression	With Compression	%Improv
ckt_4	-762	-645	15.35	7658	7413	3.20
ckt_8	-359	-245	31.75	3100	2768	10.71
ckt_9	-74	-48	35.14	1266	994	21.48

Experimental Flows



Worst Slack (ns)

	Initial	NO-TDP	%Improv	TDP	%Improv	ITOP	%Improv
ckt_1	-2.62	-2.54	3.05	-3.30	-25.95	**-1.01**	61.45
ckt_2	-0.43	-0.15	65.12	-0.17	60.47	**0.07**	116.28
ckt_3	-0.23	-0.17	26.09	-0.12	47.83	**-0.01**	95.65
ckt_4	-0.64	-0.51	20.31	-0.35	45.31	**-0.27**	57.81
ckt_5	-1.25	-1.01	19.20	-0.83	33.60	**-0.31**	75.20
ckt_6	-2.03	-1.71	15.76	-2.47	-21.67	**-1.07**	47.29
ckt_7	-1.24	-1.16	6.45	-0.75	39.52	**-0.47**	62.10
ckt_8	-0.98	-0.92	6.12	-0.56	42.86	**-0.16**	83.67
ckt_9	-0.90	-0.68	24.44	-0.46	48.89	**-0.06**	93.33
ckt_10	-0.61	-0.46	24.59	-0.40	34.43	**0.06**	109.84
ckt_11	-1.56	-1.26	19.23	-1.02	34.62	**-0.60**	61.54
ckt_12	-2.19	-1.90	13.24	-2.00	8.68	**-1.01**	53.88
Average			**20.30**		**29.05**		**76.50**

Figure of Merit (FOM) (ns)

	Initial	NO-TDP	%Improv	TDP	%Improv	ITOP	%Improv
ckt_1	-1750	-1492	14.74	**-1223**	30.11	**-1235**	29.43
ckt_2	-169	-34	79.88	-59	65.09	**-2**	98.82
ckt_3	-89	-50	43.82	-31	65.17	**-13**	85.39
ckt_4	-2036	-1469	27.85	**-581**	71.46	-645	68.32
ckt_5	-6244	-5273	15.55	-3076	50.74	**-2636**	57.78
ckt_6	-8256	-6566	20.47	-6407	22.40	**-6298**	23.72
ckt_7	-14147	-11811	16.51	-7083	49.93	**-5507**	61.07
ckt_8	-1795	-1149	35.99	-449	74.99	**-245**	86.35
ckt_9	-1537	-683	55.56	-163	89.39	**-48**	96.88
ckt_10	-111	-104	6.31	-42	62.16	**-2**	98.20
ckt_11	-96857	-77375	20.11	**-19557**	79.81	-20616	78.72
ckt_12	-10987	-9088	17.28	**-6462**	41.19	-6996	36.32
Average			**29.51**		**58.54**		**68.42**

Total Steiner Wire Length (xe6)

	Initial	NO-TDP	No-TDP / Initial	TDP	TDP / Initial	ITOP	ITOP / Initial
ckt_1	94.70	94.16	0.99	101.23	1.07	94.92	1.00
ckt_2	16.97	15.96	0.94	17.99	1.06	16.56	0.98
ckt_3	28.81	27.79	0.96	27.68	0.96	27.89	0.97
ckt_4	47.21	46.86	0.99	52.77	1.12	47.25	1.00
ckt_5	118.09	115.98	0.98	125.04	1.06	117.37	0.99
ckt_6	117.14	115.97	0.99	143.74	1.23	128.61	1.10
ckt_7	185.27	182.46	0.98	195.84	1.06	185.99	1.00
ckt_8	154.05	147.46	0.96	161.68	1.05	147.62	0.96
ckt_9	132.63	128.15	0.97	127.89	0.96	129.80	0.98
ckt_10	142.69	135.51	0.95	135.51	0.95	135.39	0.95
ckt_11	341.62	327.84	0.96	347.01	1.02	341.61	1.00
ckt_12	290.72	282.11	0.97	297.69	1.02	295.98	1.02
Average			**0.97**		**1.05**		**1.00**

Global Routing Congestion Analysis (#Nets ≥ 100%)

	Initial	NO-TDP	Increase	TDP	Increase	ITOP	Increase
ckt_1	80	77	-3	81	1	80	0
ckt_2	3053	2243	-810	4776	1723	2438	-615
ckt_3	132	152	20	0	-132	117	-15
ckt_4	262	218	-44	4756	4494	339	77
ckt_5	158	158	0	486	328	158	0
ckt_6	3837	3796	-41	31197	27360	6406	2569
ckt_7	246	169	-77	2481	2235	324	78
ckt_8	6608	6565	-43	52486	45878	6595	-13
ckt_9	919	917	-2	1964	1045	991	72
ckt_10	706	769	63	356	-350	616	-90
ckt_11	1112	7313	6201	169232	168120	17039	15927
ckt_12	10864	8951	-1913	36415	25551	13839	2975
Average			**279**		**23021**		**1747**

Runtime (sec)

	NO-TDP	TDP	ITOP	ITOP/TDP
ckt_1	1023	2538	2758	1.09
ckt_2	674	1526	1449	0.95
ckt_3	831	1931	1435	0.74
ckt_4	1046	2227	3524	1.58
ckt_5	1686	3148	4154	1.32
ckt_6	1416	3558	4273	1.20
ckt_7	2765	5835	6779	1.16
ckt_8	3631	10612	8426	0.79
ckt_9	2587	6227	8785	1.41
ckt_10	3024	9583	4100	0.43
ckt_11	9896	33673	36162	1.07
ckt_12	6964	18965	20386	1.07
Average				**1.07**

Conclusions

- **ITOP: Effectively integrates timing optimization and static timing analysis within placement**
- **Incremental timing closure flow**
  - Replace global timing-driven placement
- **Timing closure without hurting wire length and routing congestion**
- **Results**
  - Worst Slack: 56.2% and 47.5% improvement over NO-TDP and TDP
  - FOM: 38.9% and 9.9% improvement over NO-TDP and TDP
  - Wire length: 5% improvement over TDP
  - Routing Congestion: Comparable to NO-TDP