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Efficient Design Practices for Thermal Management of TSV based 3D IC System

Min Ni, Qing Su, Zongwu Tang, Jamil Kawa
Synopsys Inc.

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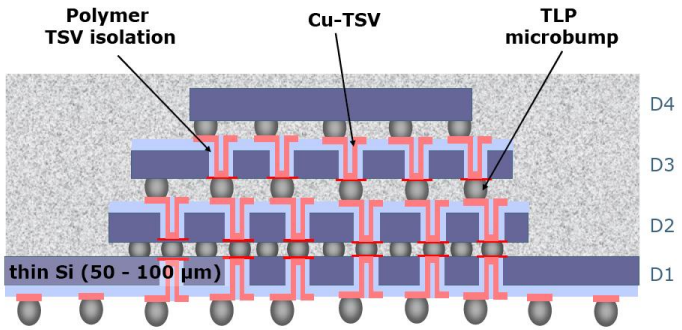
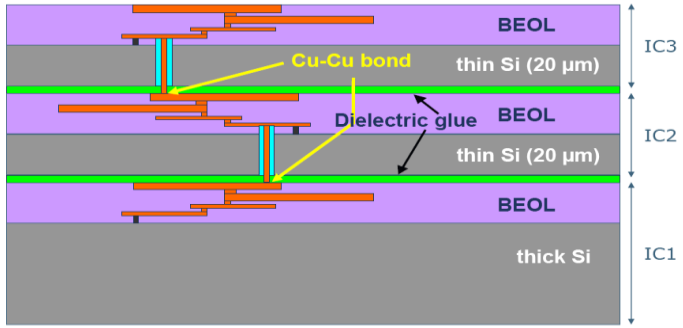
Outline

- Introduction: TSV based 3D IC
- A Review of 3D IC Thermal Management
- 3D IC Thermal Evaluation
- Thermal Impact of TSV Arrays in Close Proximity to Hotspots
- Thermal Effects of TSV as a Function of TSV Density
- Summary & Conclusions

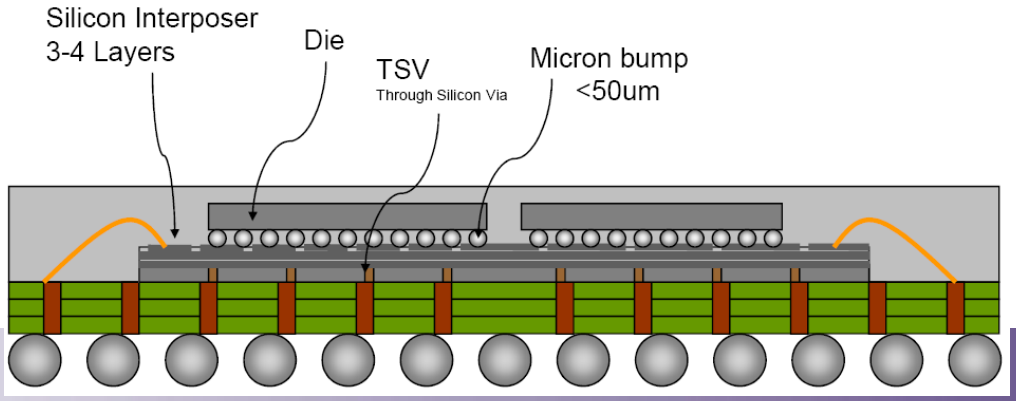
TSV based 3D IC – Two Configurations

- Vertical Stacking (source: IMEC)
  - Includes face-to-face, **and face-to-back** (with TSV) stack.





- Lateral Interposer (source: Panasonic)

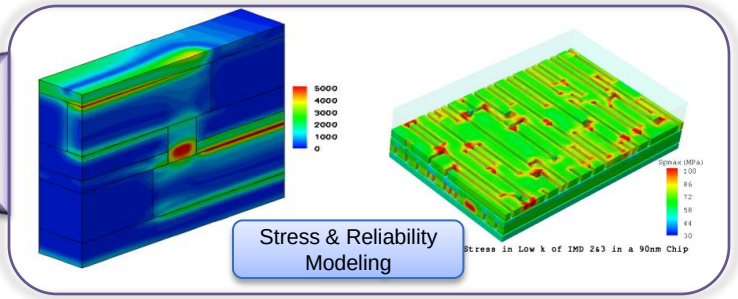


3D (TSV) IC Design Flow

Mfg.

TSV Modeling

- Thermo-mechanical stress analysis
- Electrical variation



3D IC Design & Verification

Synthesis & DFT

- TSV connectivity checking w/JTAG
- 1000x compression

Physical Design

- Multi-die bump & TSV floorplan
- TSV P&R

Parasitic Extraction

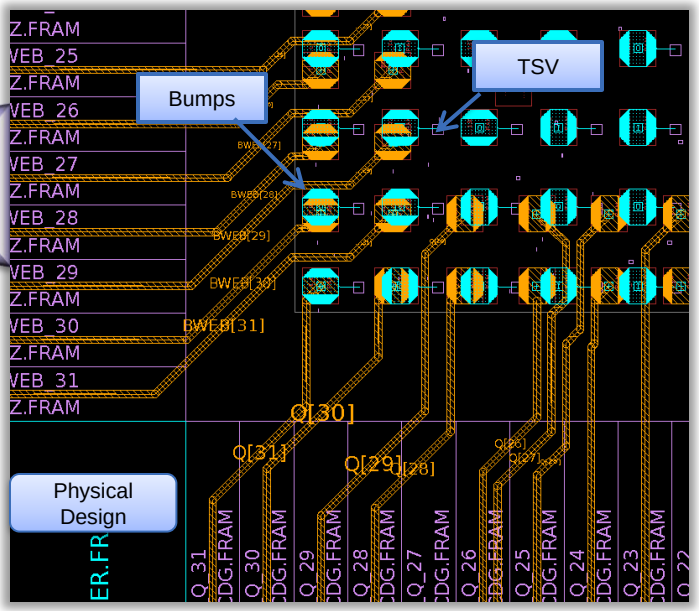
- Extract TSV, u-bump, backside RDL metal

Physical Verification

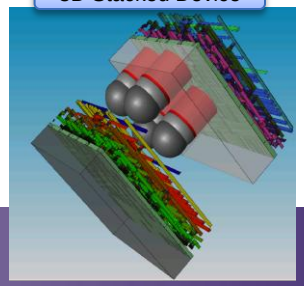
- TSV aware LVS/DRC

Stack Sign-off

- TSV aware timing, IR-Drop, EM analysis
- Thermal analysis*



3D Stacked Device



**application dependent*

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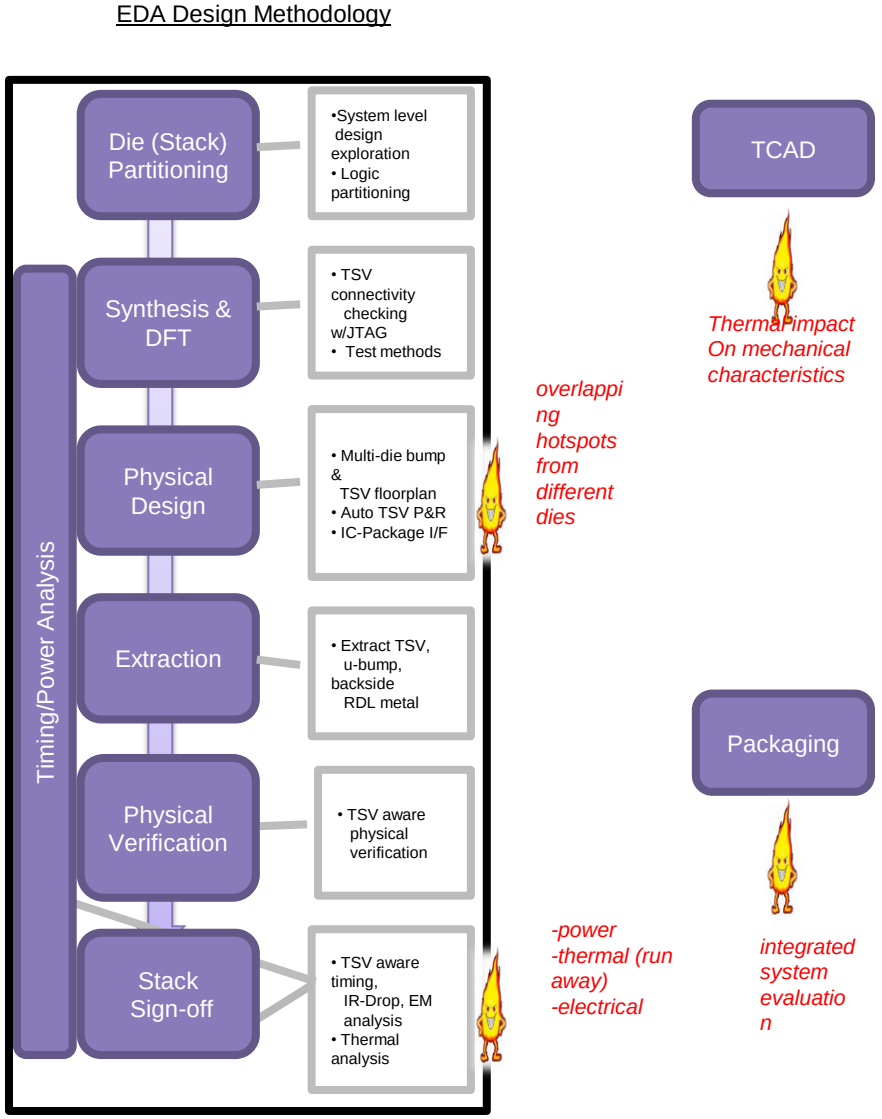
Background

- Vertical stacking exacerbates thermal problem
  - Higher peak temperature
  - Risk of hotspot alignment
  - Performance and reliability implications
- Thermal management needed early in design flow

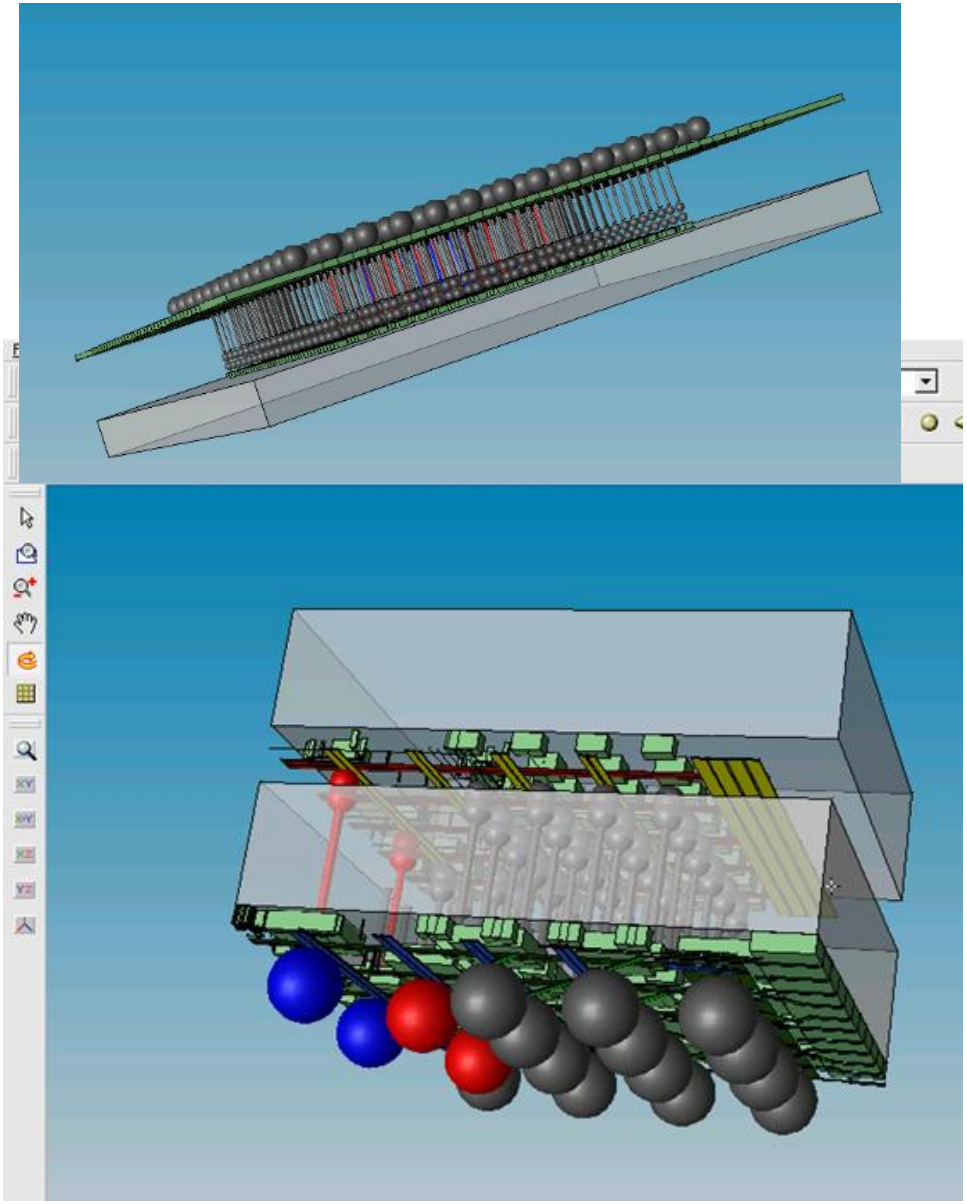


Thermal Management Perspectives

- Thermal vias & thermal TSVs
  - Pros
    - can utilize existing vias and TSVs
    - no additional processing steps needed
  - Cons
    - non-scalable due to vertical heat path.
    - area penalty for extra thermal TSVs
- Fluidic channels
  - pros
    - scalable with chip area and number of tiers
  - cons
    - design complexity
    - Extra reliability
    - needed vertical resources

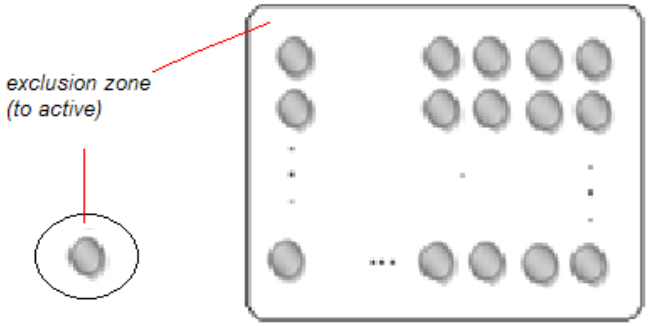
TSVs

- TSVs
  - Signal TSVs
  - PG TSVs
  - Thermal TSVs
  - Single uniform diameters



Thinking Loud

- Placement of TSVs
  - Use TSV array clusters to minimize area penalty on silicon and interconnect
  - Need to pay attention to mechanical structural balance in TSV placement
- Are dedicated thermal TSVs really needed?
  - Introduced at design planning stage?
    - Academia papers on inserting extra TSVs suggests so
      - hotspots are not necessarily known at this stage
  - In post routing stage?
    - Hotspots are known
      - Better assessment of need for extra TSVs
      - Exploit metal density and PGS TSVs requirements
      - proximity to hotspot planning

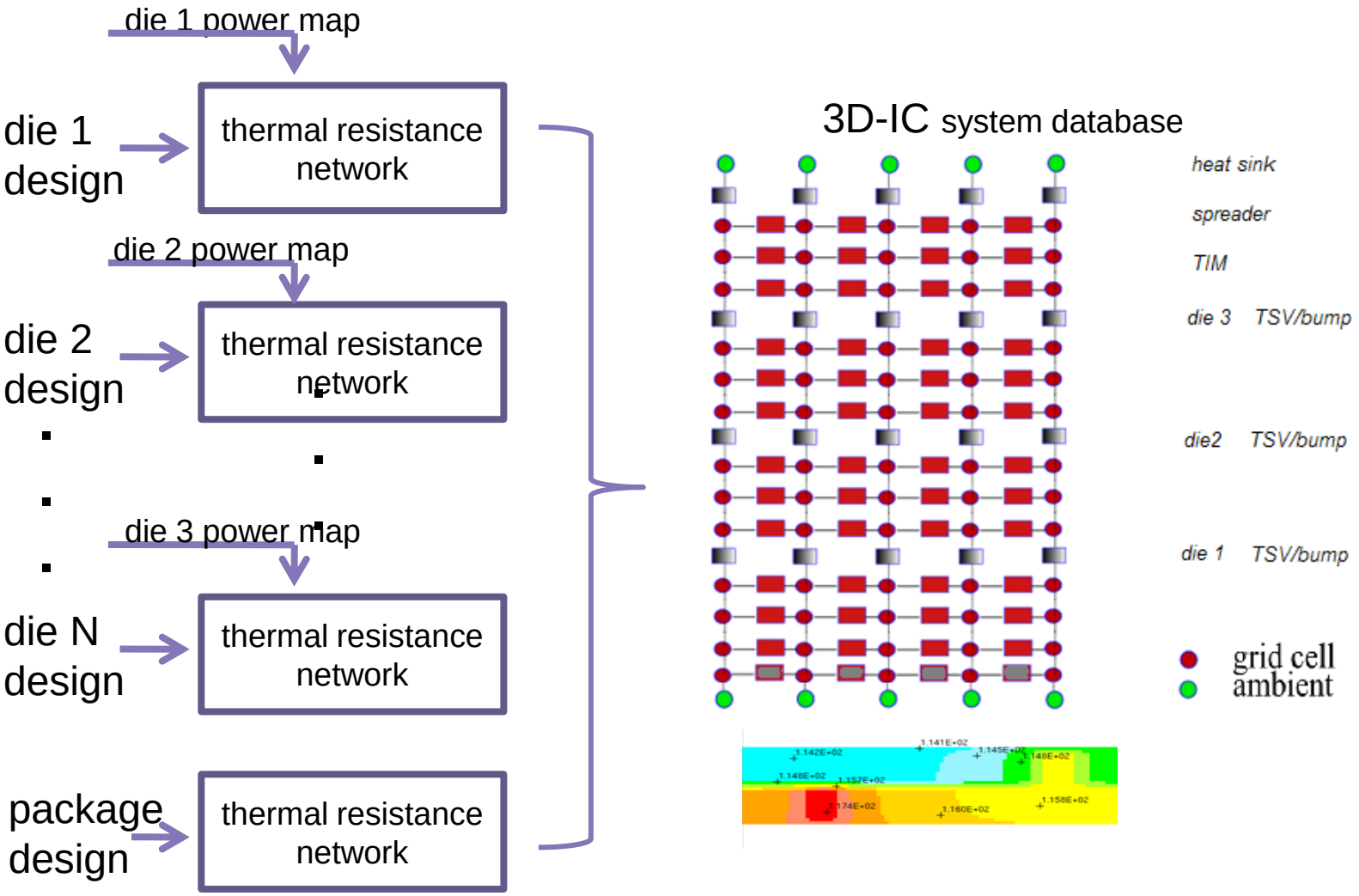


A single TSV and a TSV array. Exclusion zone is minimum space of TSV to active devices- usually 5um

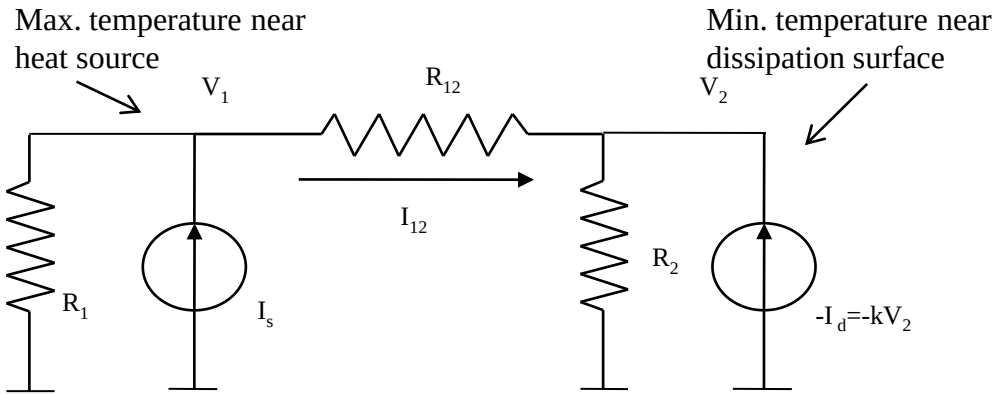
Thermal Simulation Considerations

- Consider whole system vs. 1 die at a time
  - Eliminates artificial boundary conditions
  - Eliminates need for large number of iterations
    - Smaller run time
- Used numerically based thermal simulator solving a ciruit-equivalent thermal network
  - heat source is analogous to a circuit's current source
  - thermal resistance is analogous to electric resistance
  - temperature gradient is analogous to electric potential (voltage) in circuits

An EDA Evaluation of a Thermal Structure – Our Experiments Setup



Thermal circuit equivalence

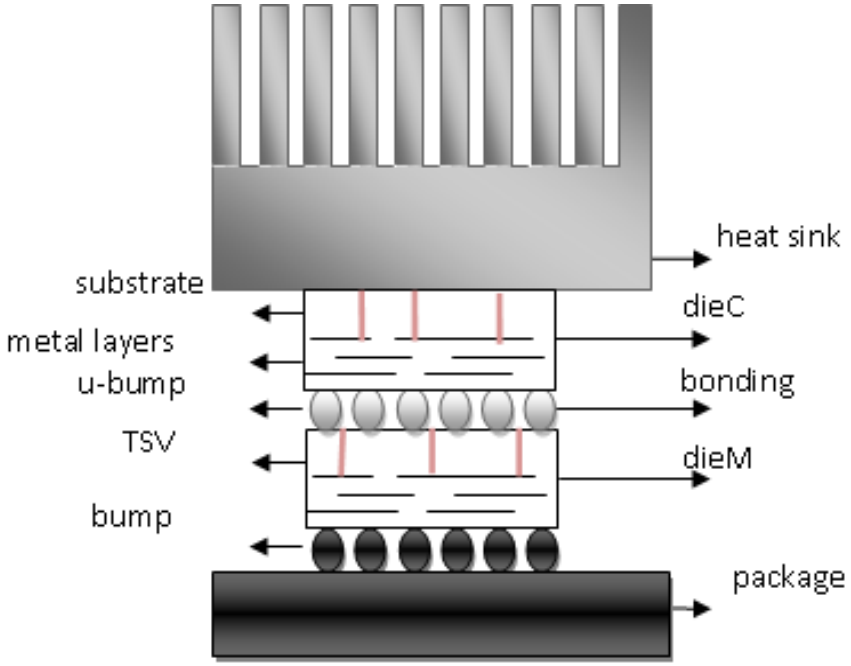


- R_1 is the relative thermal resistivity between the heat source and ambient
- R_2 is the relative thermal resistivity between the dissipation surface and ambient.
- R_{12} is the effective thermal resistivity between the hot spots and cold spots

Setup

6x6 mm2
50um thin silicon substrate

Added “connectivity” to heat sink makes thermal TSVs, in experiment

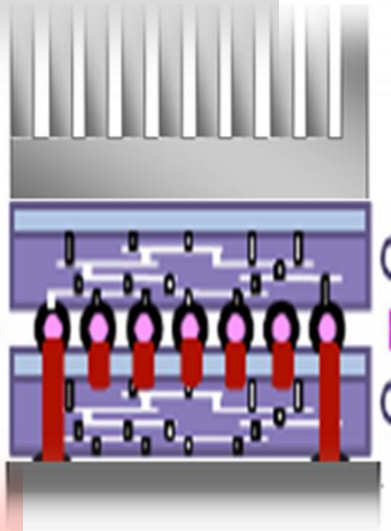


Name	Type	Power(W)	MinT(°C)	MaxT(°C)	DT(°C)
M	memory	1.18	38.9	44.0	5.1
C	logic+mem	4.05	51.8	135	83.2

3D IC construction

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
TIER {
     TYPE          = BUMP
     NAME          = die1_die2
     ;dimension of the bump array
     XDIM          = 10
     YDIM          = 10
     DIAMETER    = 15
     PITCH       = 20
     ;thickness of the bump layer
     THICK         = 30
     XCRD          = 0
     YCRD          = 0
     TCCU        = 273
     TCOX          = 66
     DEBUG_THNET    = bump_diea_dieb.
}
```

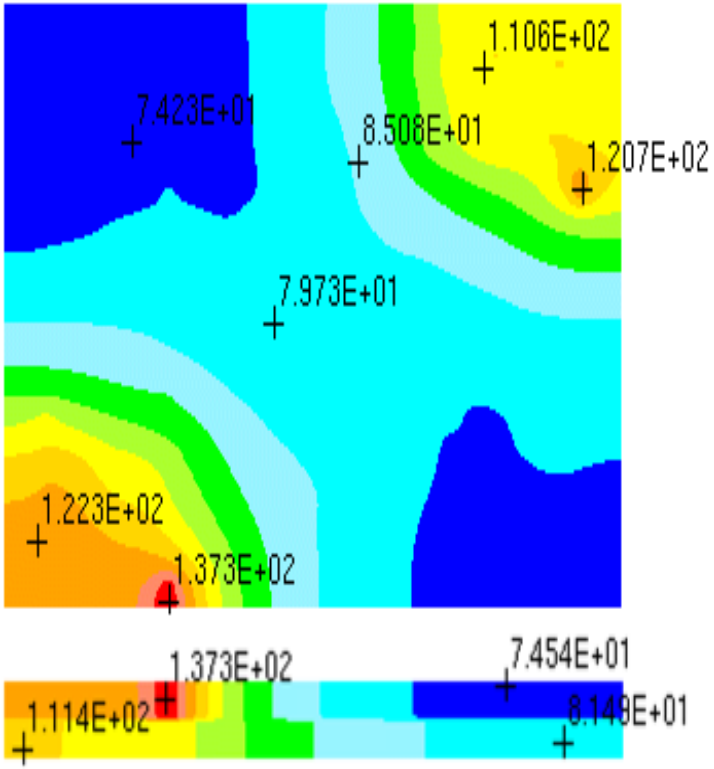
```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
TIER {
     TYPE          = TSV
     NAME          = tsvLayer
     NARRAY        = 2
     ARRAY {
          THRGH    = NO
          START    = dieA
               XDIM      = 5
               YDIM      = 5
               XCRD      = 10
               YCRD      = 20
               DIAMETER  = 15
               PITCH     = 20
               TCON      = 273
     }
}
```



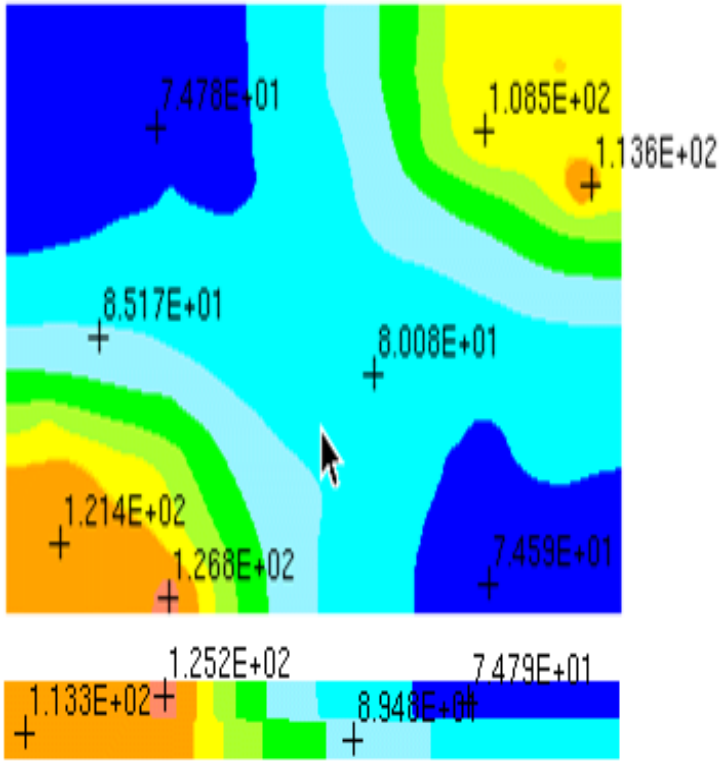

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
TIER {
     TYPE          = DIE
     NAME          = die2
     COPY          = null
     DB_PATH       = /remote/atg5/mni/sandbox2/PR_TA_Lab
     RDF           = ta_cfg.rdf
     FLIP          = XFLIP
     XCRD        = 0
     YCRD        = 0
     POWER_RAMPUP  = dieb.prp
     DEBUG_PMAP              = dieb.map
     DEBUG_THNET   = dieb.mtx
}
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
     TYPE          = DIE  ;
     NAME          = die1
     COPY          = null
     DB_PATH       =
/remote/atg5/mni/sandbox2/PrimeRail_TA_Lab
     RDF           = ta_cfg.rdf
     XCRD          = 0
     YCRD          = 0
     FLIP          = NFLIP
     POWER_RAMPUP  = diea.prp
     DEBUG_PMAP    = diea.map
     DEBUG_THNET   = diea.mtx
}
```

Thermal effects of TSVs in close proximity to hotspots



Top view



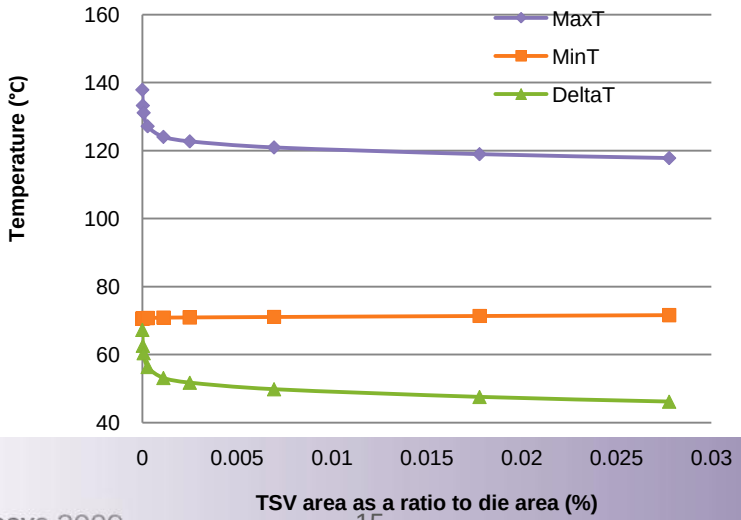
Die 1
Die 2

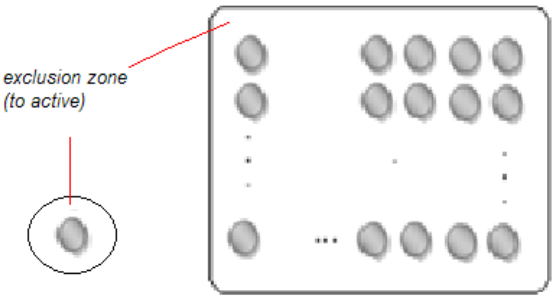
Before and after TSV array insertion

Impact of signal/power TSV array on temperature of 3D IC

with different size (one array for each of the 4 hot spots)

TSV array	TSV density	Temperature (°C)		
		Max	Min	DT
0	0%	137.9	70.6	67.3
3x3	0.003%	133.4	70.7	62.7
5x5	0.007%	131.4	70.7	60.7
10x10	0.03%	127.6	70.8	56.8
20x20	0.11%	125.8	70.9	54.9
30x30	0.25%	125.1	71.0	54.1
50x50	0.69%	123.9	71.0	52.9
80x80	1.79%	122.4	71.2	51.3
100x100	2.78%	121.6	71.3	50.3





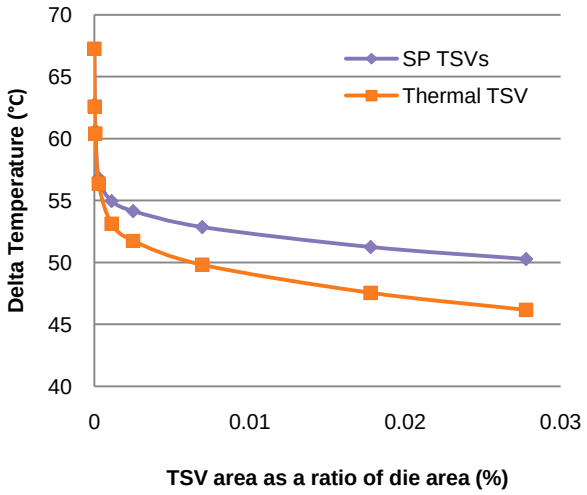
A single TSV and a TSV array. Exclusion zone is minimum space of TSV to active devices- usually 5um

The maximum temperature decreases as TSVs are inserted, however, the effects saturate quickly. The minimum temperature does not drop.

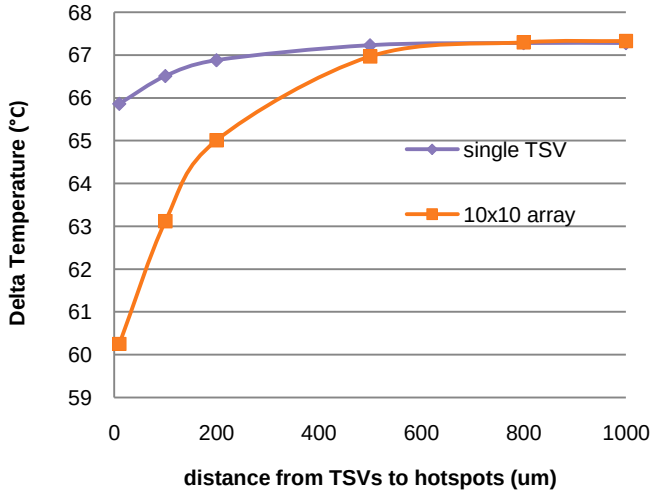
The net effect of TSV insertion in 3D IC is to reduce the peak temperature and the temperature gradient.

TSV thermal effects as a function of TSV density

with different size (one array for each of the 4 hot spots)



The ability of reducing thermal gradient is similar for both signal/power TSV and thermal (direct connection to sink)TSV arrays.



Relation between the distance from TSVs to hotspots and the reduction of temperature gradient.

Summary

- Signal and power TSV arrays are practically as efficient as thermal TSVs.
- The proximity of thermal TSV arrays to hot spots is more critical than array size. Also, for close proximity arrays size matters but benefits from increased array size saturates quickly.
- Better practice is to place TSVs in array format to minimize area penalty, close to hotspot to maximize heat conduction, with compliance to other mechanical and electrical constraints
- It is the boundary heat transfer coefficient that dictates the steady state temperature of chips, not the amount of TSVs