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Physical Design Implementation for 3D IC – Methodology and Tools

Dave Noice
Vassilios Gerousis

Outline

- 3D IC Physical components
  - Modeling
- 3D IC Stack Configuration
- Physical Design With TSV
- Summary

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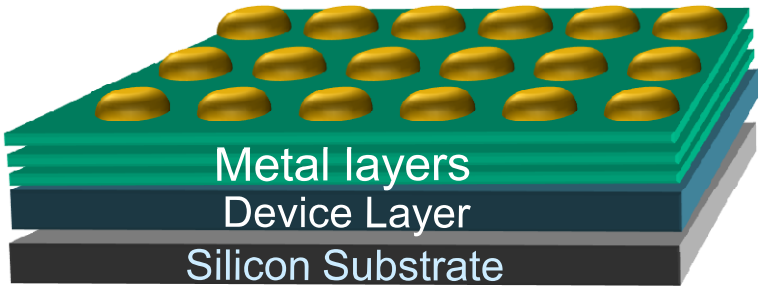
3D IC Stack Interconnect Modeling

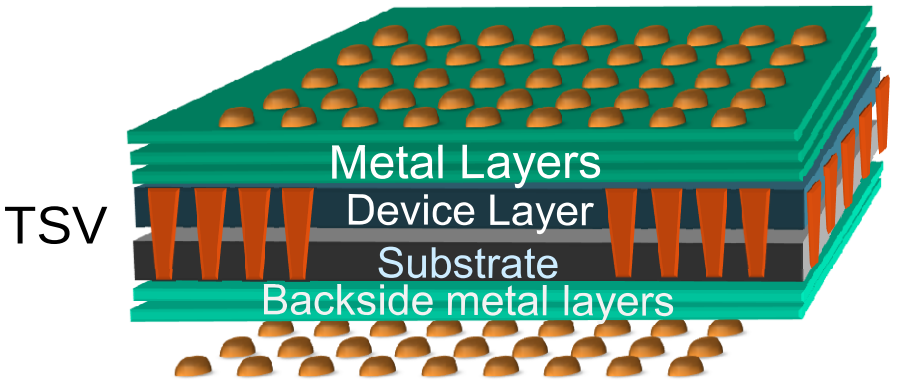
Multi-Chip Interconnect Technology

Regular Chip with
Flip Chip Bumps



Chip with TSV plus Backside Metal

- Micro-bump on the top/bottom
- or flip-chip bump on top/bottom metal



- Multi-Chip Interconnect Technology
  - **Micro-bumps layer** for interconnect between chips
  - **TSV** with **backside metals** layer to allow interconnect stacking
  - **Flip Chip Bump** for interconnect to package
- Design methodology development is critical in physical design tool development to address the different styles of 3D IC.

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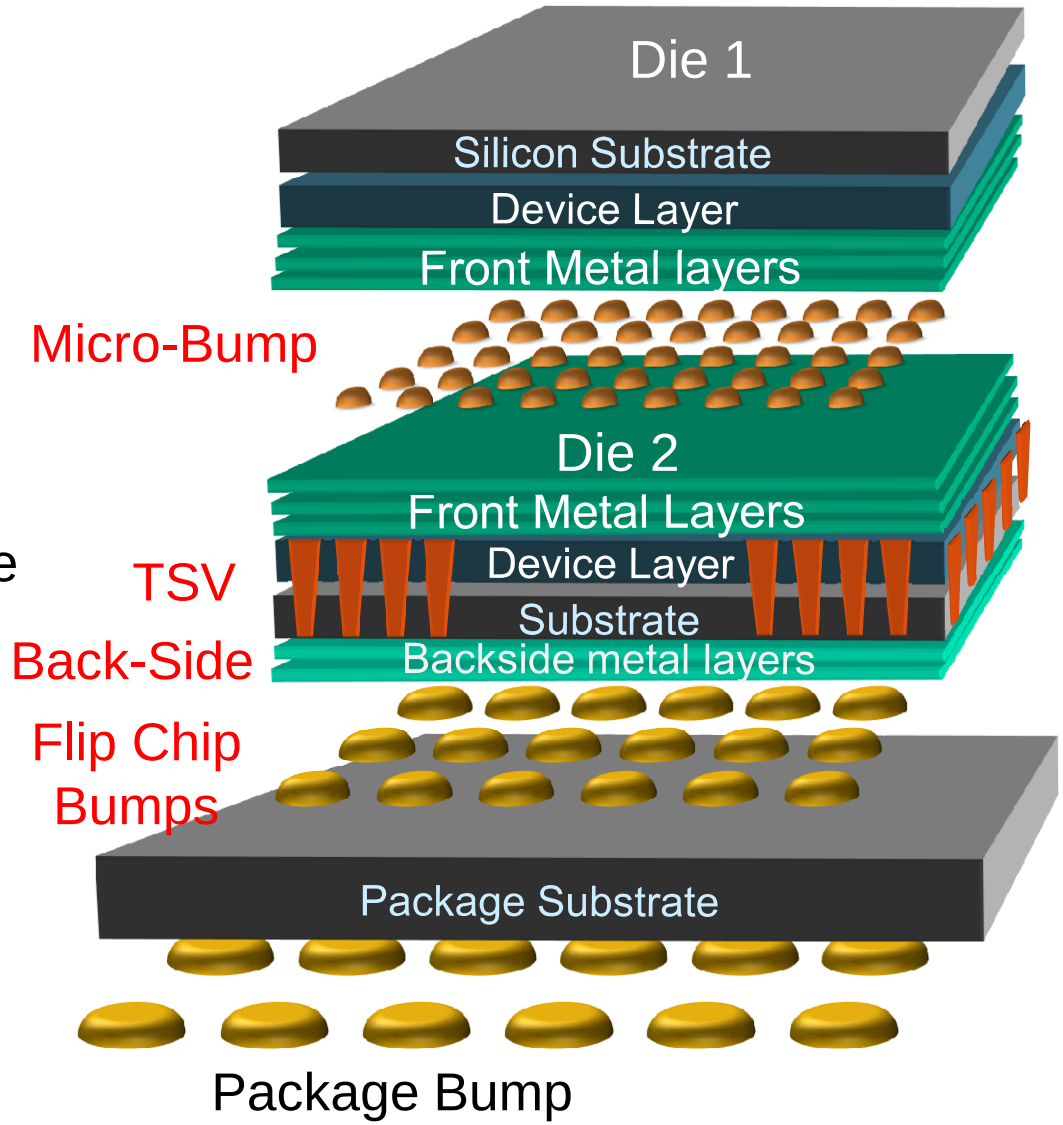
Face-To-Face 2-Chip Stacked 3D IC

3D IC Interconnect Model

- Micro-Bump: Small
  - Placed any where.
  - Size and spacing rule
- TSV: two types
  - Fine TSV: small size
  - Super-TSV: very large size
  - Size and spacing rules
- Backside metal layers: RDL layers.
- Flip-Chip Bump: medium
- Package bump: Large



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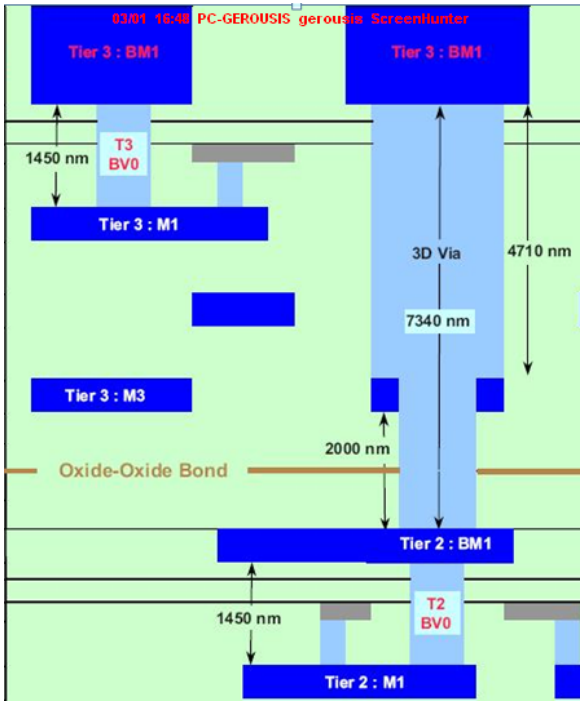
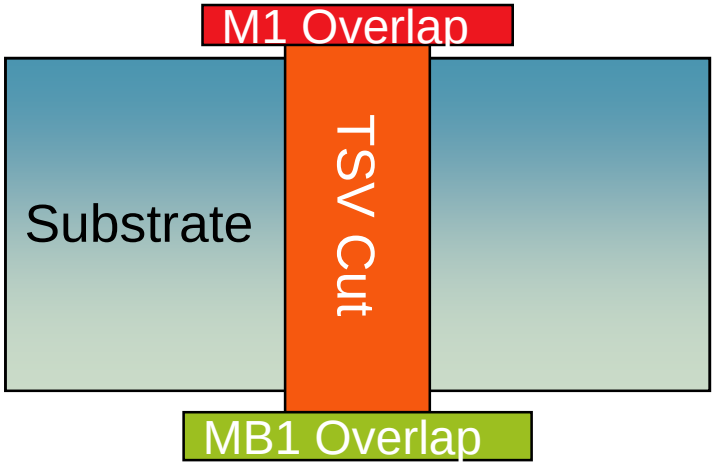
TSV Modeling = TSV is cell and a Via?

Super TSV



- Super TSV goes through substrate and metal stack.
  - Limited placement locations
- Modeled as a cell

Regular TSV



- Regular TSV (smaller geometry)
- TSV is modeled as a via.
- Can be placed anywhere inside chip with special constraints.

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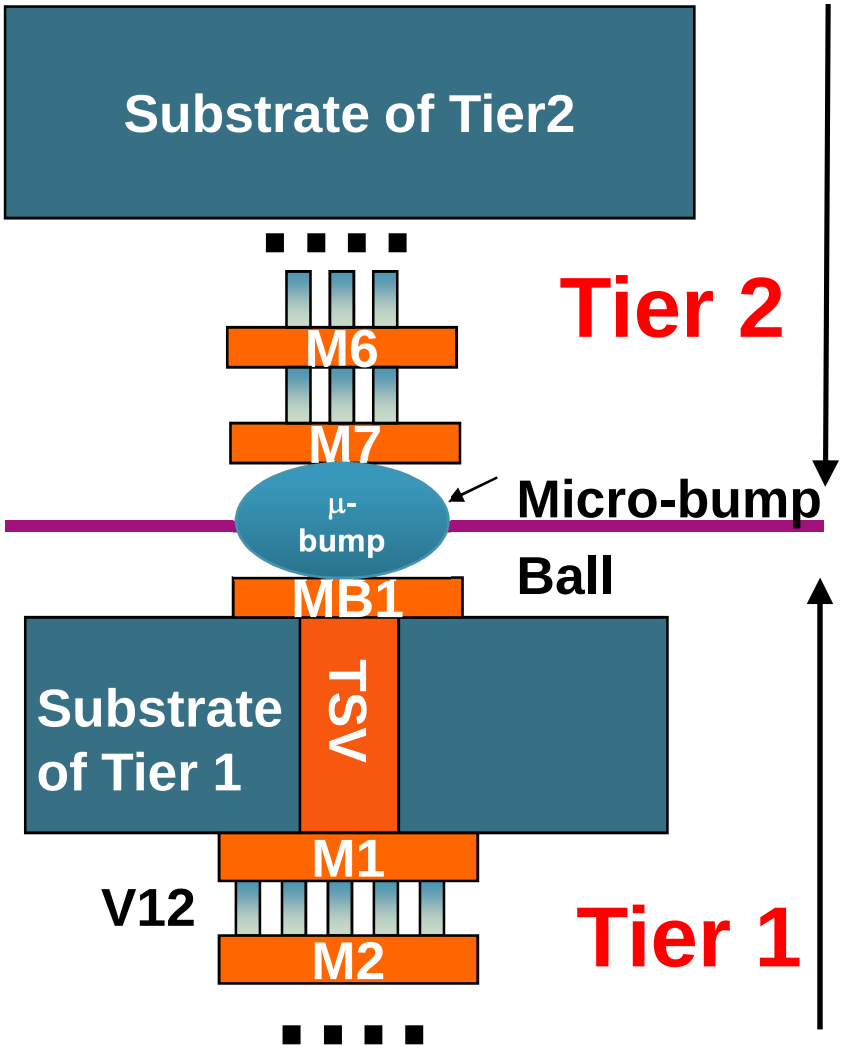
Micro-Bump: Ball and Pad

- Micro-bump interconnect contains two objects
  - The ball which is usually much smaller than flip chip bump
  - Micro-bump Pad: one pad on top (Tier2) and the other one on bottom (Tier1).
- The micro-bump ball and also the pad are modeled in the IC stack file
  - Used in analysis tools
- In the physical IC design space, only the micro-bump pad is used.
  - Micro-bump pad is modeled as a cell.



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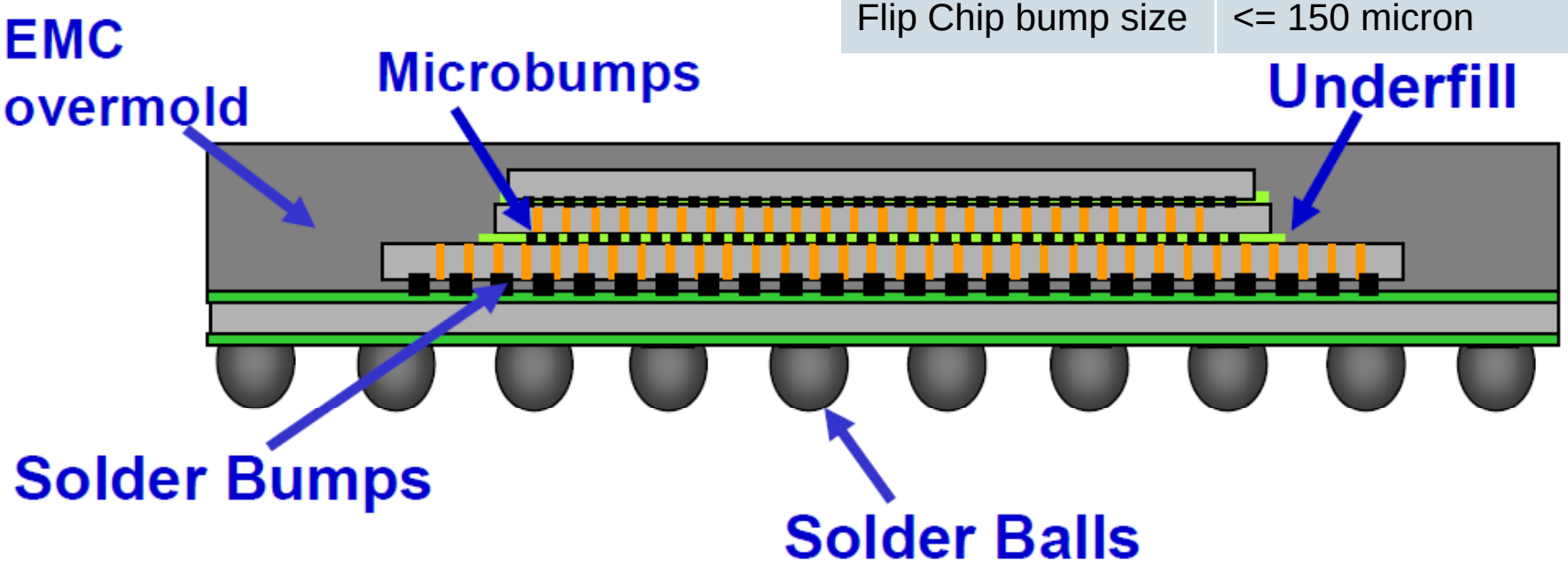
3D IC Stack Configuration

Package View of 3D IC

TSV via size	5-30 micron
Substrate thickness	50-100 micron
Micro-bump size	20 – 50 micron
Flip Chip bump size	<= 150 micron



- Stacking configuration is an essential modeling tool to drive both the physical design space and also the analysis space.
- Package pins are usually hard constraints when optimizing the Z direction.
  - Design flow can be bottom-up (package driven)
  - Design flow can be top down (IC driven)

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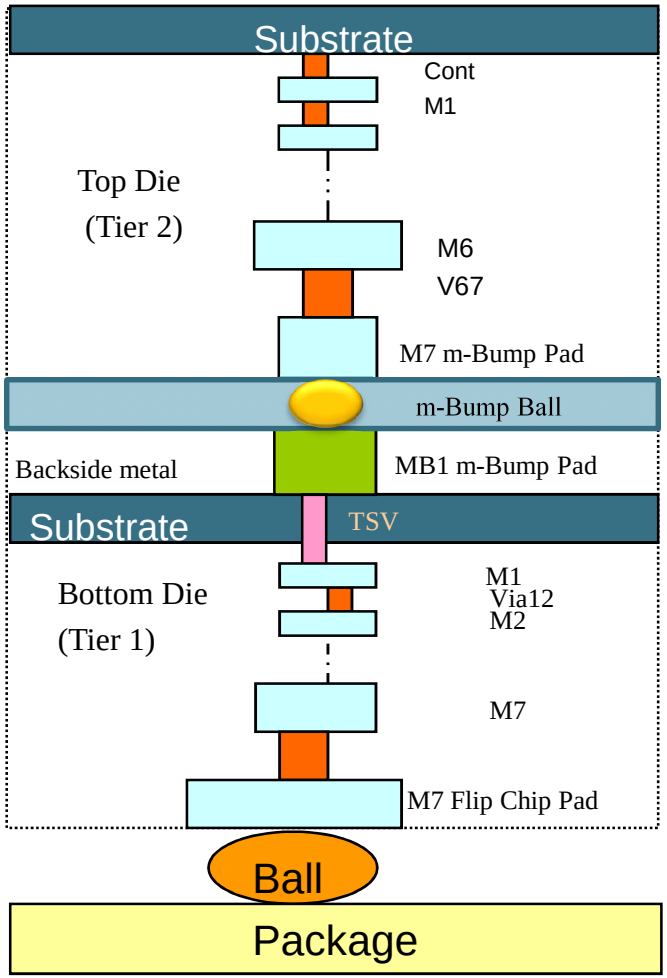
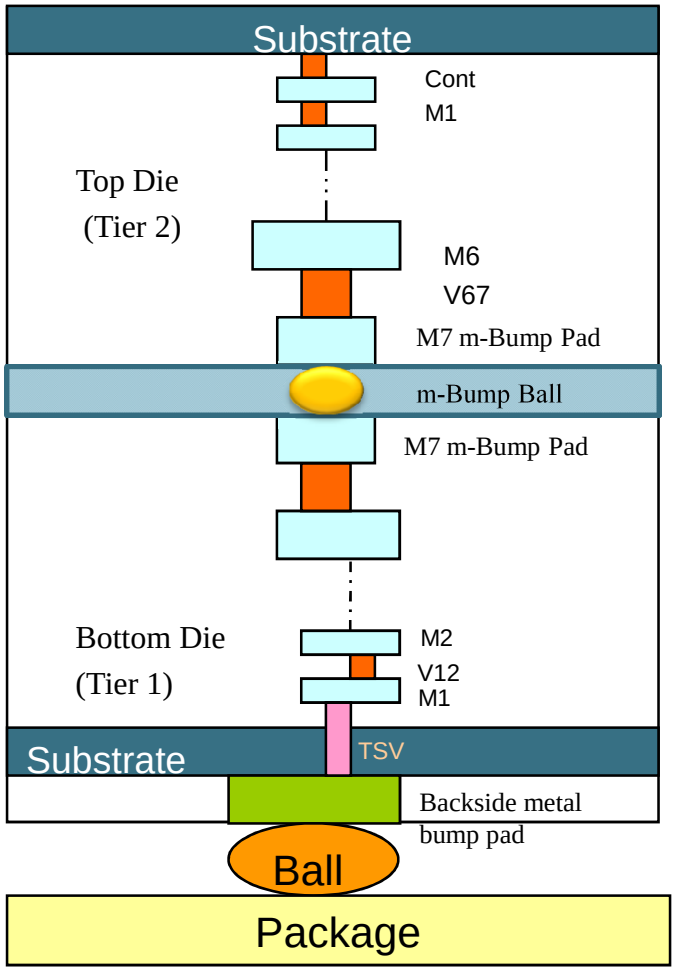
3D IC Stacked Die Configuration Examples

Back-to-front configuration



Front-to-front configuration



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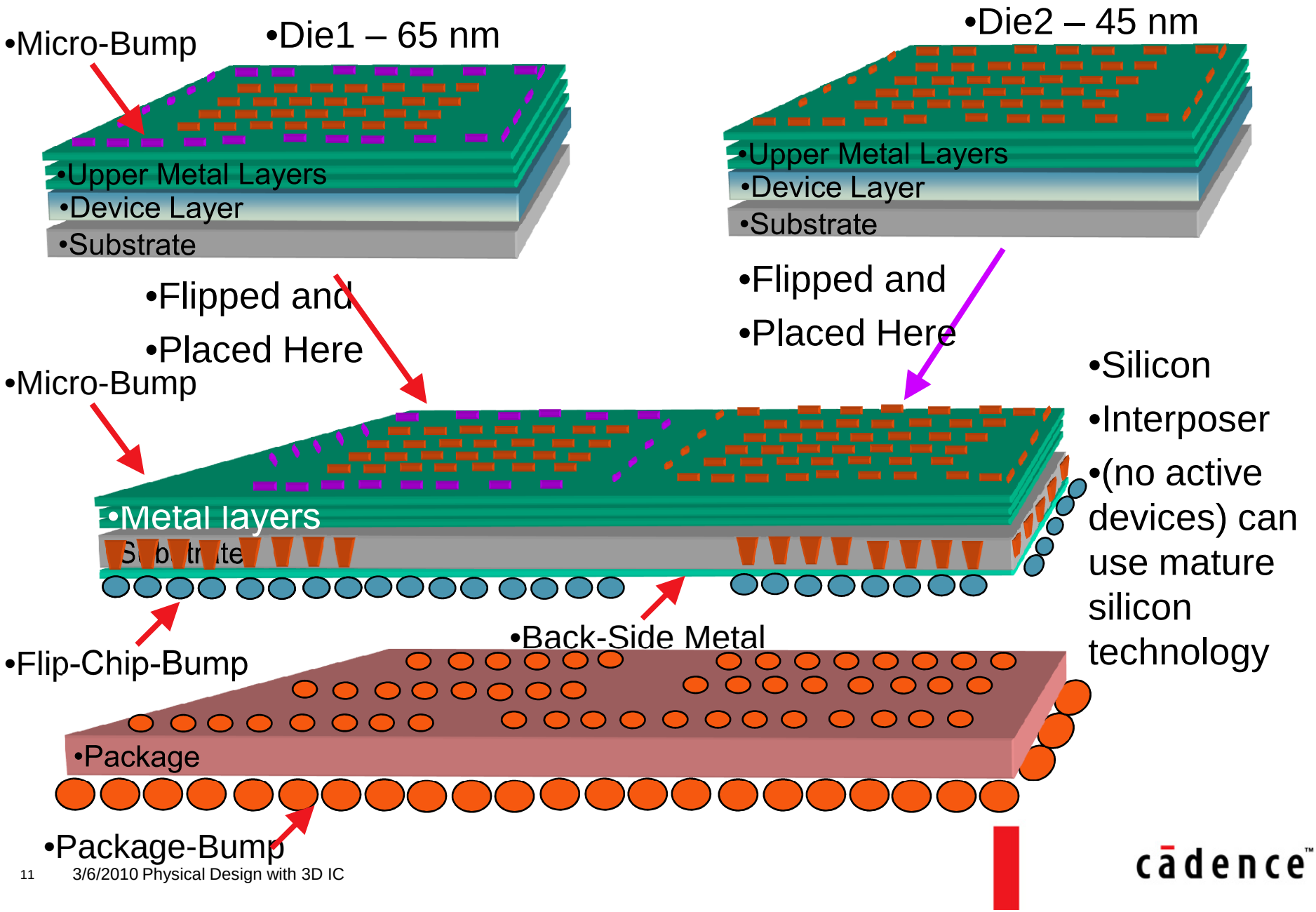
Horizontal Stacking – Silicon Interposer



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3D IC Configuration

- Need a flexible configuration specification to allow the description of
  - Vertical stack
  - Horizontal stack
  - Mixed stack
- It allows the designer with an appropriate set of tools to evaluate each stacking configuration.
- Each configuration provides different aspects of design space
  - Thermal impact
  - Routing Congestion
  - TSV via density
  - Power supply impact
- Heterogeneous die in the stack (digital, analog, RF, package) requires the use of multiple design systems.
  - Package design, Digital IC Design, Analog IC and RF design

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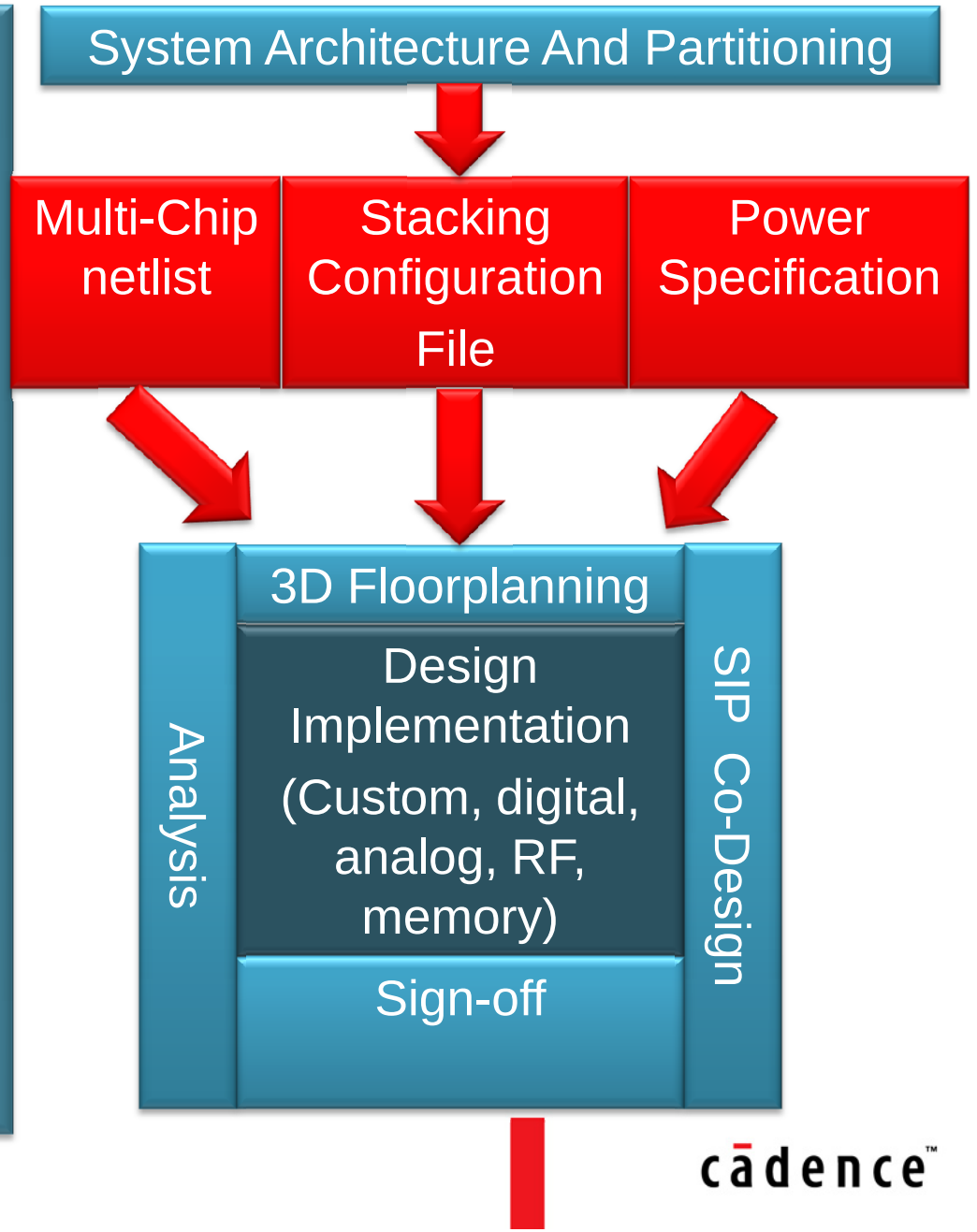
Physical Design With TSV

Design Implementation For 3D IC

- Design Description:
  - Stacking Configuration
  - Multi-chip Connectivity
  - Power Specification
- Work with existing Design Implementation Tools
  - 3D IC interconnect Model
  - 3D enabled placement and routing
- 3D Analysis tools
  - Interconnect Extraction ➔ timing & SI
  - Thermal analysis
  - Voltage drop analysis
- Integration with Package Co-Design (SIP)



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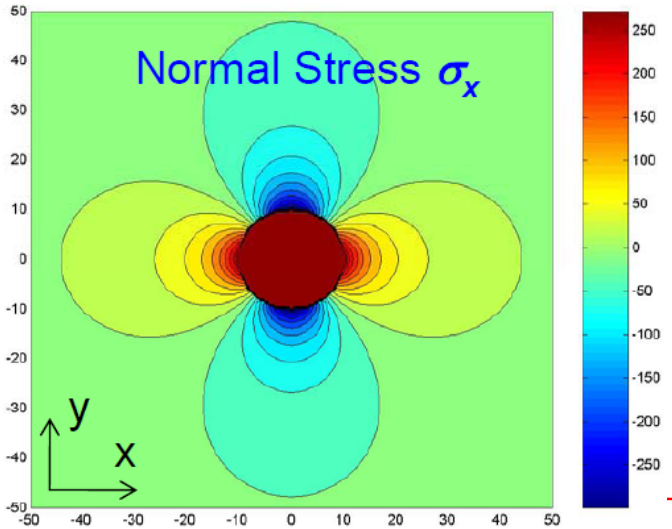
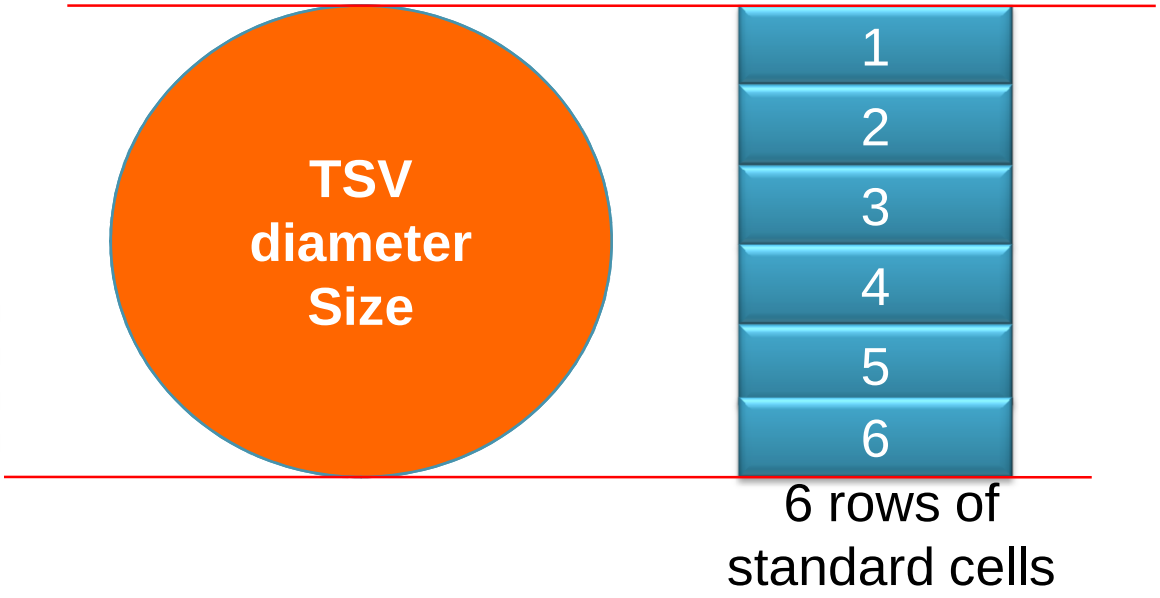
TSV size ➔ Impact on placement and routing





- TSV cut size is about 5-10X the height of standard cell in 32 nm technology.
  - TSV placement disturbs standard cell row placements
- TSV cut size is about 15-30X M1 min-width.
  - Special routing rules for M1: Use of max width wire
- TSV thermo-mechanical stress has impact on mobility of nearby devices
  - Best handled with keep out area from diffusion area
    - Small distance to digital cells and bigger distance near analog cells.

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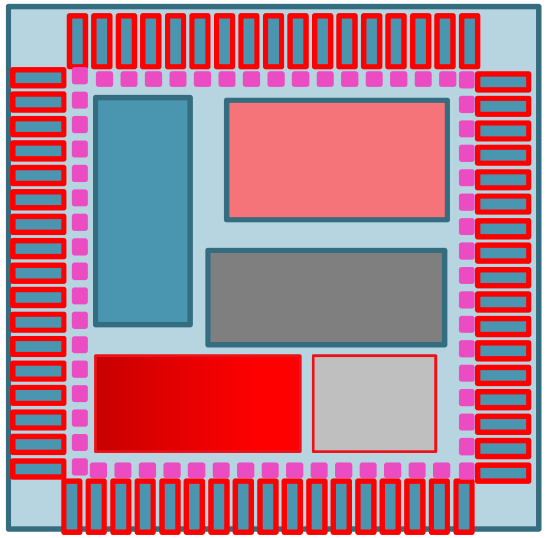
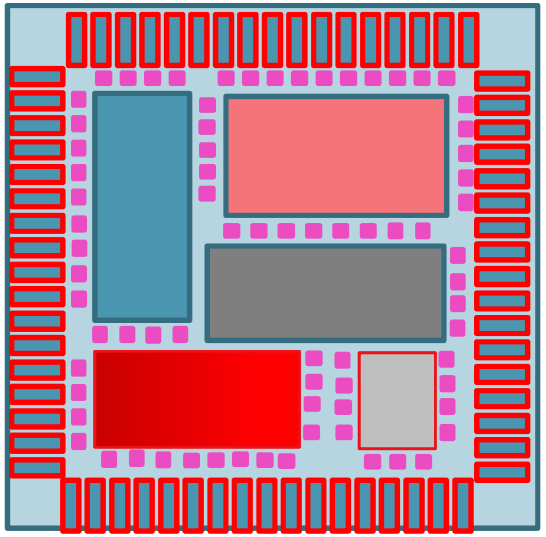
TSV Placement Methodology

Periphery Based Placement



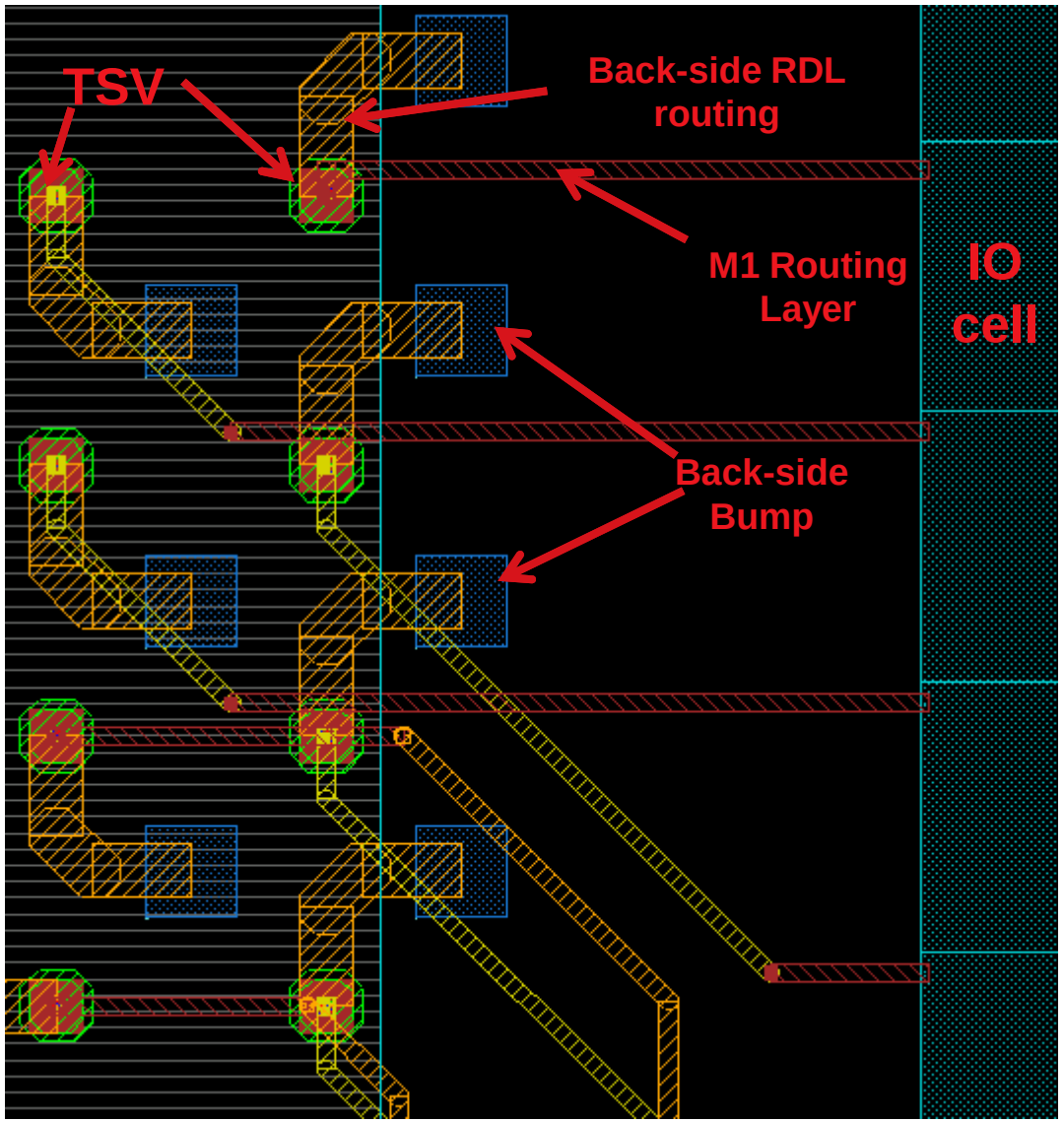
Area Based Placement

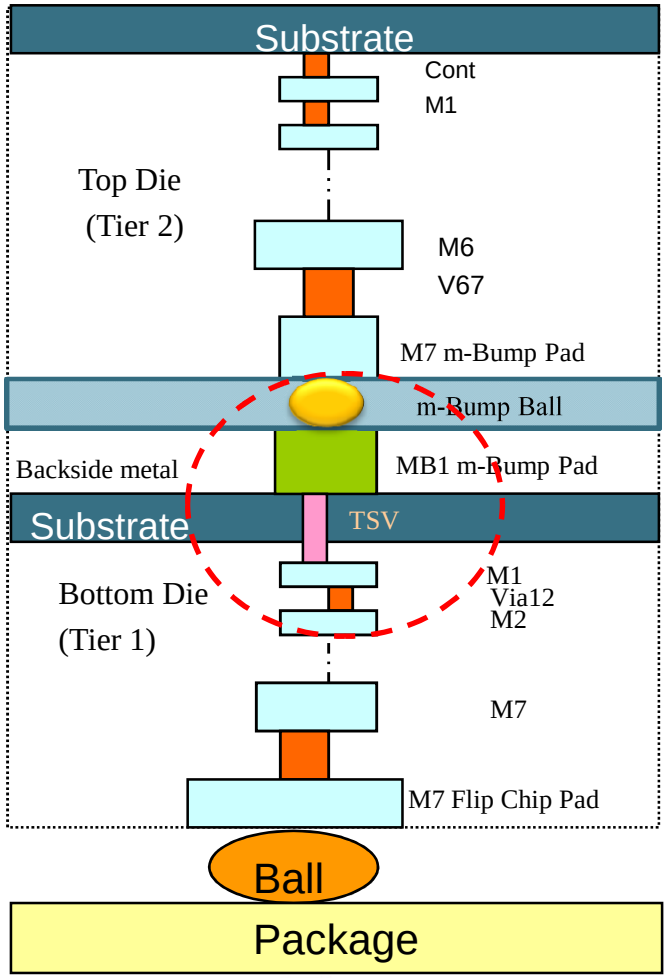


- Size and other physical constraints dictate special design methodology for TSV (and micro-bump) placement and routing. Some examples are:
  - Peripheral based: Normally connected to IO with ESD protection.
  - Area based: Can be connected to internal cells without ESD.
  - Mixed approach: some with ESD, some without ESD
- Floorplanning and placement must consider TSV and micro-bump locations.

Routing With TSV – Back to Face Example

- Routing on M1 and MB1 layer.





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Summary

- 3D IC stack introduces new interconnect components
- We introduced physical modeling for 3D IC interconnect for placement and routing
  - Two sides for the chip, where metal layers can be used
  - Micro-bump and TSV are the two main components to connect multiple dies
- Physical sizes of TSVs and also their physical properties, dictates the need for special methodology for placement and routing
  - Stress dictates special distance from cells and macros.
  - Sizes restricts where TSV can be placed on the die
    - Floor planning, placement of cells and macros is constrained by TSV and micro-bump placement
- Design methodology is critical to 3D IC physical design