Automatic Generation of Hierarchical Placement Rules for Analog Integrated Circuits

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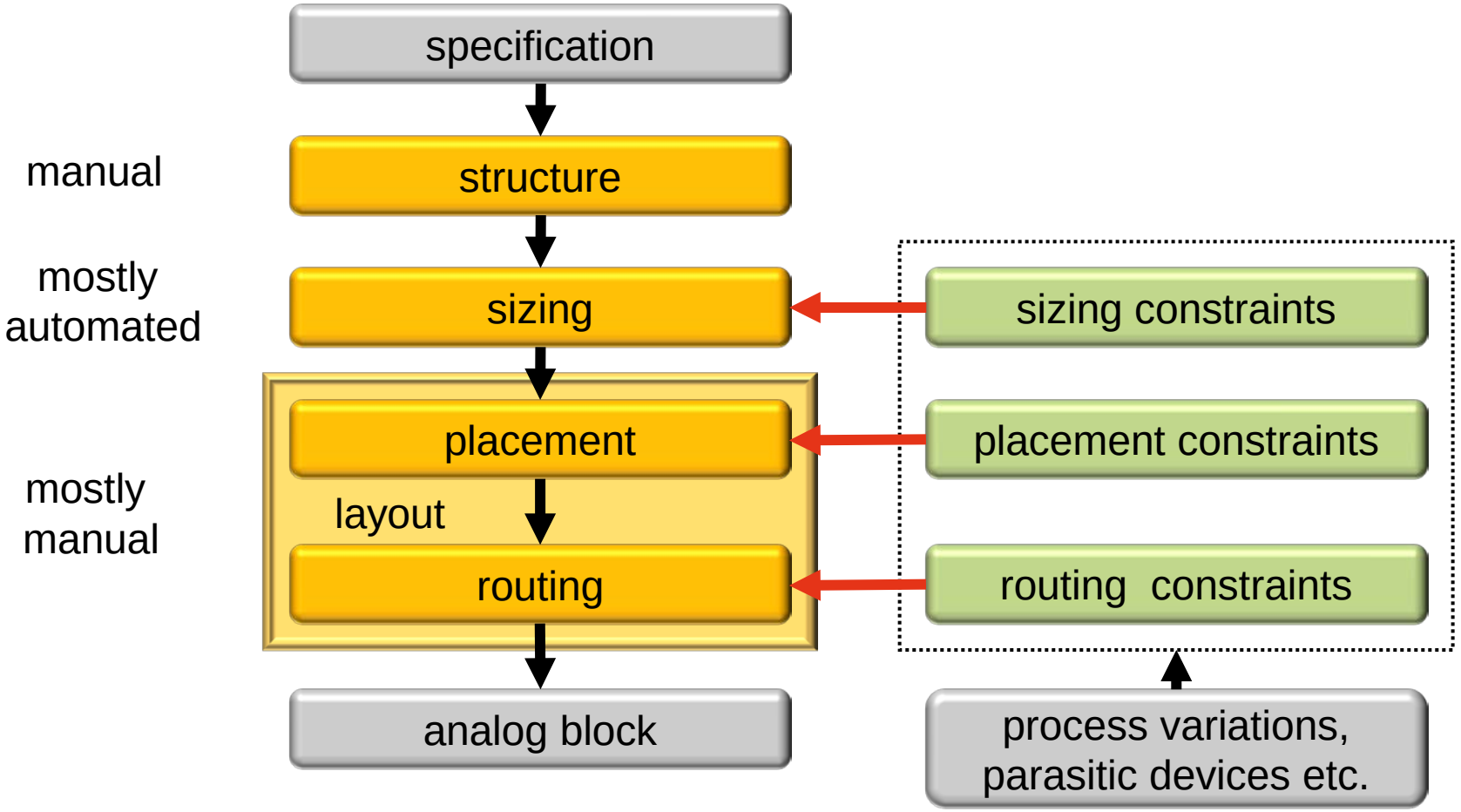
Overview

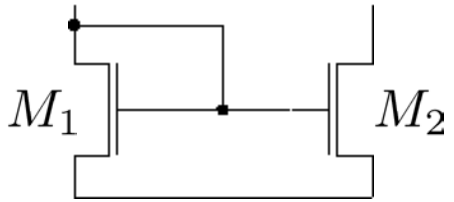
- Motivation: analog placement constraints
- Generation of hierarchical placement rules
- Experimental results
  - Comparison with industrial tool
  - Fully differential amplifier
- Conclusion

Constraints in Design Flow

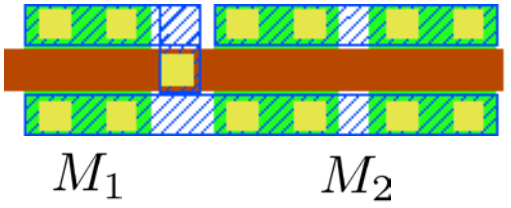


Placement Constraints – Device Matching

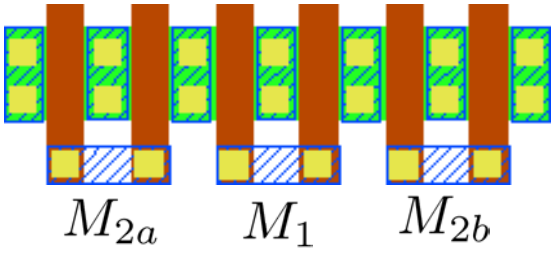
- Device matching:
  equal electrical properties
- Sources of mismatch, e.g.,
  - Distance effects
    (temperature, oxide thickness, ...)
  - Orientation effects
    (μ_0, skewed doping, ...)
- Countermeasures
  - Same variant and orientation
  - Parallel connections instead of larger transistors
  - Spatial proximity
- Common centroid



same variant



common centroid



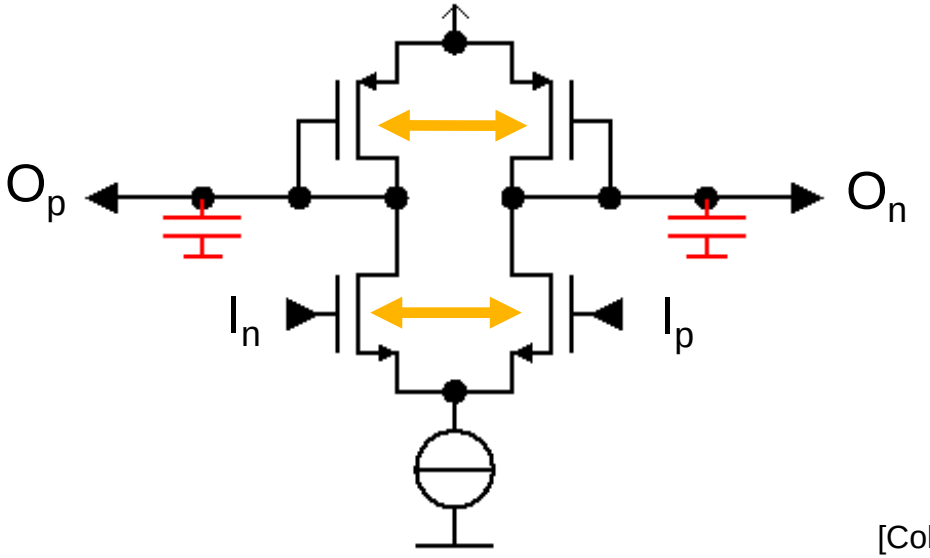
[Hastings: The Art of Analog Layout'01]

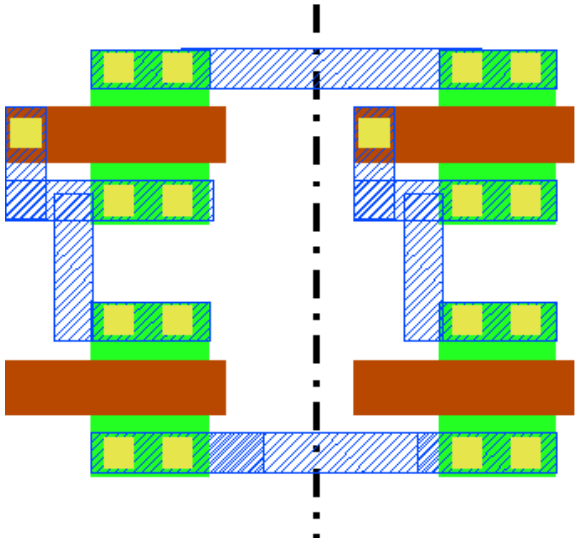
Placement Constraints - Symmetry

differential circuits: symmetrical behavior

device matching

“symmetrical” routing requires
“symmetrical” placement





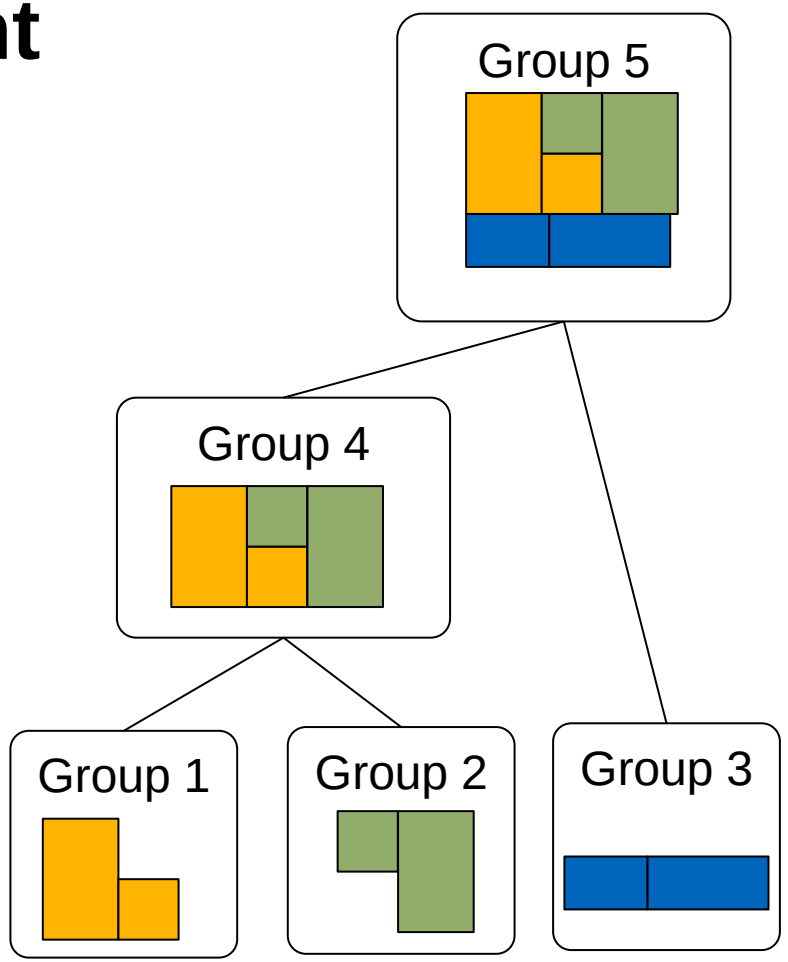
[Cohn et al.: Analog Device-Level Layout Automation’94]

State of the Art

- Sensitivity analysis
  - Parasitic devices → matching, symmetry
    [Malavasi et al. TCAD'96]
  - Net sensitivities → matching [Chen et al. IEE Proc. G'92]
- Graph isomorphism→ symmetry
  [Kole et al. ISCAS'94] [Hao et al. ICCCS'04]
- Building blocks→ matching (sizing) [Massier et al. TCAD'08]
- Retargeting using hierarchical symmetry
  [Bhattacharya et al. ASP-DAC'04]
- Circuit hierarchy not considered
  - Possibly missing constraints
  - Infeasible for hierarchical placement

Hierarchical Placement

- Plantage
  [Strasser et al., ICCAD'08]
- Placement generation controlled by inherent hierarchy
- Placement constraints within and among groups
  - Matching
  - Symmetry
  - Proximity
- Similar approach:
  [Lin et al., DAC'08]



hierarchy tree

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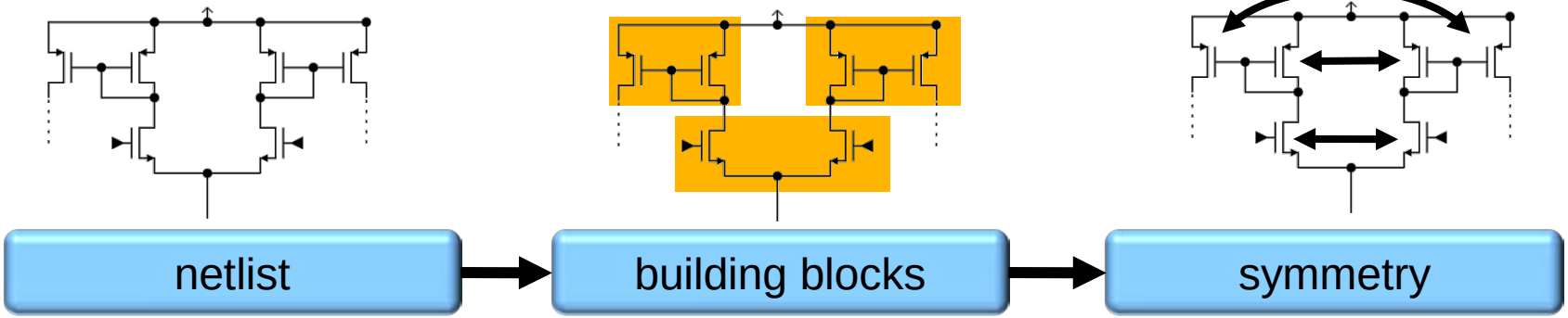
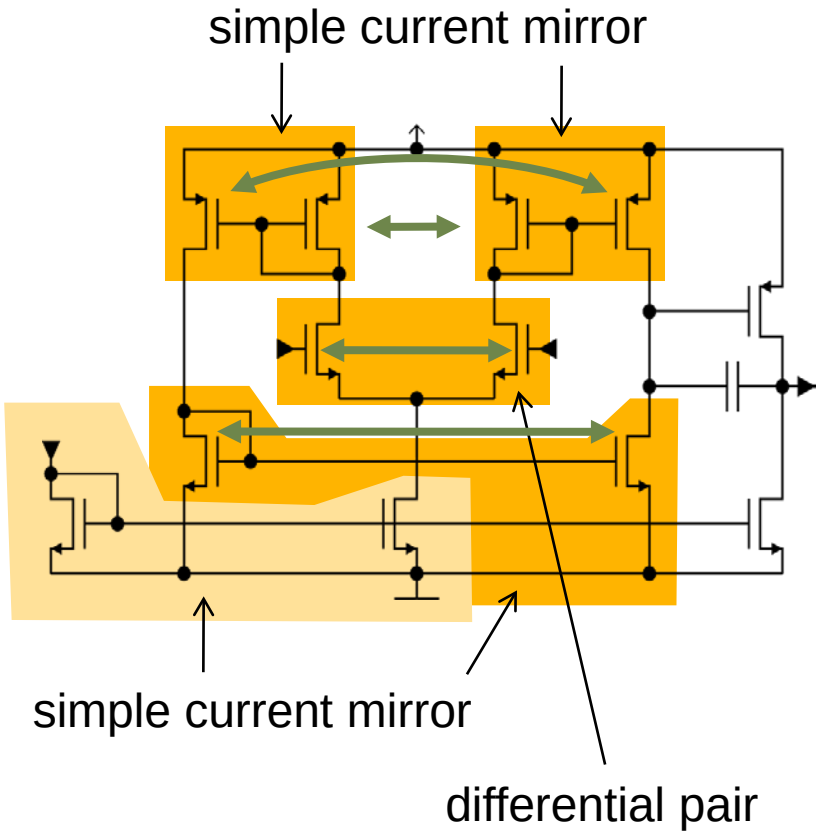
Flow Chart of New Approach

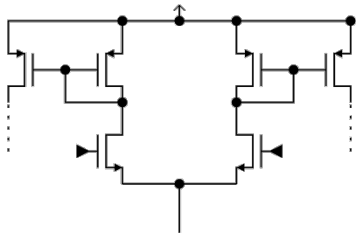


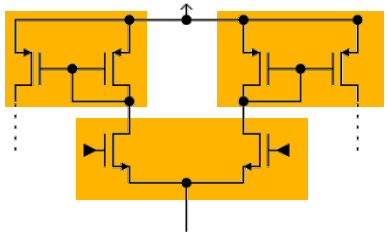
Automatic Structure Analysis

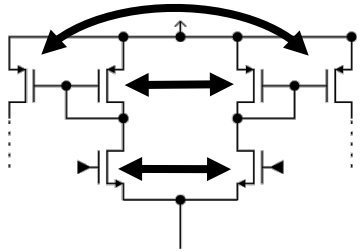
- Structure recognition
  - Comparison with building blocks from library
  - Resolution of ambiguities
  - [Massier et al. TCAD'08]
- Symmetry analysis
  - Propagation of symmetry-pairs starting from differential pair
  - similar to [Arsintescu et al. ICCD'96]

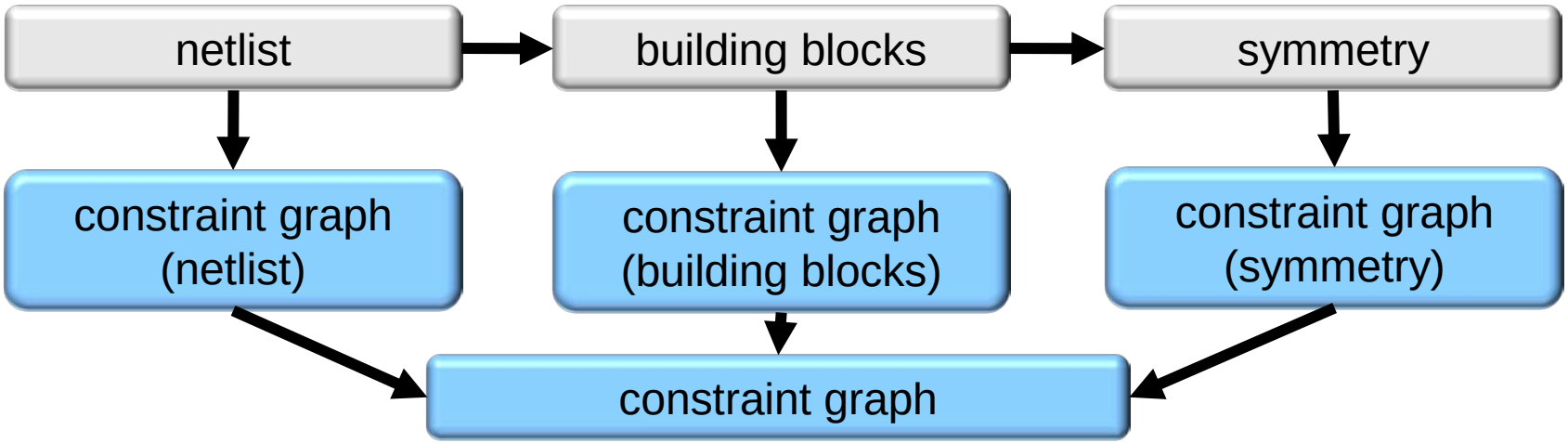


Flow Chart of New Approach







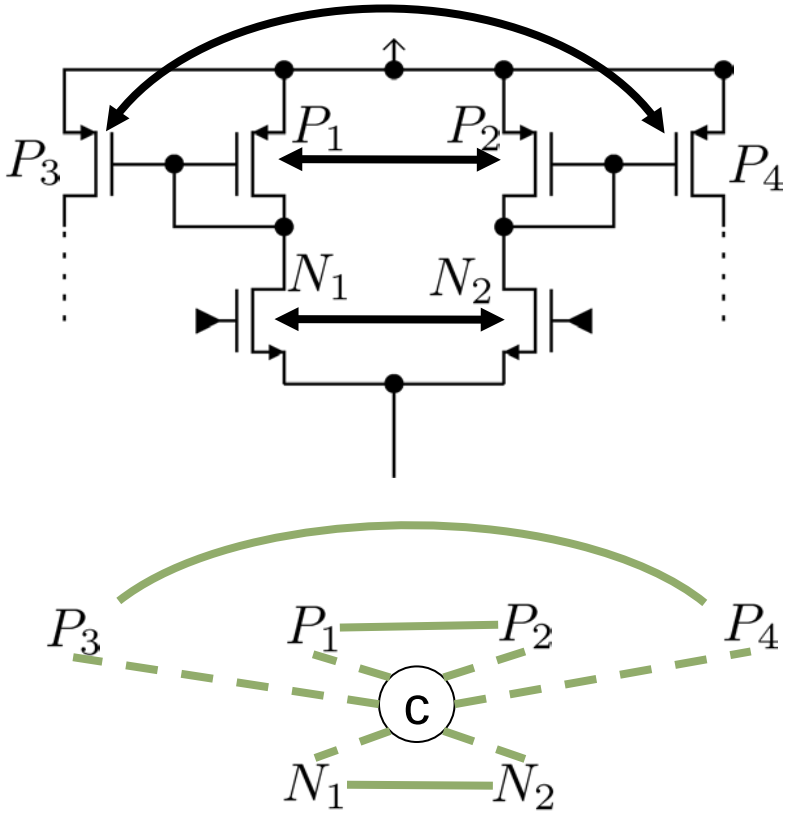


Constraint Graph (Symmetry)

- Symmetry pair→ matching constraint (symmetry)
- Symmetry pairs (d,d‘) of same axis → symmetry constraint

$$\forall_{(d,d')} \left(\frac{x_d + x_{d'}}{2} = c \ \wedge \ y_d = y_{d'} \right)$$

$x_d, x_{d'}$	device
$y_d, y_{d'}$	coordinates
c	axis coordinate



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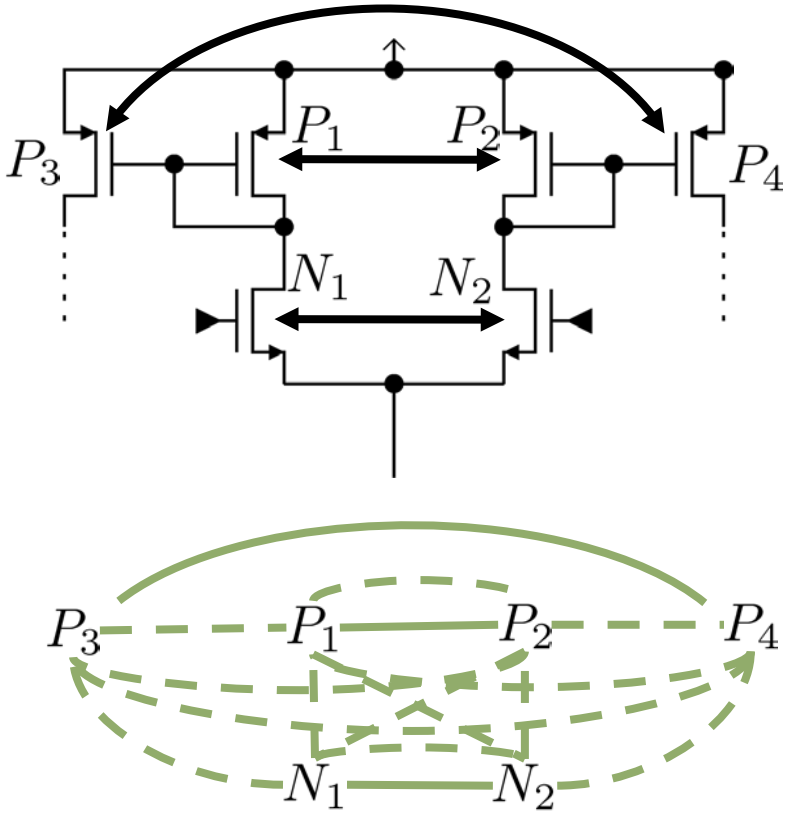
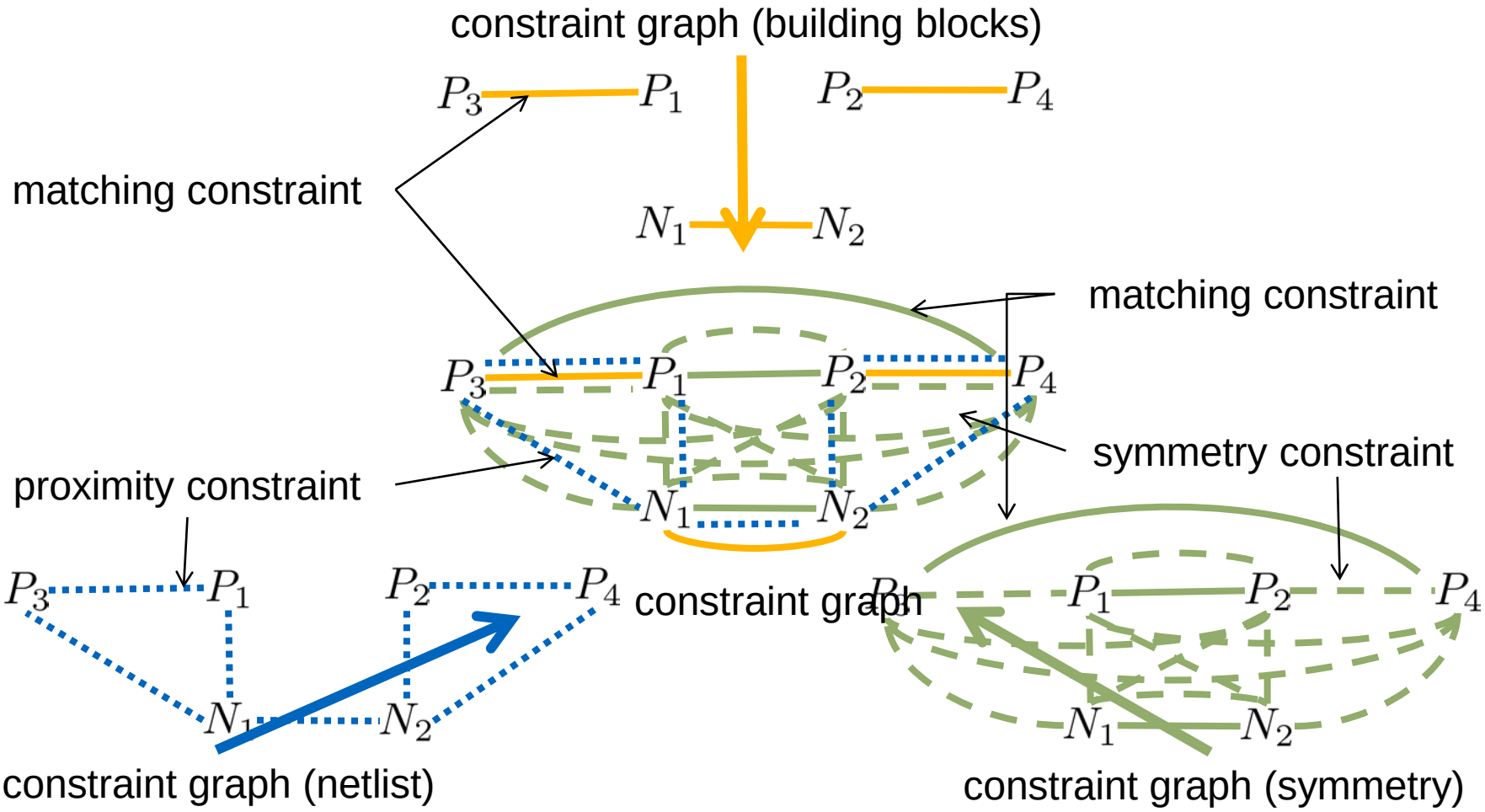
- Elimination of c → complete graph

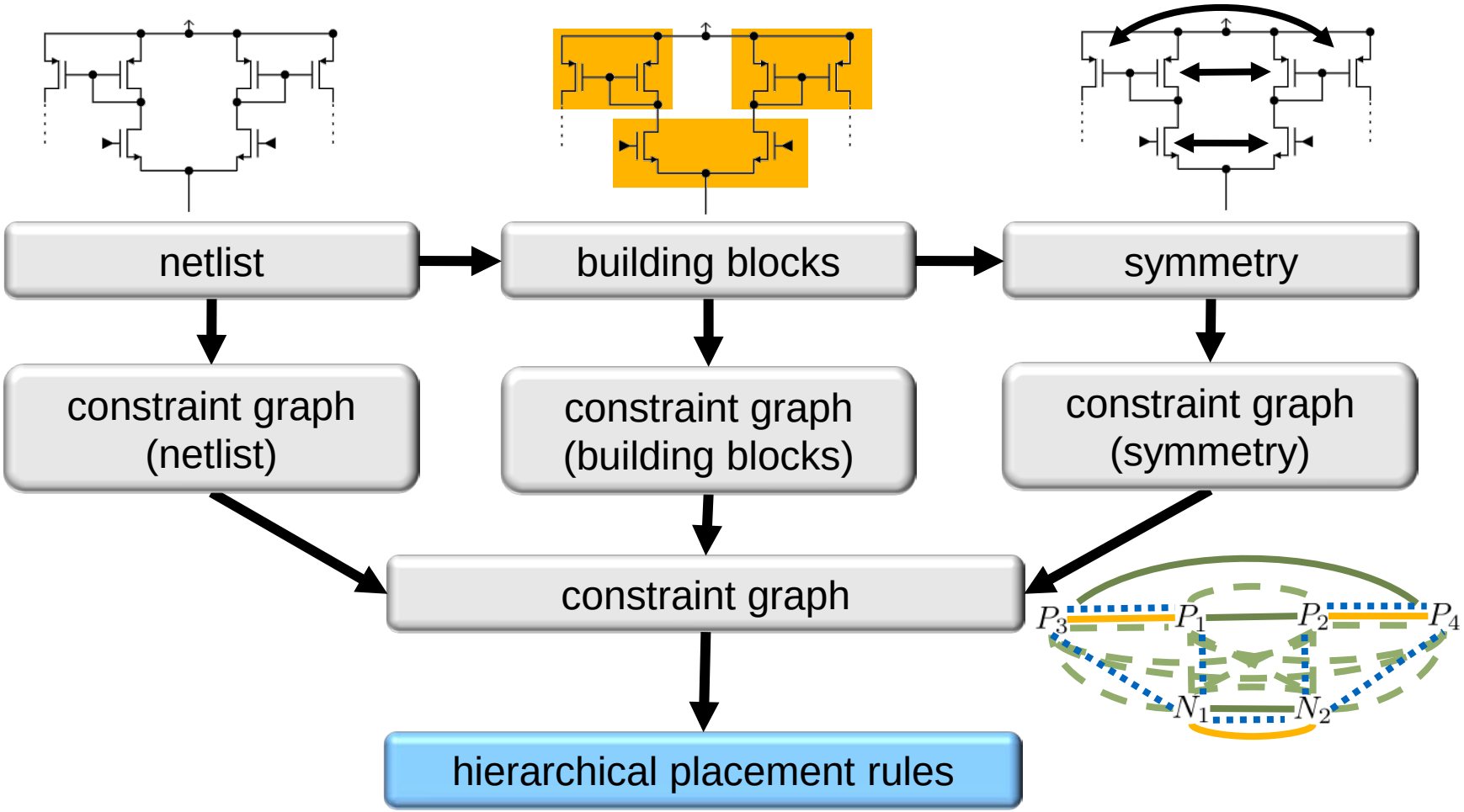


constraint graph (symmetry)

Constraint Graph

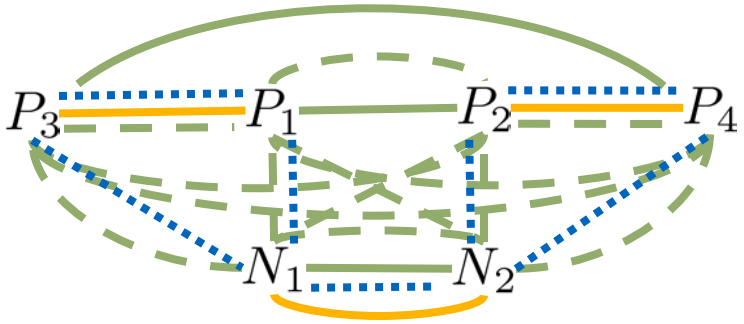


Flow Chart


netlist
building blocks
symmetry
constraint graph (netlist)
constraint graph (building blocks)
constraint graph (symmetry)
constraint graph
hierarchical placement rules
P_3
P_1
P_2
P_4
N_1
N_2

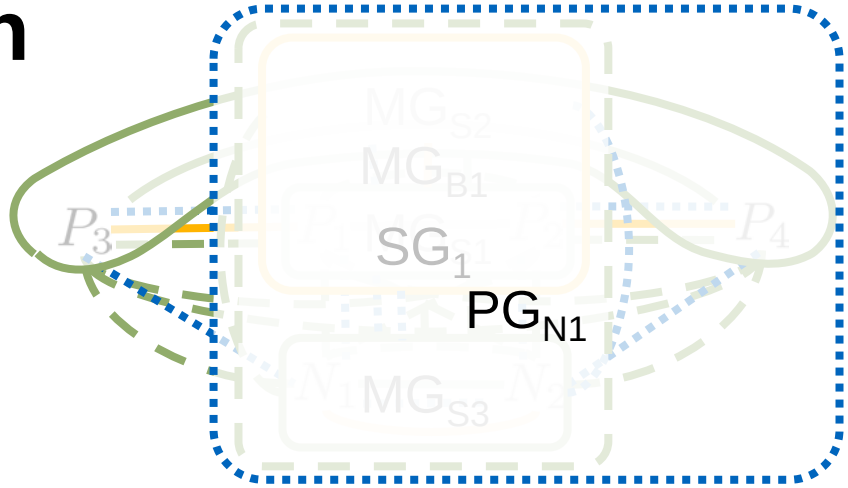
Conflict Avoidance

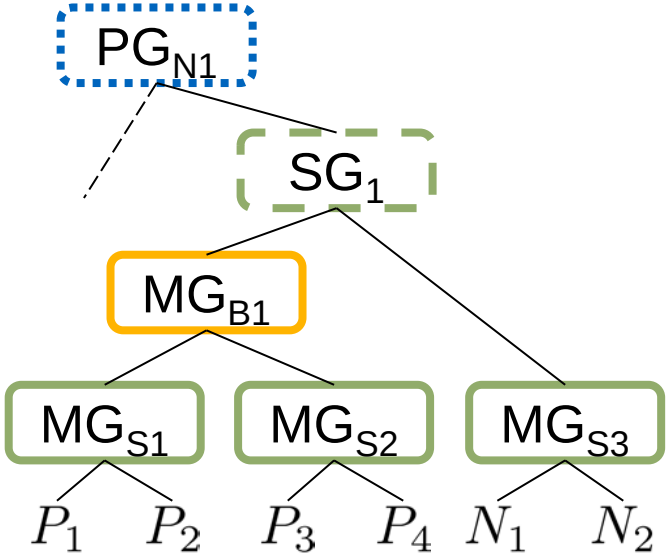
- Priority order T_I:
  1. Matching constraints (symmetry)
  2. Matching constraints (building blocks)
  3. Proximity constraints (building blocks)
  4. Symmetry constraints
  5. Proximity constraints (netlist)
- Criteria, e.g., differential principle



Hierarchy Generation

- Controlled by priority order T_I:
  1. Matching constraints (symmetry)
  2. Matching constraints (building blocks)
  3. Proximity constraints (building blocks)
  4. Symmetry constraints
  5. Proximity constraints (netlist)
- $MG_{S/B}$: Matching group (symmetry / building blocks)
- SG: Symmetry group
- PG_N: Proximity group (netlist)





Overview

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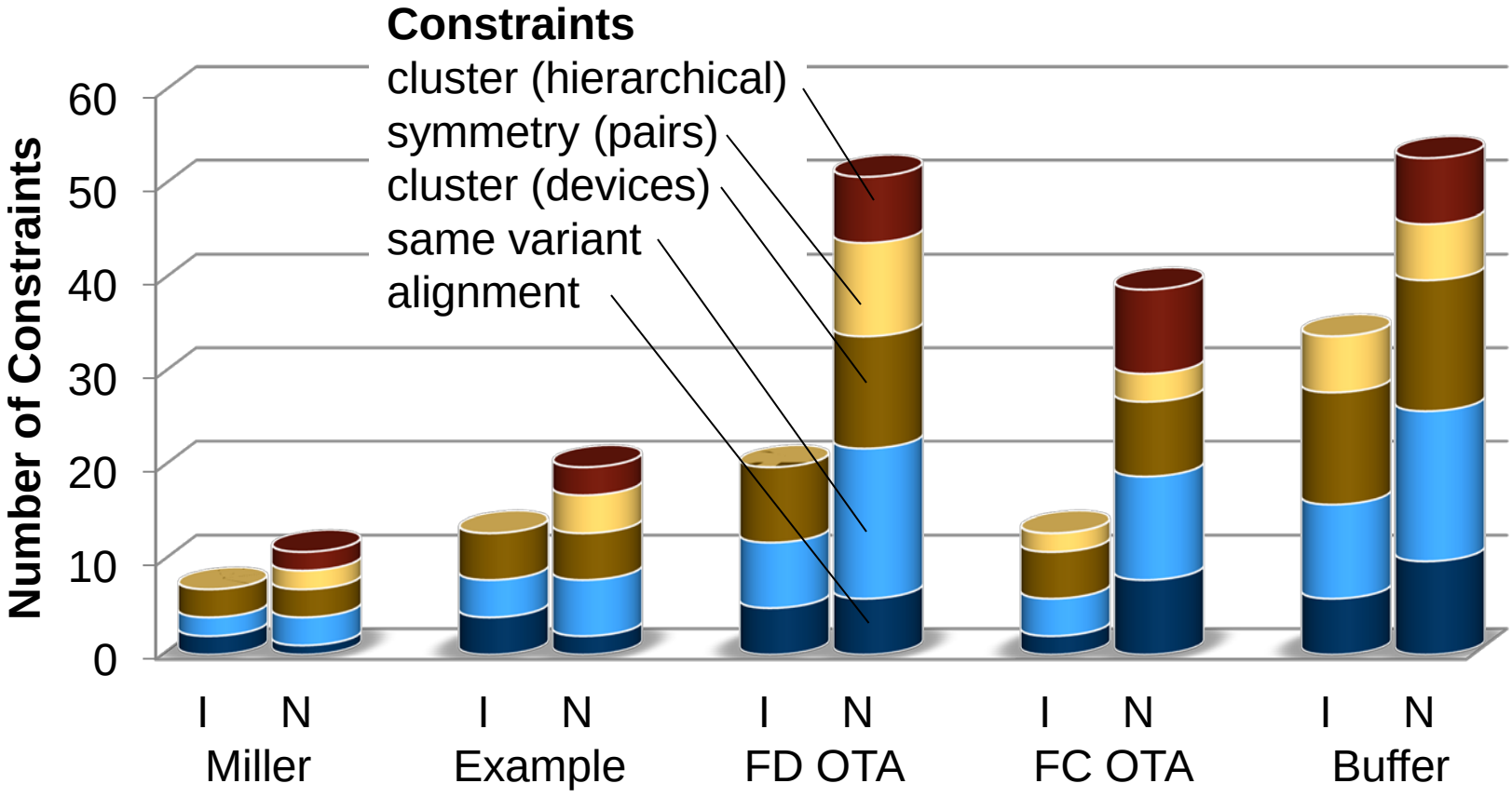
Hierarchy Generation

Circuit	Number of transistors	Groups		Runtime [s]
		Number	Size	
Miller[1]	9	5	2 – 4 (Ø 2,6)	0,14
Example	10	8	2 – 4 (Ø 2,5)	0,17
Fully Differential OTA[2]	30	19	2 – 5 (Ø 2,5)	0,46
Folded Cascode OTA[1]	22	17	2 – 3 (Ø 2,2)	0,31
Buffer[3]	42	21	2 – 14 (Ø 2,9)	0,65

- Runtime of placer ~ group size

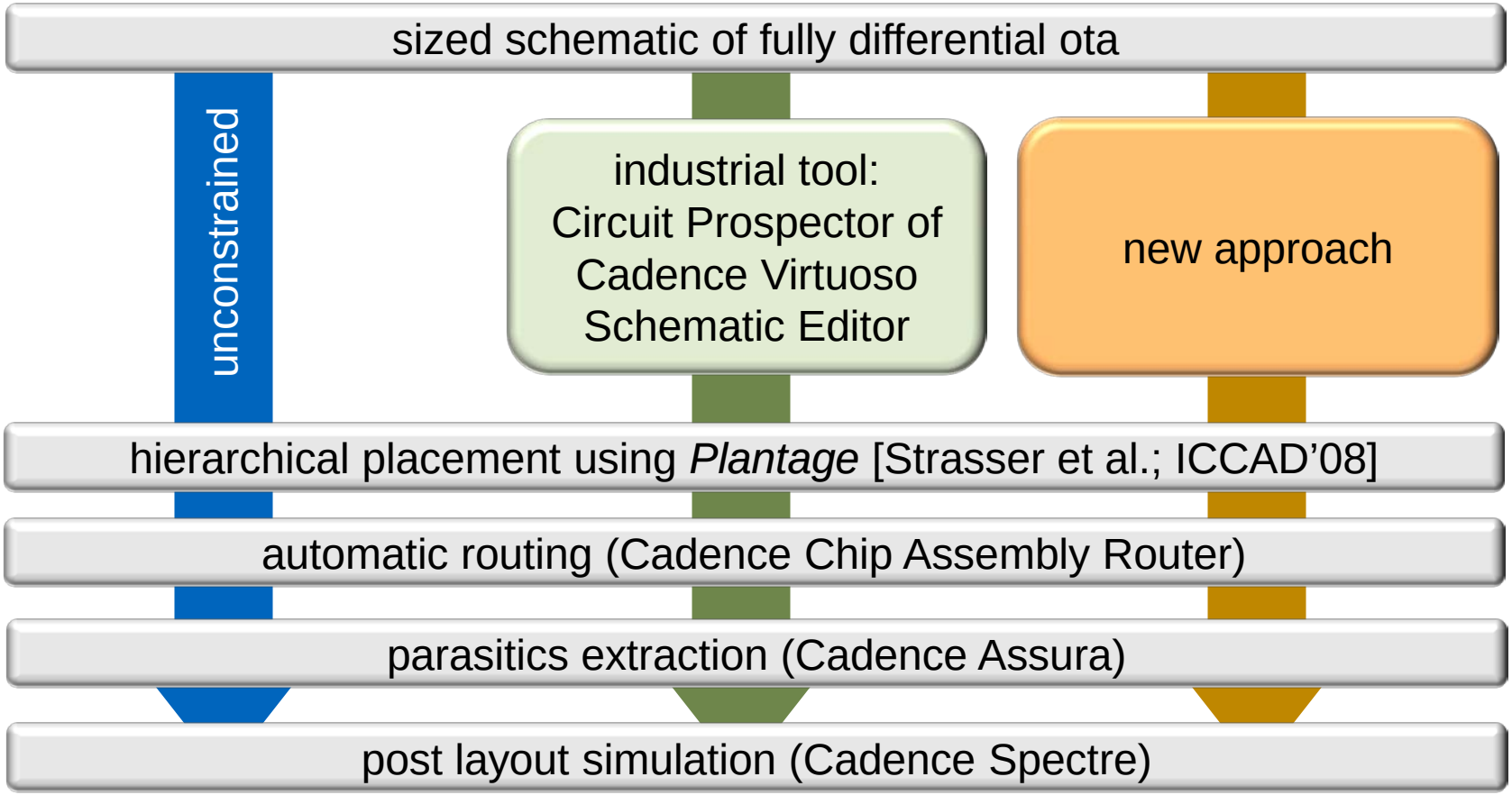
[1] [Laker, Sansen: Design of Analog Integrated Circuits 94]
[2] [Galdi et al. JSSC'08], [3] [Fisher et al. JSSC' 87]

Comparison with Cadence Virtuoso

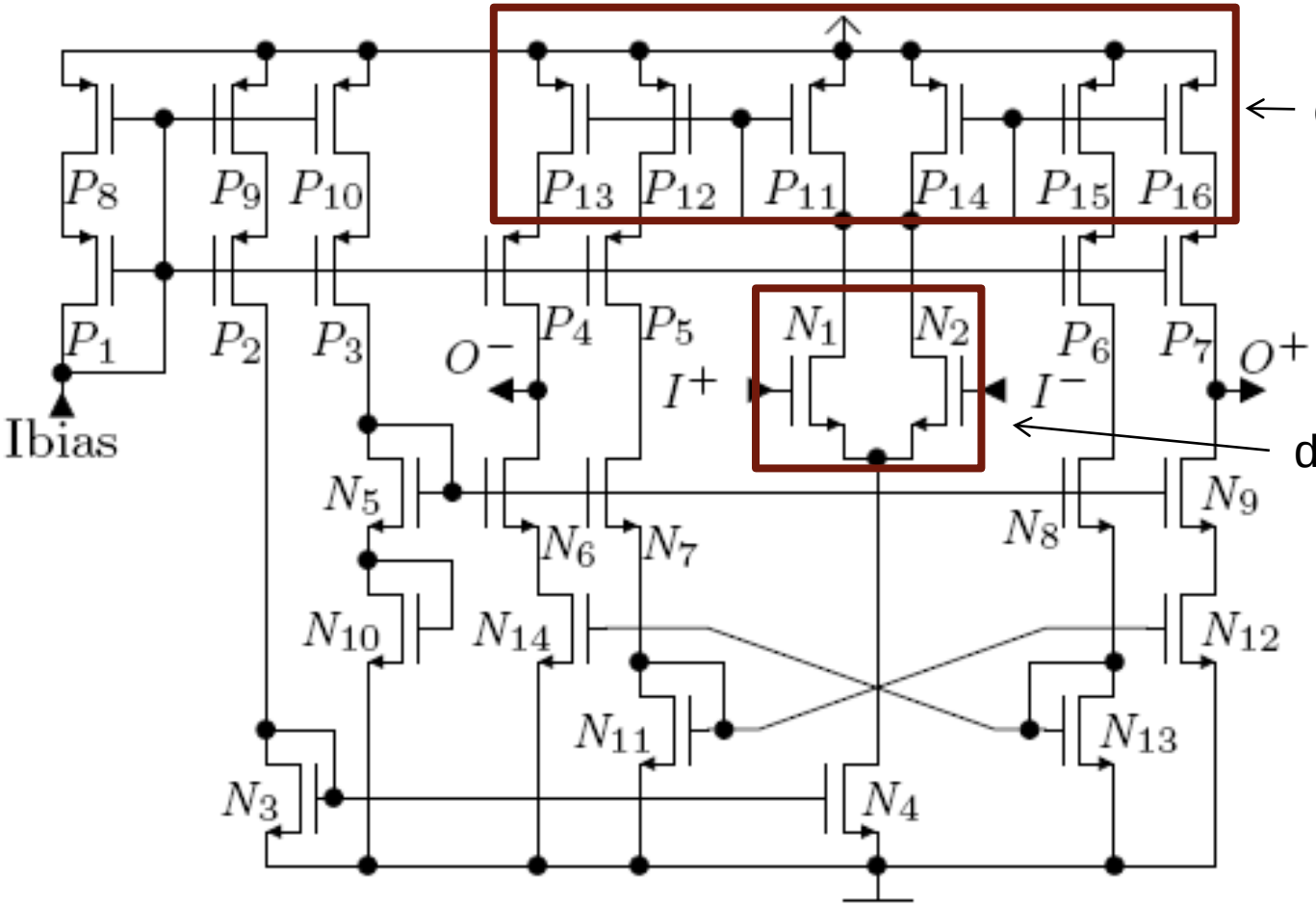


I: Cadence Virtuoso Schematic Editor XL; N: New approach

Experimental Set-up

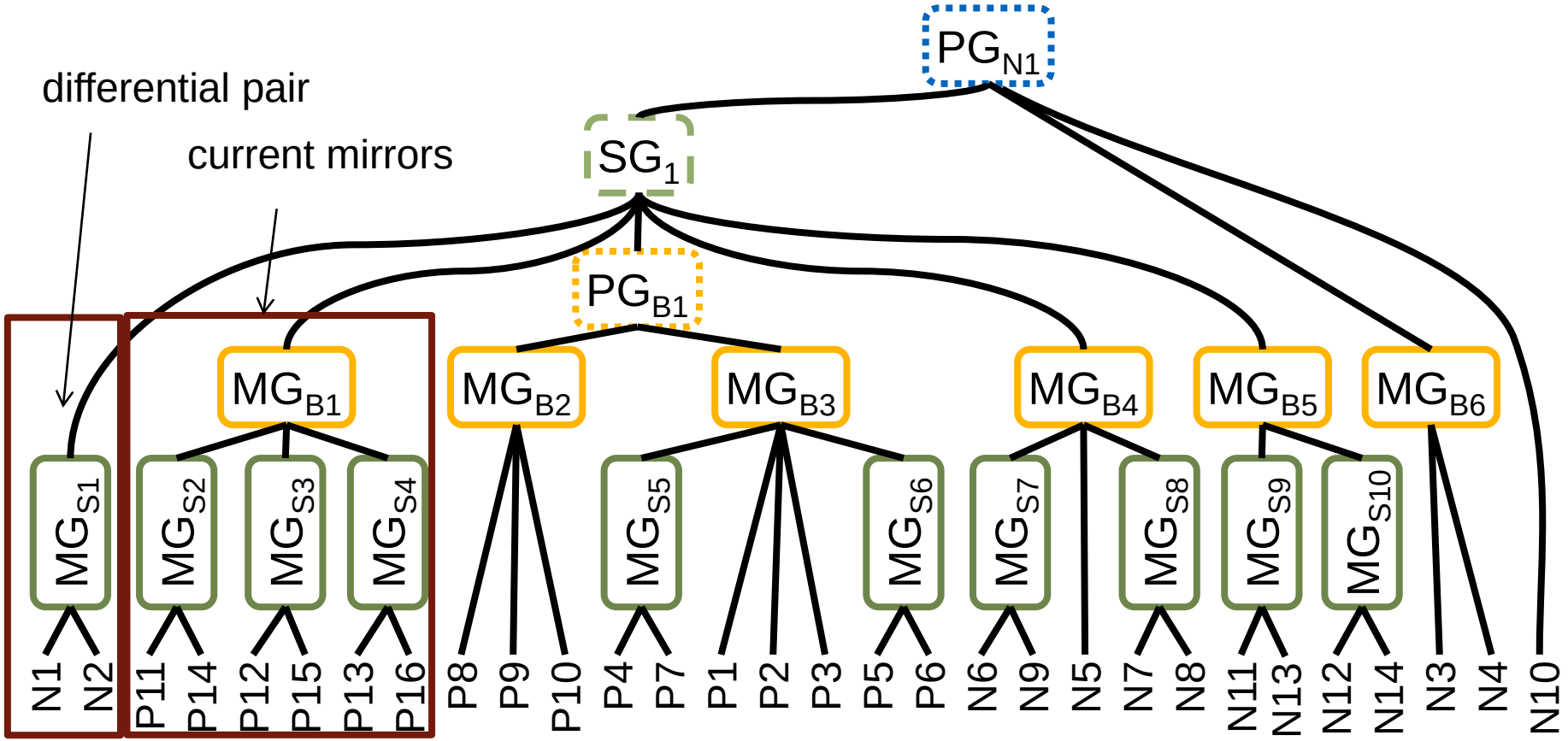


Schematic of Fully Differential OTA



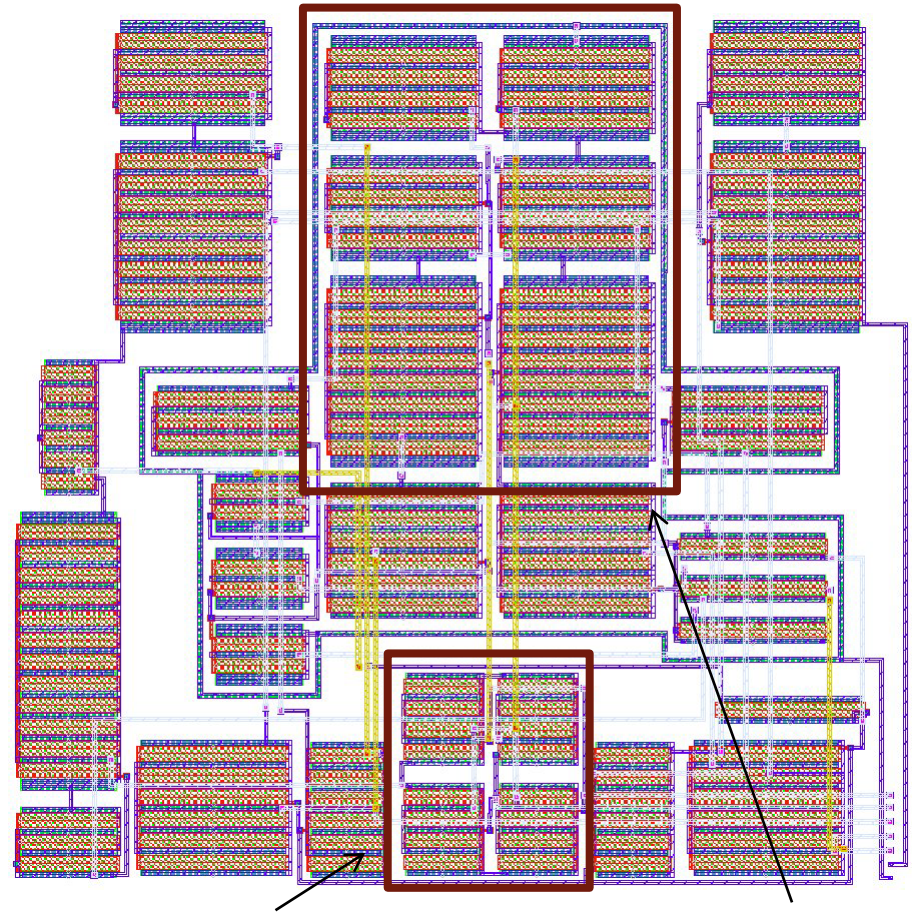
[Galdi & al., JSSC'08]

Hierarchical Placement Rules of FD OTA



$MG_{S/B}$: Matching group (symmetry / building blocks); SG: Symmetry group;
$PG_{B/N}$: Proximity group (building blocks / netlist)

Layout and Post Layout Simulation



Post layout simulation

perfor-mance	placement constraints: unconstr-ained	industrial	new approach
A_0 [dB]	72	72	72
f_0 [MHz]	22	22	22
V_{offset} [µV]	140	93	-6.6
CMRR [dB]	78	76	110

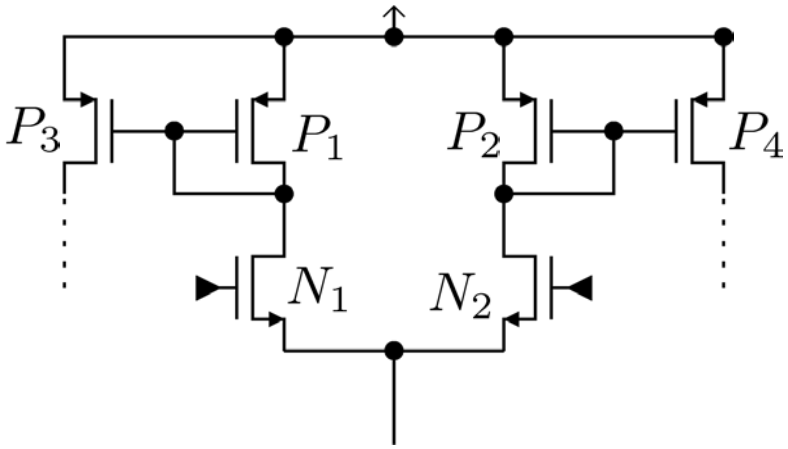
Conclusion

- Generation of hierarchical placement rules
  - Structure and symmetry analysis
  - Assignment of constraints to constraint graph
  - Generation of hierarchical groups
  - Constraints within and among groups: matching, symmetry, proximity
- Experimental results
  - Feasible for hierarchical placement approaches
  - Comprehensive constraint generation
  - Improved post layout performance

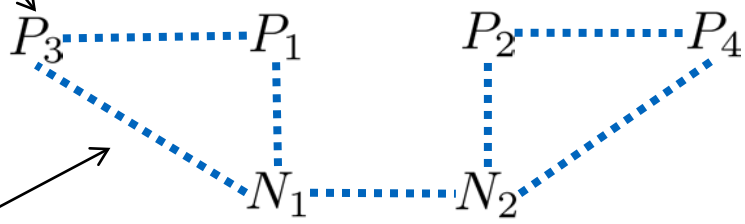
Thank you!

Constraint Assignment (Netlist)

- Connections → proximity constraints (netlist)
- Beneficial for routing



Nodes = Devices

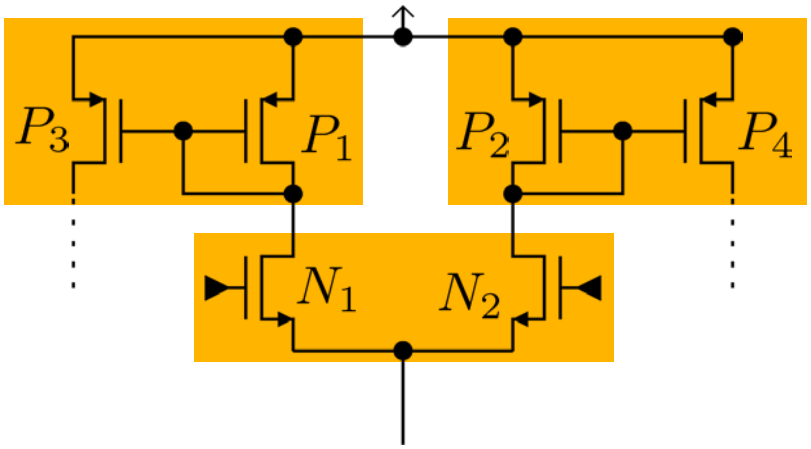


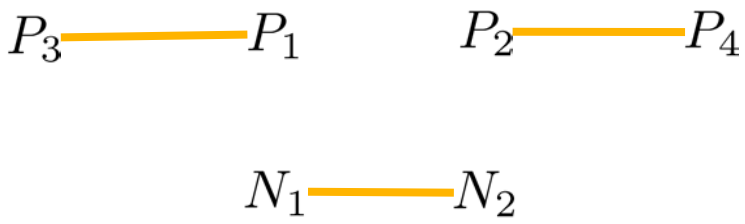
Edges = Constraint Requirements
Here: Proximity Constraint (Netlist)

Constraint Requirement Graph (Netlist)

Constraint Assignment (Building Blocks)

- Two transistor blocks → matching constraints (building blocks)
- Larger blocks: additional proximity constraint (building block)



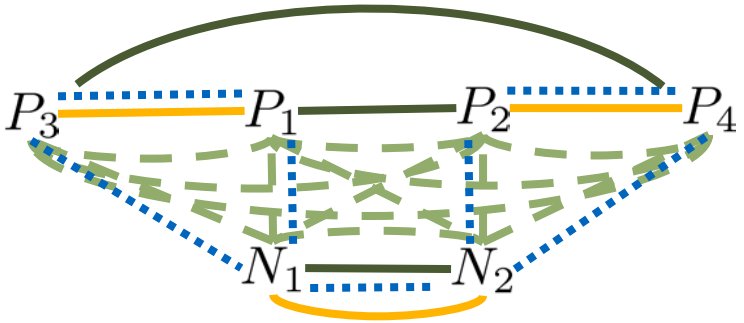


Requirement Graph (Building Blocks)

Conflict Avoidance

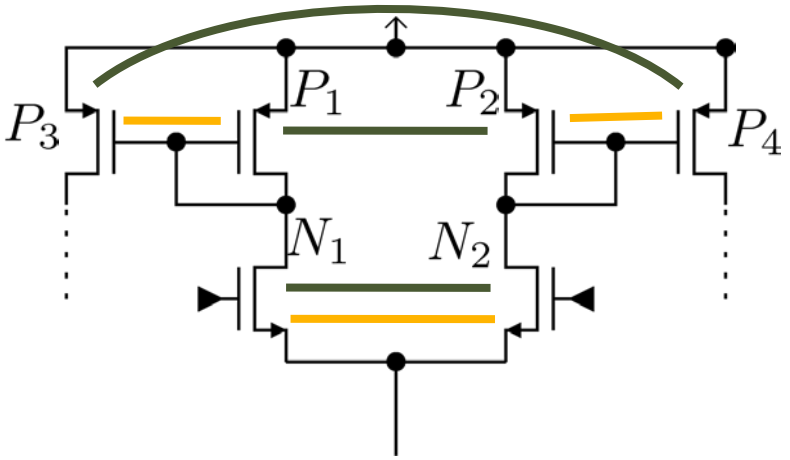
Priority order T_I:

1. Matching constr. (symmetry)
2. Matching constr. (building b.)
3. Proximity constr. (building b.)
4. Symmetry constr.
5. Proximity constr. (netlist)

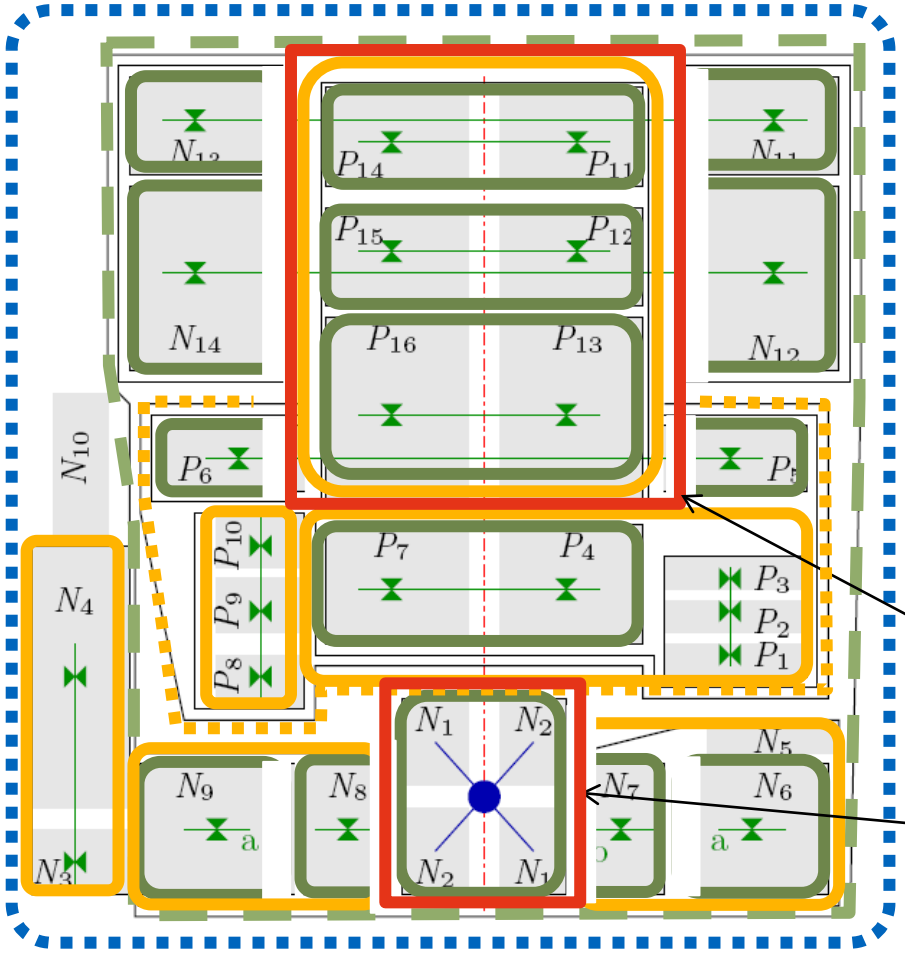


Criteria:

- Differential principle
- Increasing size



Generated Placement



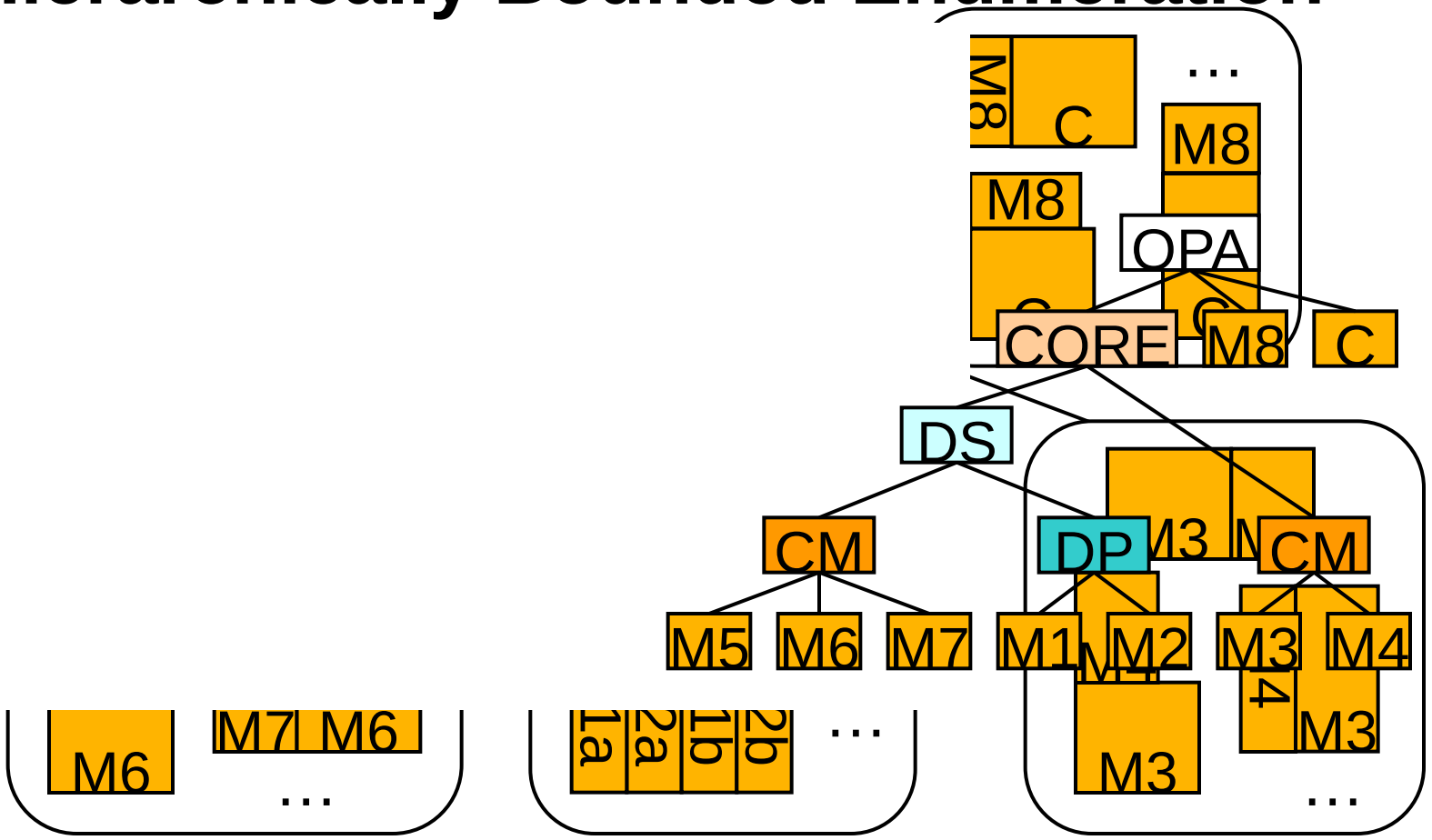
Placement Constraints:

- alignment
- common centroid
- symmetry axis
- group

current mirrors

differential pair

Hierarchically Bounded Enumeration



Enumeration of placements of fundamental module sets

Enhanced Shape Functions

- Hierarchical approach
- Good for **semi-automatic** layout generation
- High flexibility
- Enhanced shape function for each node of hierarchy
- Close proximity of modules is achieved by hierarchy