#### IBM Corp.

# What Makes A Design Difficult to Route

Charles J. Alpert, Zhuo Li, Michael Moffitt, Gi-Joon Nam, Jarrod Roy, Gustavo Tellez

#### What Does This Man and a Router Have in Common?



Young math whiz

Discovers computer programming

Drops out of Harvard

**Starts Microsoft** 

Works really hard

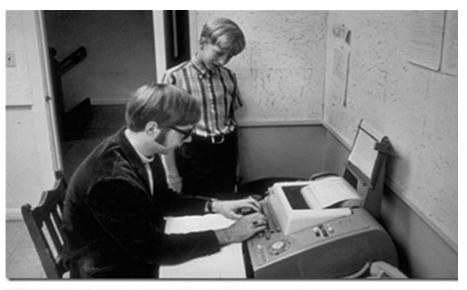
Becomes very rich

### Bill's Opportunities

### **ASR-33 Teletype**



1968: 8th grade



1968: Bill Gates (standing) and Paul Allen working at the computer terminal at Lakeside school





1955

#### Some Math Whiz, Computer Programmer, Hard Working Guys



Bill Gates Oct. 1955



Steve Jobs Feb. 1955



Bill Joy Nov. 1954



Scott McNealy Nov. 1954

Eric Schmidt Apr. 1955

### What's the Difference Between These Guys?

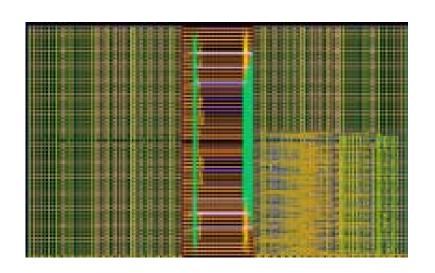




1973

1969

#### What Does a Router Have in Common with Bill Gates?

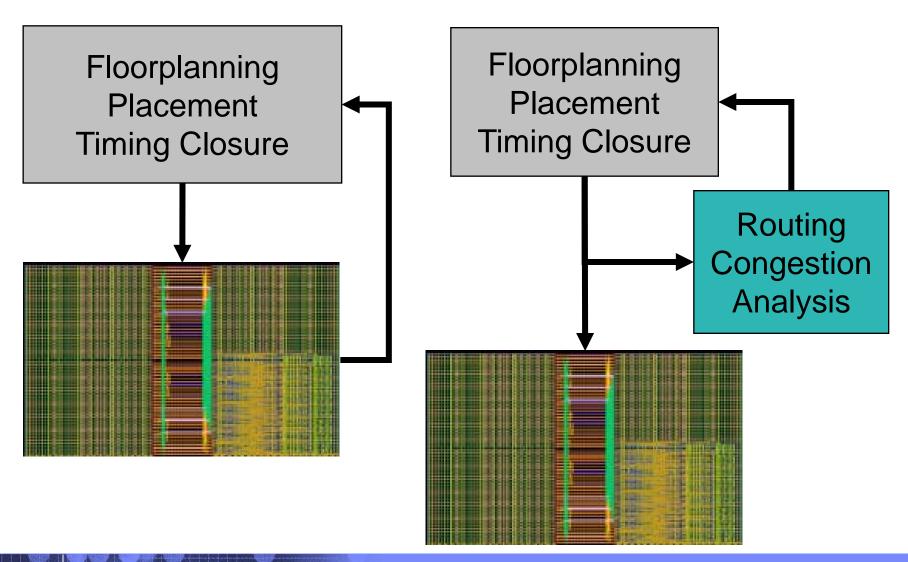




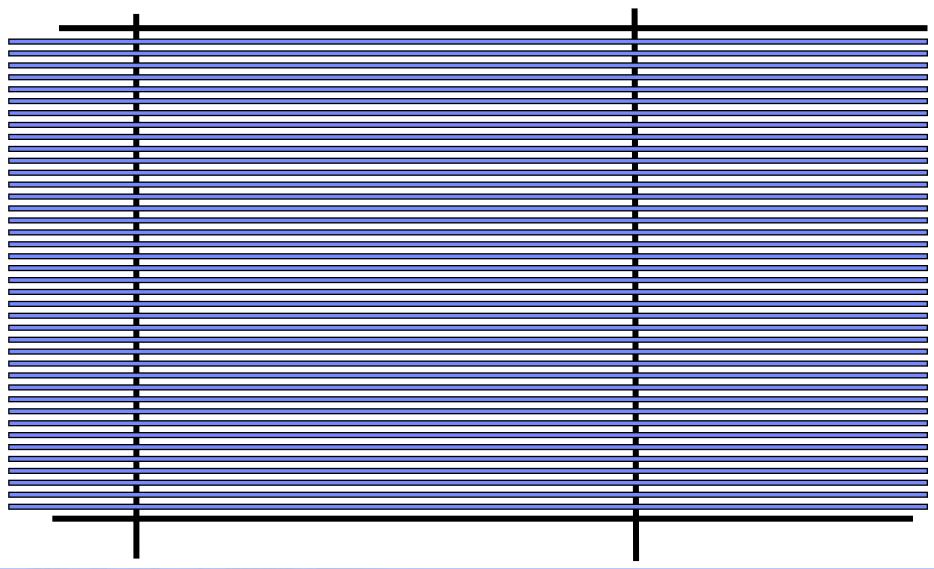
Give them the opportunity to succeed, and they will

Take away the opportunity to succeed, and they won't

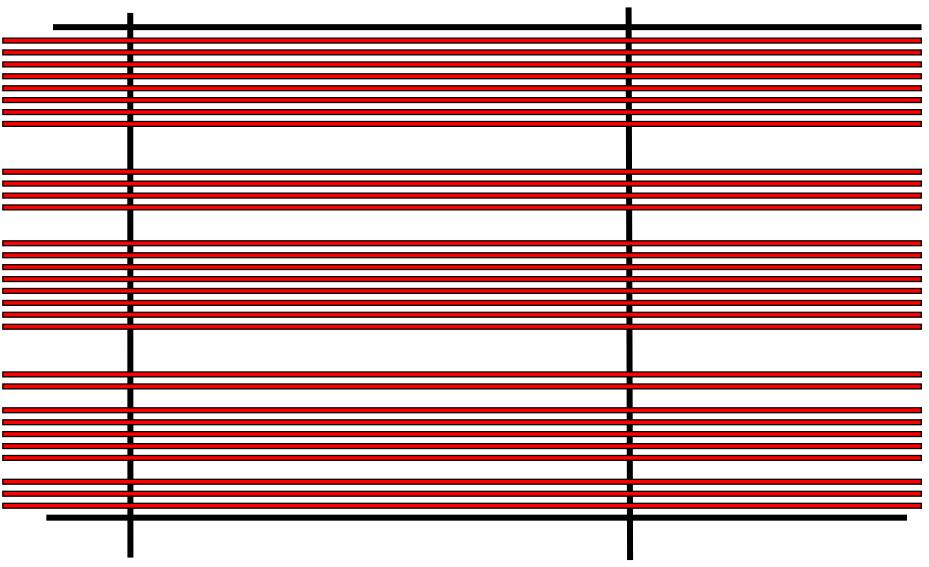
#### Routing is From Venus, Congestion Analysis is From Mars



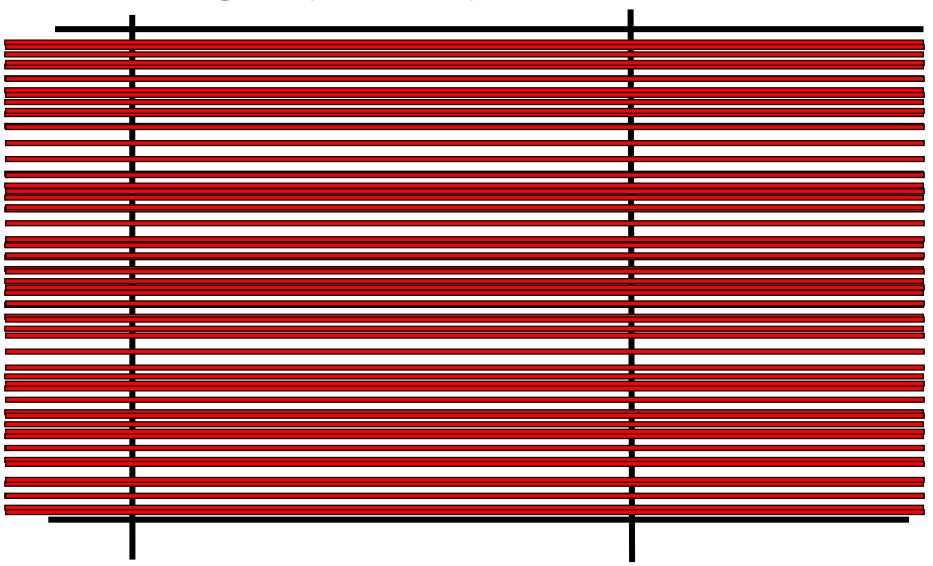
### Measuring Routing Quality (40-track per gcell)



### Routable gcell (75% full)

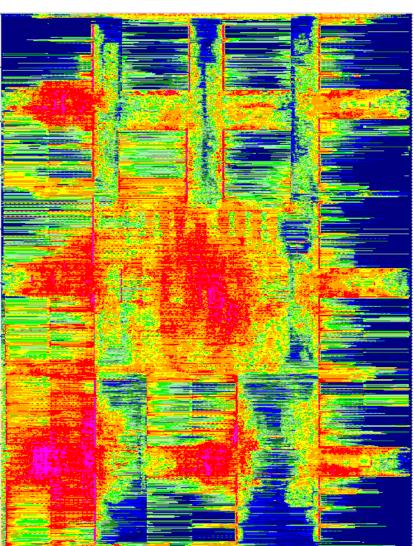


### Unroutable gcell (150% full) – 20 Nets of Overflow

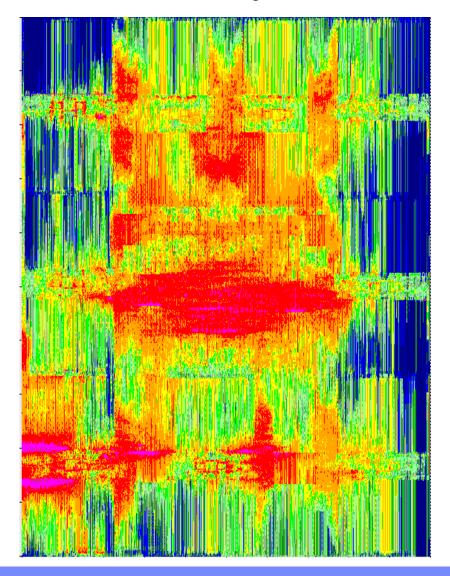


### **Example Congestion Map**

Horizontal Congestion



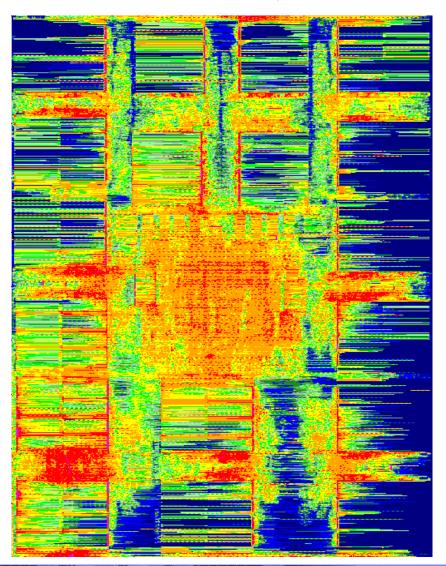
**Vertical Congestion** 

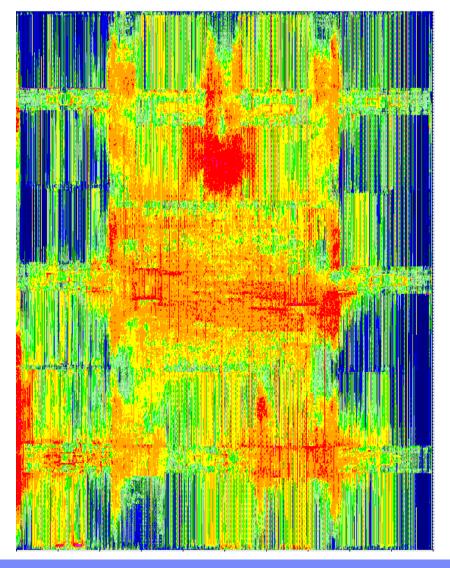


### Congestion Map with Better Physical Synthesis

**Horizontal Congestion** 

**Vertical Congestion** 





### **Common Routing Metrics**

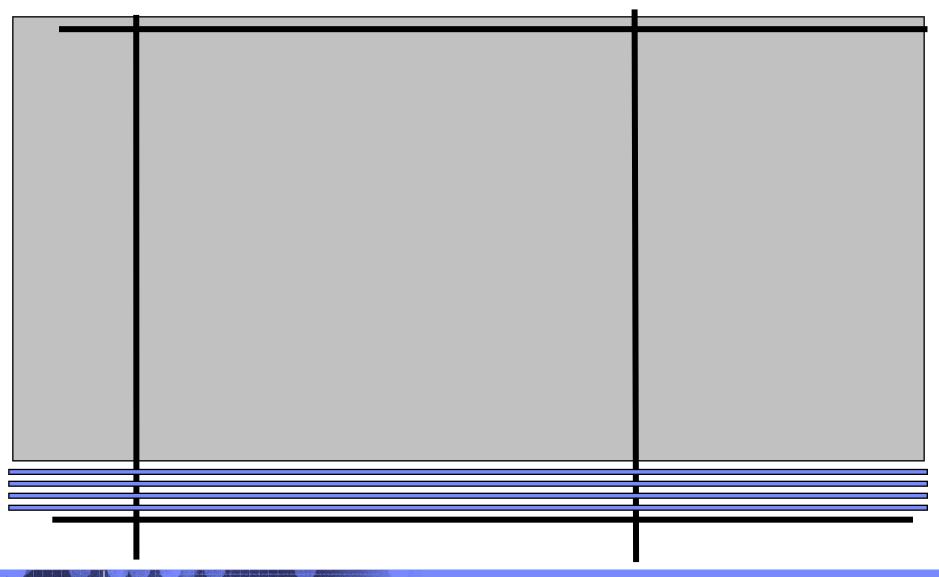
Number of Overflow Nets = Number of Nets Over 100% Congested

Number of nets over 90% congested

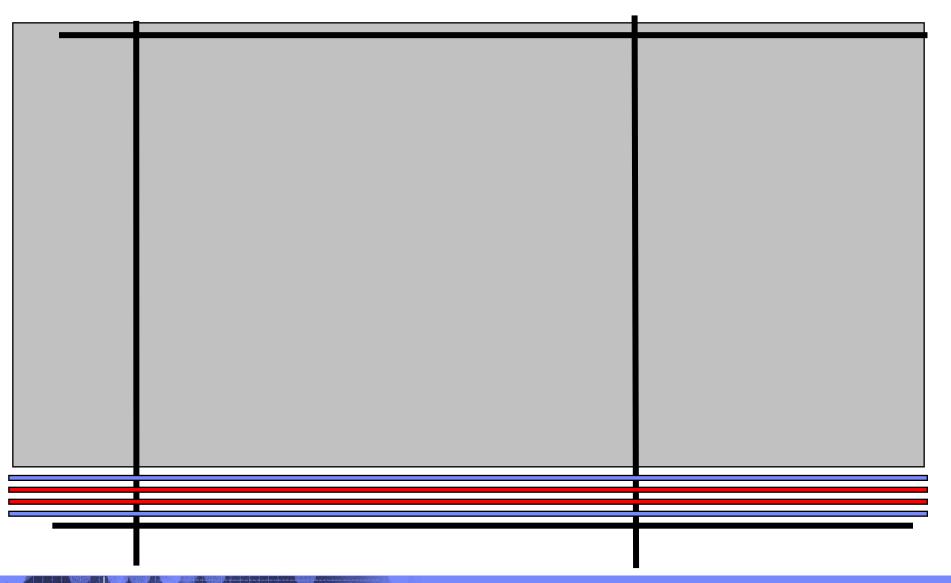
Number of nets over 80% congested

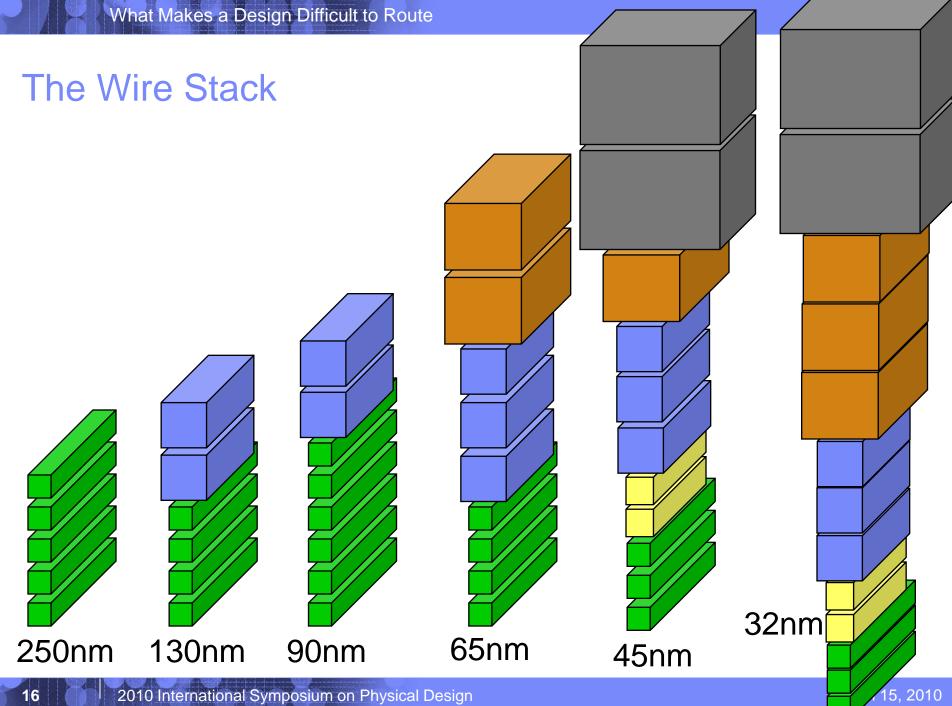
Average congestion of 20% worst gcells

### Handling Routing Blockages

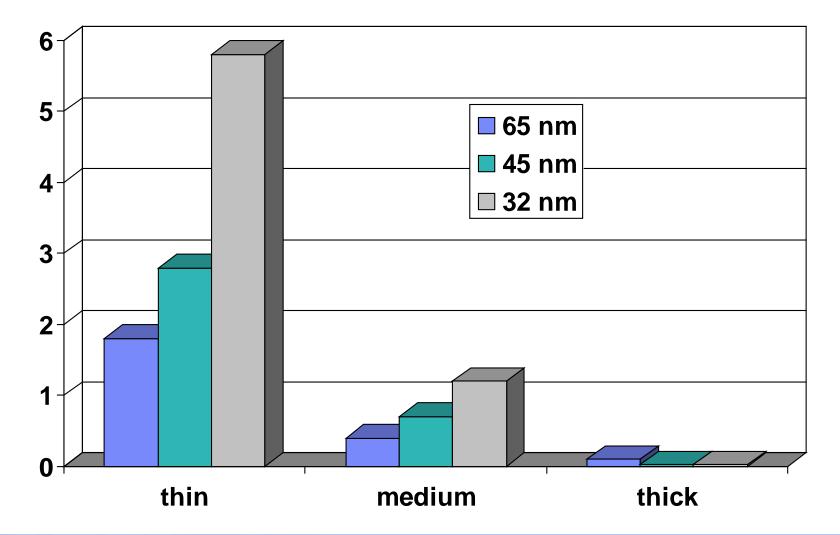


#### 50% Full or 95% Full?

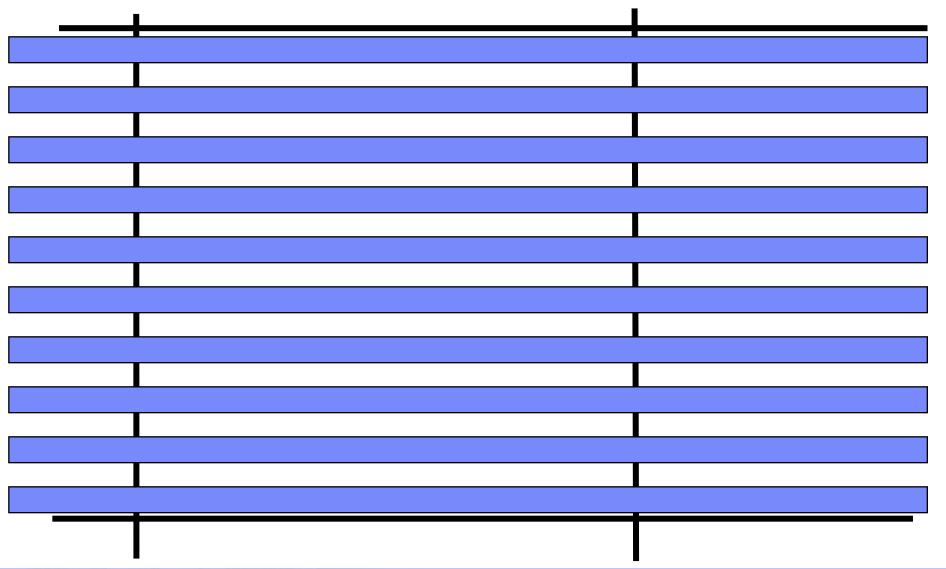




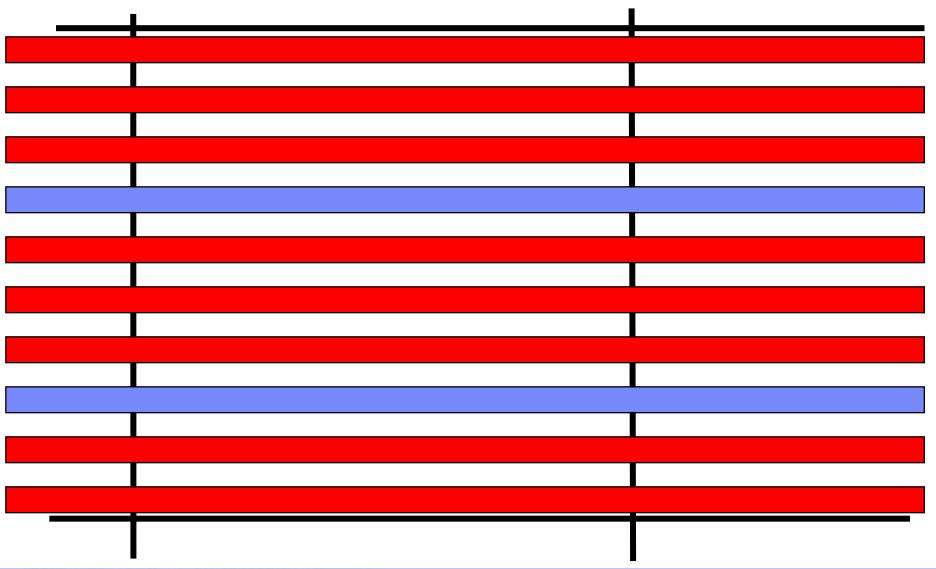
### Resistance per mm



### Routing Tracks on 4X Metal



### Only 2 Tracks Left, but Not Congested



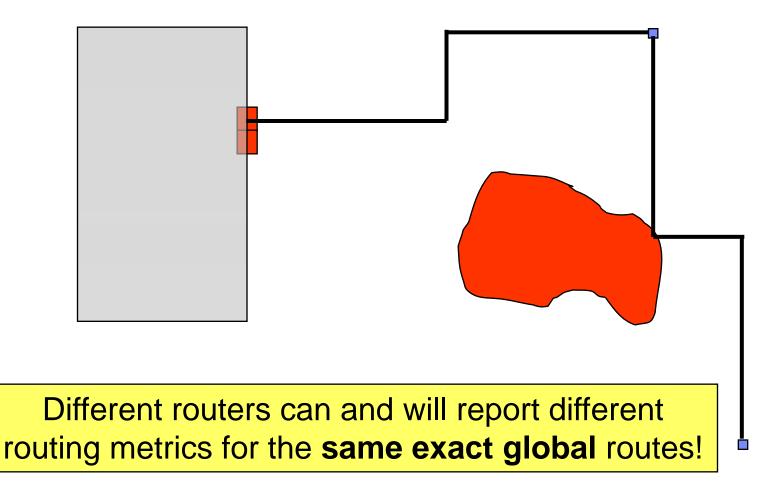
### Routing Tracks on 10X Metal



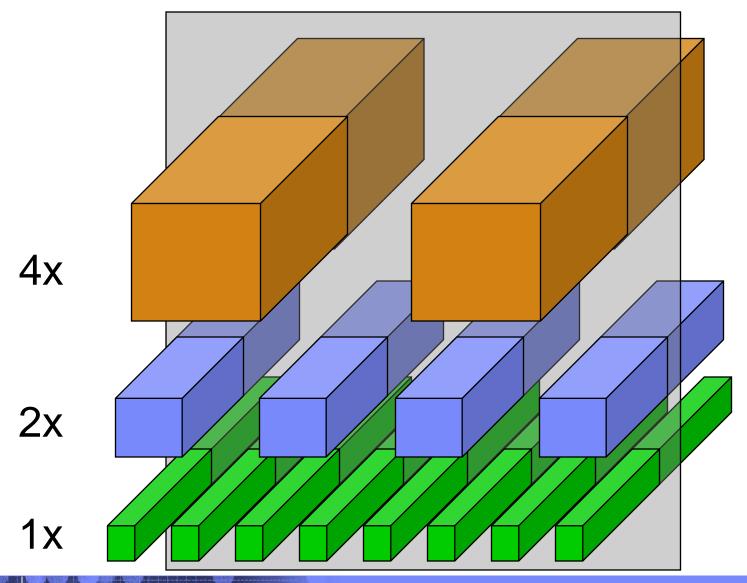
### Routing Tracks on 16X Metal



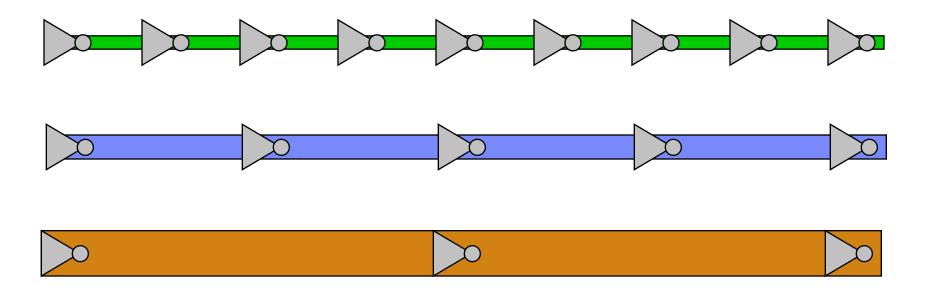
### Is This Net Congested?



### Cross section of a gcell

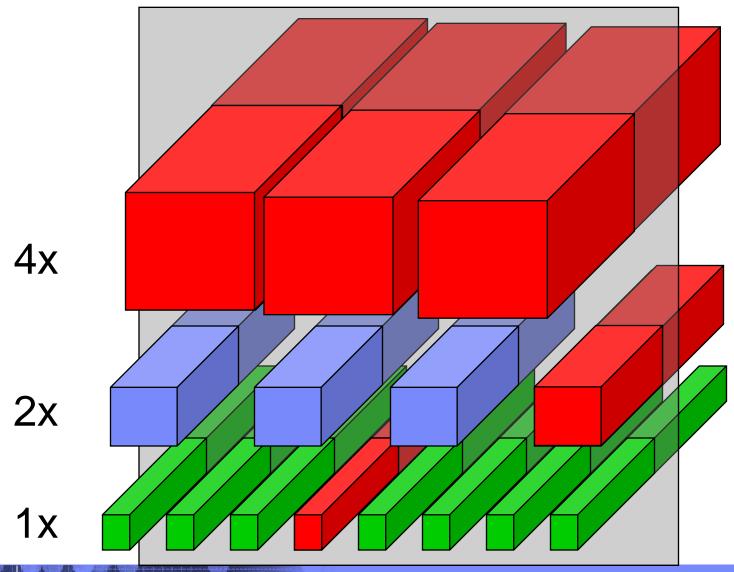


### Timing Closure Constrains The Router



Layer assignment / wire sizing assigns constraints for the router

### Is This a Congestion Problem?



#### Is It Routable?

$$Avg 20\% = 89.1$$

$$\#$$
nets >  $100\% = 9532$ 

$$\#$$
nets > 90% = 25785

$$Avg 20\% = 83.5$$

$$\# nets > 100\% = 532$$

$$\#nets > 90\% = 2785$$

$$Avg 20\% = 81.7$$

$$\#$$
nets >  $100\% = 3942$ 

$$\#nets > 90\% = 11880$$

$$Avg 20\% = 78.2$$

$$\#$$
nets >  $100\% = 16$ 

$$\#$$
nets > 90% = 753

### Congestion Analysis Versus Routing

## **Congestion Analysis**

**Probabilistic** 

Route Fast



No Scenic A Little Scenic

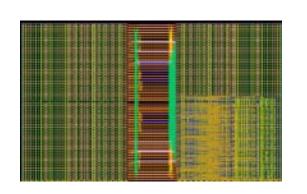
Completely Scenic

Over Blockages

Around Blockages

Obey layer constraints

May violate layer constraints



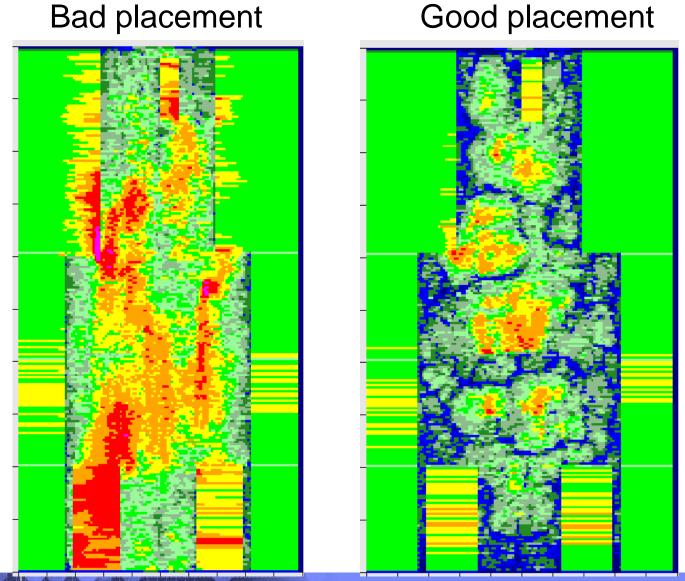
**Route Carefully** 

Completely Scenic

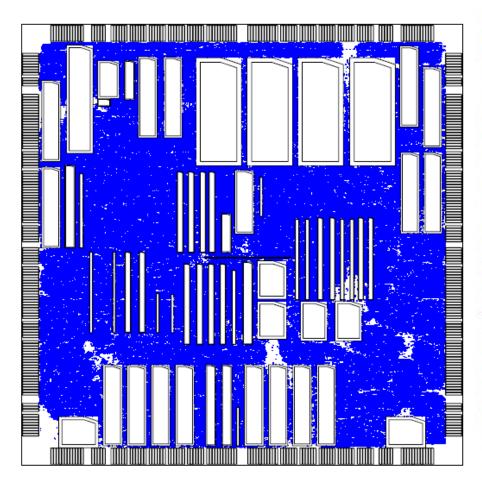
Around Blockages

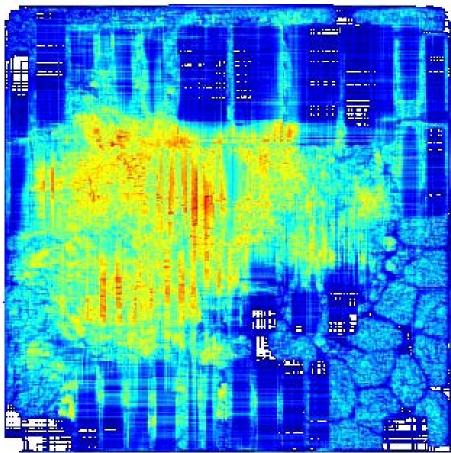
May violate layer constraints

### Minimizing Wire Generally Improves Congestion

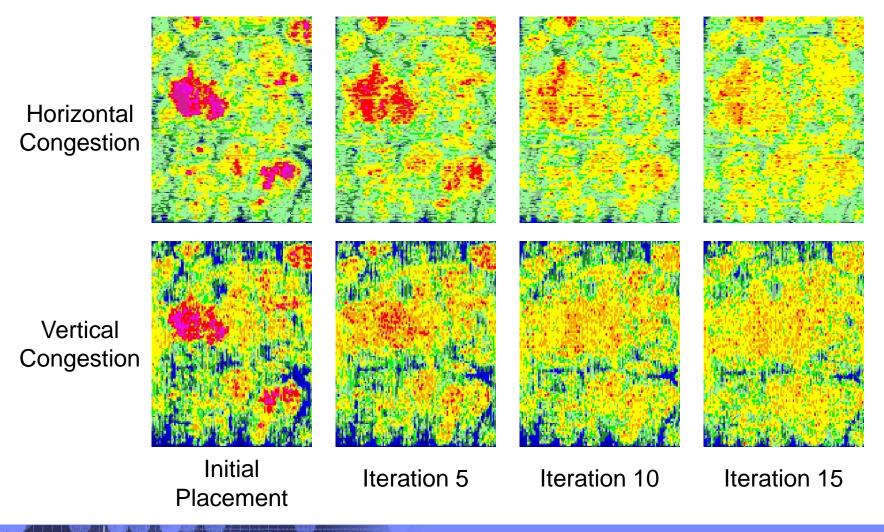


### Spread it Uniformly Doesn't Always Work



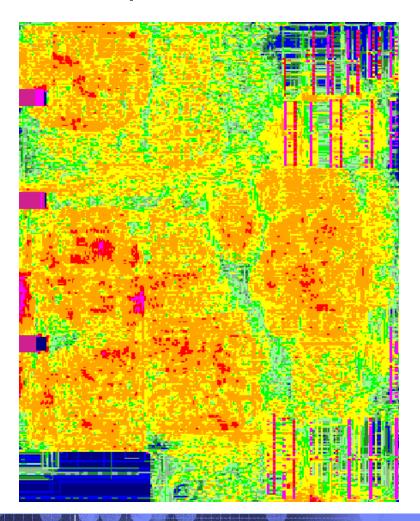


### **CRISP Progression**

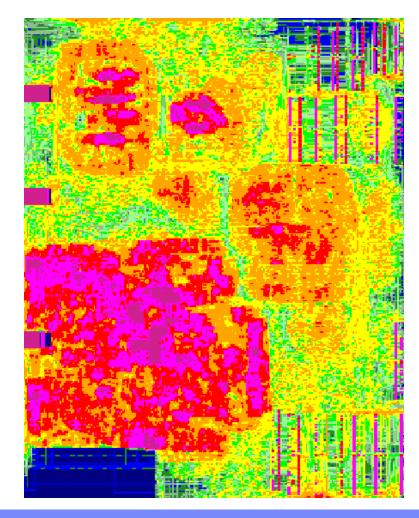


### Effect of Timing Driven-Placement

#### Initial placement



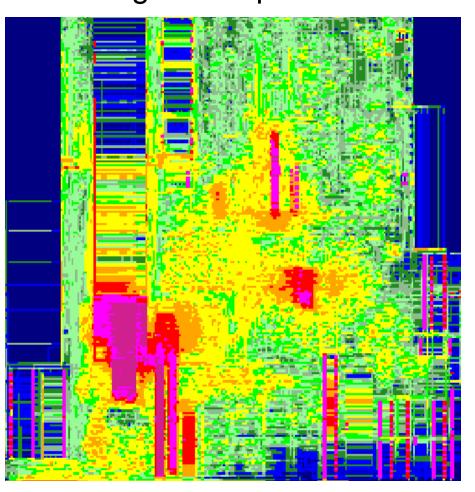
#### Timing-driven placement



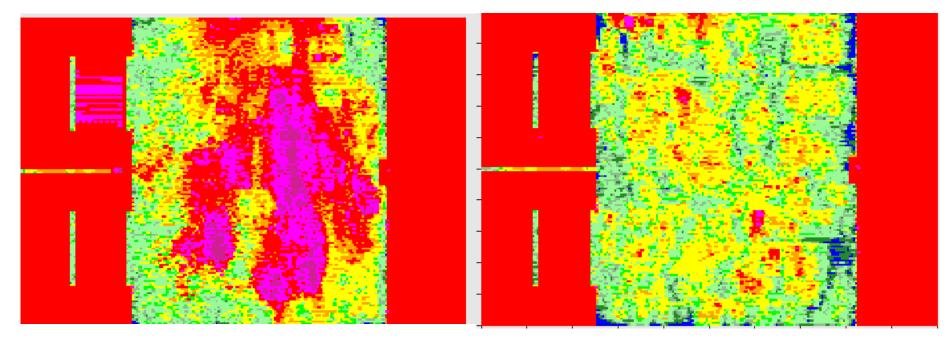
### Effect of Timing Driven-Placement

#### Initial placement

#### Timing-driven placement



### Impact of More Efficient Area Usage



Avg 20%: 108.06

>90% nets: 37855

>100% nets: 21364

Avg 20%: 86.89

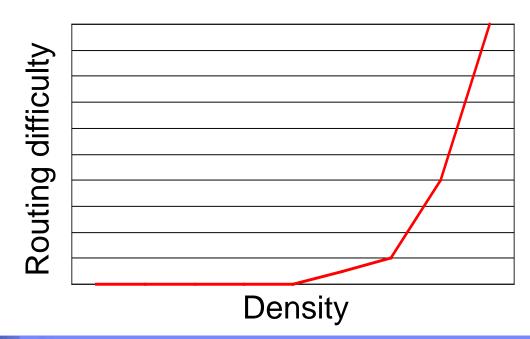
>90% nets: 7307

>100% nets: 1147

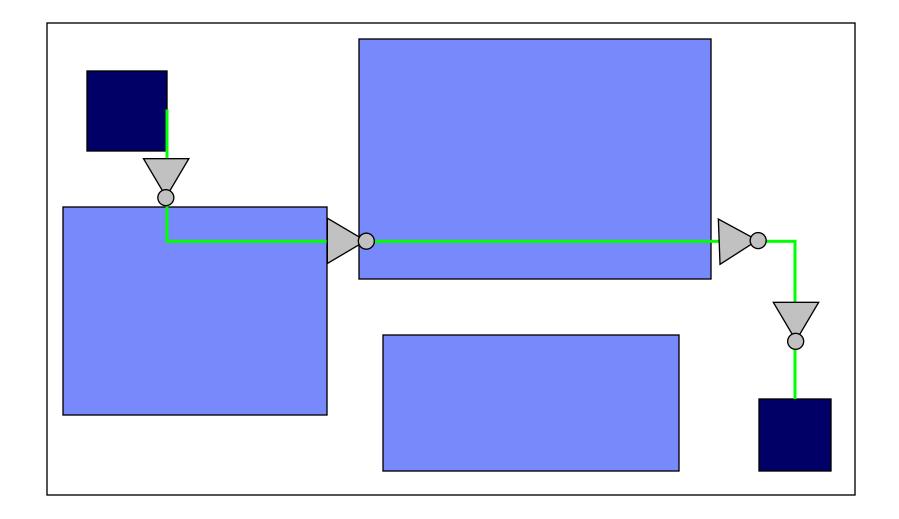
### "Sitting" in the Student Section



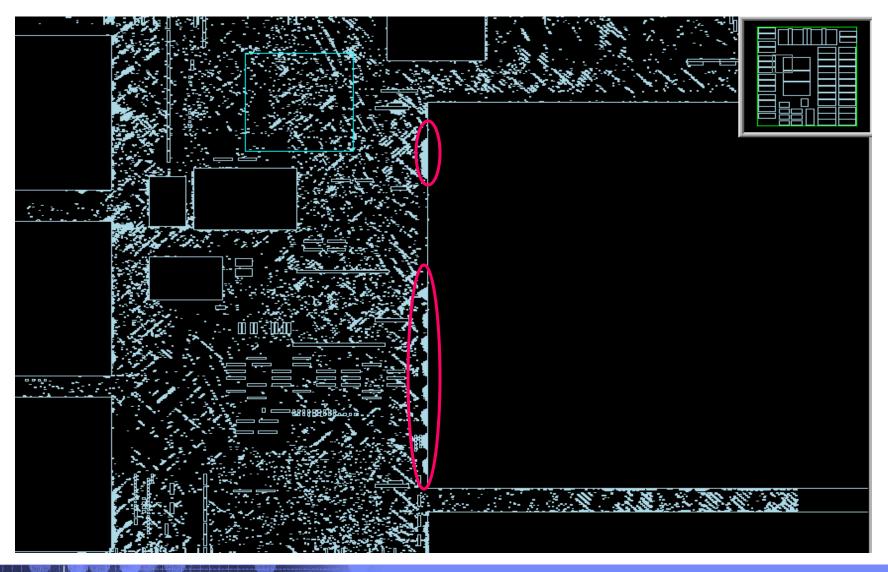




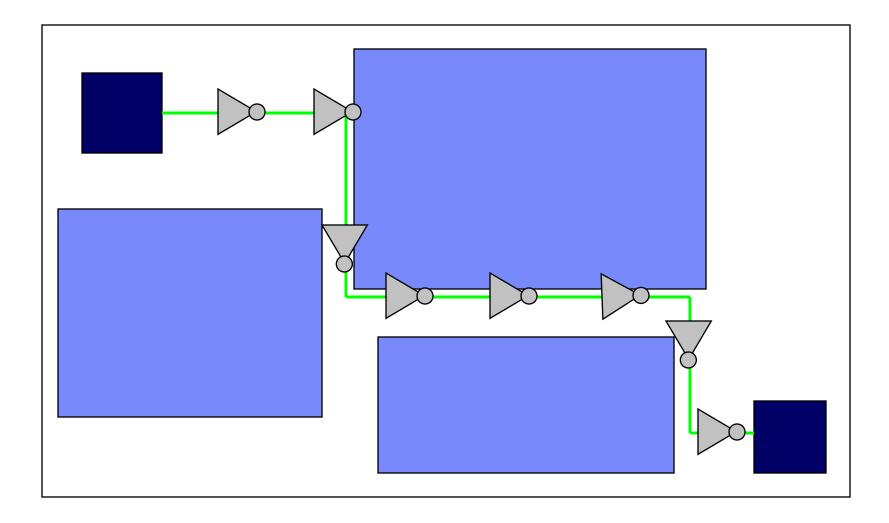
### Buffering Along A Global Route



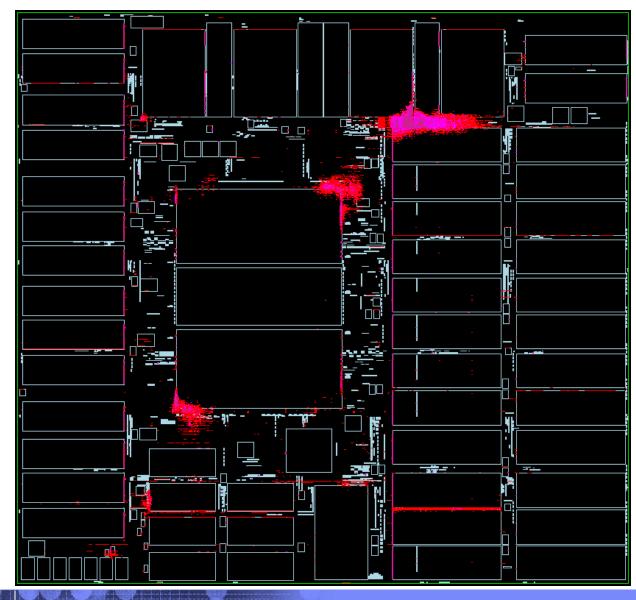
### **Buffer Packing**



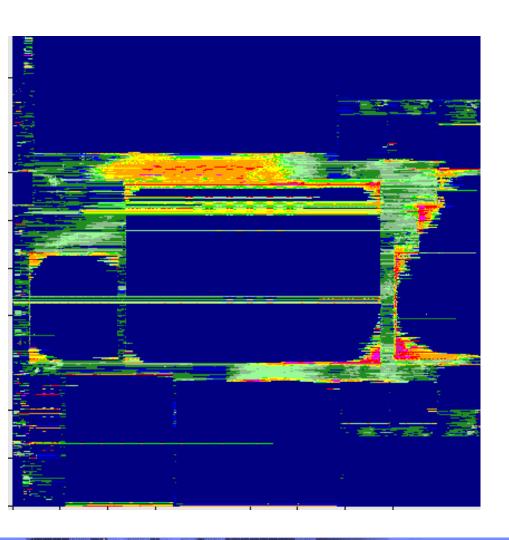
### **Blockage Avoidance Routing**

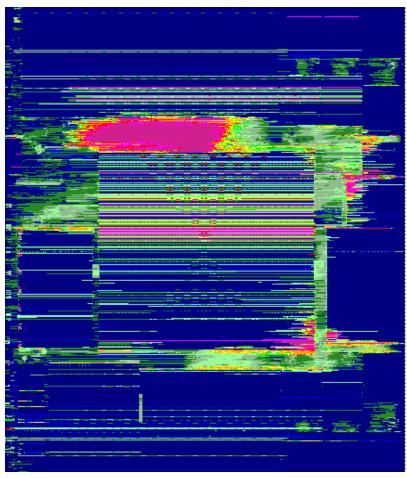


#### The Corona Effect

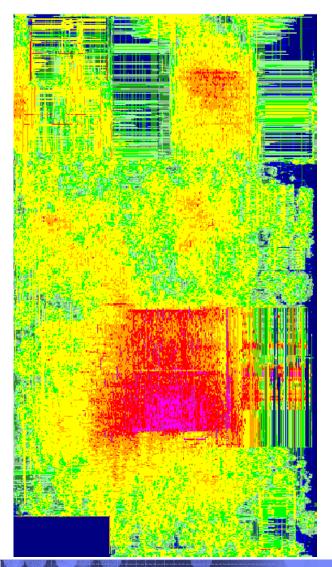


### Corona Effect + Too Much Thick Metal





### Hot Spots versus Opens and Shorts



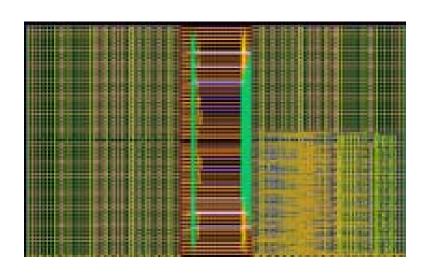


### What Makes a Design Difficult to Route?

- Bad floorplan
- Over packing dense logic
- Inefficient area minimization
- Over weighting for timing-driven placement
- Buffering too packed
- Over-constraining router
- Not capturing local routing isses
- Even if successful, don't mess up timing too much

#### What Does a Child Have in Common with a Router?





We want to create opportunities to succeed.

Just because opportunity is provided, they may not take advantage.

We don't really know what the best opportunities are.