Design Planning
Trends And Challenges

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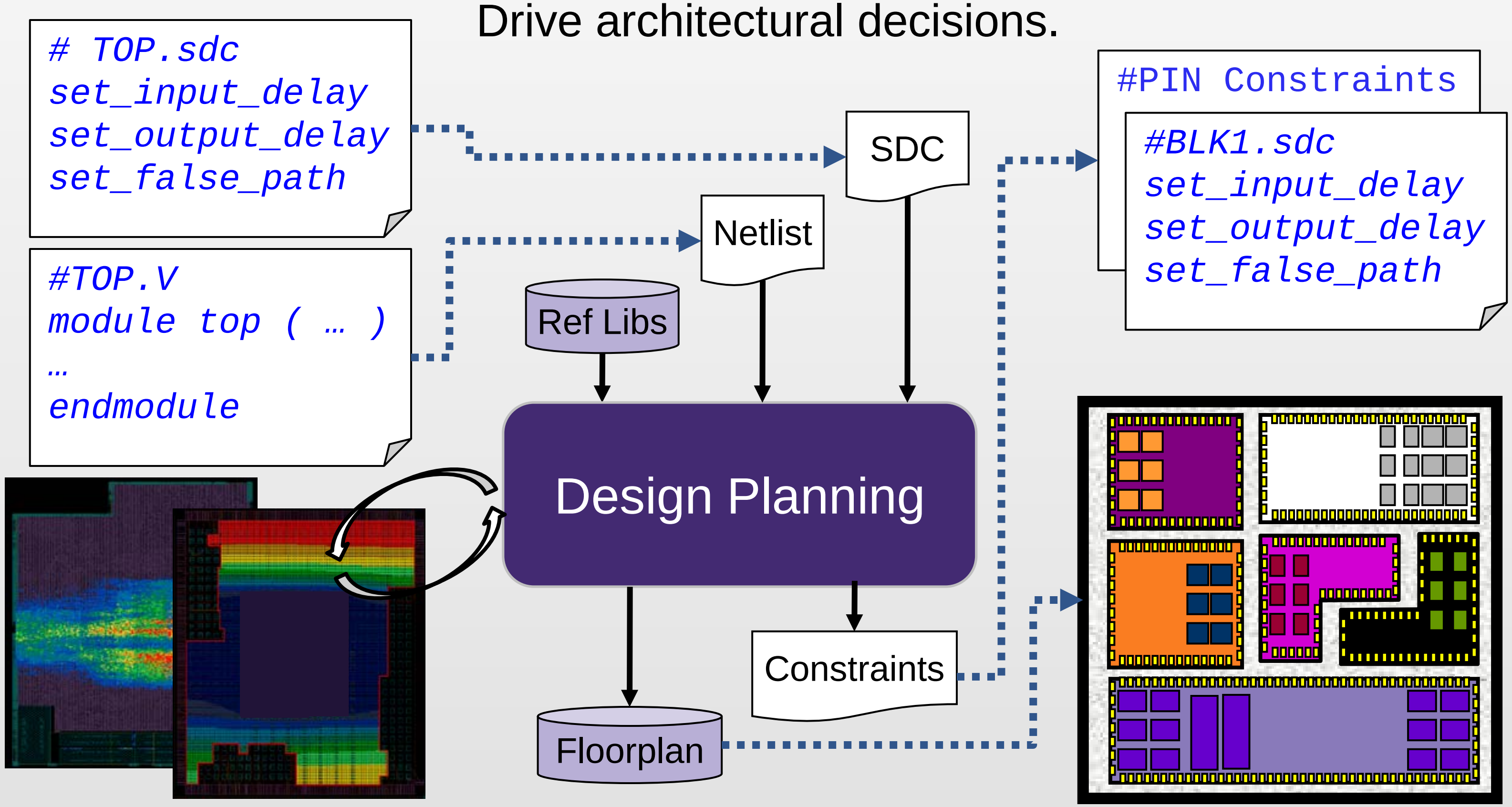
Agenda

- Design Planning: What and Why
- Design Trends
- Design Planning Challenges
- New Trends
- Discussion

What Is Design Planning?
A Process To Create Chip Floorplan And Constraints

Assess routing, timing, power feasibility. Create input for implementation. Drive architectural decisions.

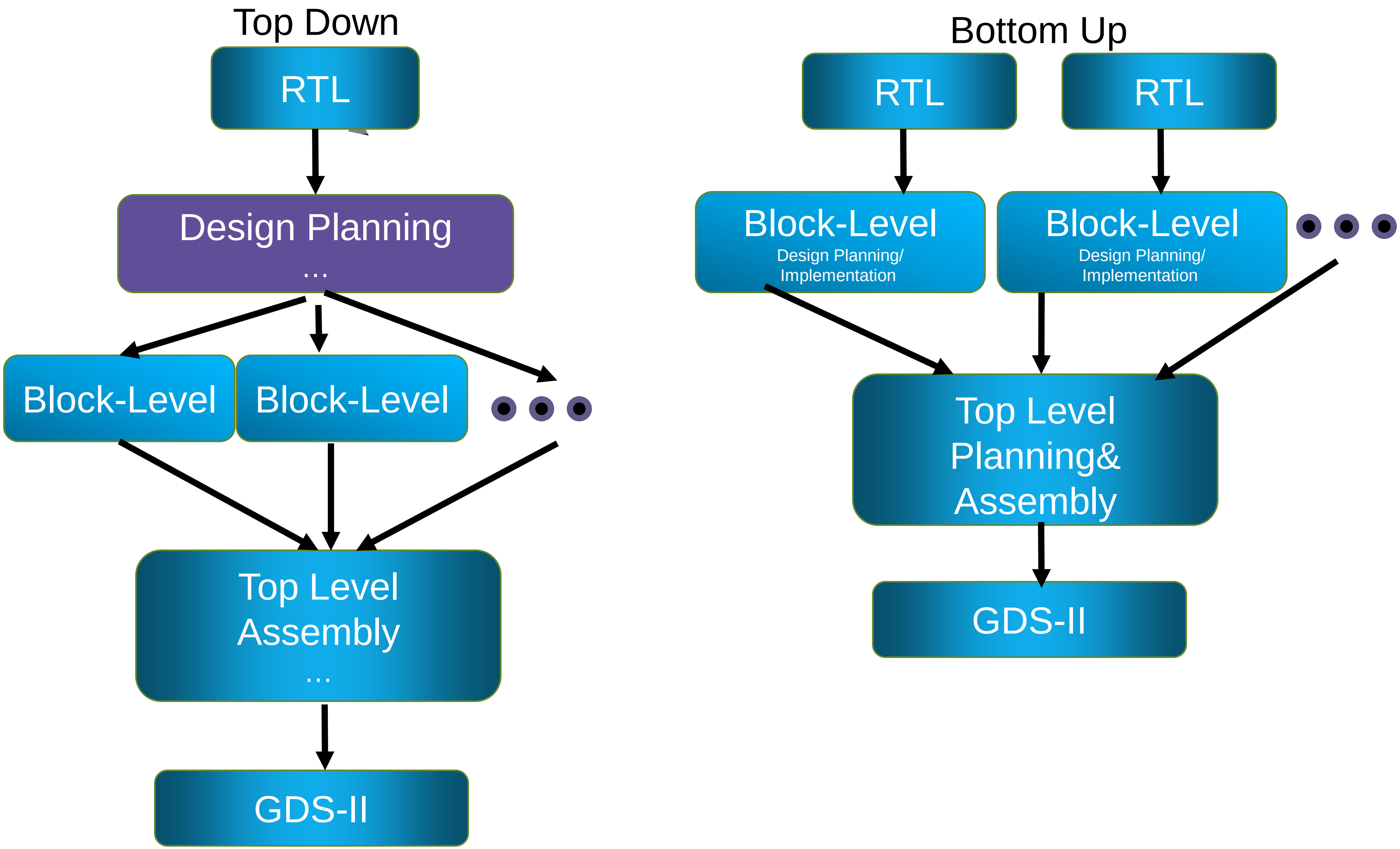


Key Aspects Of Design Planning

For Flat And Hierarchical Methodologies

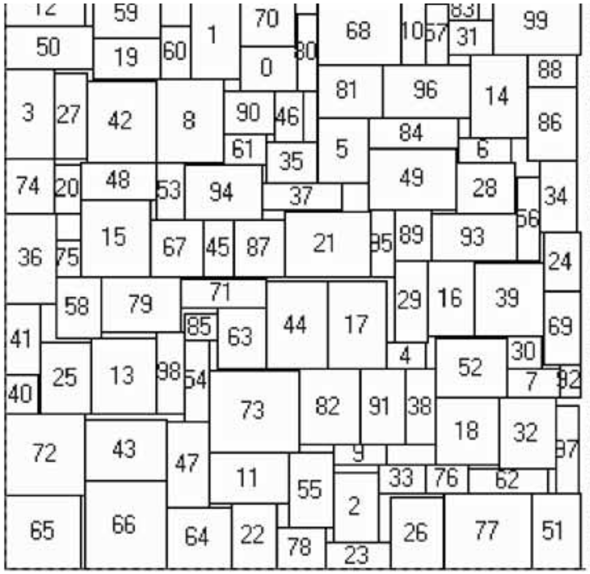
- Prototyping
  - Exploration of implementation strategies
  - Identify and address gross implementation issues
  - Feedback to RTL designs/synthesis
  - Architectural exploration
- Detailed Planning
  - Prepare best input/constraints for detailed implementation
  - Maximize QoR and Minimize runtimes for implementation

Hierarchical Design Methodologies



Traditional Floorplanning Problem

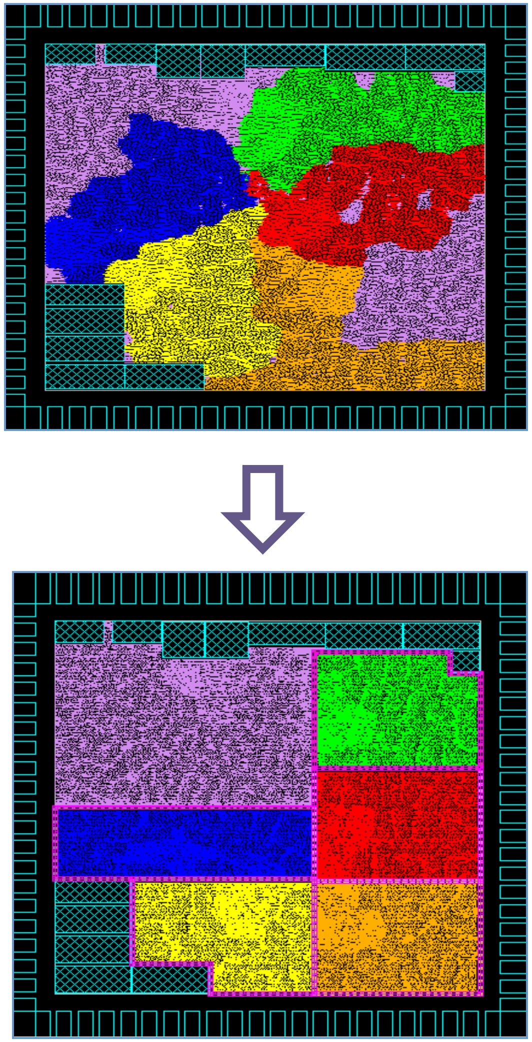
Objective



- Produce overlap free block placement
- Minimize
  - Area, Wirelength
  - White space
- Other considerations
  - Chip Area, Aspect ratio
  - IO PADs
  - Buss Driven

T-C Chen et. al., TCAD 2006
S.N. Adya et. al. , ICCD 2001
H. Xiang et. al., ICCAD 2003

Full Chip Virtual Flat Floorplanning



- Full netlist available
- Quick flat placement
  - Wirelength minimization
  - Congestion, timing
- Block placement, shapes
  - Cover standard cell, Macro areas

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- Design Planning Complexities
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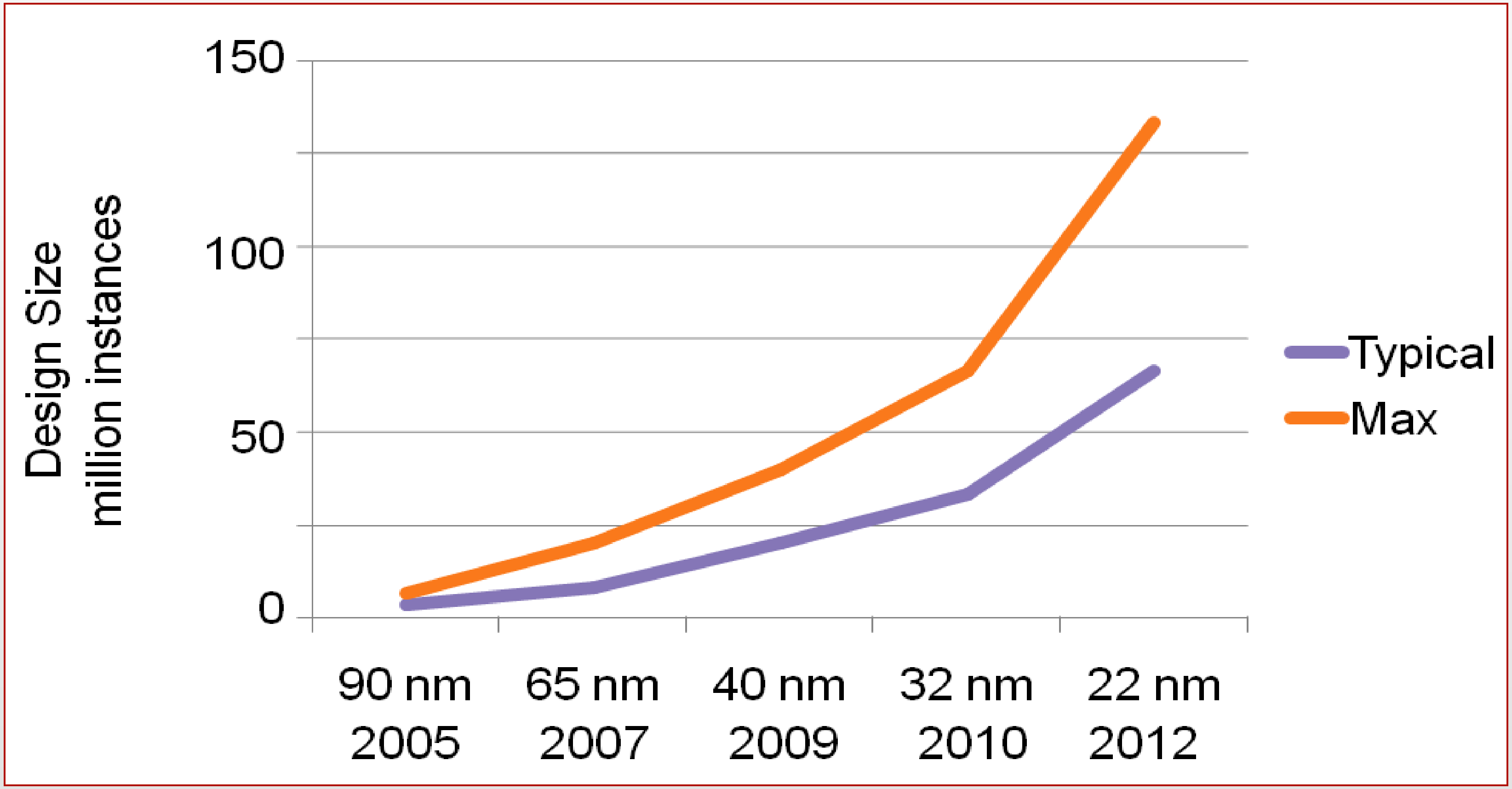
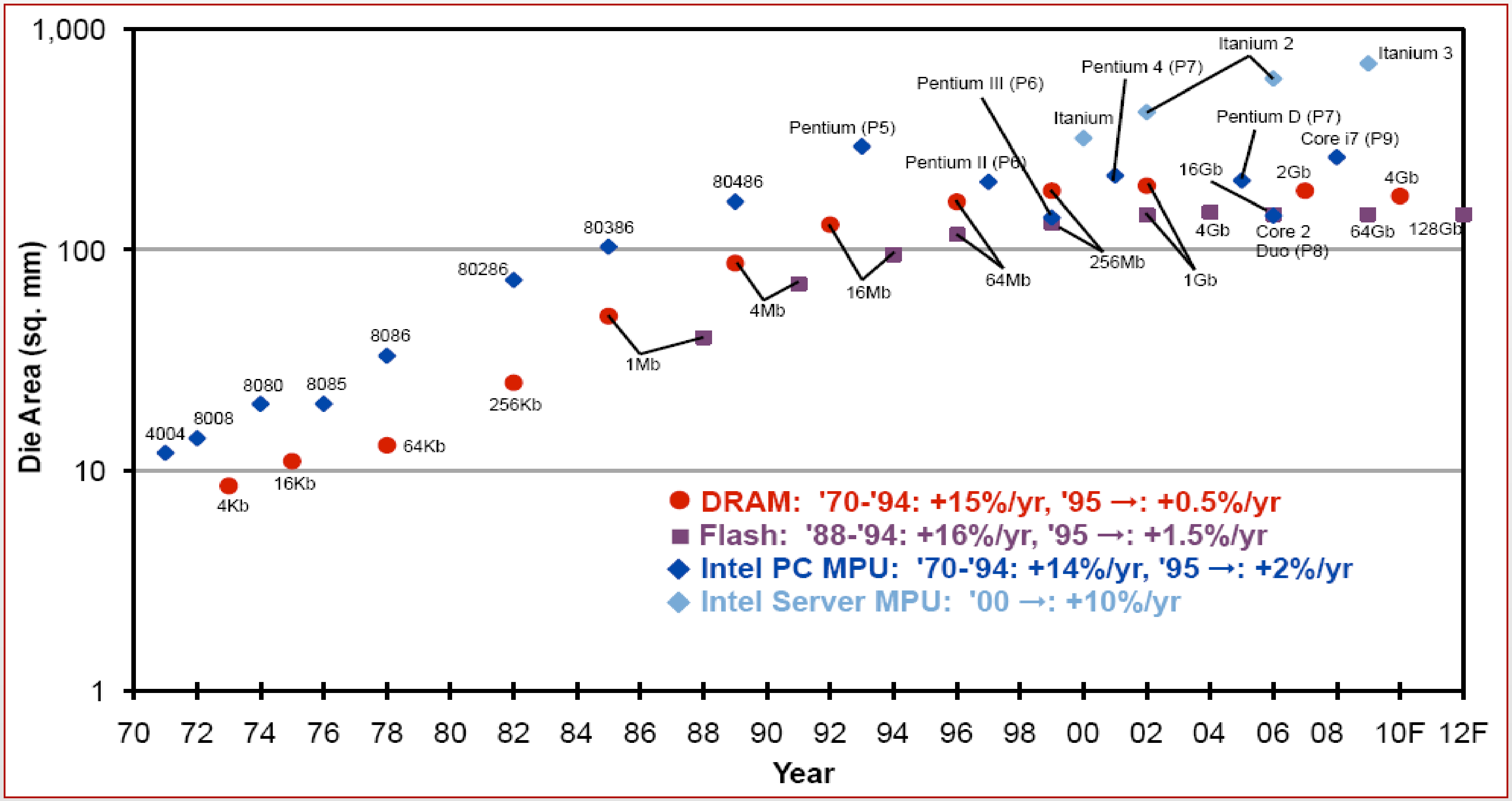
Design Complexity Trends

Smaller Process Nodes Leading To Increased Design Size



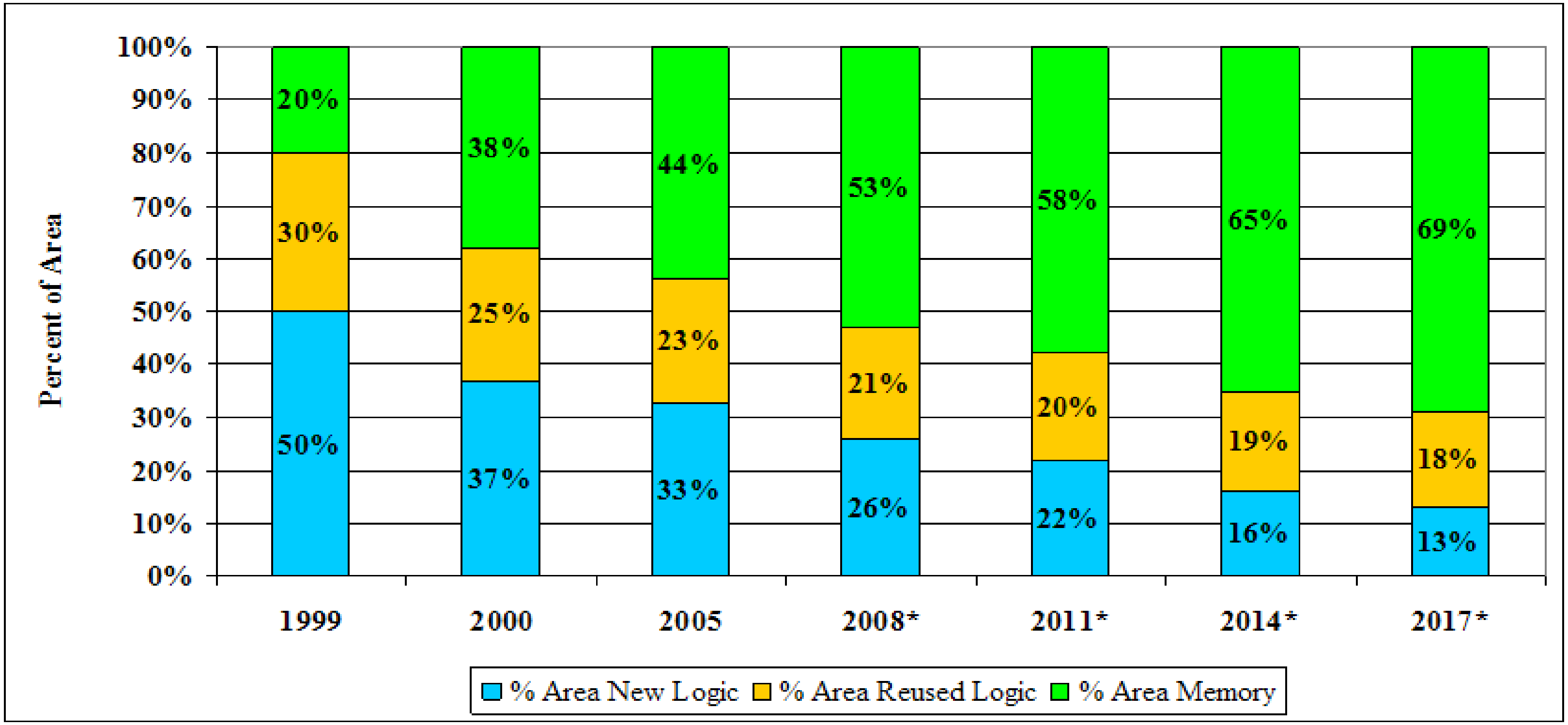
Chip Size Trends



McClean Report, 2009 Edition, IC Insights

Roadmap For Die Area Partitioning

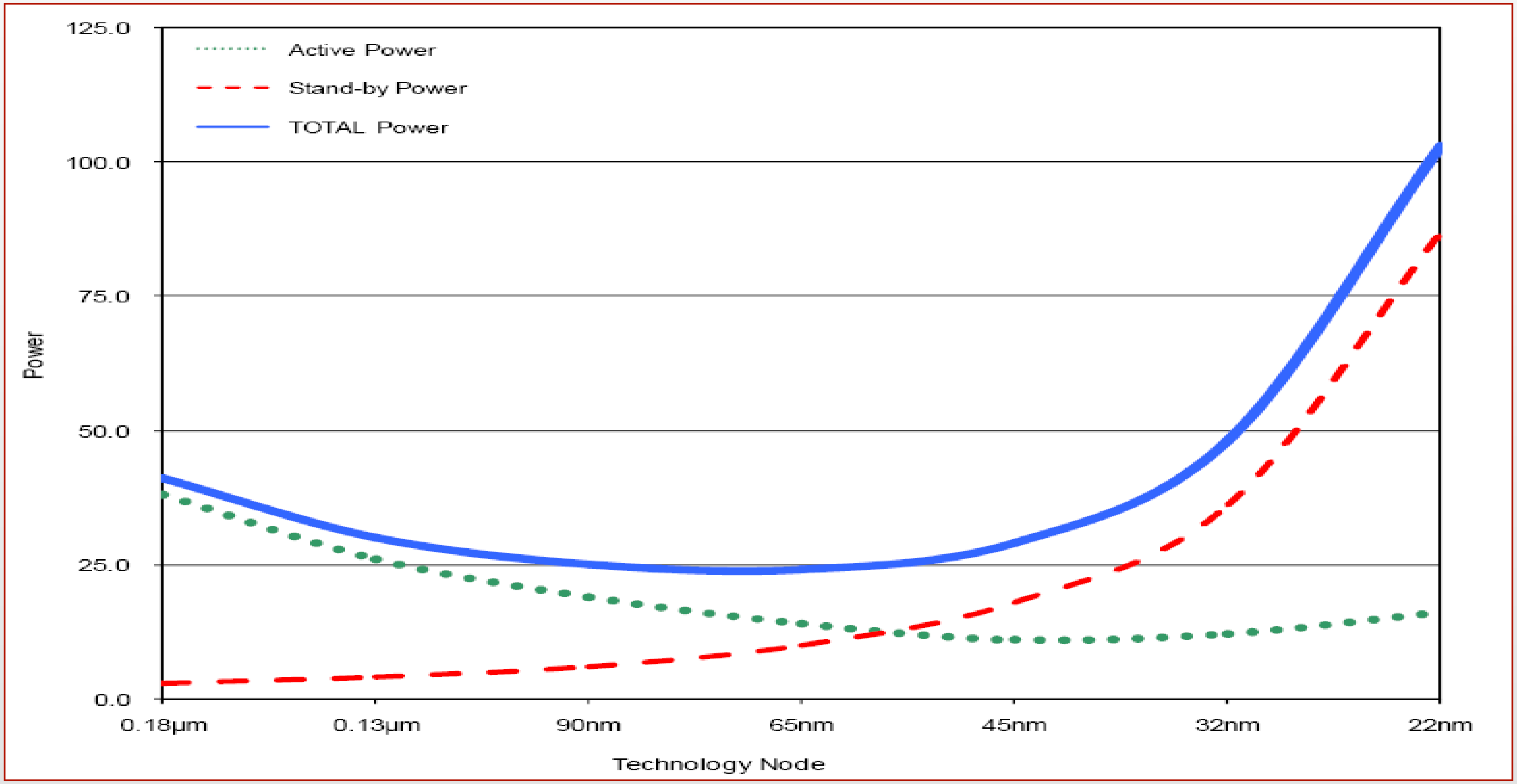
1999 To 2017



***Forecast**

Semiconductor Intellectual Property: Continuing On The Path Toward Growth, 2008, SEMICO Research Corp

Power Trends



Power Management Technologies, 2009, IBS

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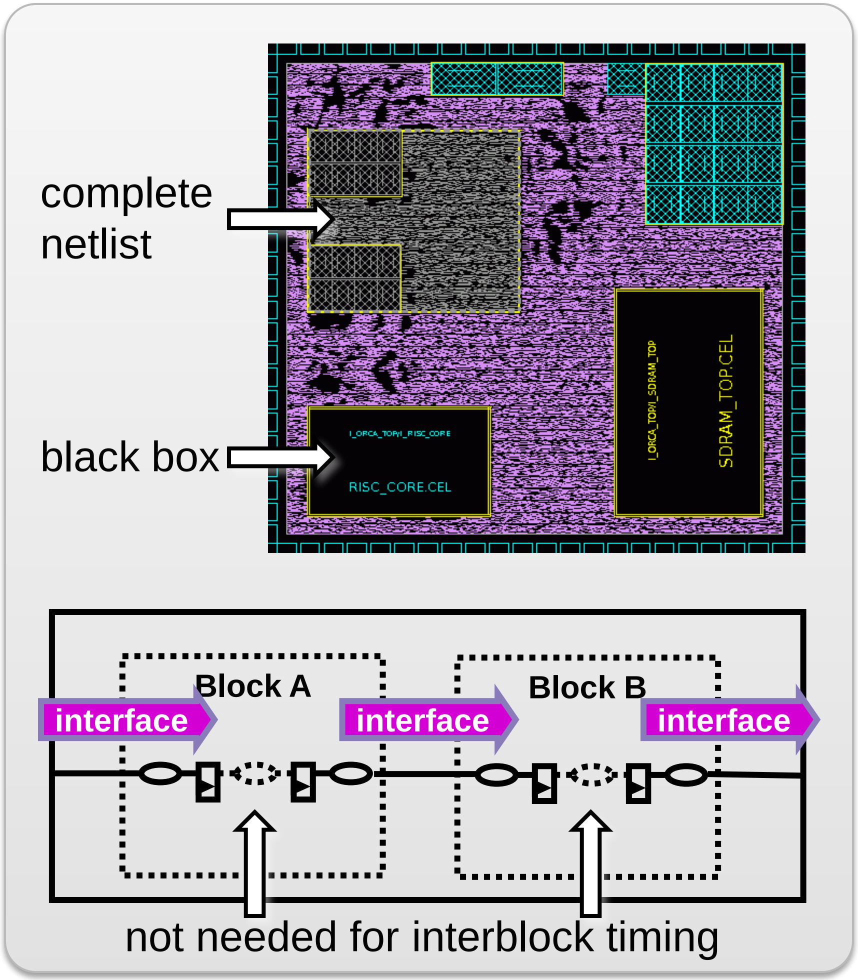
Design Planning Challenges

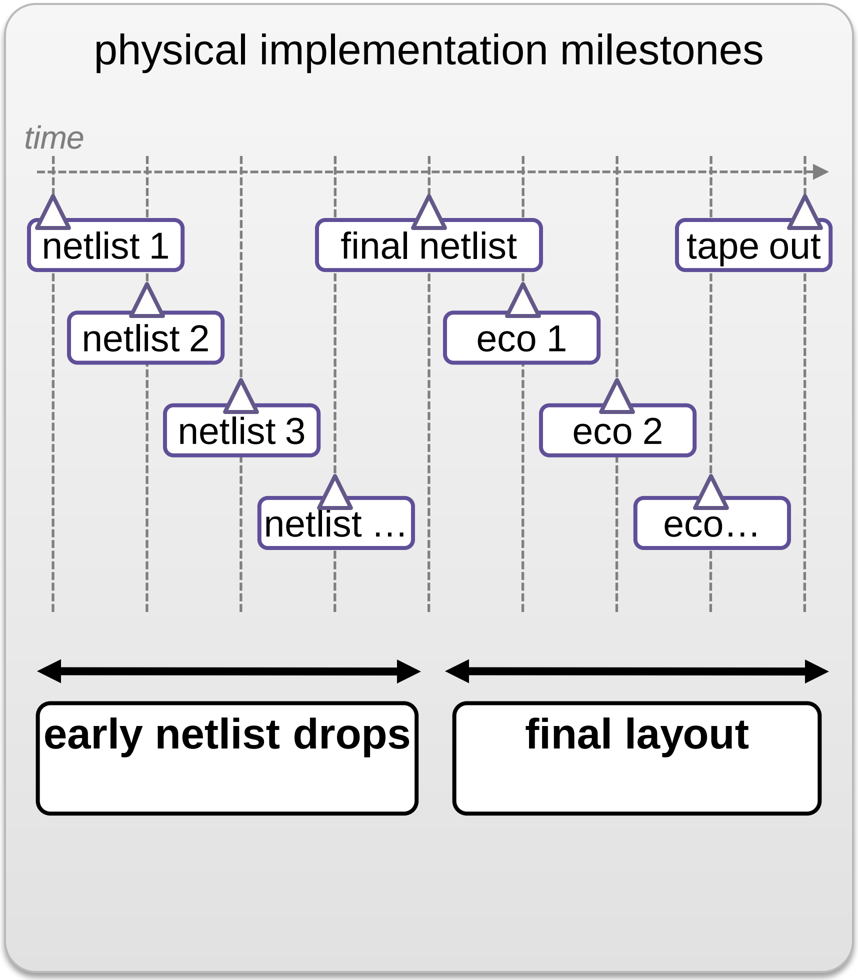
- Design sizes
- Evolving netlist and constraints
- Complex IO structures
- Large number of embedded macros
- Fast and accurate predictability
- Abutted and semi-abutted partitions
- Repeated blocks
- Low power challenges
- Clock planning

Increasing Design Sizes



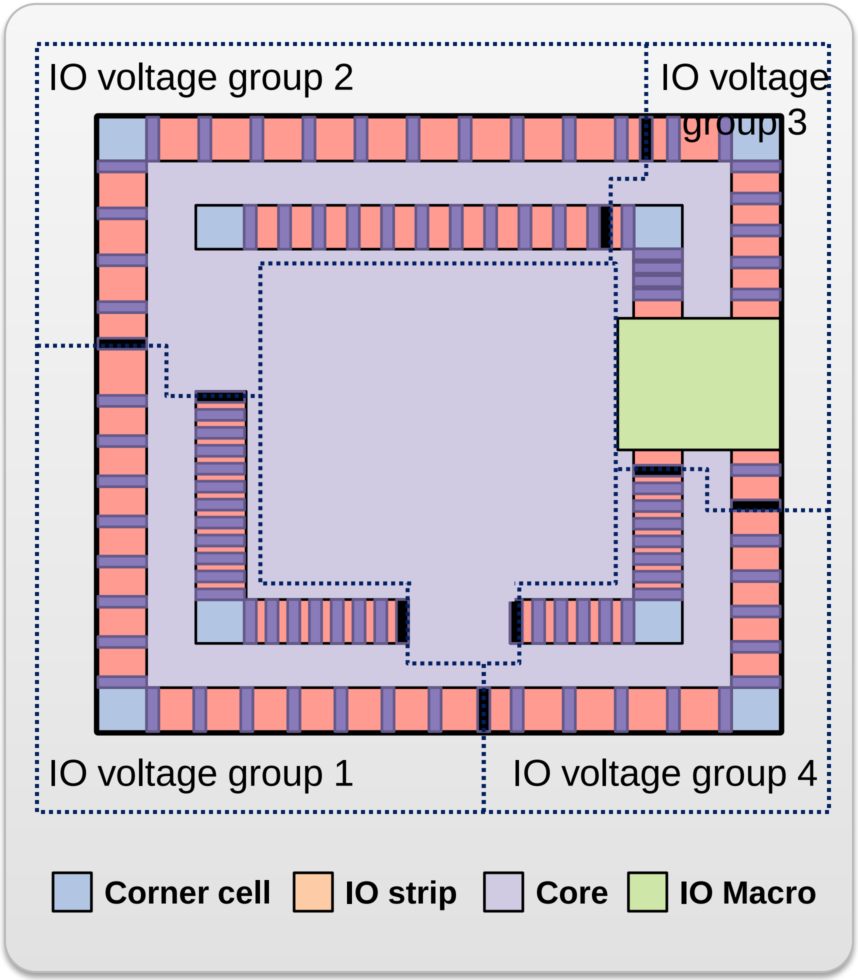
- Full-chip design planning
- Large netlists: 20-40M instances
  - Load essential data
  - Levels of abstraction
  - Partial netlist planning
- Large die sizes

Evolving Netlists And Constraints



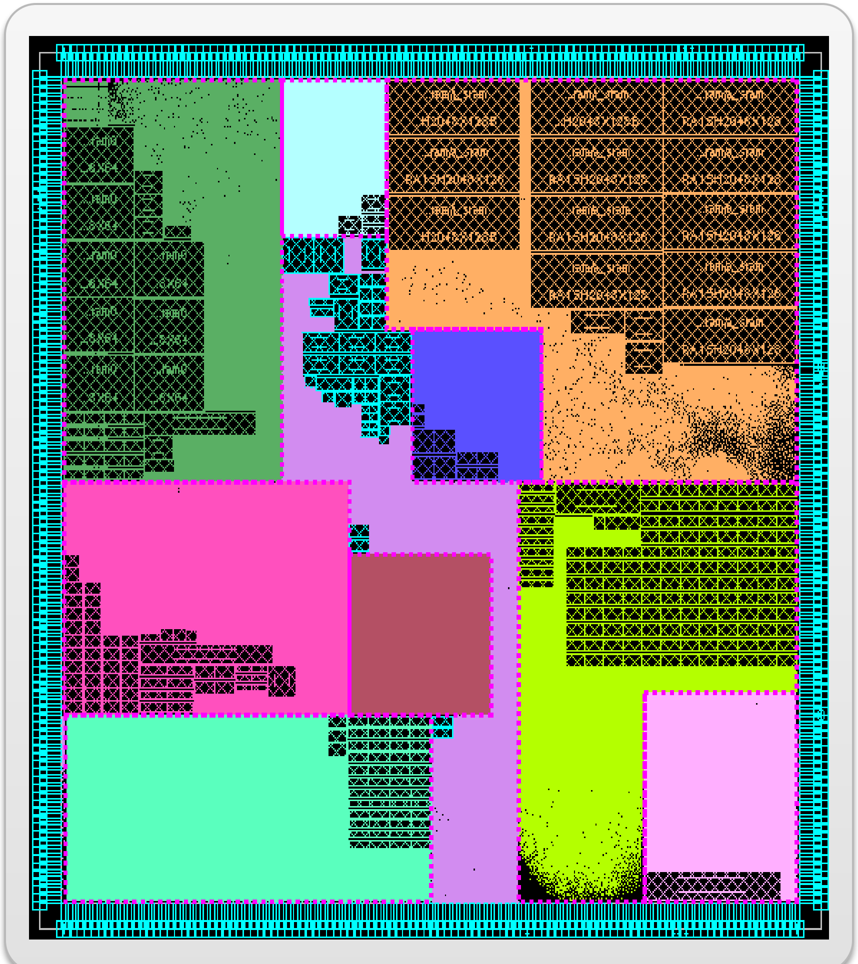
- Parallel RTL and physical design
- Constant netlist changes
- Incomplete netlist, libraries
- Inconsistent and mismatched data/netlist
- Incomplete constraints
- Missing clocks

Complex IO Structures



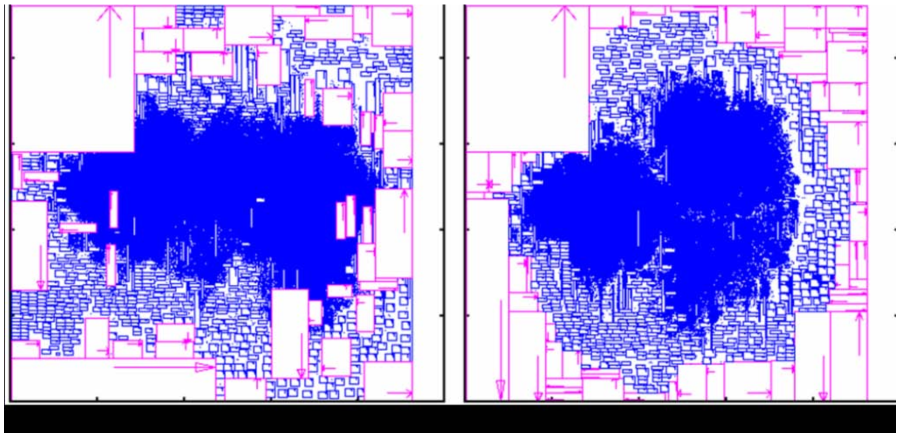
- Multi-ring IO PADs
- Multi-height IO PADs
- Mixed Macros and PADs
- Mixed IOs and pins
- Multi-VDD PADs
- Rectilinear boundaries

Large Number Of Embedded Macros
Considerations



- Large percentage of die area
- Varying sizes/shapes/rectilinear
- Place and route blockages
- Relative constraints
- Macro orientations
- Fragmented SC areas
- Channels

Large Number Of Embedded Macros
Objectives



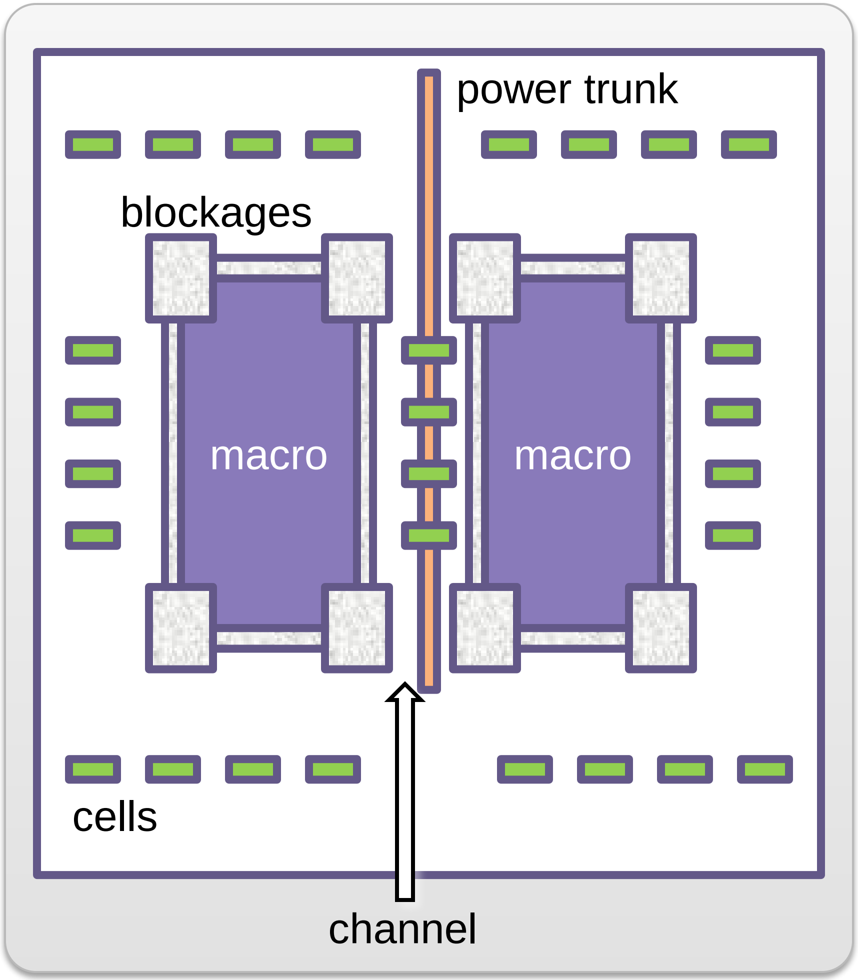
TCG Based   MP-Tree based

- Produce legal placement
  - Non overlapping macros
- Minimize
  - Wirelength, timing, congestion
  - Displacement from initial placement
- Maximize
  - Contiguous routing areas

H-C, Chen et. al., ICCAD 2008
T-C Chen et. al., TCAD 20008
T. Gao, DAC 1992

Large Number Of Embedded Macros

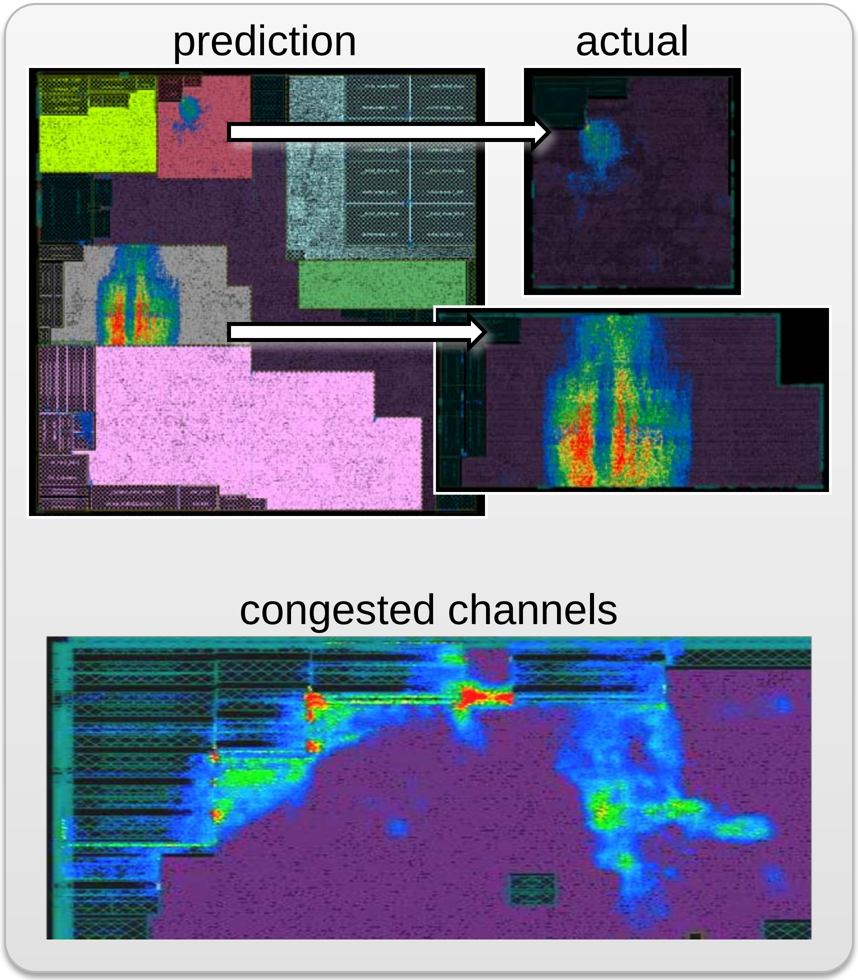
Sub-problems



- Channel sizing
  - Routing estimation
  - Power for std. cells
- Blockage creation
  - Avoid edge and corner congestion

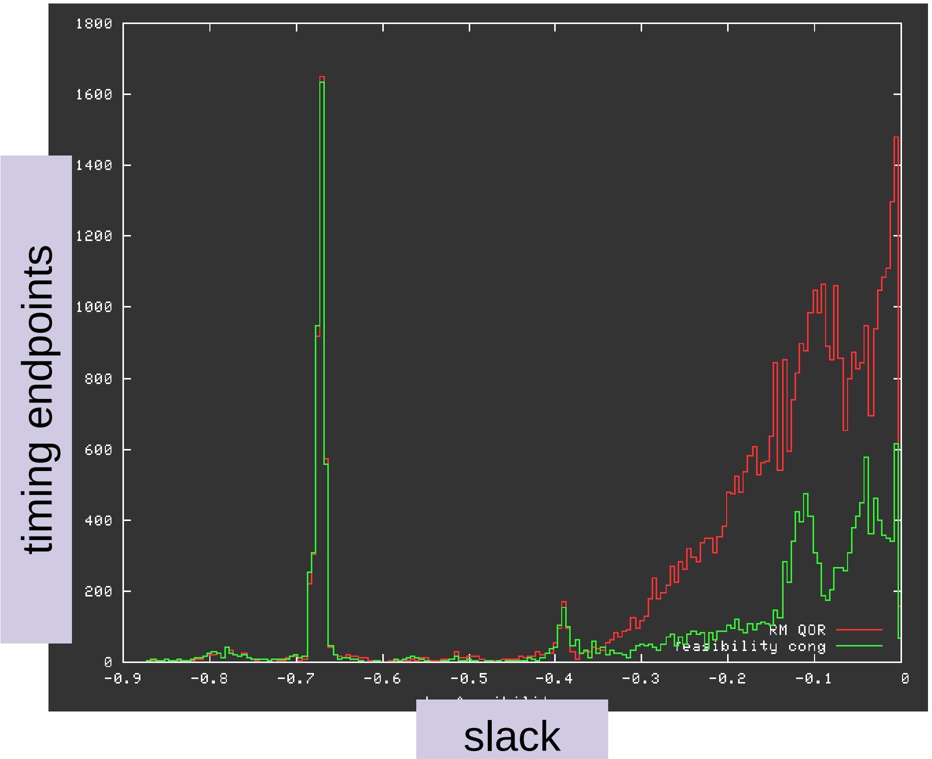
H-C, Chen et. al., ICCCAD 2008
T-C Chen et. al., TCAD 20008
T. Gao, DAC 1992

Fast and Accurate Predictability



- Quick assessment of floorplan feasibility
- Routability
  - Fast congestion estimation
  - Dirty floorplans
- Channel and block congestion

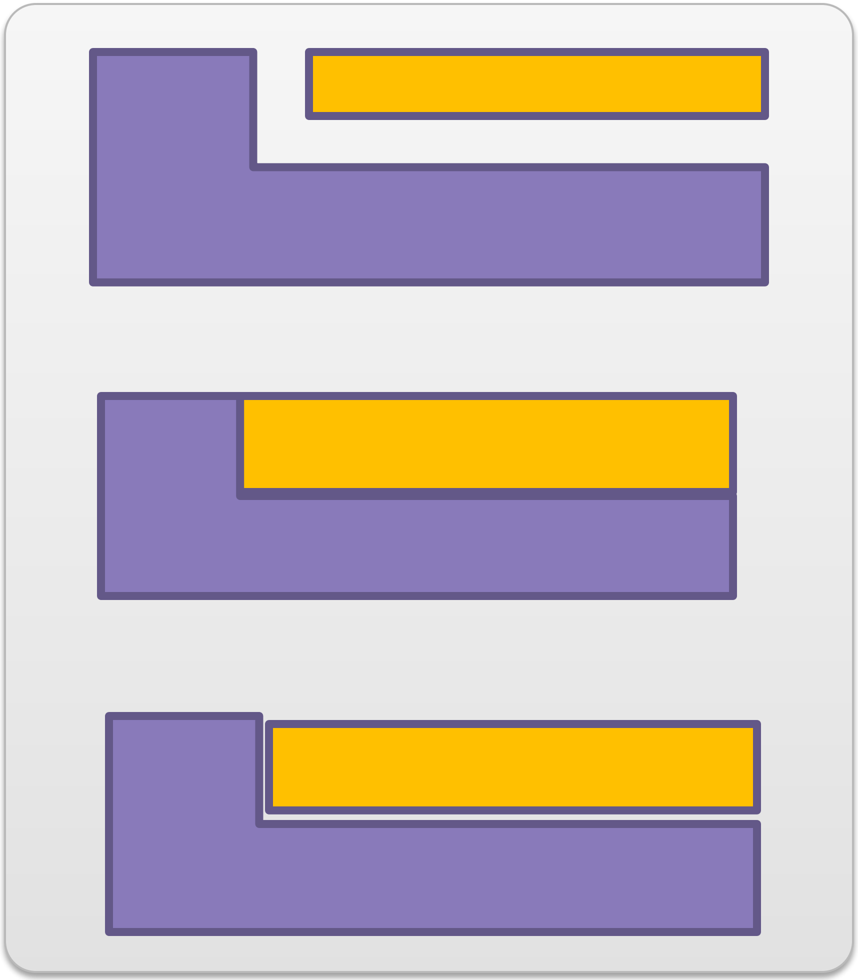
Fast and Accurate Predictability



- Timing predictability
  - Virtual timing estimation
  - Quick buffering
  - Estimated timing models
  - Dirty constraints
- Area assessment
  - Estimated buffer count and cell area
  - Die area
  - Block area

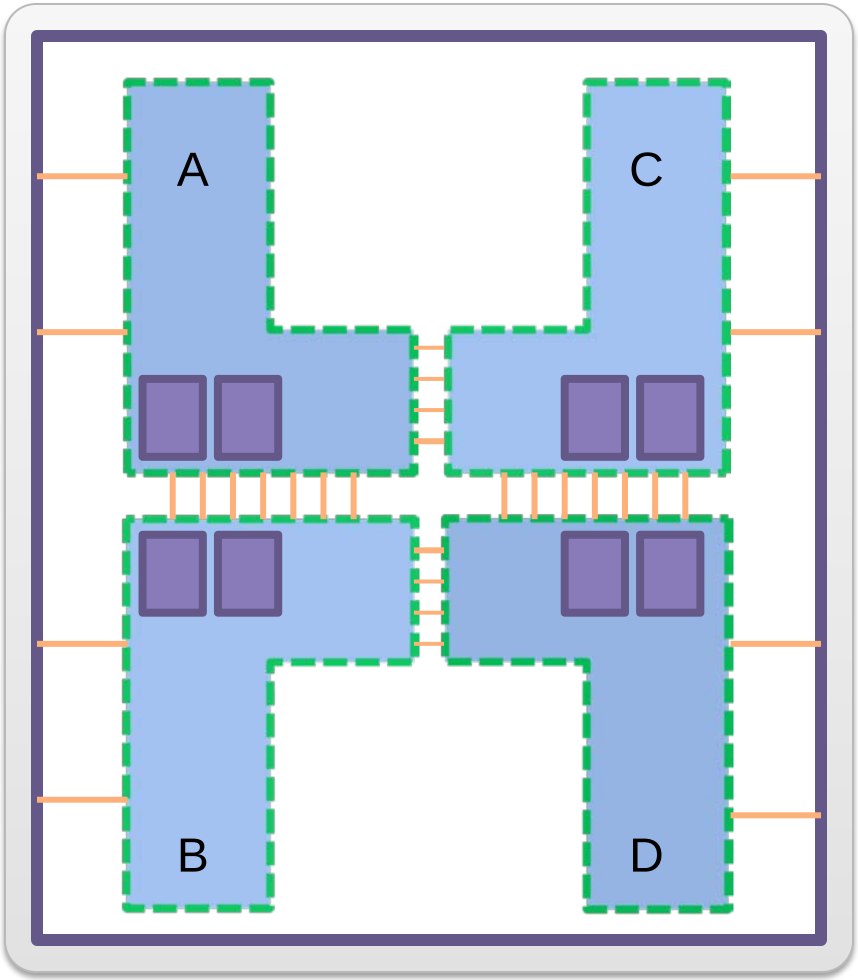
Hierarchical Designs

Channeled, Abutted, and Near Abutted



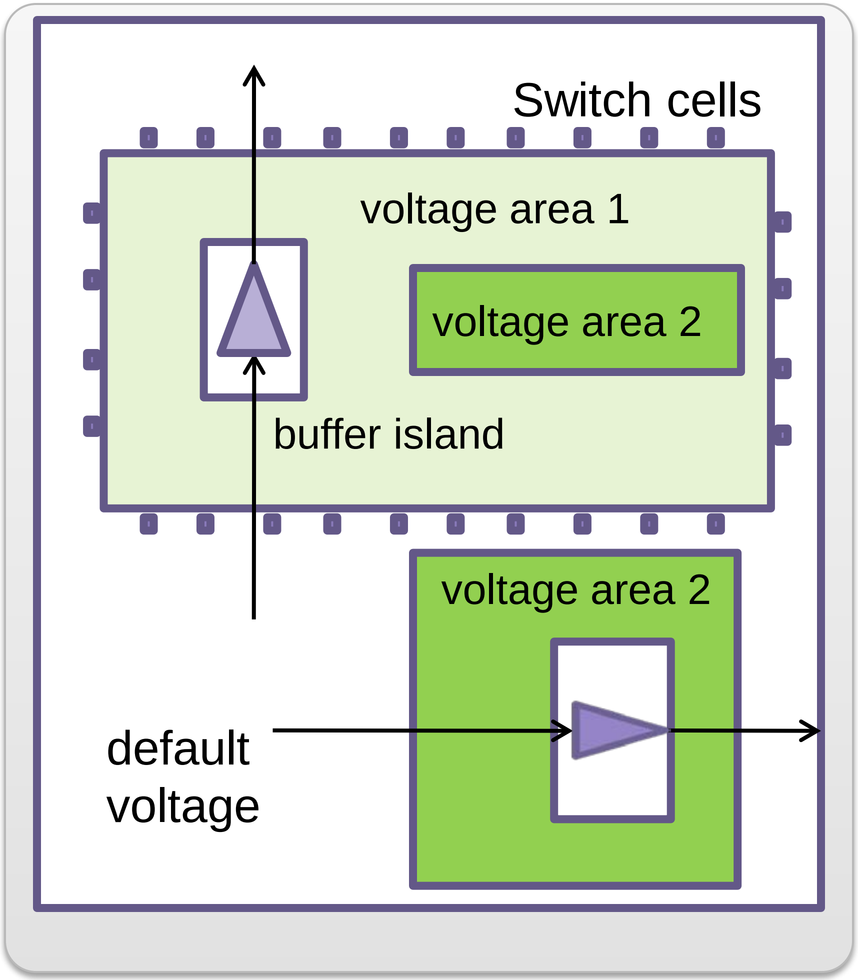
- Channeled (most common)
  - Top level logic and channels
  - Relatively simple to plan and to close top level
- Abutted (high end)
  - No top level logic and channels
  - Better die area
  - Needs robust interblock planning
  - Complex clock design
- Near abutted (gaining popularity)
  - No top level logic
  - Narrow channels for buffers, clocks
  - Good tradeoff between channeled and abutted

Repeated Blocks



- Functionally identical blocks layed out identically
- Bottom up design
  - Simple, sub-optimal
- Top down in-context design
  - Automatic identical shapes, pins, constraints
  - Rotations, mirroring

Low Power Planning

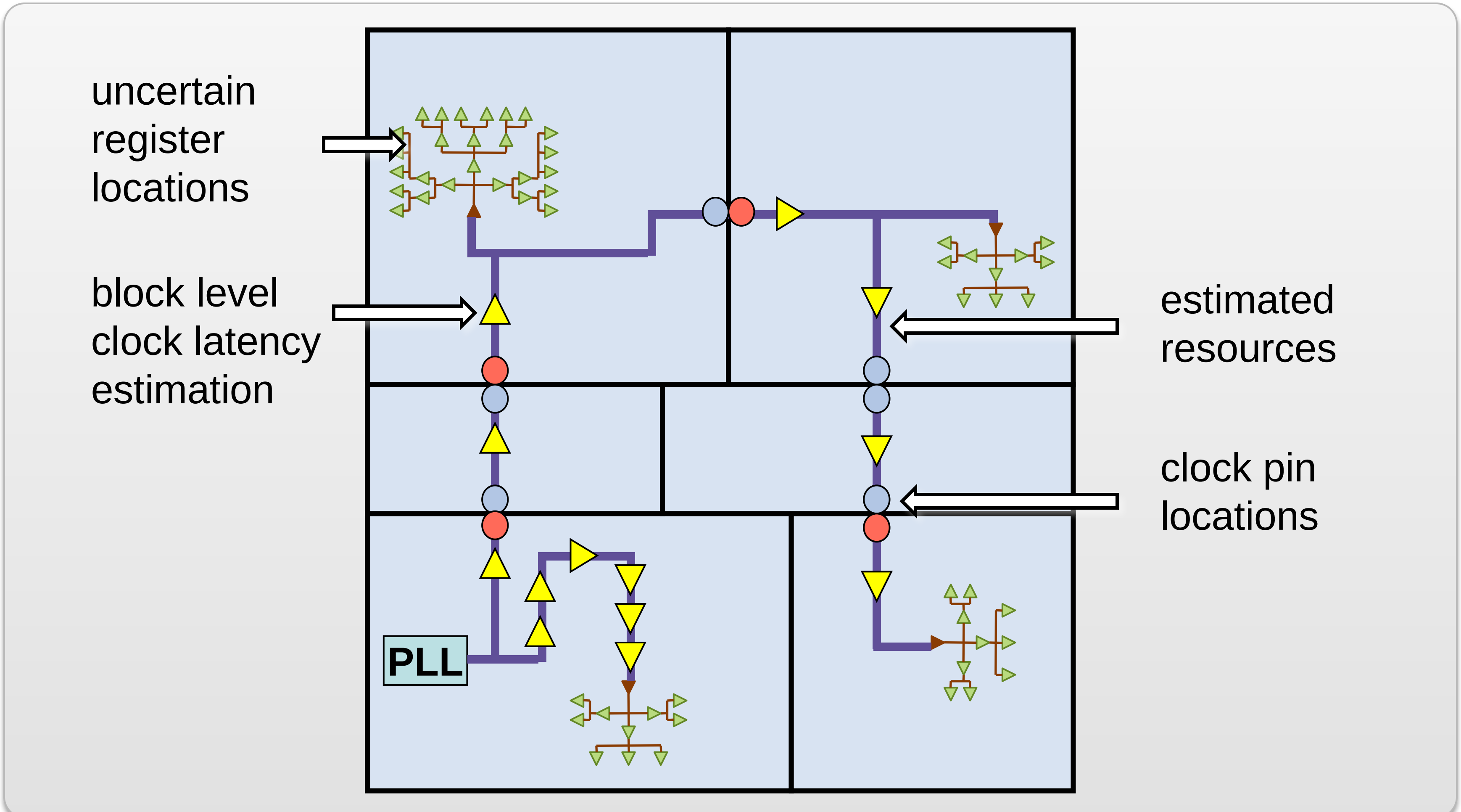


- Power domains/voltage areas
  - Physical locations/shapes
  - Congestion/timing
- Shutdown regions
  - Switch cell planning
    - Area/Power/performance tradeoff
  - Turn-on sequence
- Buffer islands in voltage areas

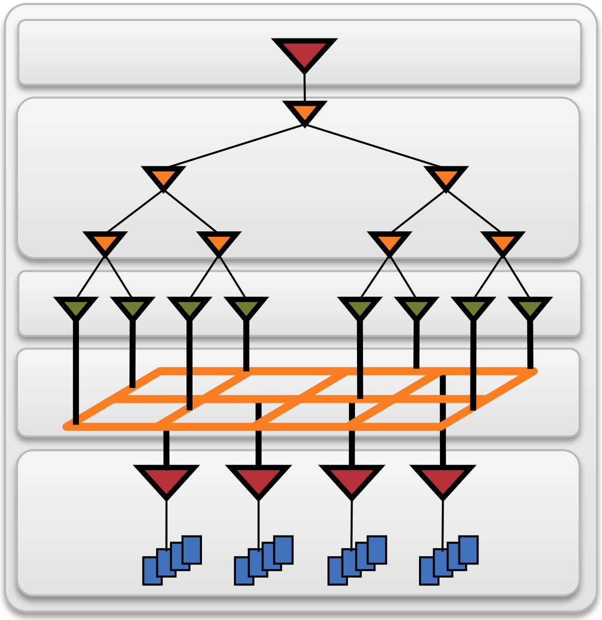
H-S Won et. al., ISLPED 2003
C-Y Yeh et. al., SOCC 2007

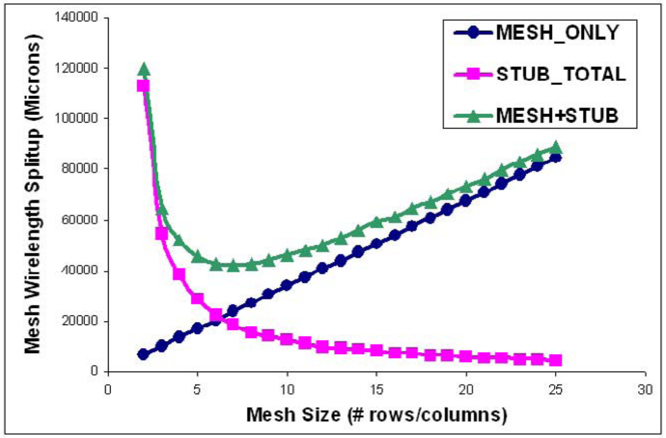
Clock Planning

Top Level Clock Tree



Clock Mesh Planning

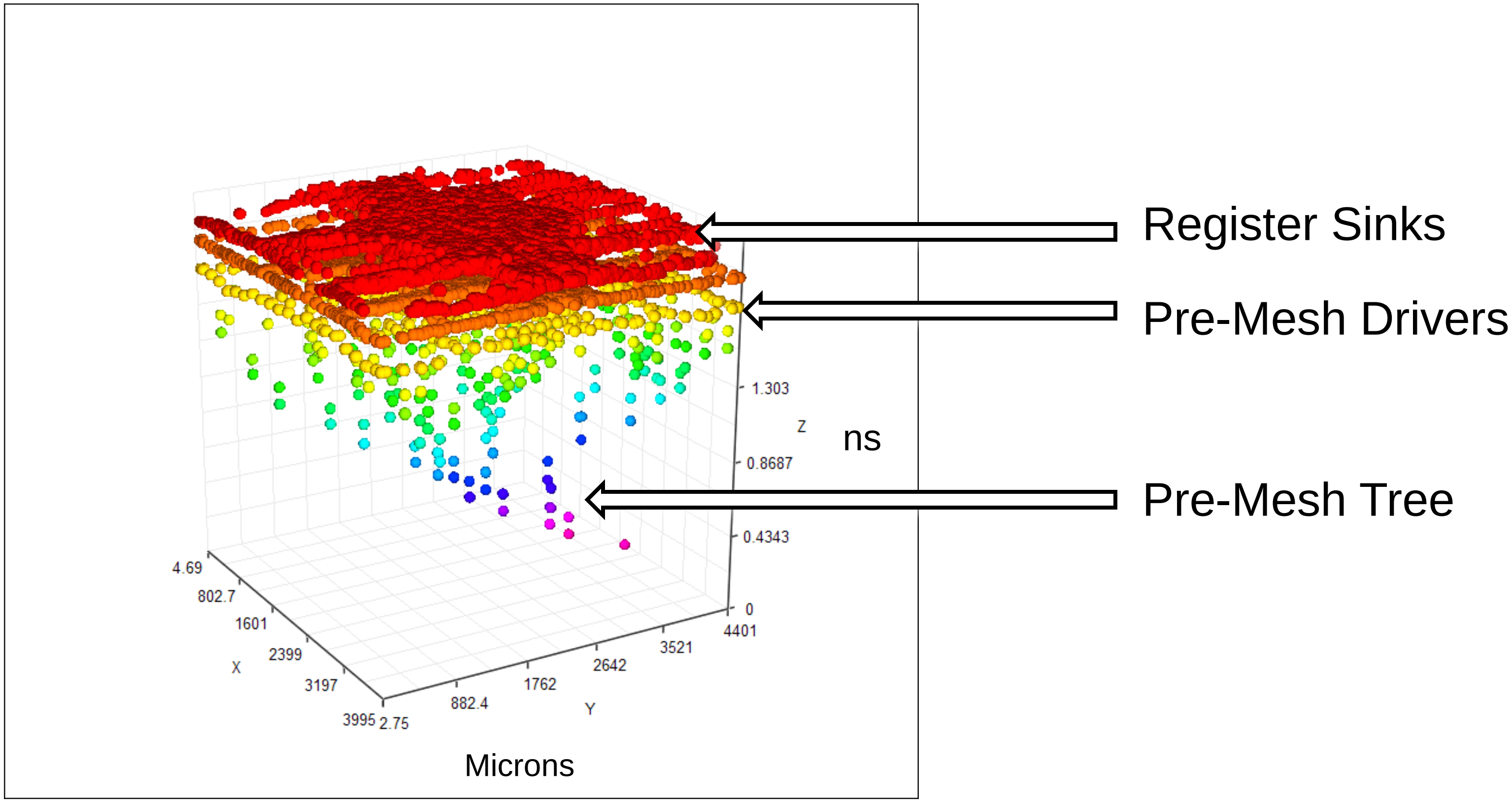




- Plan mesh
  - Skew constraint
  - Minimize Mesh size + stub/twig routes
  - Layers
- Mesh drivers
  - Number, size, location
- Mesh Analysis
  - Multi-driver analysis

A. Rajaram et. al., DAC 2008.

3D Visualization of Clock Mesh Simulation



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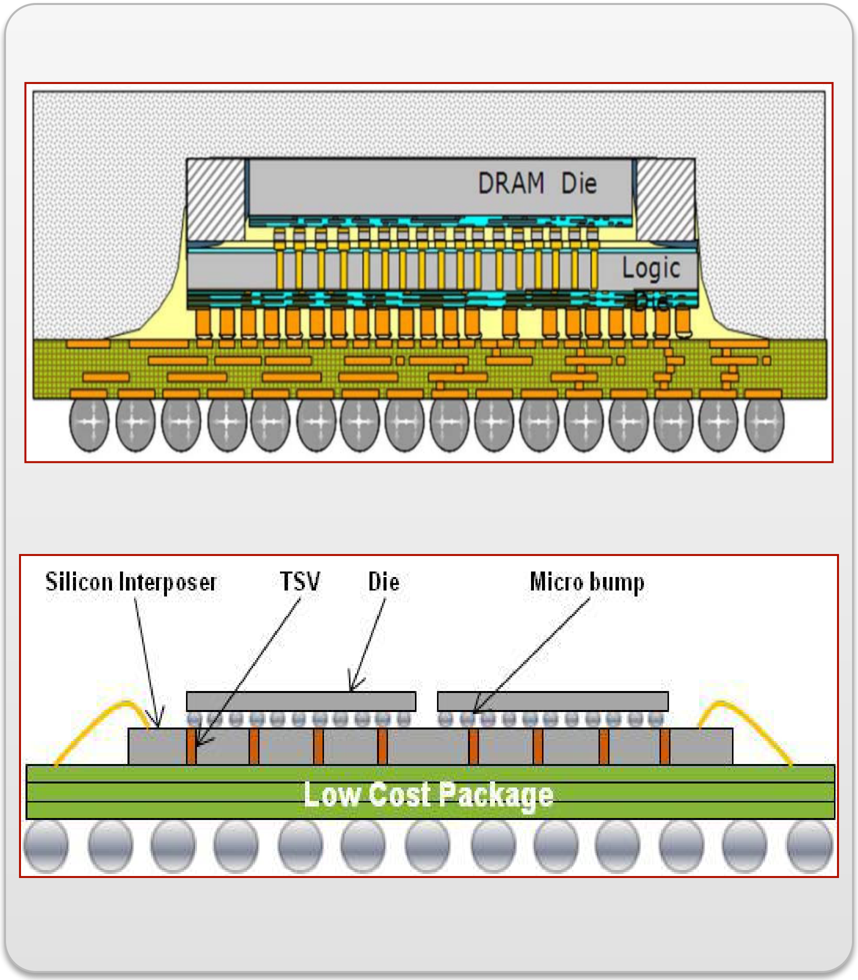
New Trends

- 3D chip planning
- Multi-level hierarchical planning
  - For increasing design sizes
- Design Planning and Logic Synthesis

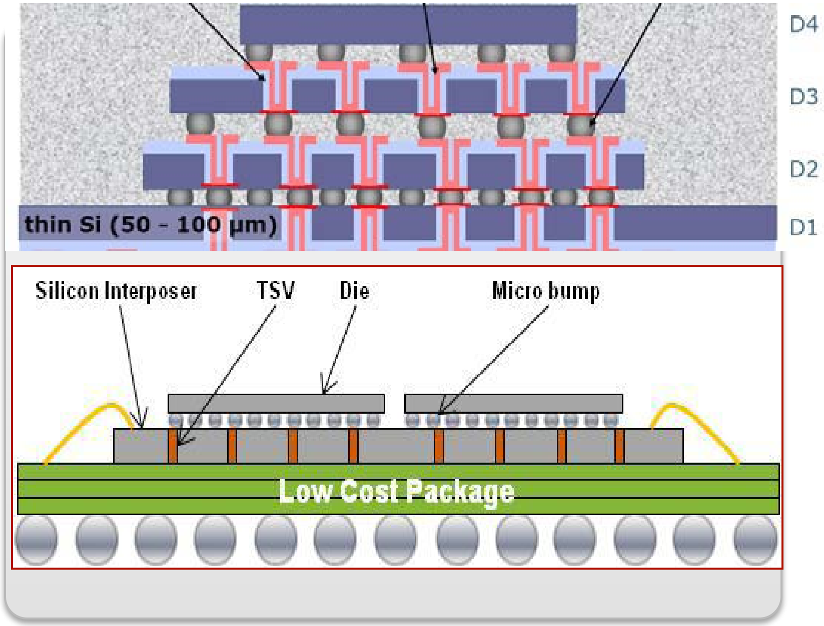
3D Chip Design Planning

Objectives



- Overlap-free placement of the design blocks
- Minimize wirelength (performance)
  - 3D **within** and between blocks
- Minimize power
  - Reduce IOs or use weaker ones
  - Minimize wirelength
  - Design each layer in its optimal technology node
- Minimize area

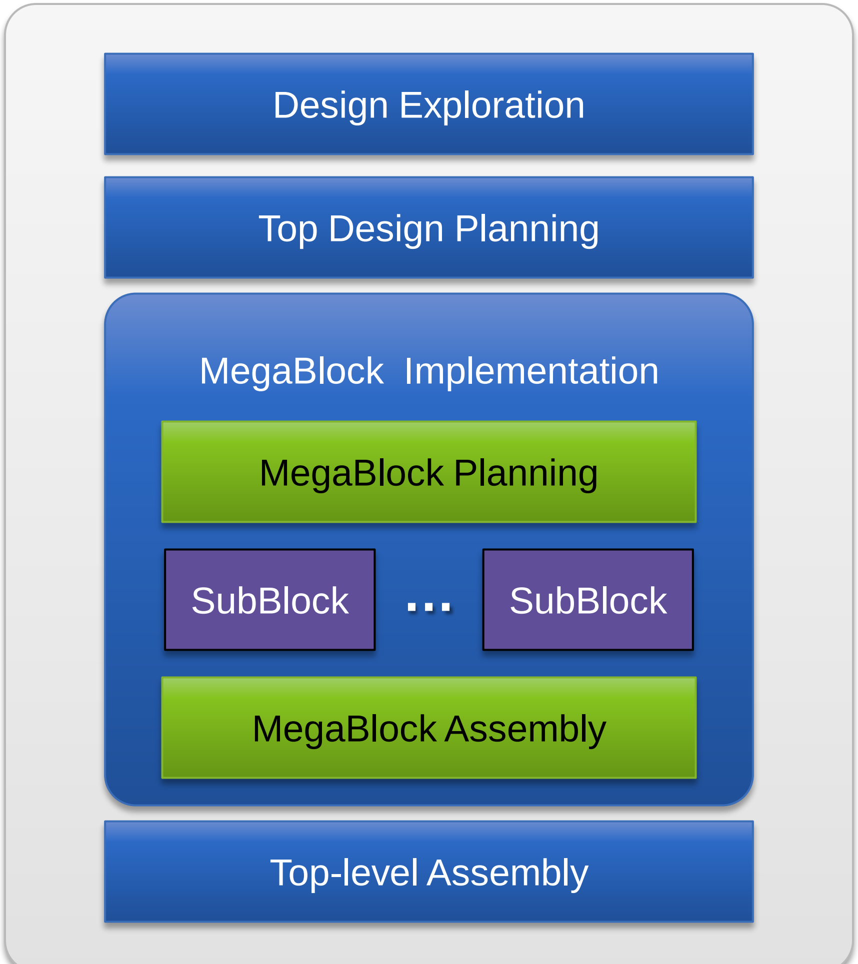
3D Chip Design Planning
Sub-problems

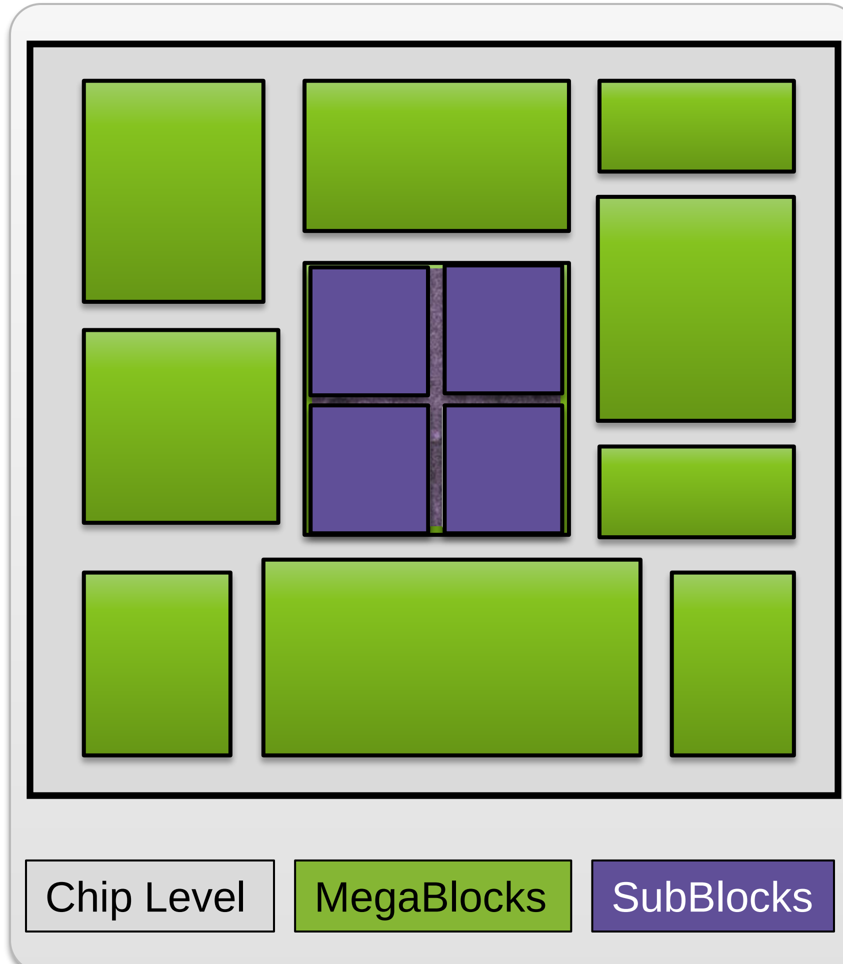


- Multi-die partitioning and floorplanning
  - Timing, power density
  - Through-silicon via planning
    - Optimal through silicon via assignments
    - Through-Si VIA and pin assignment
  - 3D visualization

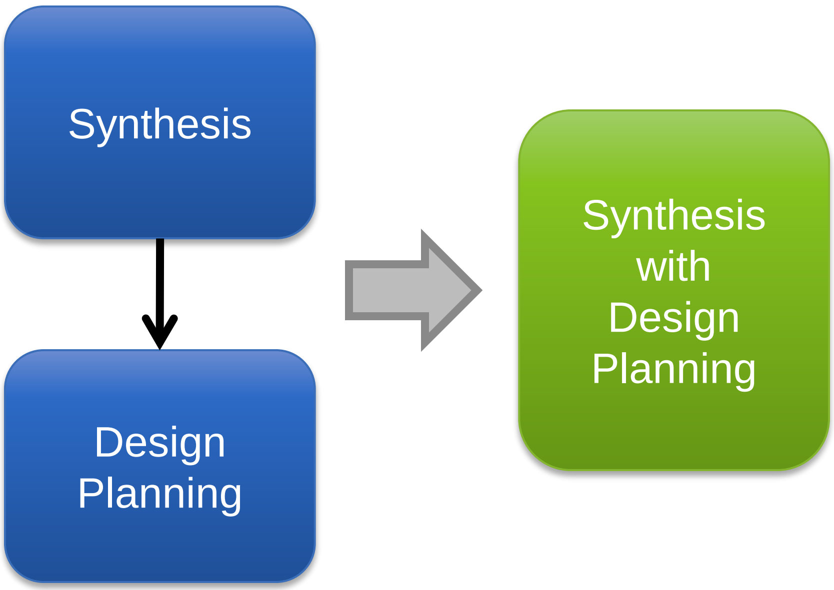
S.Fujita et al. "Perspectives and Issues in 3D-IC from Designer's Point of View", IEEE International Symposium on Circuits and Systems, 2009.
Xu He, et. al., SLIP 2009.

Multi-Level Hierarchical Design





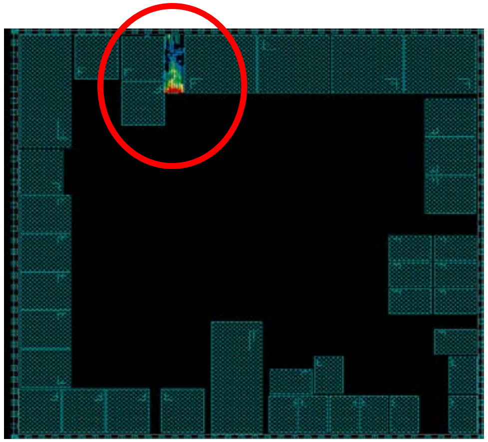
Design Planning and Logic Synthesis



- Floorplanning and logic synthesis impact each other
- Solving timing/congestion problems need synthesis and floorplanning solutions
- Enabling architectural decisions
- There is a need to bring logic synthesis and design planning closer

Design Planning and Logic Synthesis

Identify Congestion



Modify Floorplan

Congestion Fixed

Discussion

- Bringing design planning earlier into design flows is key to productivity and convergence
  - RTL design and synthesis with design planning
  - Handling evolving designs, constraints

- Traditional design planning to deal with emerging complexities in low power, design size, 3D chips.

Acknowledgements

- Jamil Kawa, Group Director R&D, Synopsys Inc.
- Dwight Hill, Principal Engineer, Synopsys Inc.
- Steve Kister, TMM, Synopsys Inc.