Wire Shaping is Practical

Hongbo Zhang and Martin D.F. Wong, **U of Illinois**
Kai-Yuan (Kevin) Chao, **Intel**
Liang Deng, **Broadcom**

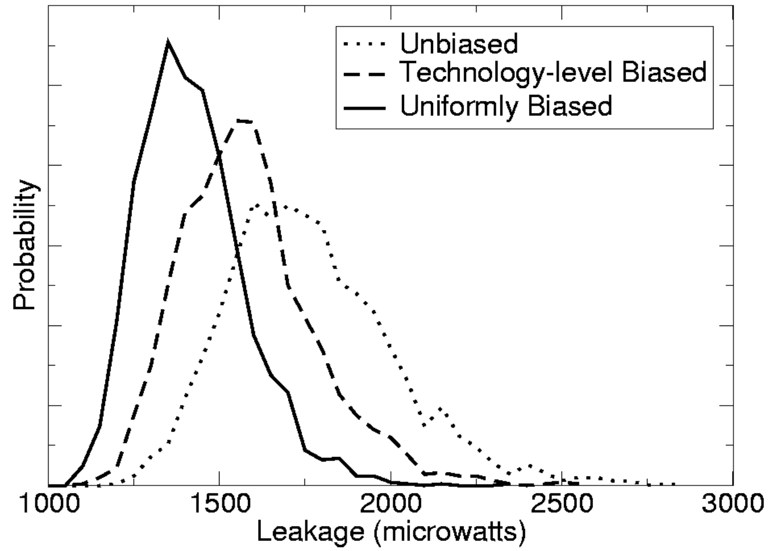
ISPD-09

Overview

- Practical wire shaping methodology for power minimization
- Manufacturing for design (MFD)
- Minimal design/manufacturing overhead
- Printability analysis of non-uniform wire shape by litho simulations

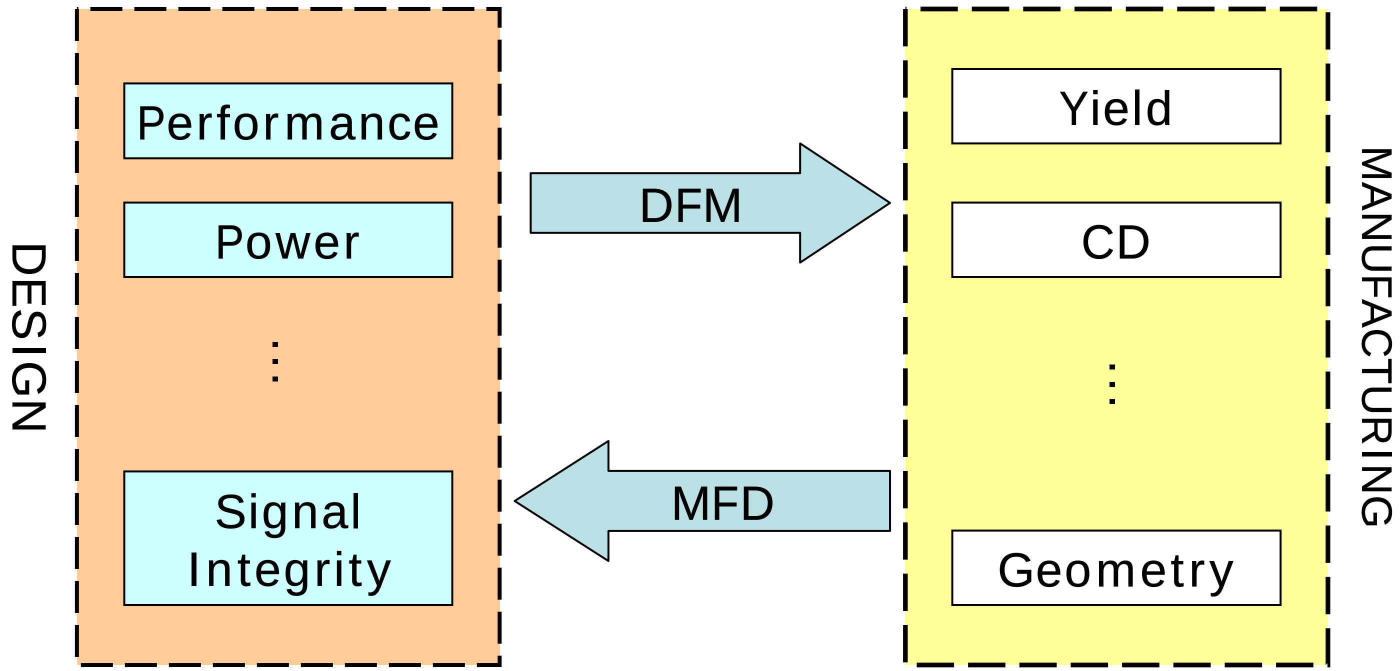
Manufacturing Impact Design

- Manufacturing has inevitable impacts on design
  - CMP → thickness
  - Lithography → pattern
  - Dummy fill → coupling capacitance
- Circuit properties can be modified during manufacturing
  - Poly gate bias for leakage



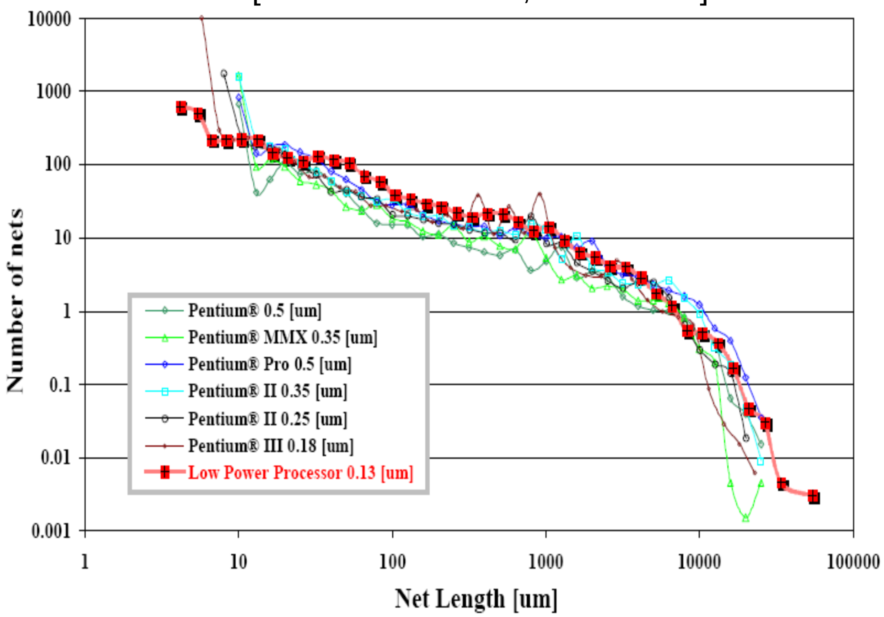
[Gupta & Kahng DAC04]

Manufacturing for Design



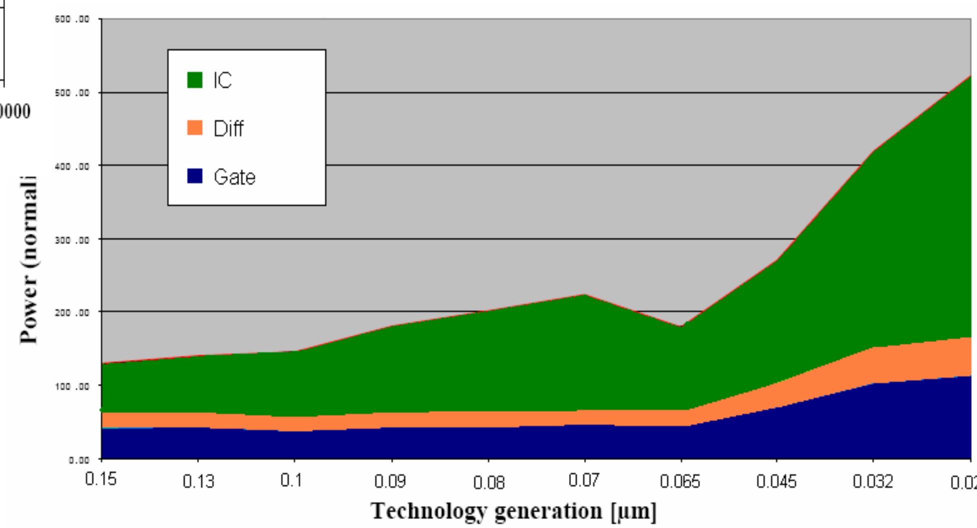
Interconnect Power Consumption

[Shekhar Y. Borkar, CRL – Intel]



- Reducing dynamic power consumption is important

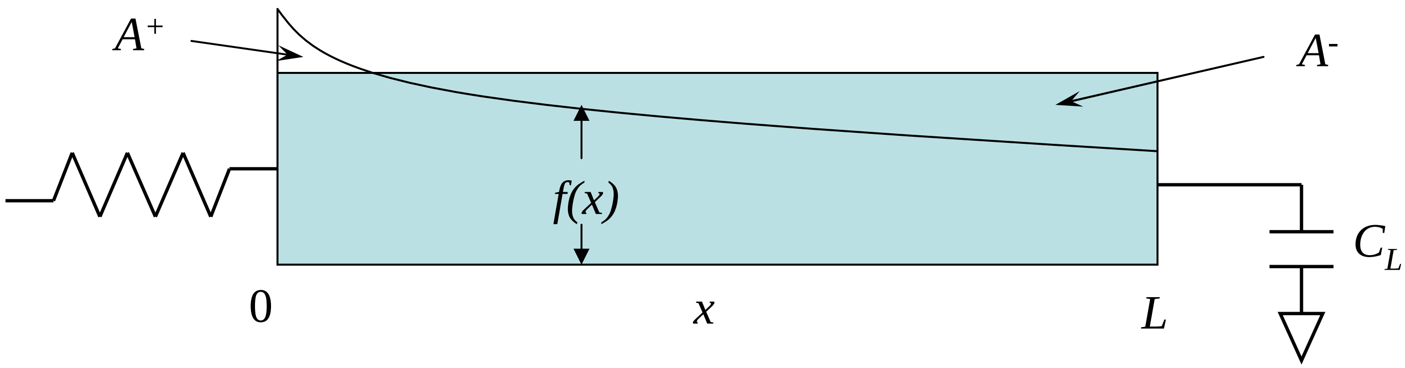
[Magen, et. al., SLIP04]



- Dynamic power consumption in interconnect makes up of 53% of the total dynamic power
- The share is increasing

Non-Uniform Wire Shape

- Non-uniform wire shape was studied for delay minimization (RC depends on wire shape)
- Exponential wire shape has been found to be effective for delay minimization



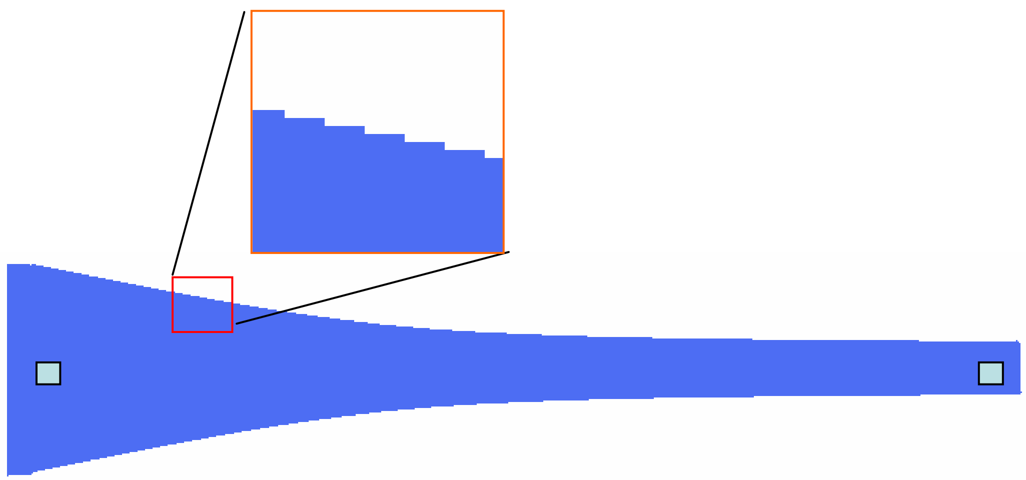
- We would like to use non-uniform wire shape to reduce power

$$\Delta P \propto \Delta C \propto \Delta A = A^{+} - A^{-}$$

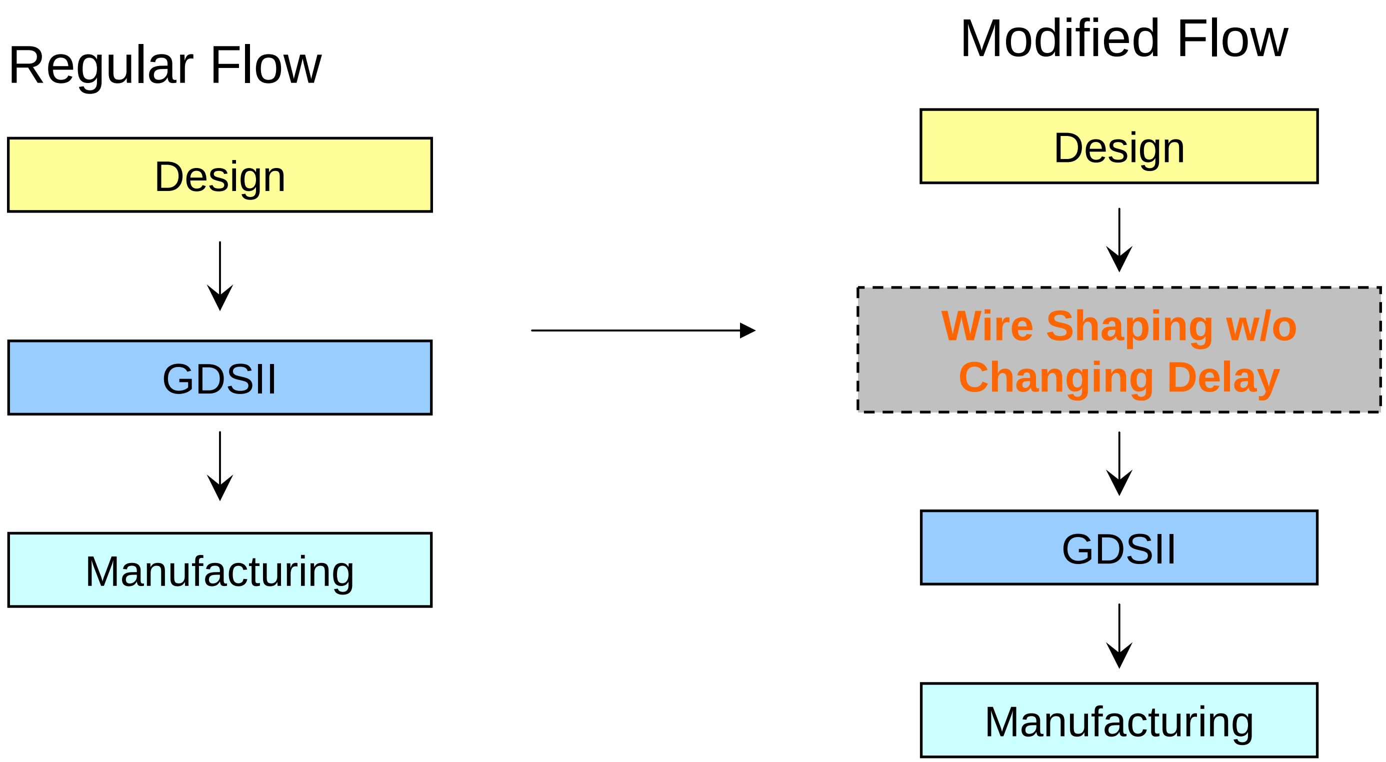
Is Non-Uniform Wire Shape Practical?

- Non-uniform wire shape was considered not practical
  - Routing tools can not handle it
  - Design database becomes too large
  - DRC issue

GDSII:



A Practical Flow with Wire Shaping



A Practical Flow with Wire Shaping

Design
↓
Wire Shaping w/o Changing Delay
↓
GDSII
↓
Manufacturing

GDSII size explosion!

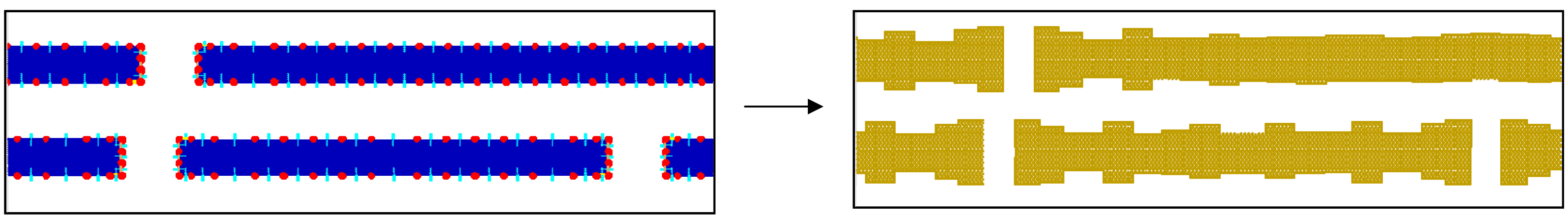
Design
↓
Wire Shaping w/o Changing Delay
↓
GDSII*
↓
Manufacturing*

GDSII*: GDSII with shape annotation
Manufacturing*: Minor modification for non-uniform wire shape

Manufacturing Non-Uniform Wire

- Current OPC technology can be easily modified to produce non-uniform wire shape
- OPC edge movement can be targeted for non-uniform wire shape
- Minimal extra cost

OPC

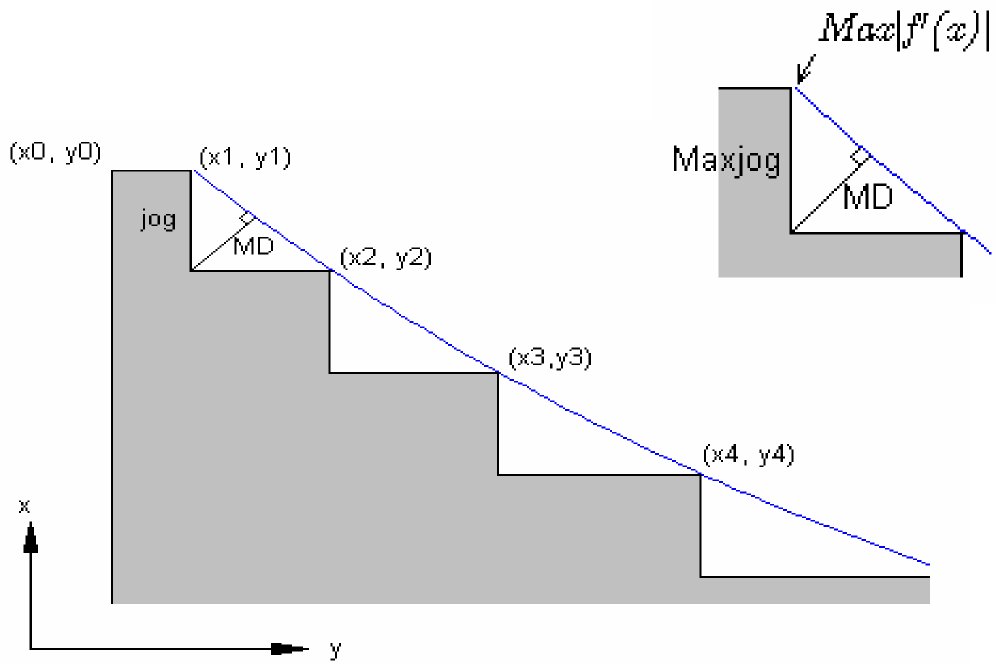


Edge Segmentation

Edge Movement + Optical Simulation

Improved Wire Segmentation for OPC

- Minimize number of stages by an improved wire segmentation scheme
- Can be easily integrated into mainstream OPC tools



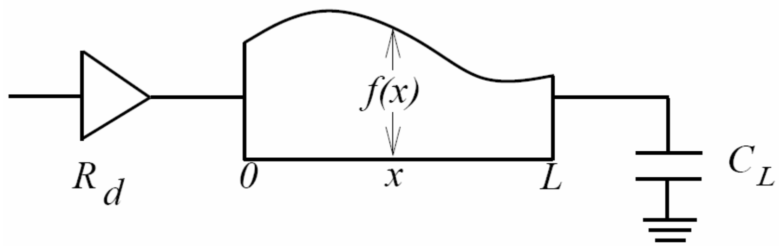
Algorithm for Wire Segmentation

- Trade-off between number of segments and error of wire shape approximation
- Minimize number of segments subject to given error bound on shape approximation
- Iterative algorithm
  - Pick next segmentation point by the equation

$$x_{i+1} = x_i + \frac{\max\_jog}{f'(x_i)} \sqrt{\frac{f'^2(x_i)+1}{\max^2 \left| f'(x) \right| + 1}}$$

  - Stage length is monotonically increasing

Exponential Wire Shape



Delay: $D(f) = R_d(C_L + \int_0^L c_0 f(x)dx) + \int_0^L \frac{r_0}{f(x)}(\int_x^L c_0 f(t)dt + C_L)dx$

Dynamic Power: $P(f) = \alpha(C_L + c_f L + c_o \int_0^L f(x)dx)V_{DD}^2 f_{clk}$

Problem: Minimize $P(f)$ s.t. $D(f) = delay$

Optimal Solution: $f(x) = ae^{-bx}$

Wire Shape Optimization

Known: min $D(f)$ → f is exponential

Our Problem: min $P(f)$ s.t. $D(f) = delay$

Equivalent Problem: min $P(f)$ s.t. $D(f) \leqslant delay$

Can be solved by Lagrangian Relaxation (LR):

- Discrete version: min $P(y_1, \ldots, y_n)$ s.t. $D(y_1, \ldots, y_n) \leqslant delay$
- Geometric program → Convex → Exactly solved by LR
- Fix $\lambda \geq 0$, solve min $P(y_1, \ldots, y_n) + \lambda (D(y_1, \ldots, y_n) - delay)$
- Update λ and iterate
- Discrete version → Continous version as $n \to \infty$

Wire Shape Optimization

min $P(f)$ s.t. $D(f) = delay$

$\Downarrow$

min $P(f) + \lambda\,(D(f) - delay)$

$\Downarrow$

min $\lambda\ \mathbf{D}(f)$ + constant

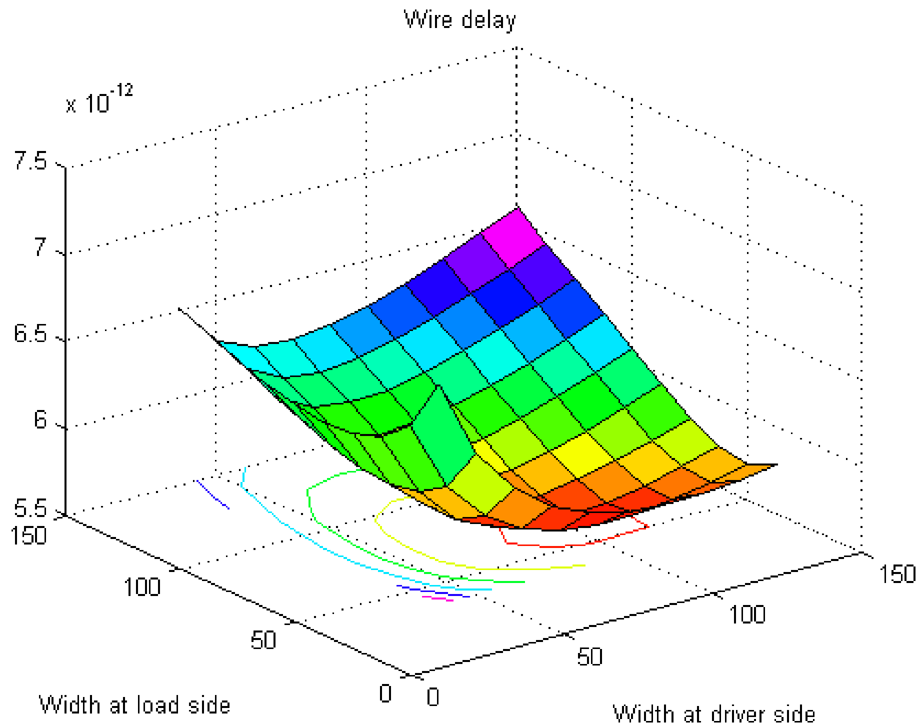
$\Downarrow$

min $\mathbf{D}(f)$

D(f) is delay with modified driver resistance

Exponential Wire Shape!

Wire Delay vs. Wire Shape

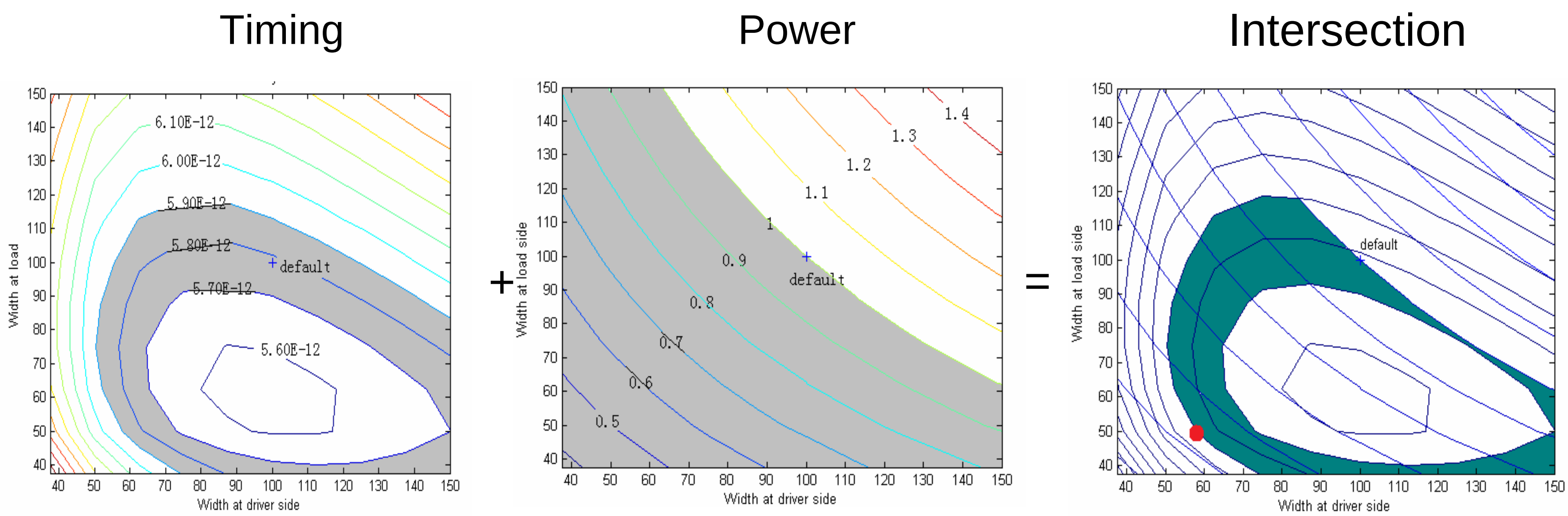


Wire Delay vs Wire Shape

100um length, 45nm technology
Original: 100nm wire width

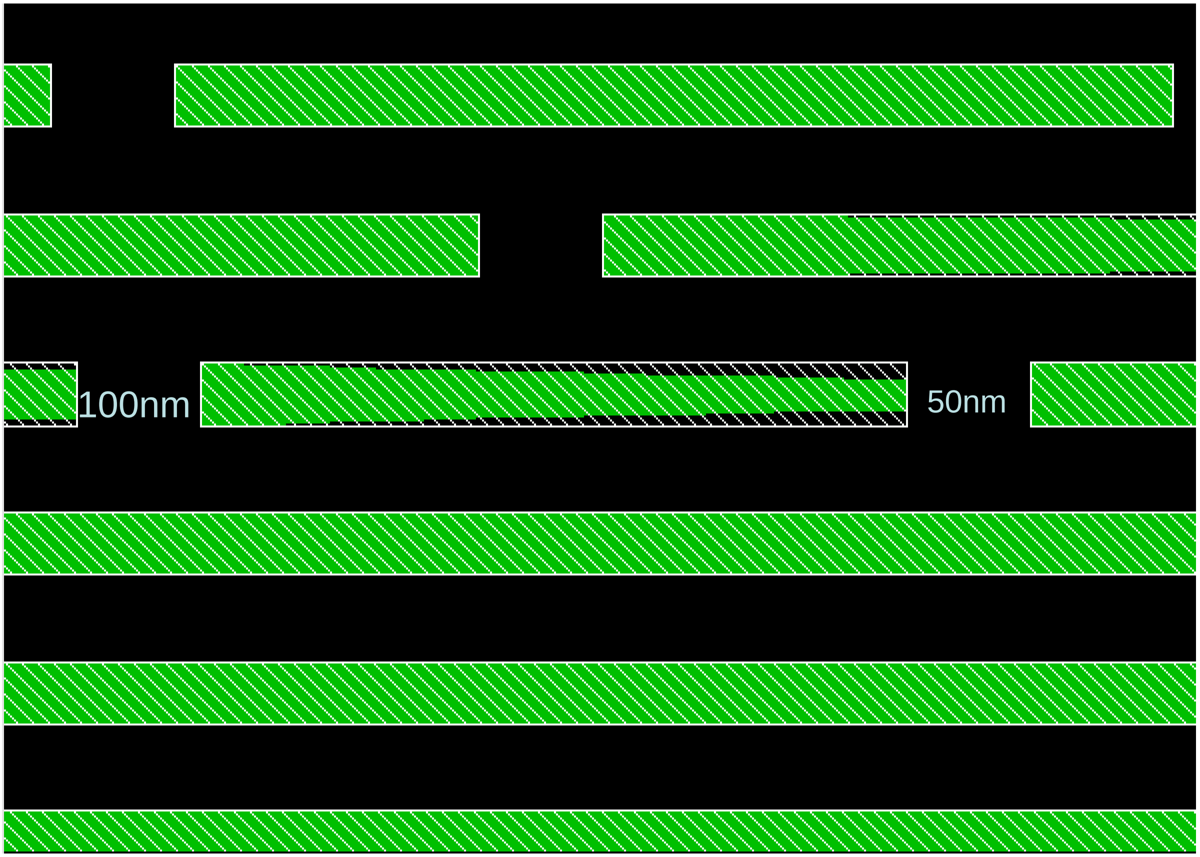
- HSPICE
- Constraints:
  - Small timing range
  - W_{max} and W_{min}
  - Exponential wire shape

Optimal Wire Shape



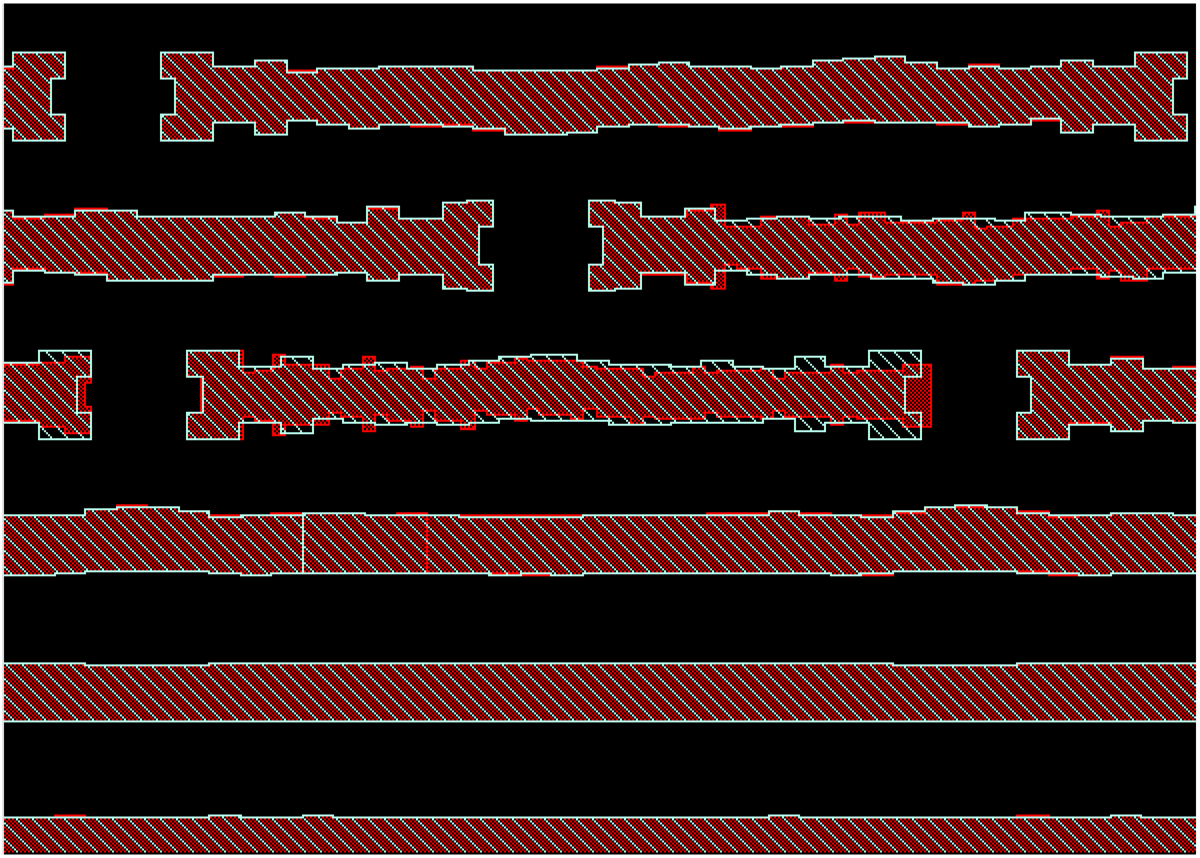
Obtain optimal wire shape from a set of wire shape candidates

Exponential vs. Uniform (Ideal)

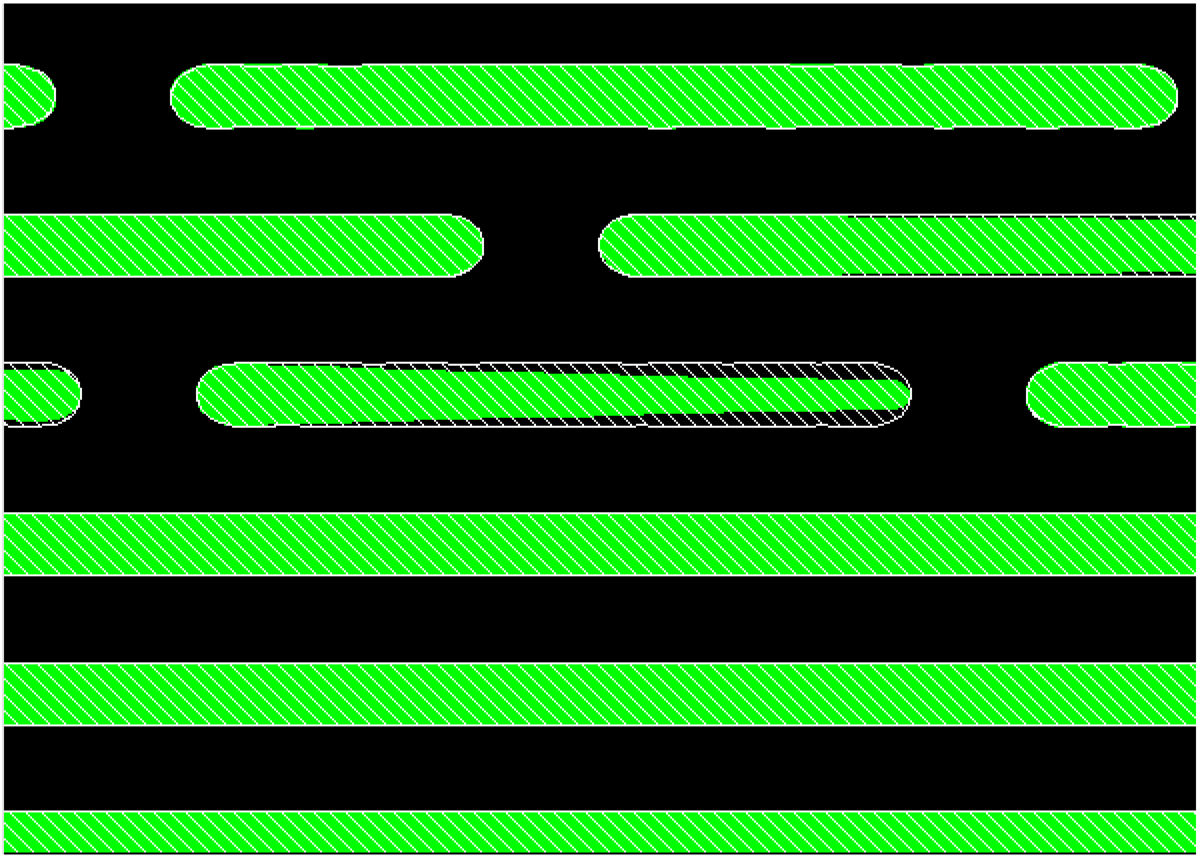


Pitch: 240nm
Max: 100nm
Min: 45nm

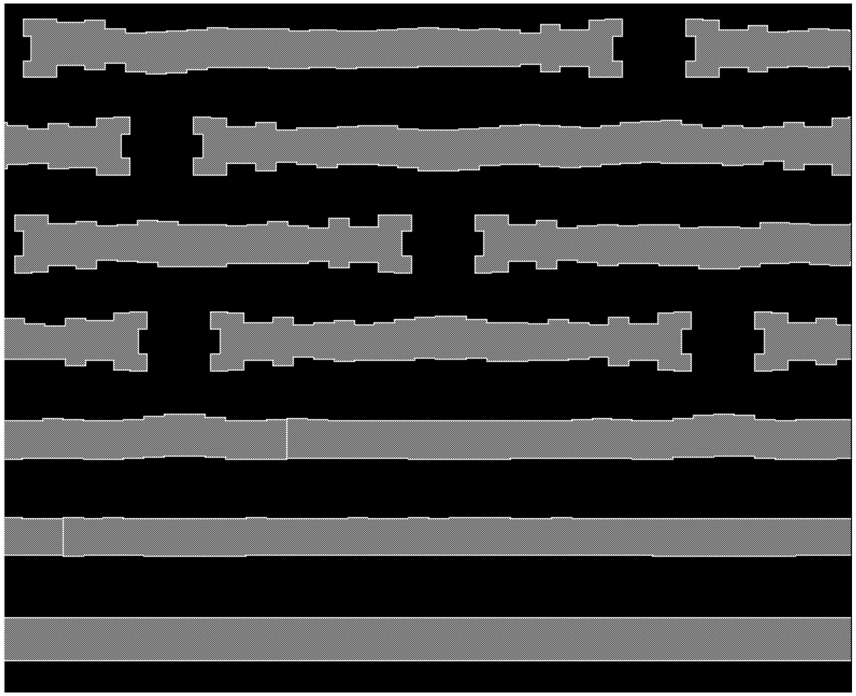
Exponential vs. Uniform (Mask)



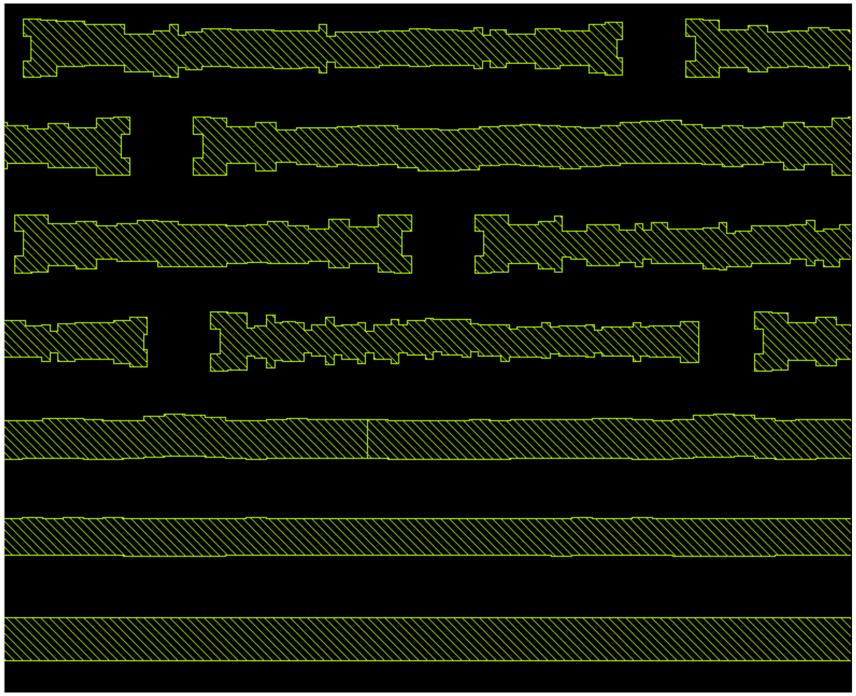
Exponential vs. Uniform (Silicon)



Similar Mask Complexity

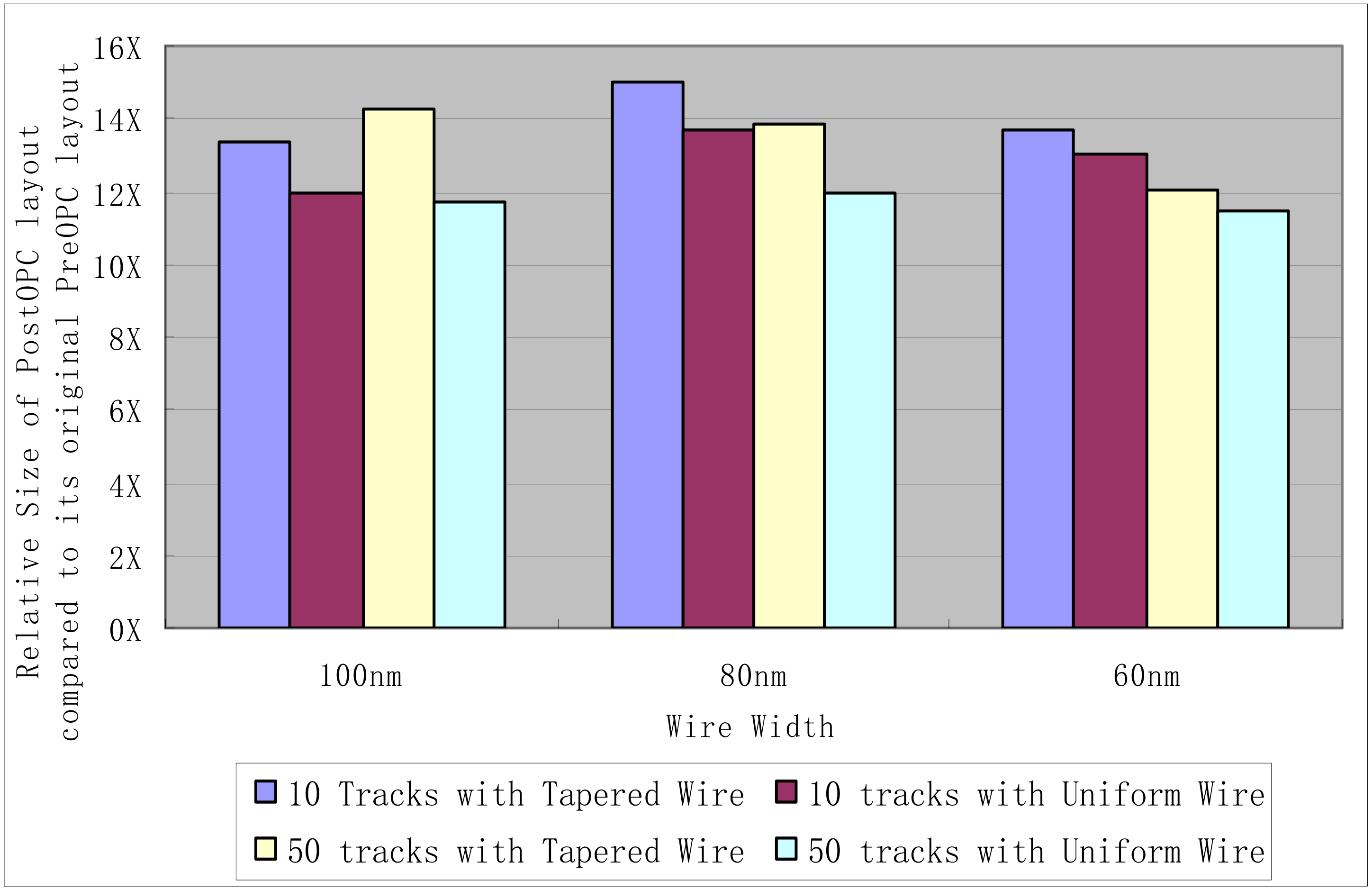


uniform



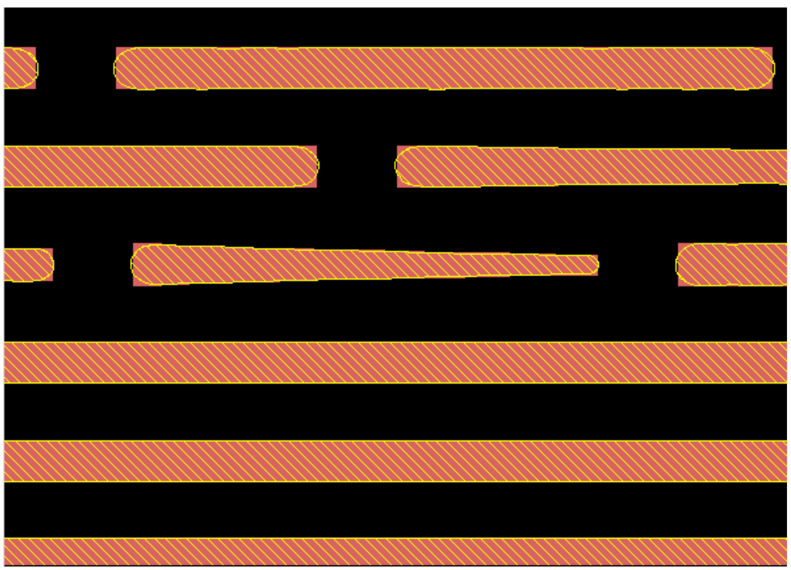
exponential

Post-OPC GDSII Size Comparison



Accurate Fabrication of Exponential Wire

- Original wire width is 100nm and pitch is 240nm
- Extraction and timing simulation are based on post-OPC simulation
- Timing and area control is accurate



Wire Length (um)	Wsource (nm)	Wsink (nm)	Diff in Capacitance	Diff in Timing
50	65	52.5	4.61%	-0.32%
75	60	50	2.97%	-0.43%
100	65	50	5.55%	-0.68%
250	70	47.5	-0.29%	-1.23%
500	75	47.5	-3.54%	-1.22%
750	67.5	45	-3.17%	-0.44%
1000	67.5	45	-3.28%	-0.43%

Intended wire shape vs. simulated wire shape

Results on Power Minimization

Wire Length (um)	Wsource (nm)	Wsink (nm)	Saving in Capacitance	Saving in Dynamic Power	Delay Variation
50	65	52.5	38.71%	17.50%	1%
75	60	50	43.47%	24.04%	1%
100	65	50	39.57%	24.64%	2%
250	70	47.5	42.03%	33.83%	1%
500	75	47.5	41.79%	37.28%	2%
750	67.5	45	46.16%	42.71%	1%
1000	67.5	45	46.22%	43.58%	1%

Power Minimization v.s. Delay Minimization

- Wire Shaping is more effective for power minimization

Power Minimization

Wire Length (μm)	W_{source} (nm)	W_{sink} (nm)	Decrease in Capacitance	Saving in Dynamic Power	Delay Variation
50	65	52.5	38.71%	17.50%	1%
75	60	50	43.47%	24.04%	1%
100	65	50	39.57%	24.64%	2%
250	70	47.5	42.03%	33.83%	1%
500	75	47.5	41.79%	37.28%	2%
750	67.5	45	46.16%	42.71%	1%
1000	67.5	45	46.22%	43.58%	1%

Delay Minimization

Wire Length (μm)	W_{source} (nm)	W_{sink} (nm)	Decrease in Capacitance	Saving in Dynamic Power	Saving in Delay
50	87.5	62.5	26.72%	12.08%	2.91%
75	87.5	62.5	26.79%	14.82%	5.15%
100	100	62.5	20.98%	13.06%	5.46%
250	125	50	20.18%	16.25%	5.61%
500	150	45	14.62%	13.04%	8.06%
750	150	45	14.65%	13.55%	11.93%
1000	150	45	14.72%	13.88%	12.42%

Conclusion

- Presented a wire shaping methodology with minimal design/manufacturing overhead
- Demonstrated accurate printing of exponential wire shape by litho simulations
- Obtained substantial reduction of power without affecting timing closure
- An excellent example of manufacturing-for-design
- Wire shaping is practical