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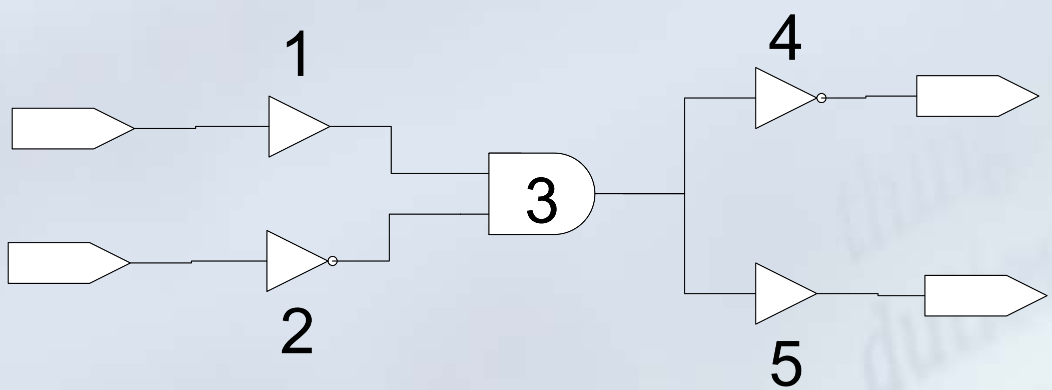
Multi-Voltage Floorplan Design with Optimal Voltage Assignment

Introduction

- Dilemma between delay & power
  - Power is proportional to Voltage
  - Gate Delay is adversely proportional to Voltage



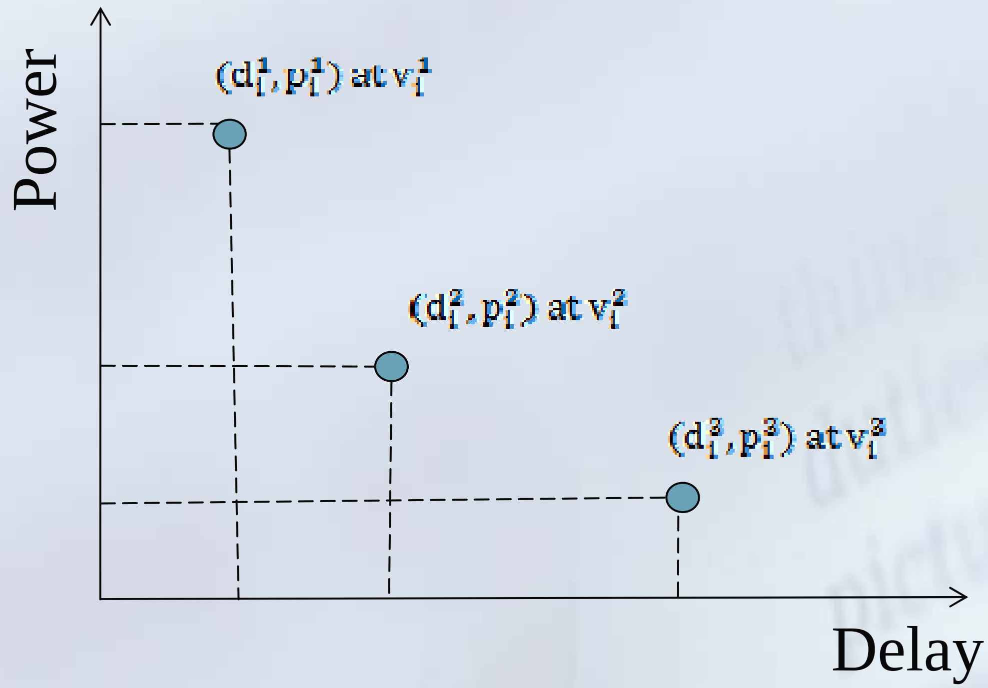
Problem Formulation

- *Given a netlist of modules, each of which has multiple choices of supply voltages and corresponding power consumptions, and a clock cycle, generate a floorplan with a voltage assignment to each module such that the timing constraint is satisfied and a weighted sum of the total power consumption (due to cells and level shifters), power network routing resources, area and wire length is minimized*

Problem Formulation

- Power-delay trade-off

The power-delay trade-off in cell m_l is represented by k_l delay-power pairs, $\{(d_l^1, p_l^1), (d_l^2, p_l^2), \ldots, (d_l^{k_l}, p_l^{k_l})\}$.



Problem Formulation

Minimize: $\sum_{v_i \in V} \sum_{q=1}^{k_i} p_i^q u_i(q) + \sum_{e(i,j) \in E} LS(i,j) \cdot \varphi$ (1a)

Subject to:

$$\sum_{q=1}^{k_i} u_i(q) = 1 \quad \forall v_i \in V \qquad (1b)$$

$$\sum_{e(i,j) \in C} \left(\sum_{q=1}^{k_i} d_i^q u_i(q) + \rho LS(i,j) + \omega(i,j) \le T_{cycle} \right) \quad \forall C \in \Phi_k \qquad (1c)$$

$$LS(i,j) = \begin{cases} 0 & \sum_{q=1}^{k_i} v_i^q u_i(q) \ge \sum_{q=1}^{k_j} v_j^q u_j(q) \\ 1 & \text{otherwise} \end{cases} \qquad (1d)$$

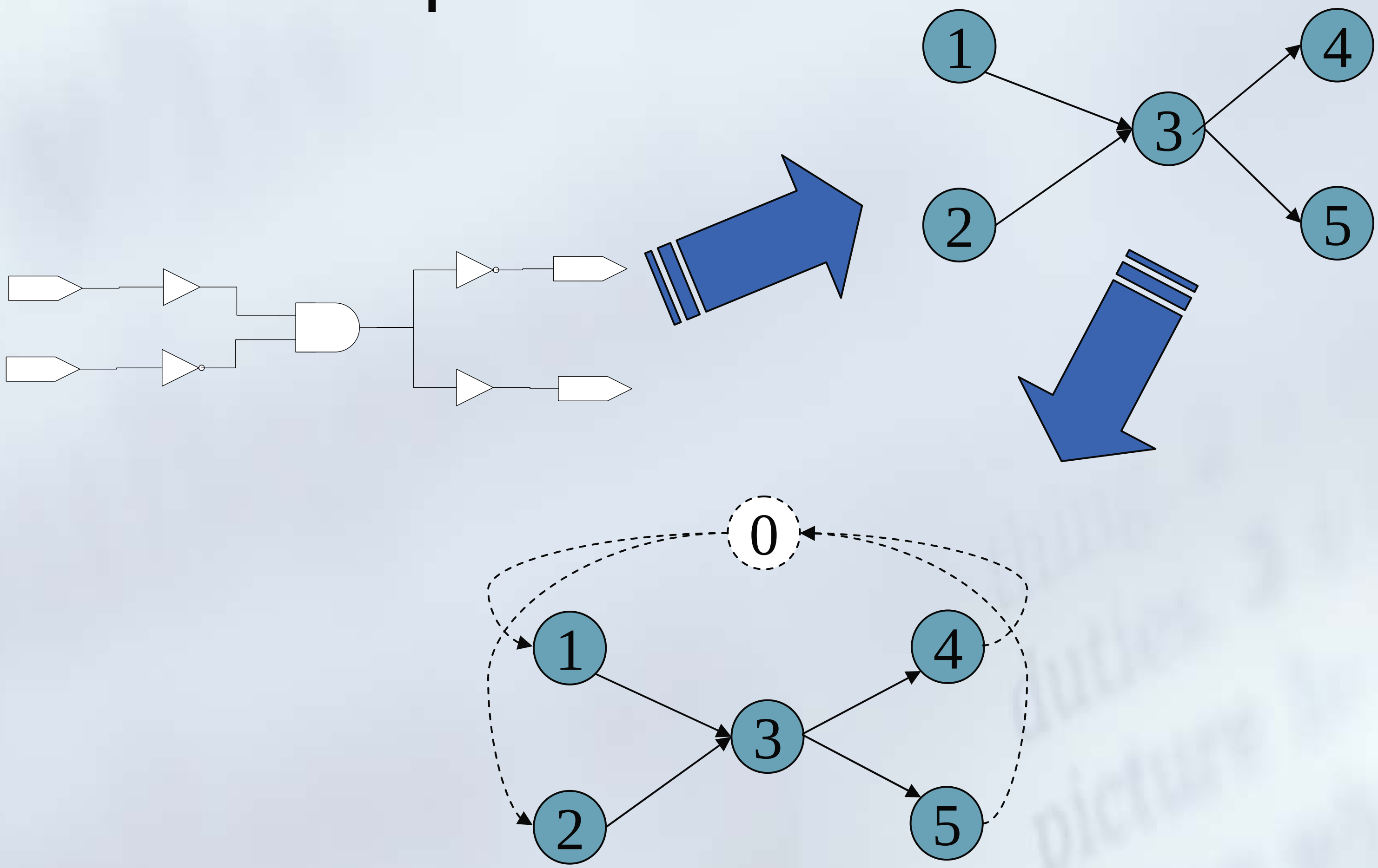
$$u_i(q) \in \{0,1\} \qquad q = 1,2,\ldots,k_i, \forall v_i \in V \qquad (1e)$$

Problem Formulation

- Modeling used in our approach
  - Directed Graph
  - DP-Curve

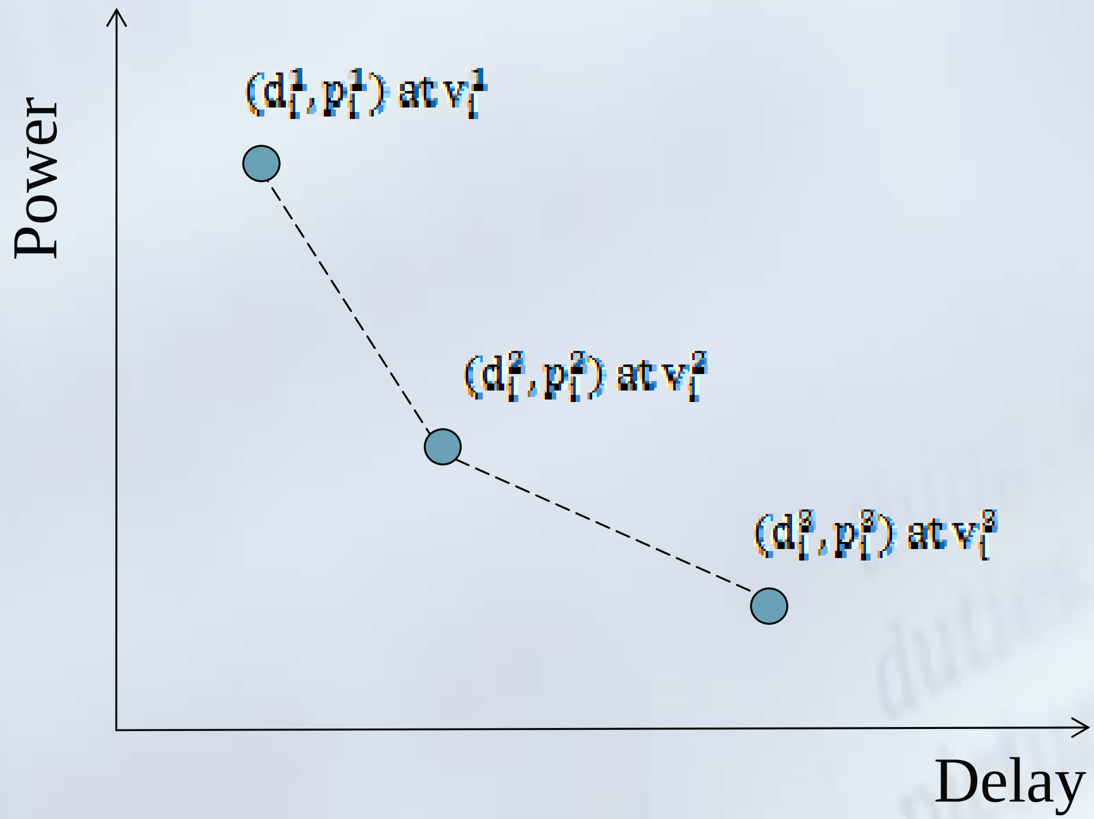
Problem Formulation

- Directed Graph



Problem Formulation

- DP-Curve

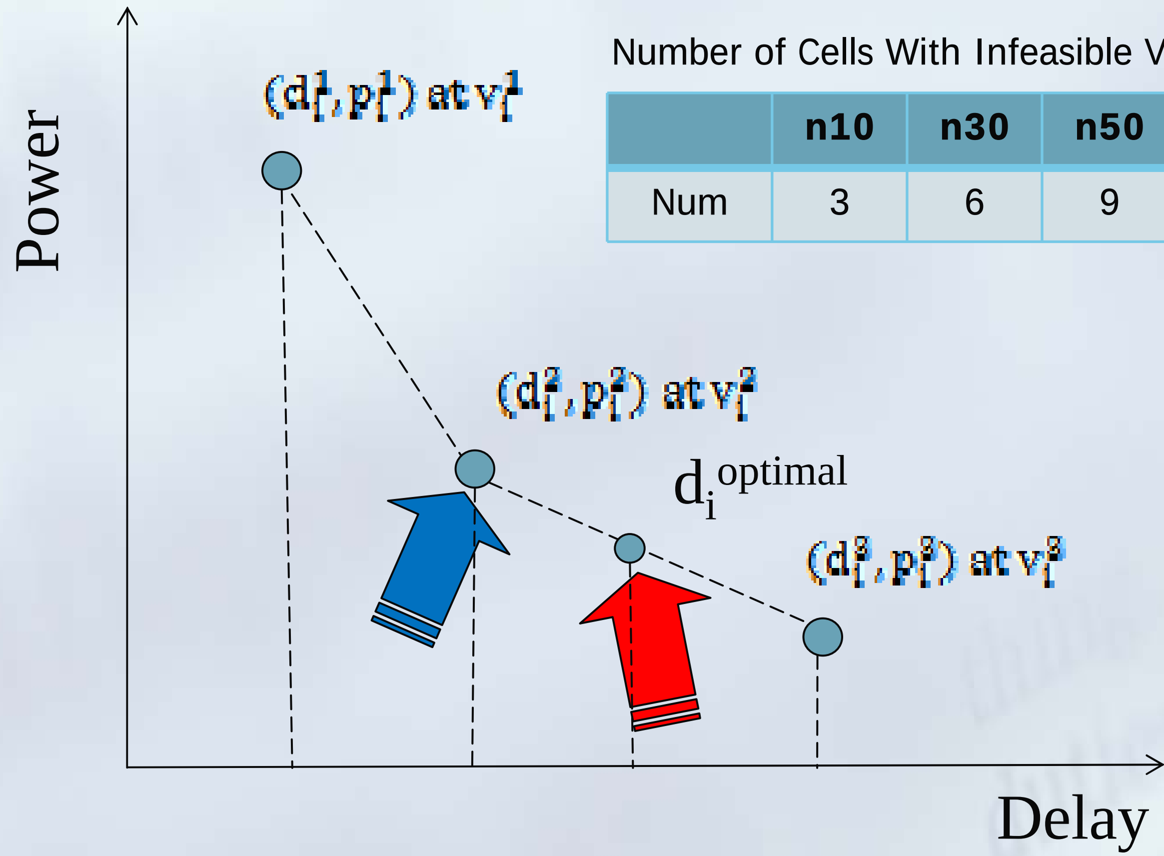


Previous Work

- [1]W.-P. Lee, H.-Y. Liu and Y.-W. Chang, “An ILP Algorithm for Post-Floorplanning Voltage-Island Generation Considering Power-Network Planning”, ICCAD 2007

- [2]Q. Ma and Evangeline F.Y. Young, “Network Flow Based Power Optimization Under Timing Constraints in MSV-Driven Floorplanning”, ICCAD 2008

Previous Work



Number of Cells With Infeasible Voltage Levels

	n10	n30	n50	n100	n200	n300
Num	3	6	9	5	21	13

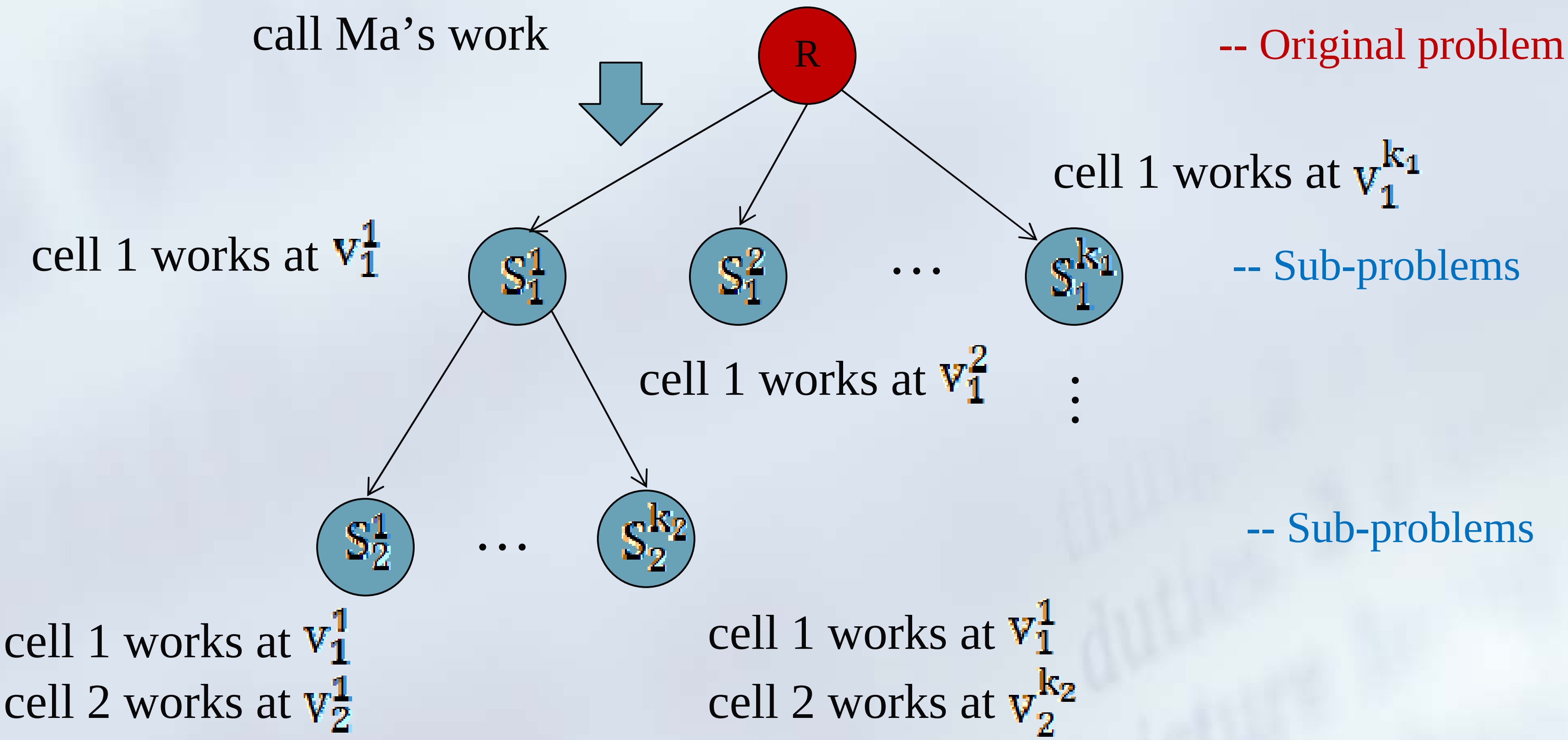
[2] Q. Ma and Evangeline FY. Young, "Network Flow Based Power Optimization Under Timing Constraints in MSV-Driven Floorplanning", ICCAD 2008

Our Approach-Branch and Bound

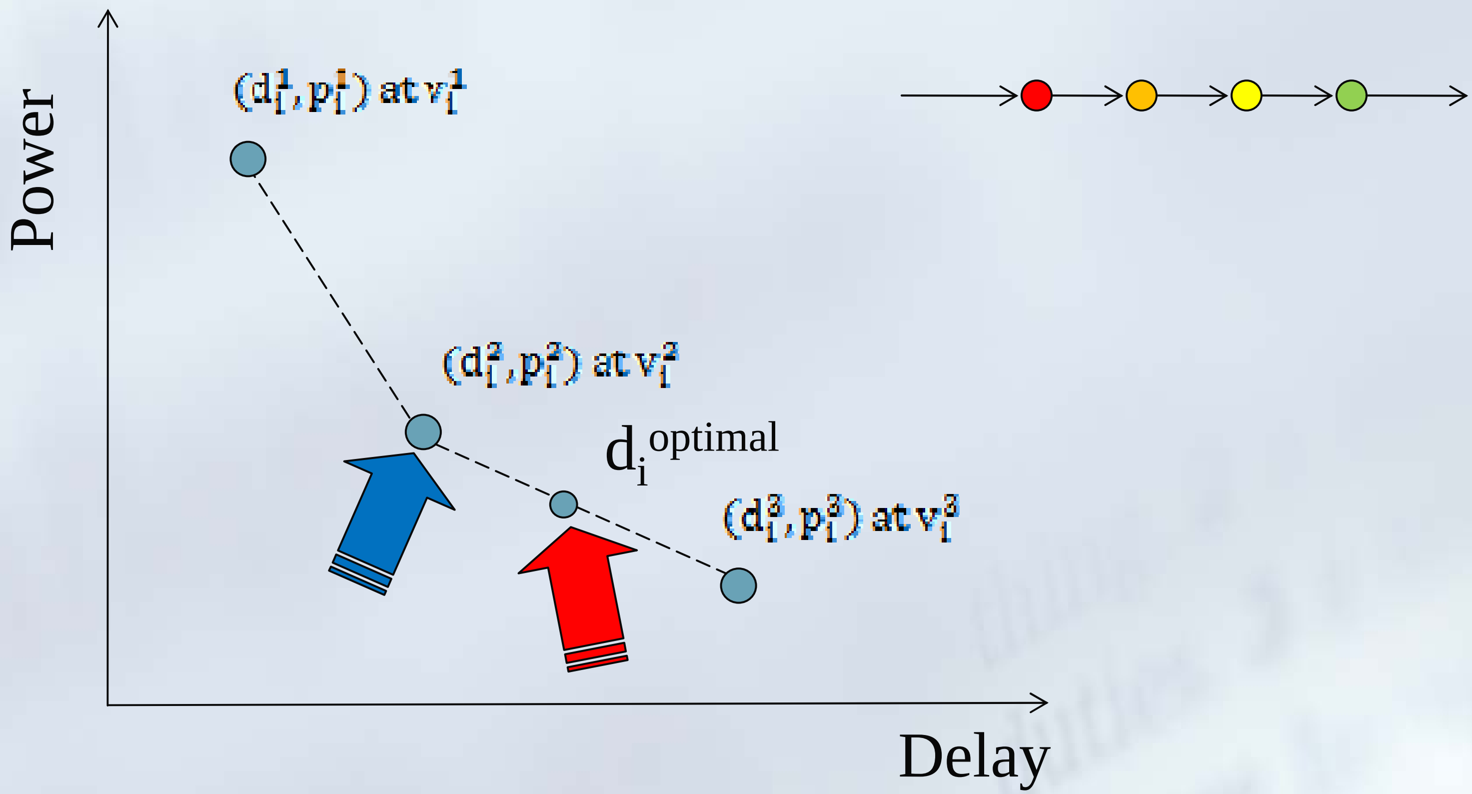
- NP-hard[3]
- Branch & Bound Search
  - Branching Rules
  - Upper Bounds
  - Lower Bounds
  - Pruning Rules
  - Value-Oriented Searching Rules

[3] J.-M. Chang, M. Pedram, “Energy Minimization Using Multiple Supply Voltage”, VLSI SYSTEMS, VOL.5, NO.4, DEC. 1997

Branching Rules



Upper Bound



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Lower Bound

- Linear Relaxation

$$\text{Minimize: } \sum_{v_i \in V} \sum_{q=1}^{k_i} p_i^q u_i(q) + \sum_{e(i,j)\in E} LS(i,j) \cdot \varphi \qquad (5a)$$

Subject to:

$$\sum_{q=1}^{k_i} u_i(q) = 1 \quad \forall v_i \in V \qquad (5b)$$

$$\sum_{e(i,j)\in C} \left(\sum_{q=1}^{k_i} d_i^q u_i(q) + \rho LS(i,j) + \omega(i,j) \leq T_{cycle} \right) \quad \forall C \in \Phi_k \qquad (5c)$$

$$LS(i,j) \geq u_i(q_1) + u_j(q_2) - 1$$

$$\forall e(i,j) \in E, \forall q_1 \forall q_2 \text{ s.t. } (0 \leq q_1, q_2 \leq k) \wedge (q_2 > q_1) \qquad (5d)$$

$$0 \leq LS(i,j) \leq 1, \forall e(i,j) \in E \qquad (5e)$$

$$0 \leq u_i(q) \leq 1, \quad q = 1,2,\ldots,k_i, \forall v_i \in V \qquad (5f)$$

Pruning Rules

- We will prune a subtree when
  - The approach in [2] cannot return a feasible supply voltage level satisfying the timing constraint even assuming a continuous domain for the module voltage
  - Lower bound is greater than or equal to the global upper bound

[2] Q. Ma and Evangeline F.Y. Young, “Network Flow Based Power Optimization Under Timing Constraints in MSV-Driven Floorplanning”, ICCAD 2008

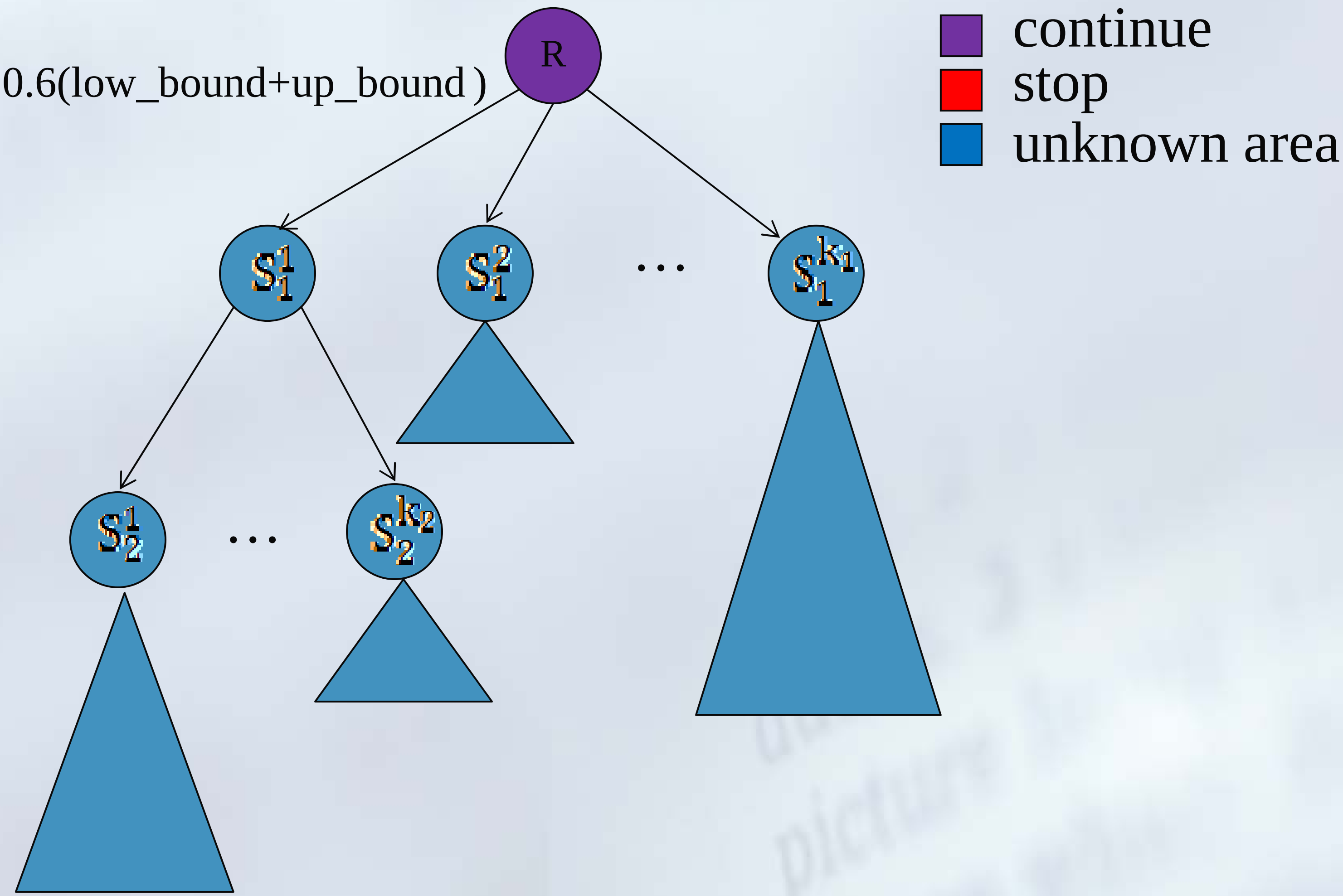
Value-Oriented Searching Rules

- Search those sub-trees with a higher chance of returning an optimal solution
- Use a variable called “target” to guide the searching
- Search into a sub-tree of some vertex only when the lower bound of that vertex is less than this target
- Increase the target by a constant after each searching

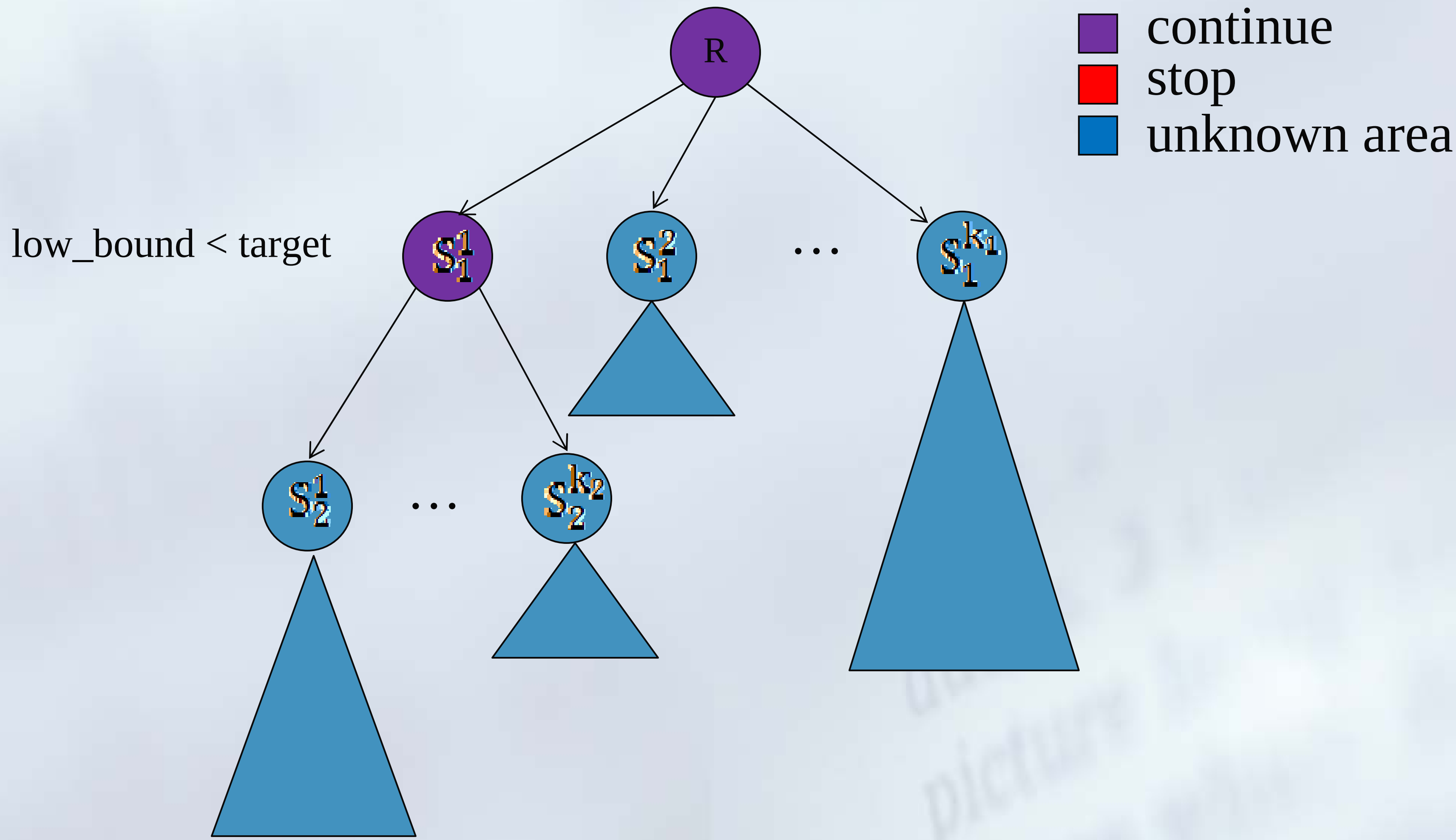
Value-Oriented Searching Rules

Initially

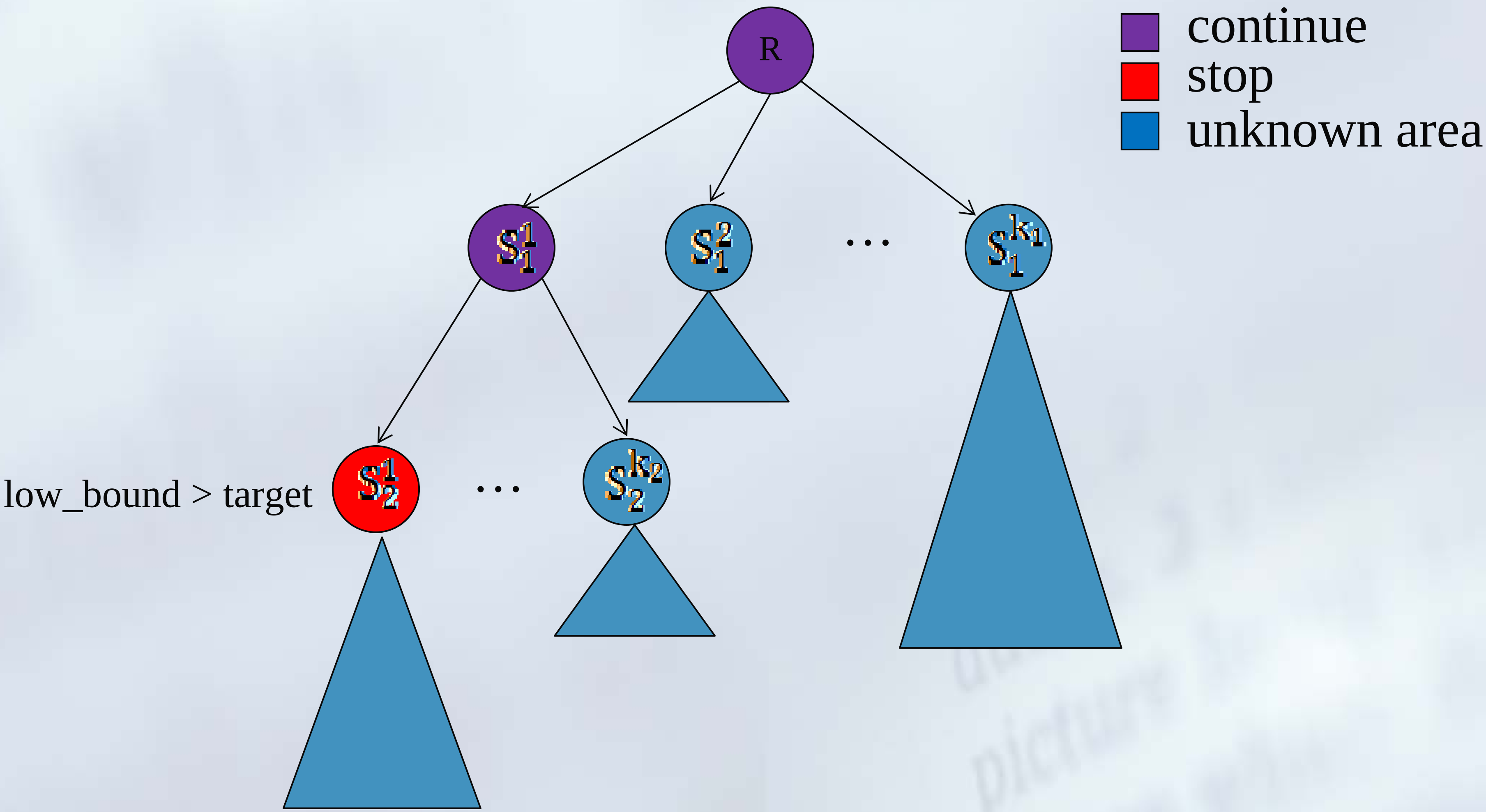
target = 0.6(low_bound+up_bound)



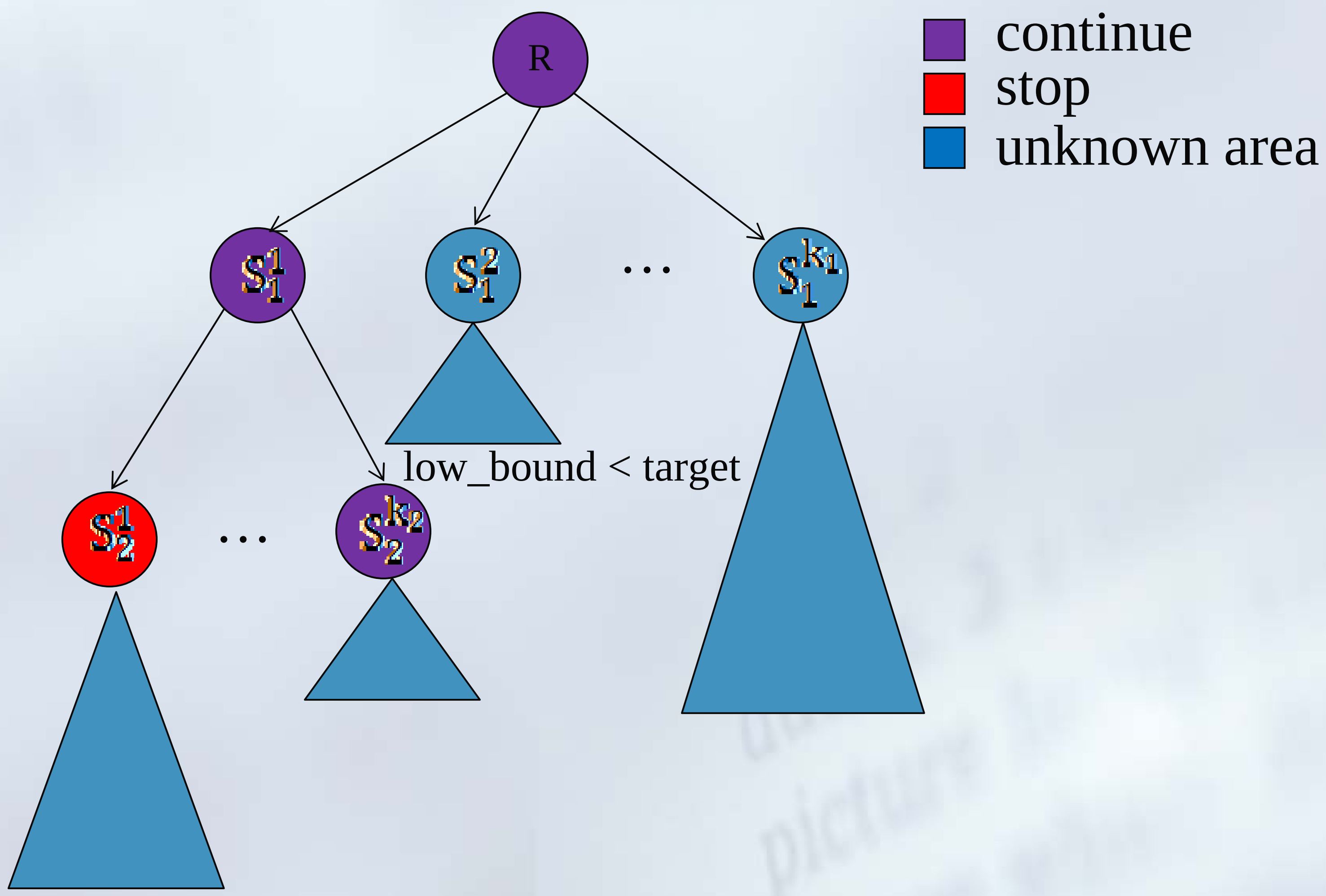
Value-Oriented Searching Rules



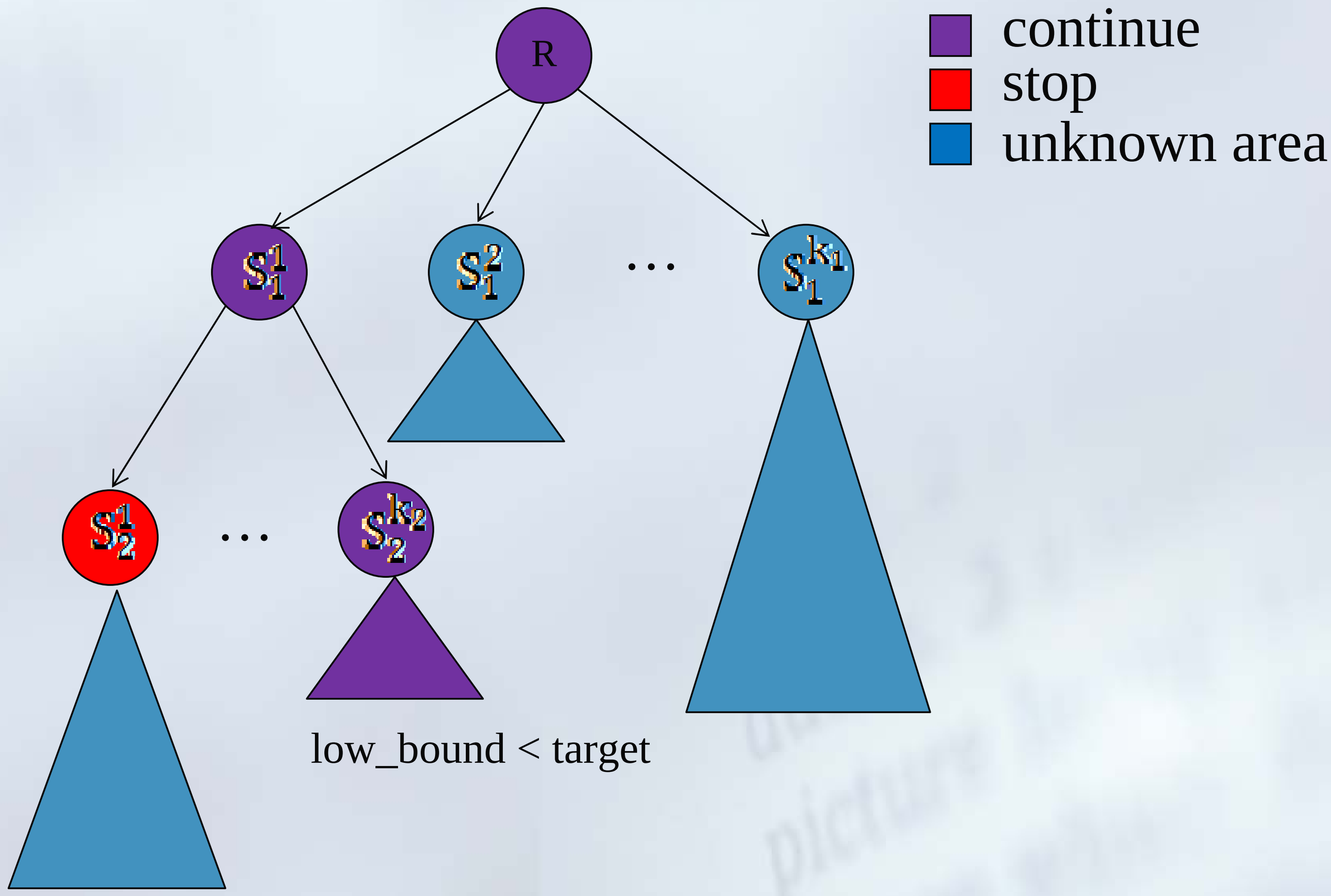
Value-Oriented Searching Rules



Value-Oriented Searching Rules

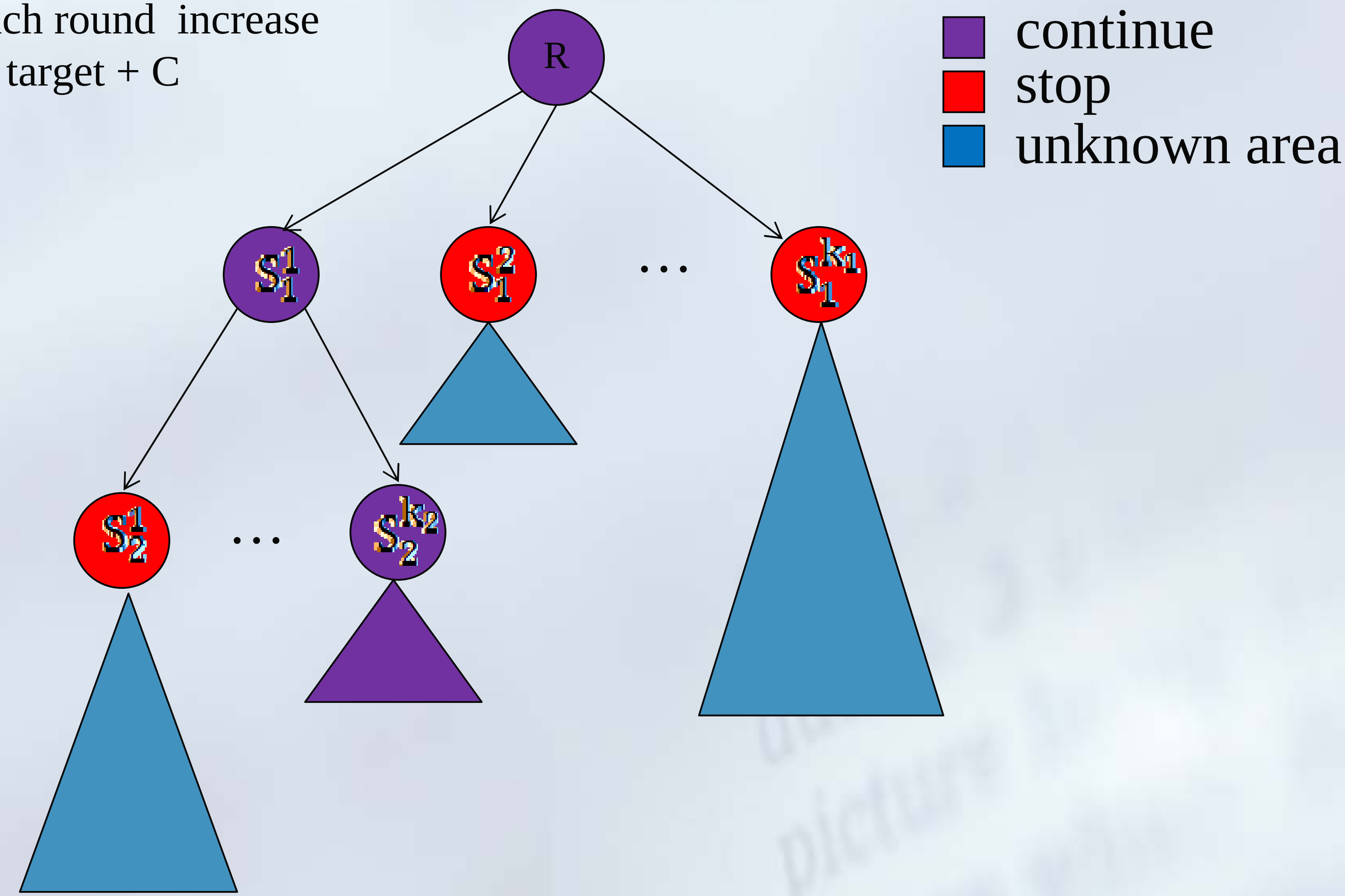


Value-Oriented Searching Rules



Value-Oriented Searching Rules

After each round increase
target = target + C



Multi-Voltage Assignment Results

Test benches	Power		Ratio	Average No. of cells with Different Voltages
	[2]	VOBB		
n10	202709	185270	91.4%	1.7
n30	162534	155853	95.9%	2.9
n50	166931	157163	94.1%	7.8
n100	137608	126855	92.2%	9.9

VOBB: Our Value-Oriented Branch and Bound

[2] Q. Ma and Evangeline F.Y. Young, "Network Flow Based Power Optimization Under Timing Constraints in MSV-Driven Floorplanning", ICCAD 2008

Multi-Voltage Assignment Results

Test Benches	Power		Runtime	
	VOBB	[1]	VOBB	[1]
n10	169058	169058	1.2 s	0.0 s
n30	143460	143460	12.1 s	10 h
n50	138983	138983	35.0 s	11.1 m
n100	113231	*117761	10.0 m	10 h
n200	*119229	*116341	10 h	10 h
n300	142641	*143041	32.4 m	10 h
Average	137767	138107	-	-

[1] W.-P. Lee, H.-Y. Liu and Y.-W. Chang, “An ILP Algorithm for Post-Floorplanning Voltage-Island Generation Considering Power-Network Planning”, ICCAD 2007

Floorplanning

- VOBB-FP
  - Initial Floorplan
  - Optimal Voltage Assignment (VOBB)
  - Second Floorplan
  - Final Optimal Voltage Assignment (VOBB)

Floorplanning Results

Test Benches	Power Cost with Level Shifters(P)		Power Network Routing Resources		Level Shifter Number		Dead Space (%)		Wire Length	
	VOBB-FP	[2]	VOBB-FP	[2]	VOBB-FP	[2]	VOBB-FP	[2]	VOBB-FP	[2]
n10	169058	189942	1373	1530	8	4	2.12	1.77	6920.7	7781.3
n30	143460	151483	1354	1577	21	25	7.05	9.12	28814.2	29283.0
n50	138983	153084	1662	1641	32	34	10.82	9.72	64532.2	64623.6
n100	113231	120850	1446	1528	50	77	9.59	8.64	116552.8	116681.6
n200	121222	130489	1626	1584	94	129	14.30	12.49	198205.8	210457.2
n300	142641	161464	1690	1806	30	92	12.52	10.37	229116.1	240326.2
Average	**138099**	**151219**	**1525**	**1611**	**39**	**60**	**9.46**	**8.68**	**107357.0**	**111525.5**

[2] Q. Ma and Evangeline F.Y. Young, “Network Flow Based Power Optimization Under Timing Constraints in MSV-Driven Floorplanning”, ICCAD 2008

Conclusions

- This work is a major extension over the previous work [2]. The work [2] requires continuous delay domain, while this work removes this restriction
- We show that the general MVA problem under timing constraints can be solved optimally by our value-oriented branch-and-bound based algorithm in a reasonable amount of time

Q&A

Thanks