ISPD 2009

Prototyping to Design: Early Analysis for Power Distribution Network

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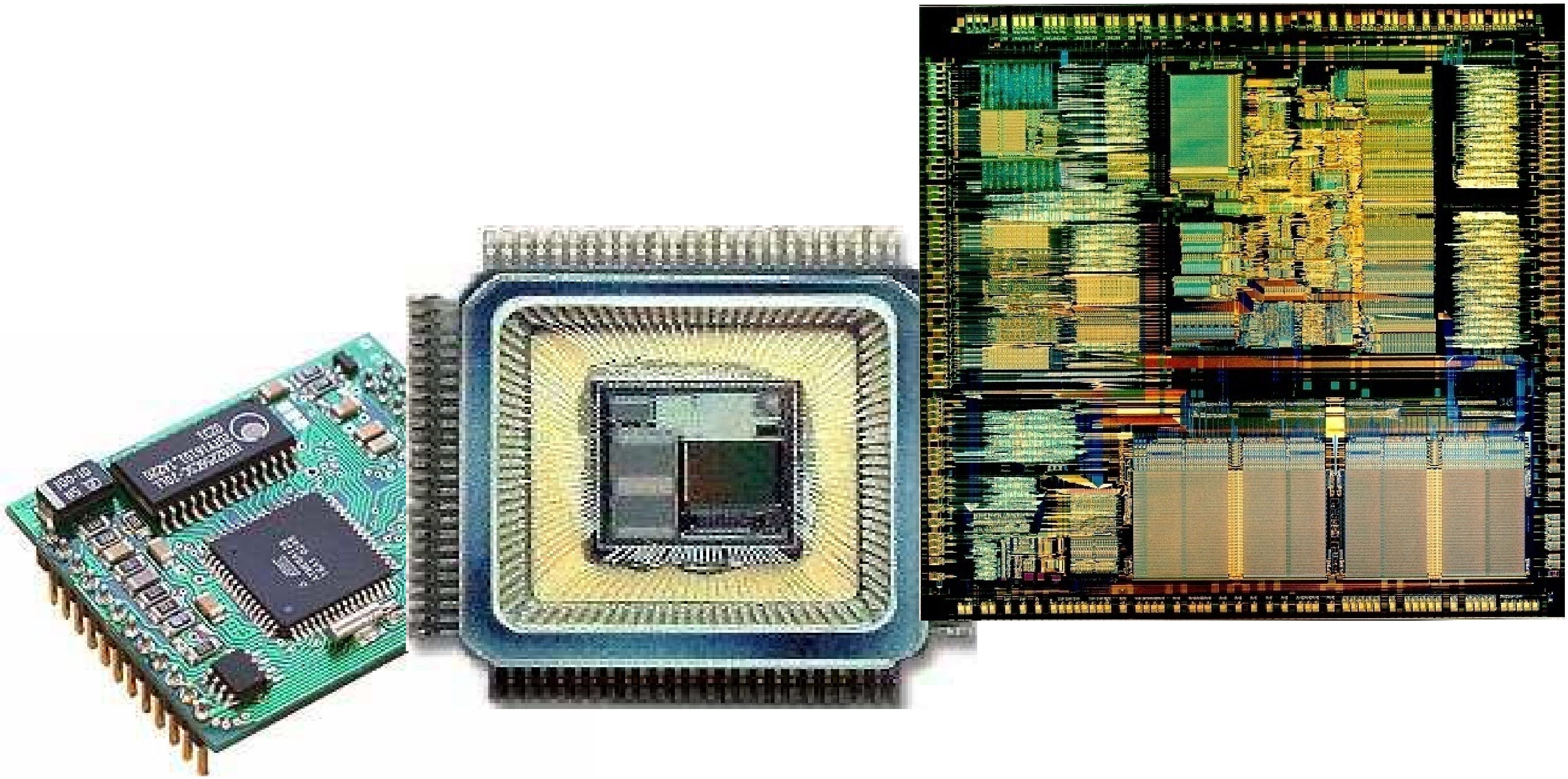
Kai Wang, Aveek Sarkar, Norman Chang, Shen Lin
Apache Design Solutions Inc.

Outline

- Power integrity challenges
- Early analysis overview
- Power distribution
- Power grid planning
- Static analysis
- Dynamic analysis
- Power switch optimization
- Early CPM

Whatever the chip does

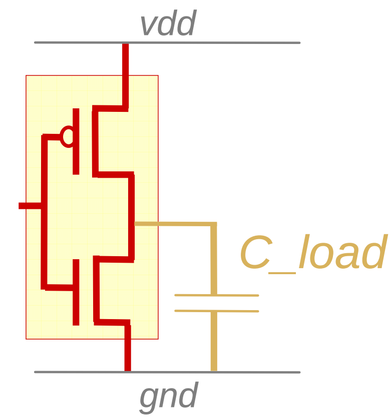


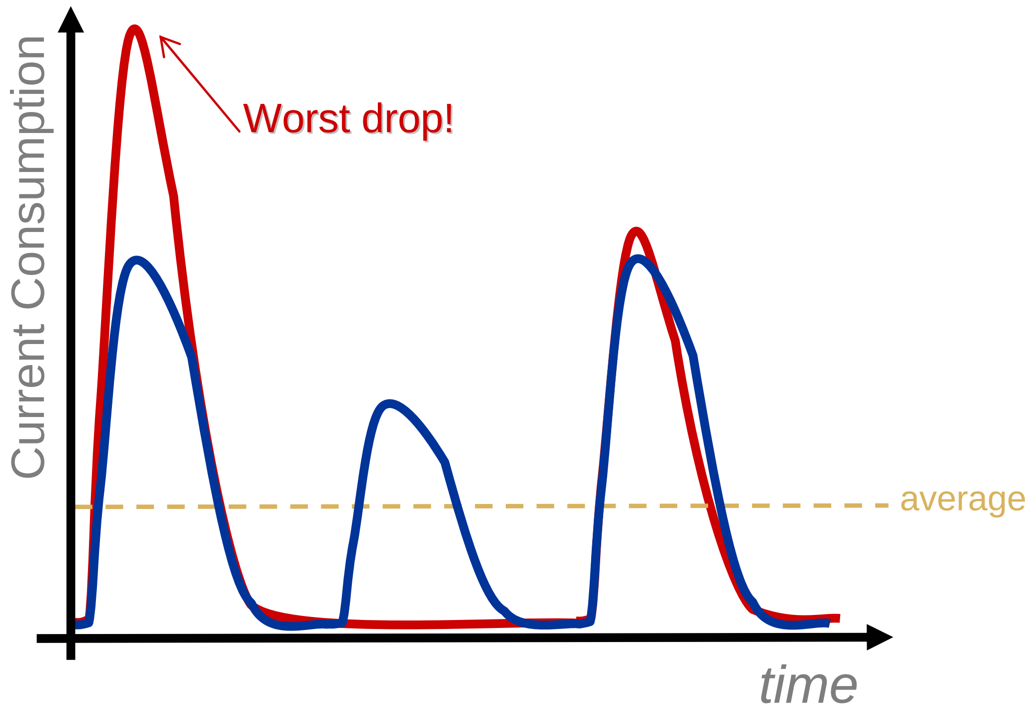
It is all about Switching Current

Switching Power:

Average current = ***f***(freq, charge, V) = ½ **C.V**^{2}**.*freq***

Peak current = ***f***(slew, charge, transition, V)





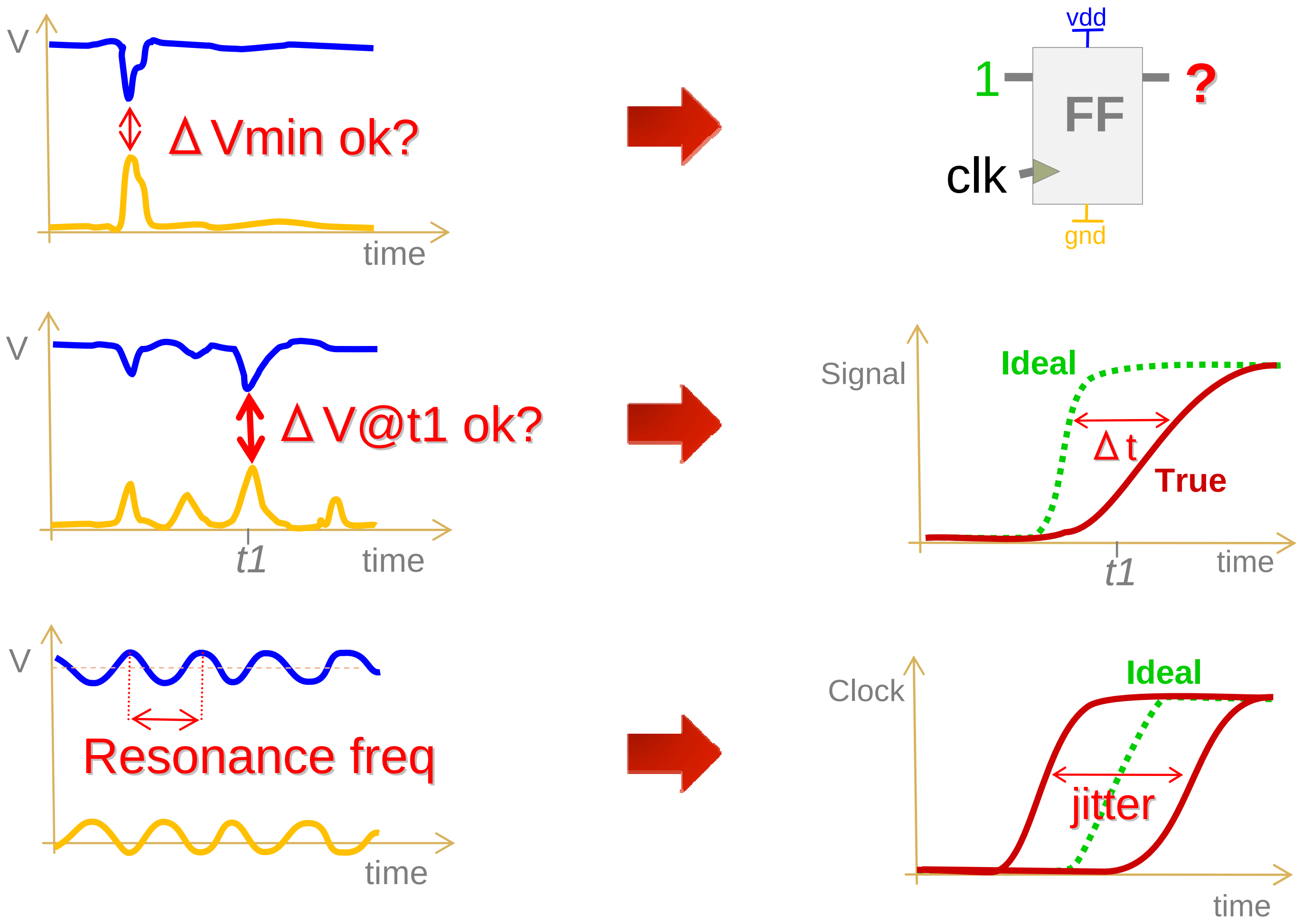
Case A: Load C & Freq f

Case B: Load 2C & Freq ½f

Same Average

but Different Dynamic Drop!

Voltage Drop Impacts



Logic Failure?

Timing Failure?

Clock Failure?

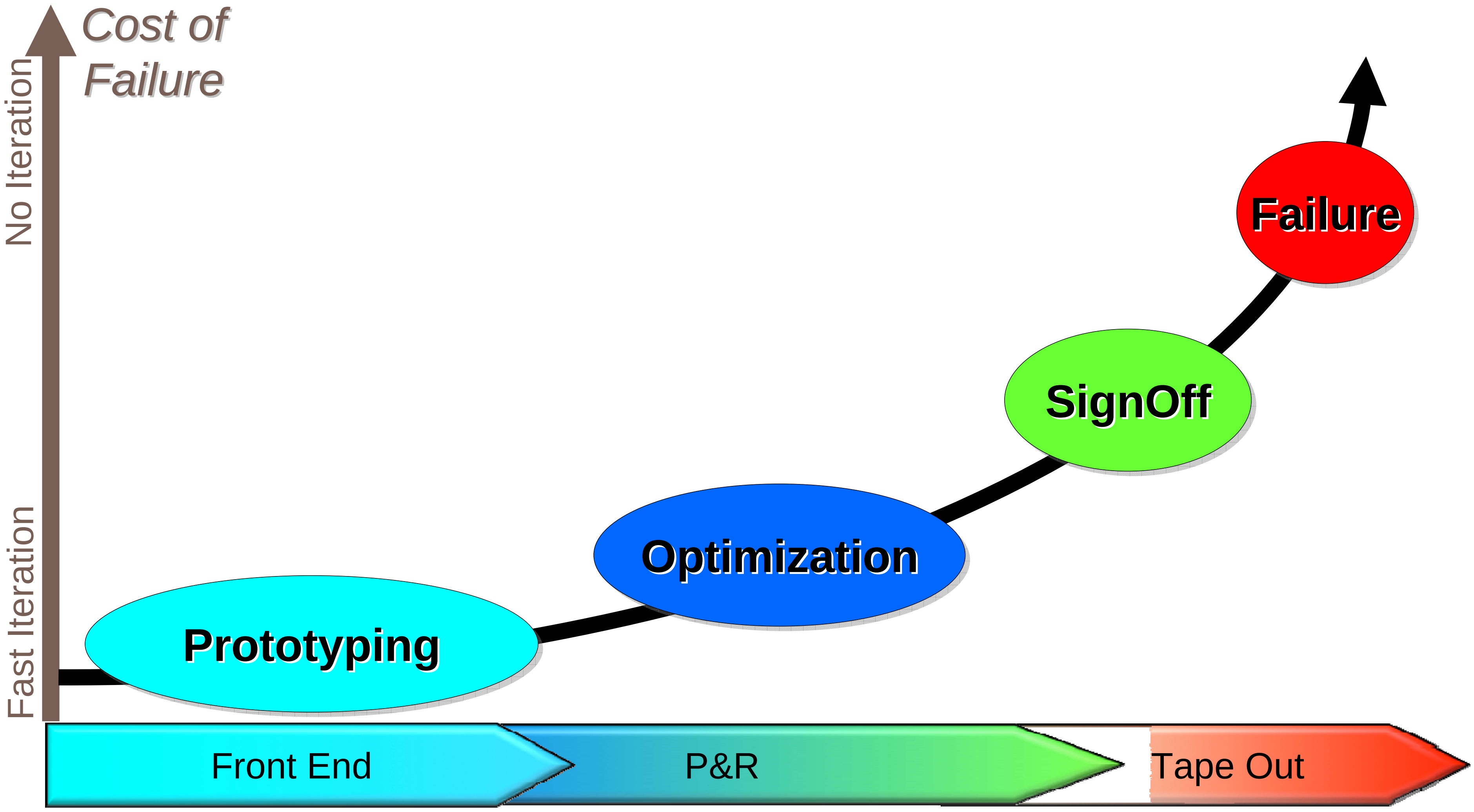
Noise Integrity Challenges

Voltage Drop	Functional and timing malfunction
Timing/Jitter	Package-induced timing uncertainty
ESD	Low yield from electrostatic discharge
Substrate	Analog failure from digital noise injection / coupling
EMI	Excessive chip emission and high electromagnetic interfere
Package	Inadequate package selection for noise and heat toleration

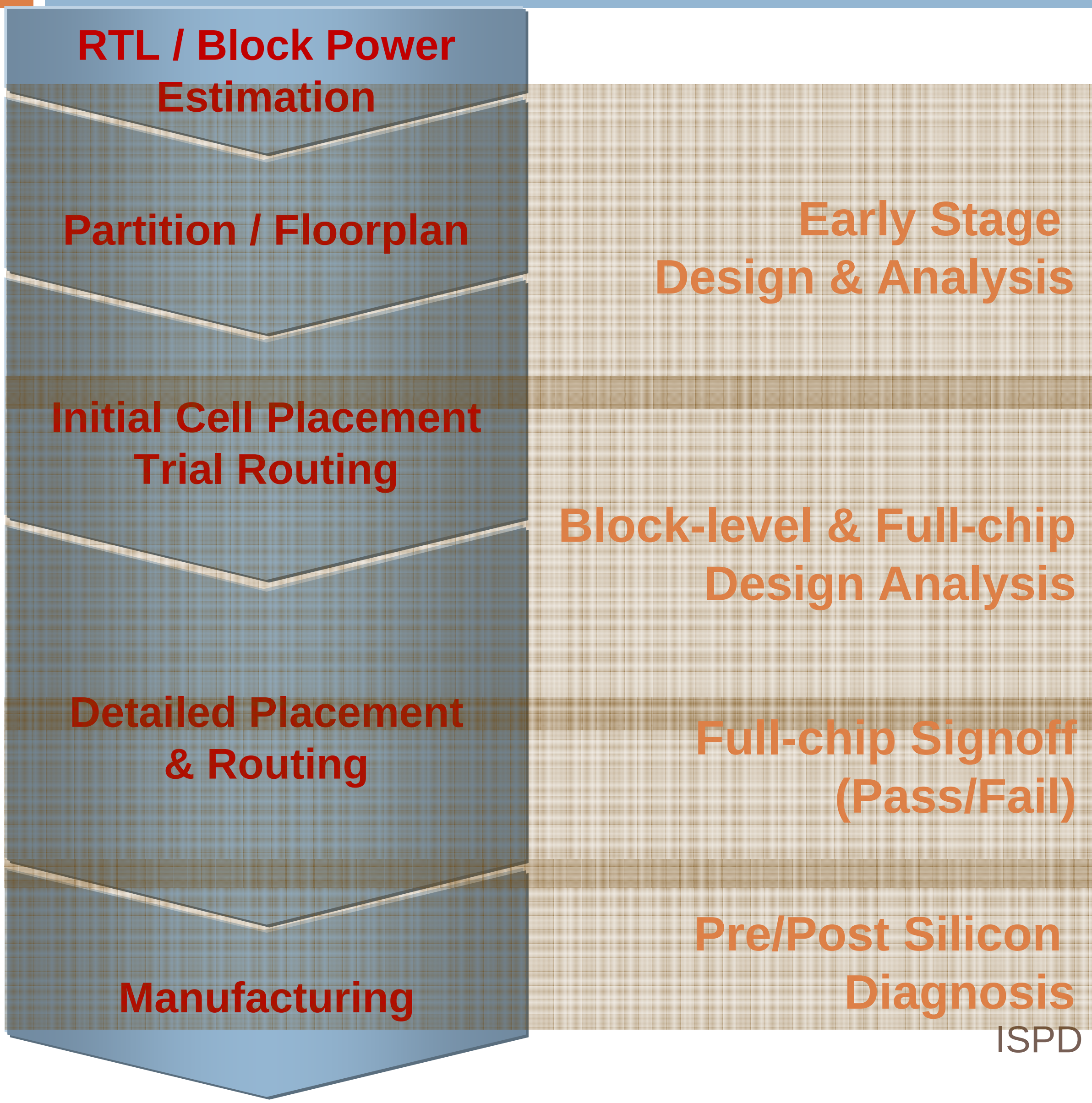
Why Early Analysis?

- Time-to-Result breakdown for power sign-off flow
  - **Time to collect clean data ~40%**
  - Time to setup the flow/tool ~30%
  - Time to run the analysis ~10%
  - Time to interpret results ~20%
- How to improve?
  - Optimize project setup
  - Trained users
  - **Start sooner!**

Why Early Analysis?



SoC Power Flow



- **Grid / pad / switch prototyping**
- **Chip power model**
- **Package selection**
- **Clamp cell placement guidance**

- **Full-chip transient**
- **Vectorless and VCD dynamic**
- **On-chip inductance**

- **IR / DvD**
- **Jitter**
- **Thermal**
- **EM**
- **Timing**

- **Root cause identification**
- **Chip power model**

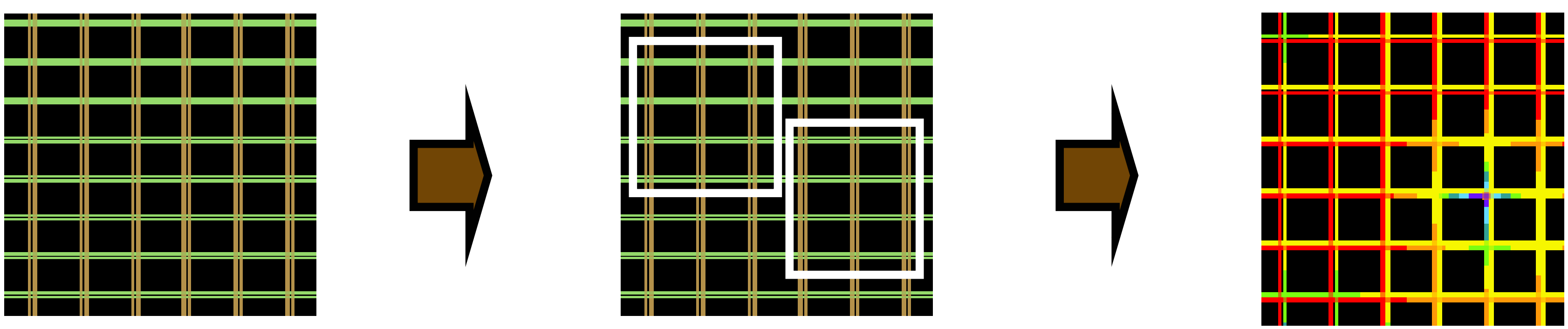
Early Prototyping and Analysis

Prototyping

- **Grid and pad exploration**
- **Package planning**
- **Switch and pad planning**
- **Decap strategy**

Implementation

- **Partial design information**
- **Early dynamic and Chip-Power Model (CPM)**
- **Significantly improve time-to-result**



Generate grid **Define “regions”** **Voltage/current Maps**

Early Analysis Options

Extensive capabilities to design and prototype power grid

Different types of analysis to design and verify system power integrity

Prototyping
Excel2IR, Power-Grid Plan

Early Grid-Check
Power routing, Robustness checks

Switch/Pad planning
Design, placement, count

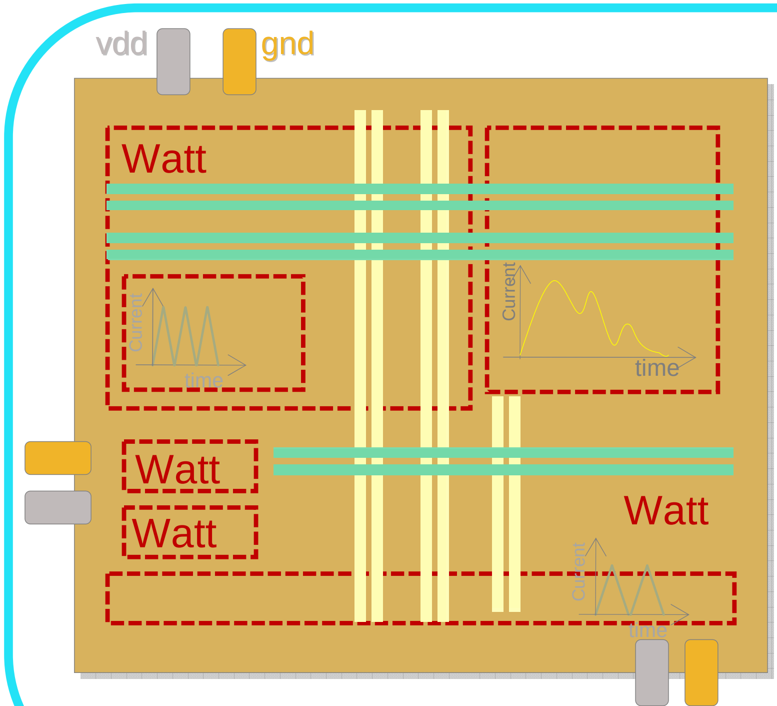
Early Static
EM checks, Pad placement

Early Dynamic
Multi-state multi-cycle analysis

Early Chip Power Model
Early Package Design

How does it work?

Prototyping Flow



1. Define your floorplan (REGIONs)
2. Define associated power
3. Define your PG grid
4. Define the PG Pads

⇒ **Run your Static Analysis**

5. Define Frequencies or Current profile
6. Assign On-Die Decoupling

⇒ **Run your Dynamic Analysis**

FAO What If?

FAO What If?

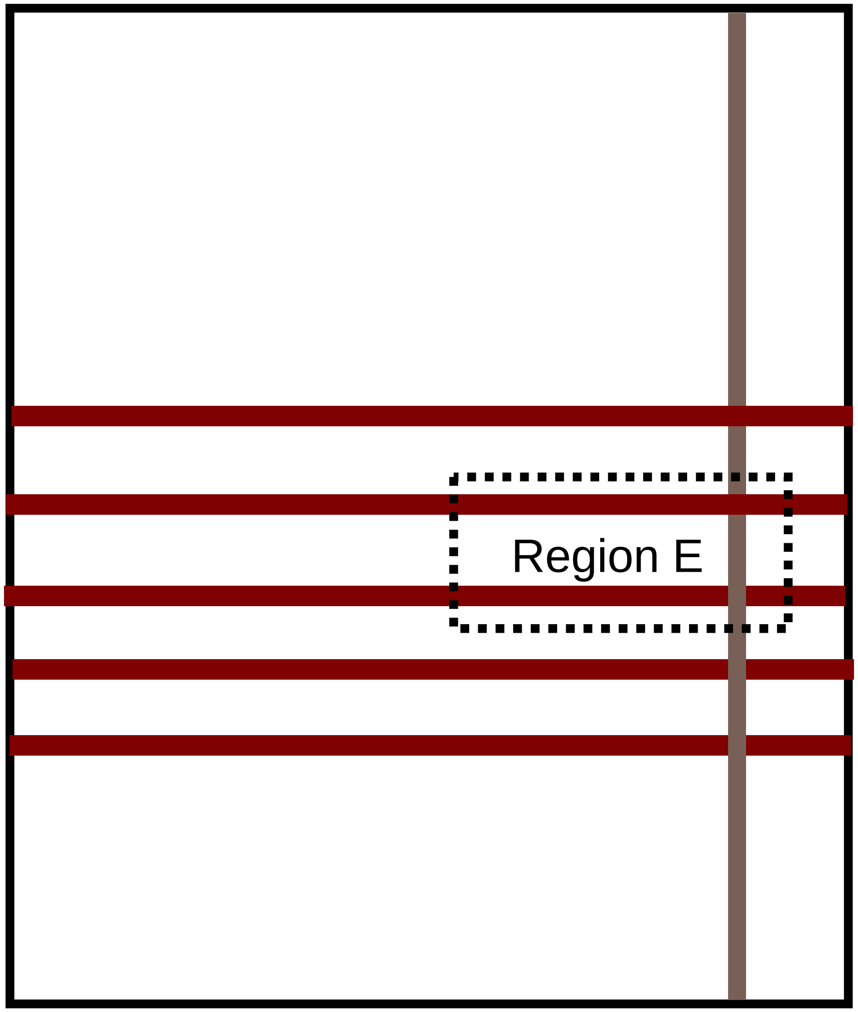
Front End | P&R | Tape Out

Project's Time Line

Power Distribution

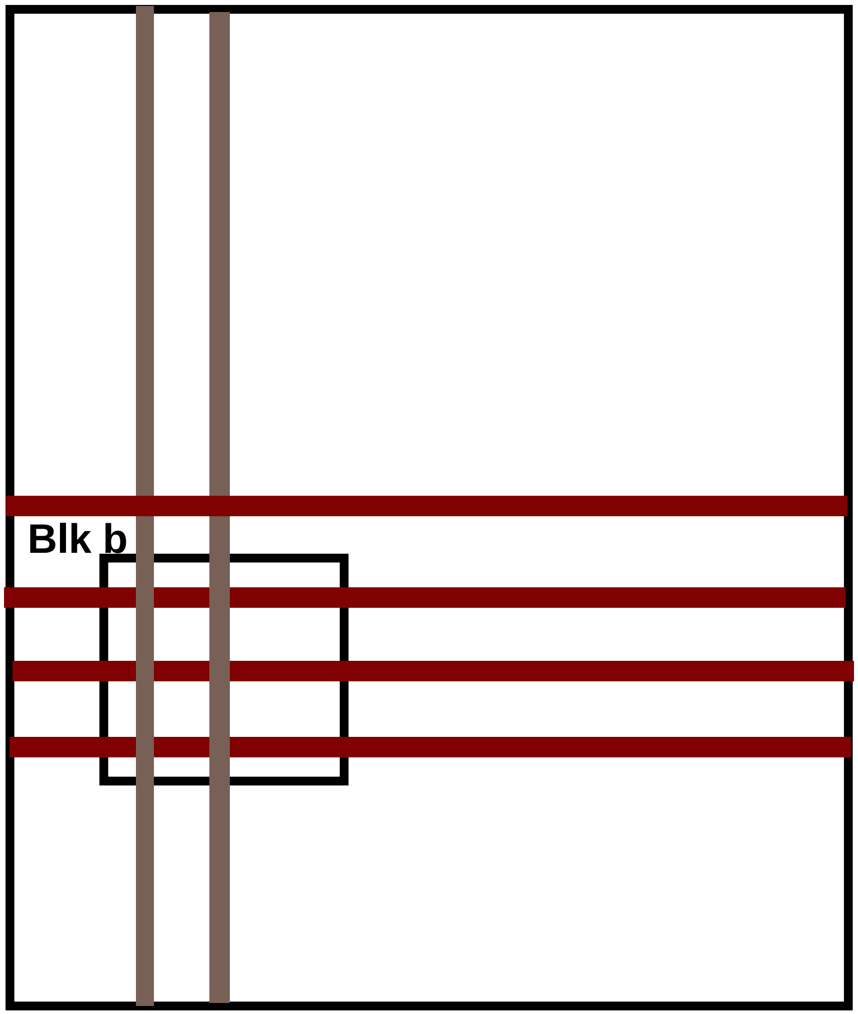
- Distribute user input power uniformly over user specified regions and/or over user specified IP/blocks
- Static: use DC current
- Dynamic:
  - Triangular waveforms
  - User specified PWL waveforms
  - Transistor-level simulation waveforms

Option 1



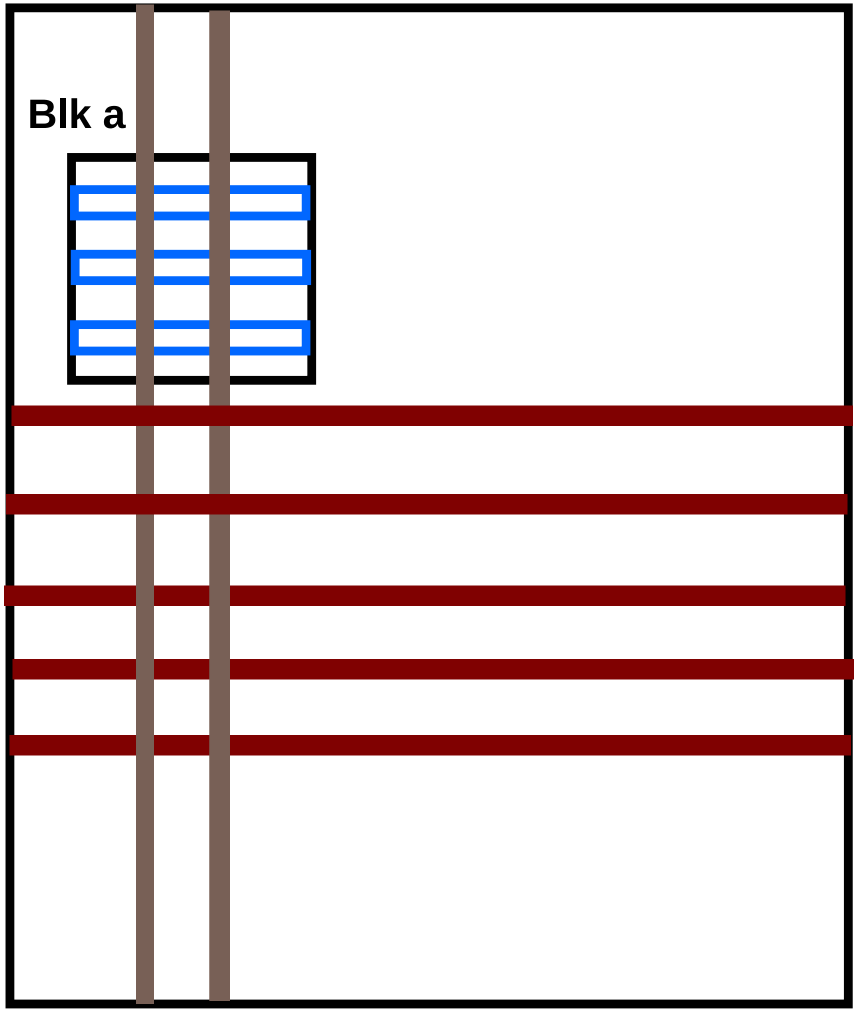
- Region E – User specified region. User specified power for this region to be distributed uniformly over power routes in the area

Option 2



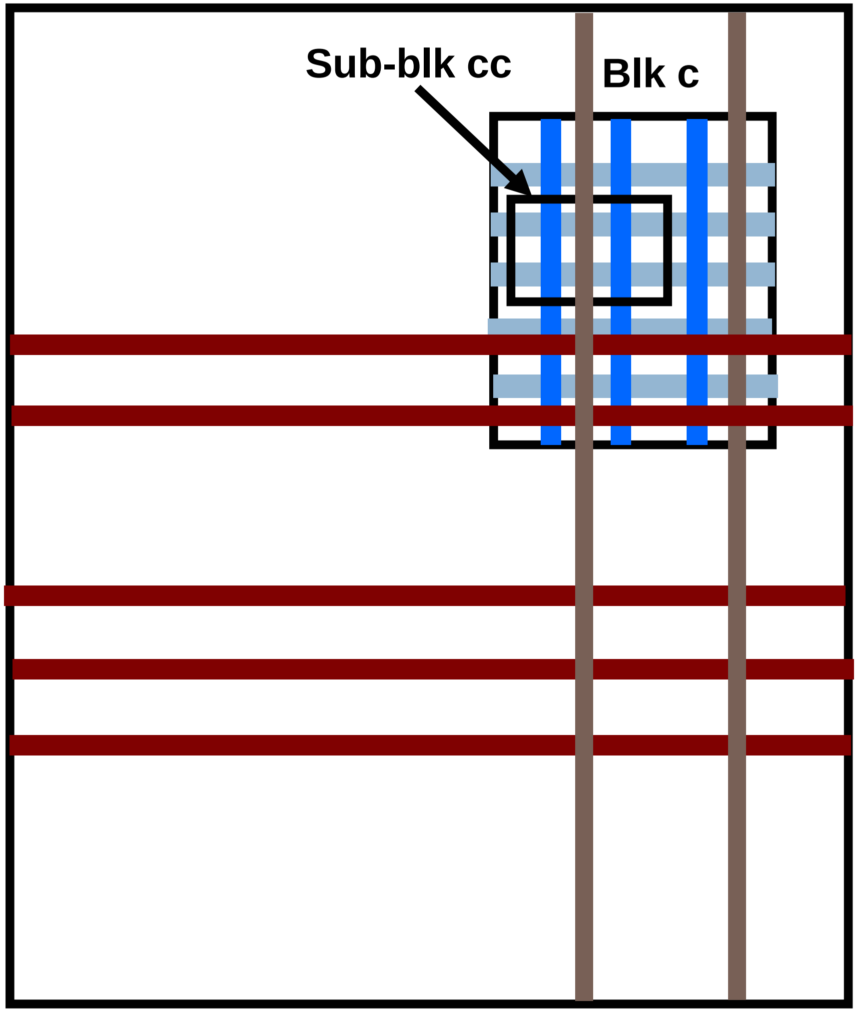
- When pin view (LEF) or detailed view (routing) is not available.
- Distribute power over top level routes over a block.

Option 3



- When LEF pin view available but detailed view (routing) not available.
- Distribute power uniformly over pins based on their connectivity to the top routing.

Option 4



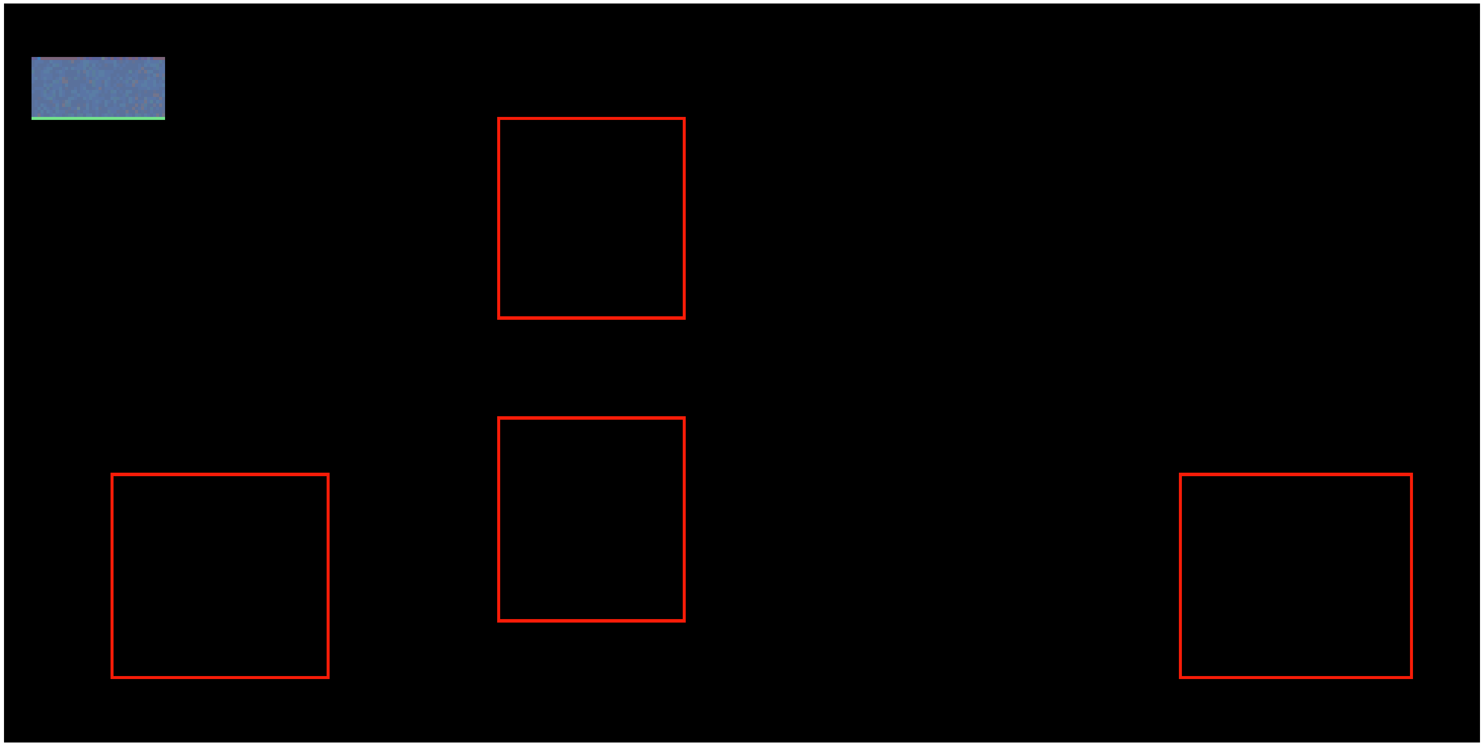
- Blk c: hierarchical block with routing
- Sub blk cc: sub-block with routing
- Assign power to routing inside block or sub-block based on layer specification.

Power Grid Prototyping

- A simple & quick method for analyzing voltage drop impact.
  - Grid creation
  - Via dropping
  - Pad placement
  - Switch insertion

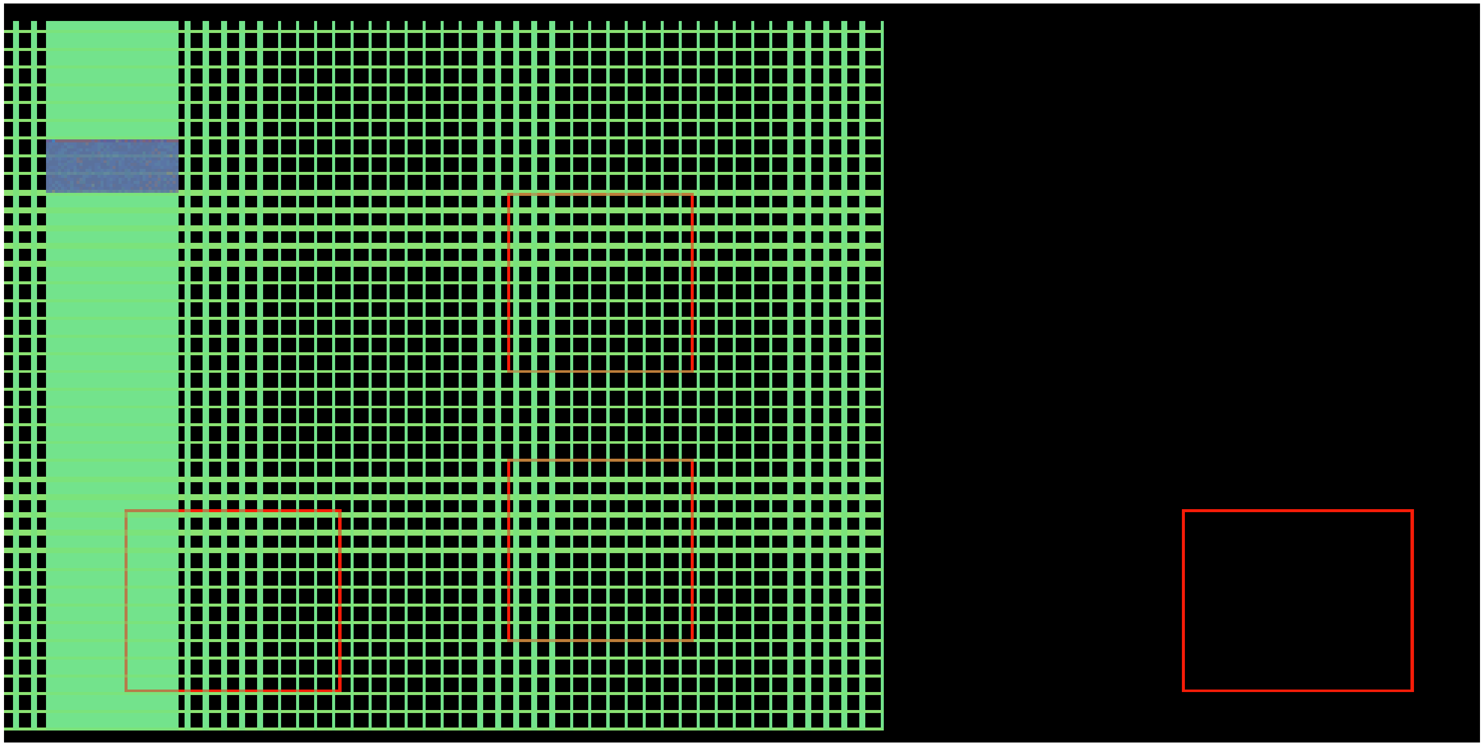
Prototyping Example

- Define regions and distribute power



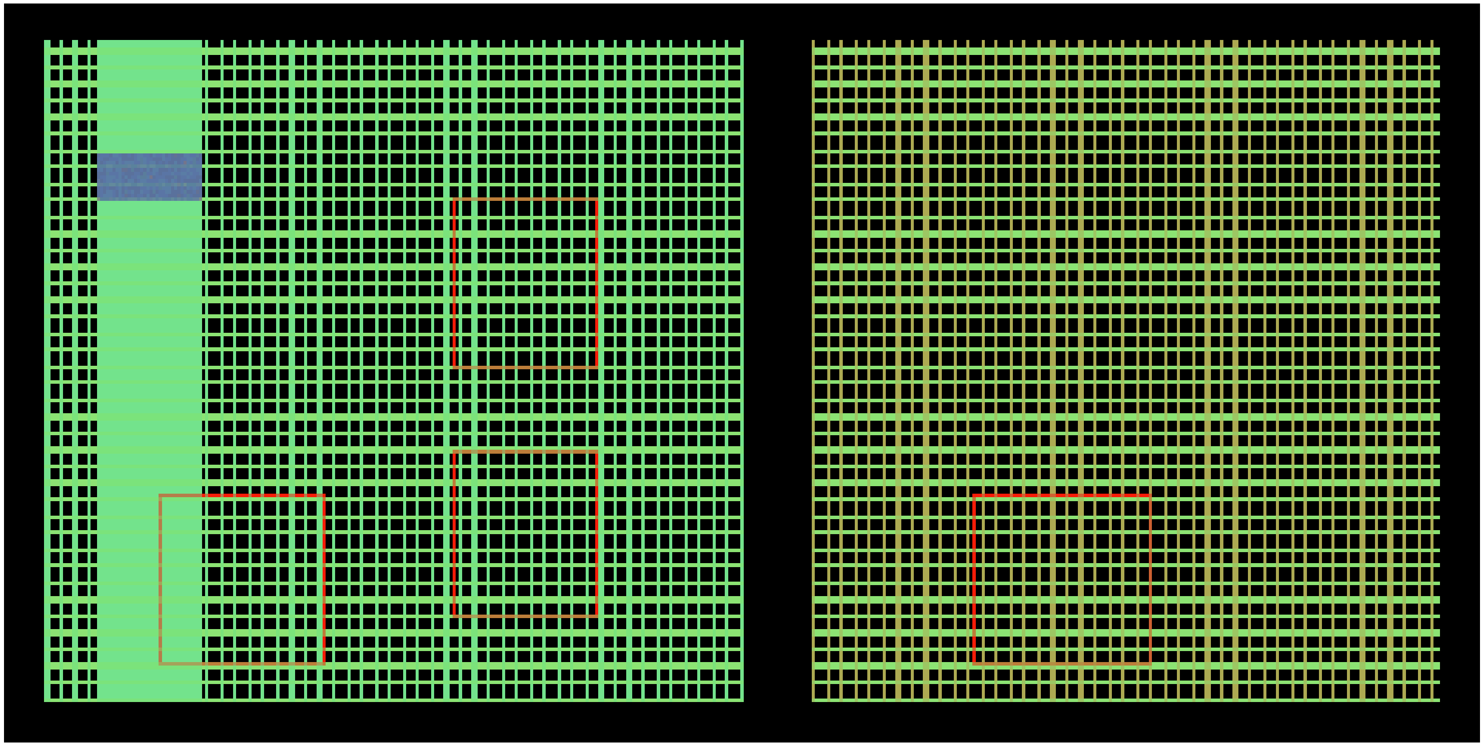
Prototyping Example (Cont'd)

- Create mesh for internal power domain



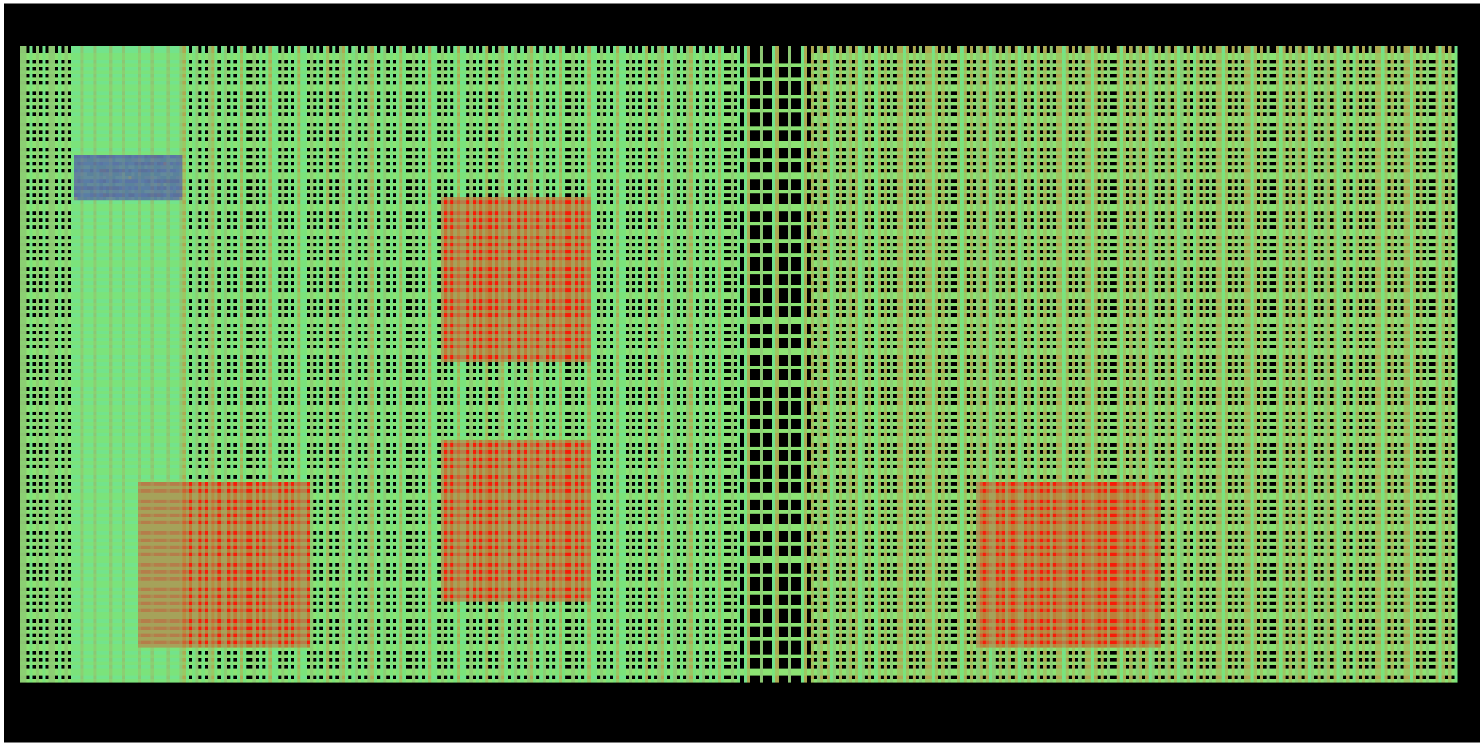
Prototyping Example (Cont'd)

- Create mesh for external power domain



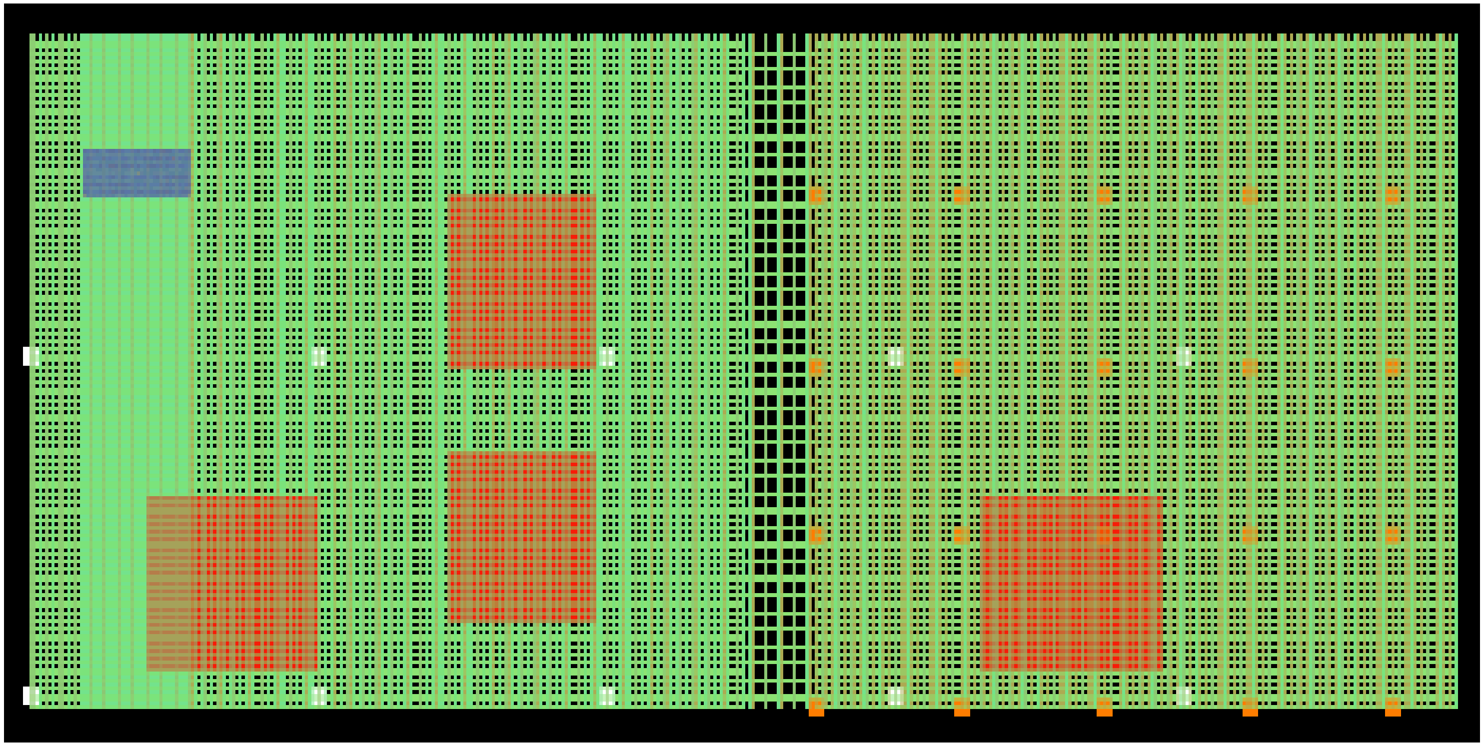
Prototyping Example (Cont'd)

- Create mesh for ground domain



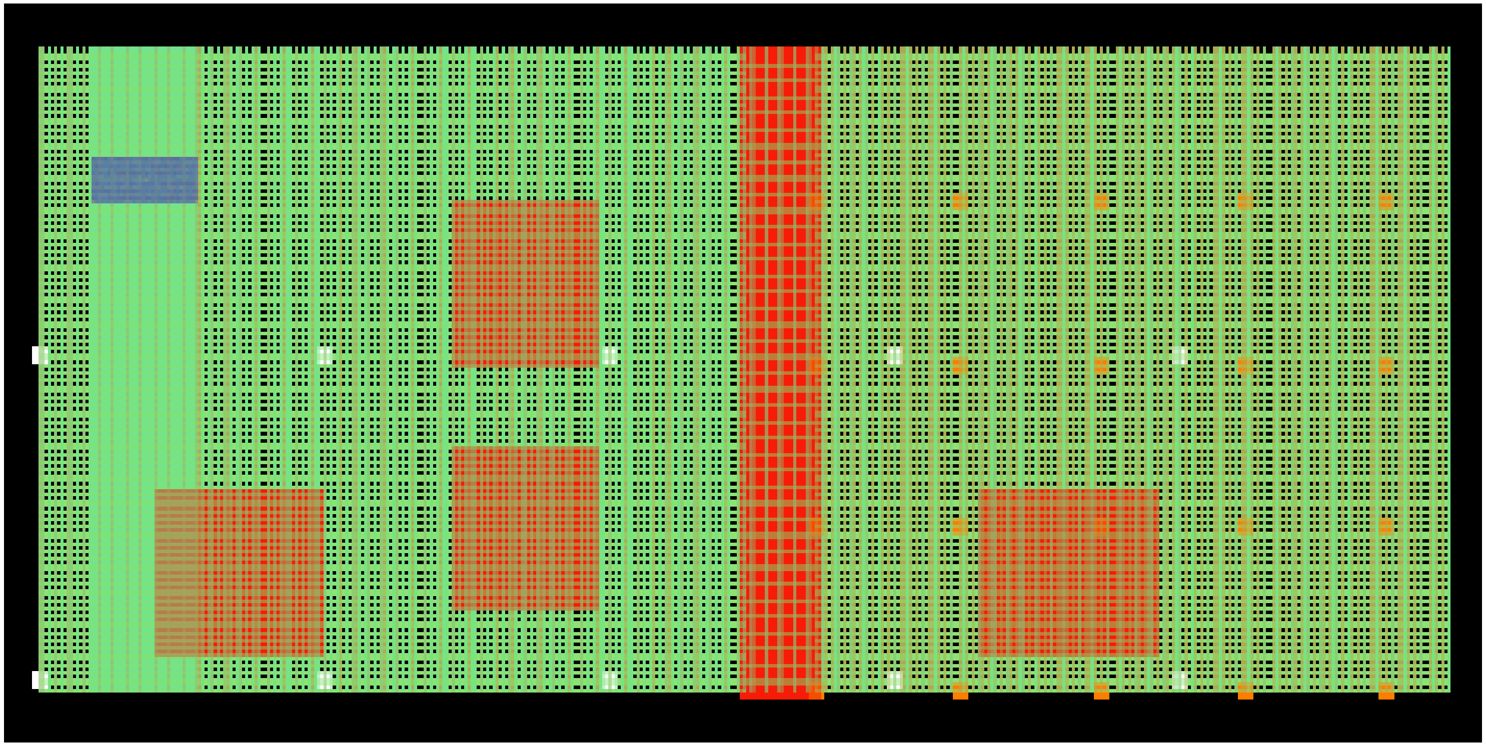
Prototyping Example (Cont'd)

- Add pads



Prototyping Example (Cont’d)

- Insert switches



Grid Connectivity Checks

GridCheck

Connectivity checks

Normalized or effective

Missing Vias

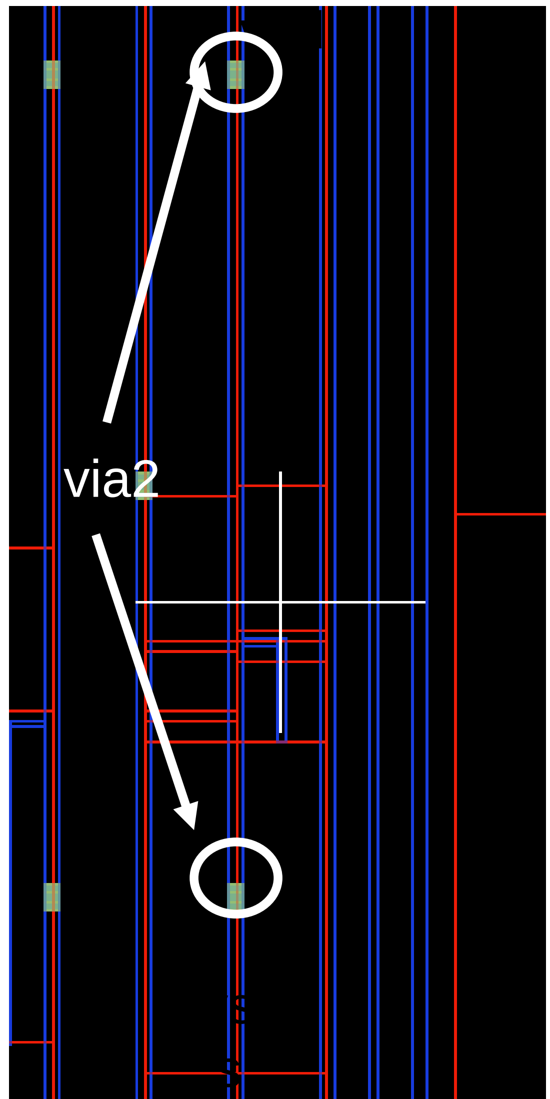
Stacked or layer by layer

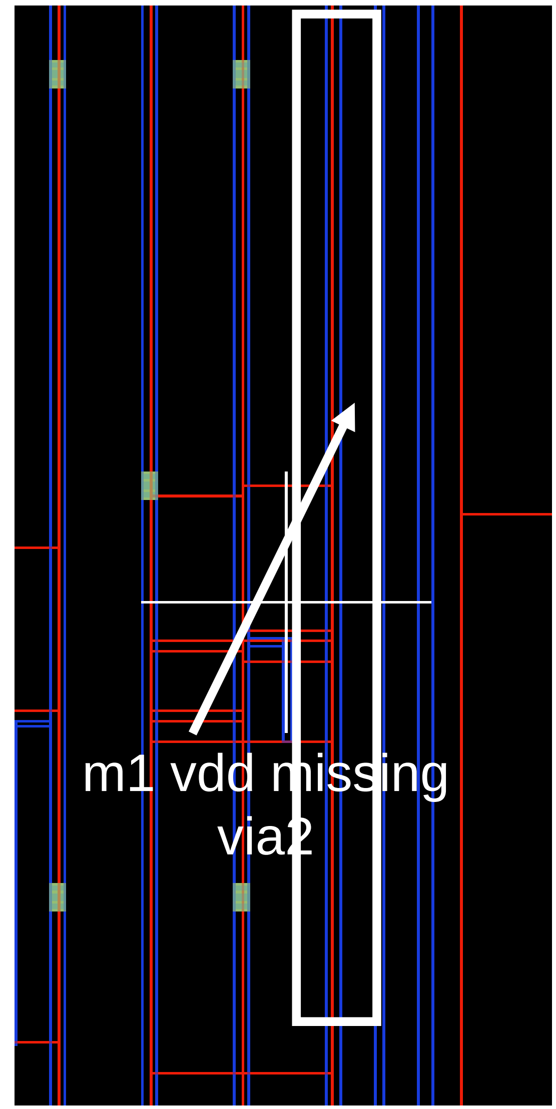
Filtered by user constraints

Shorts / Unconnects

Analysis w/ unclean layout

List of shorts / opens





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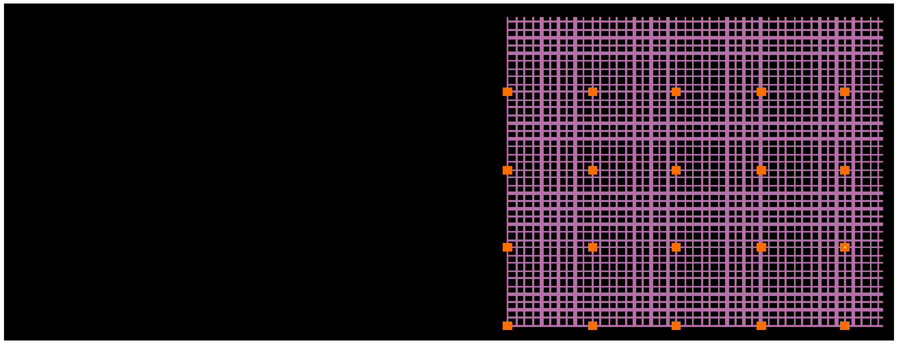
Static Analysis

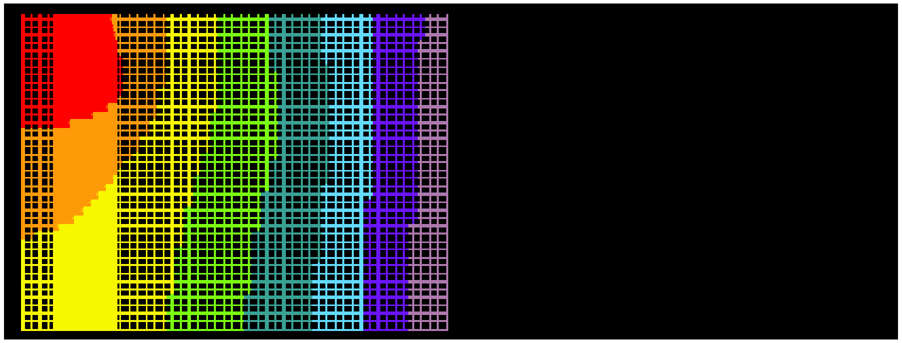
- R network extraction
- DC simulation

Static Analysis Results: IR Map

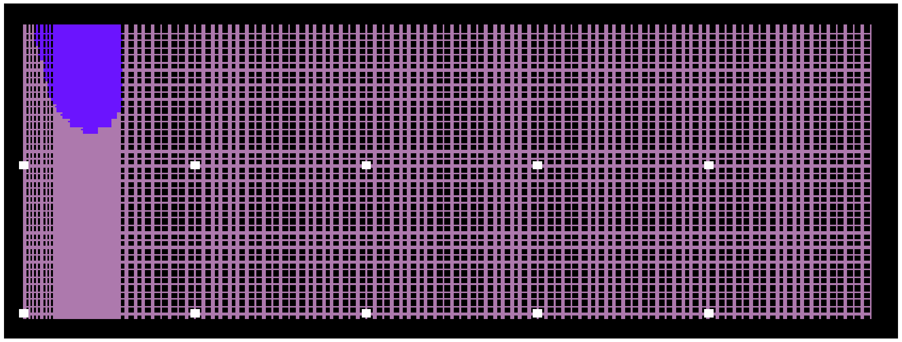
- External Power Domain



- Internal Power Domain



- Ground Domain

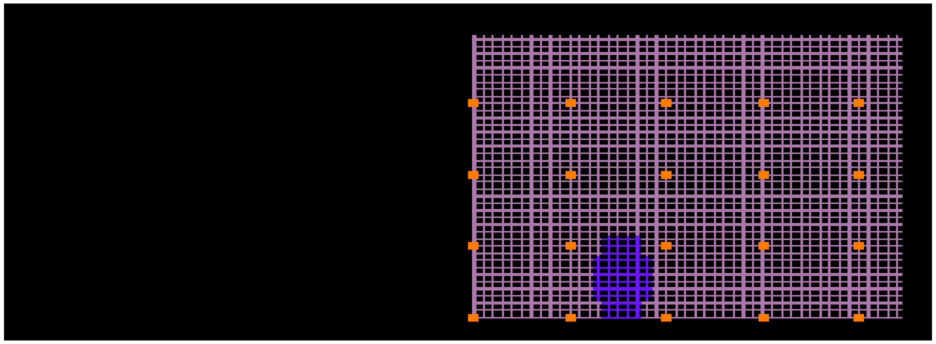


Dynamic Analysis

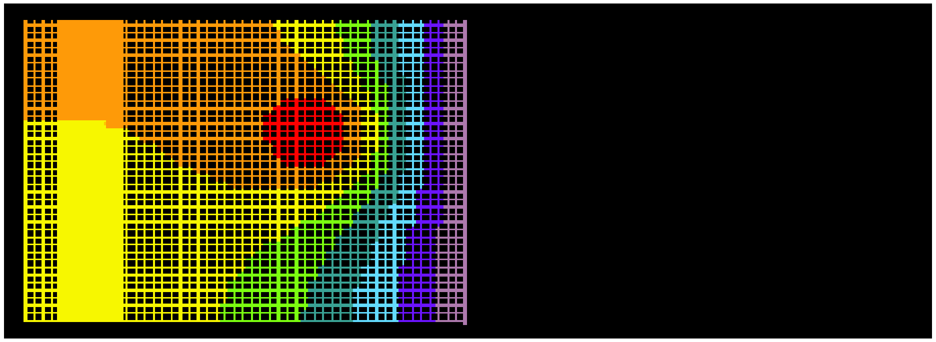
- RC/RLC network extraction
- User provides current profiles (optional)
- User provides timing windows for switches (low-power design)
- Transient simulation

Dynamic Results: IR Map

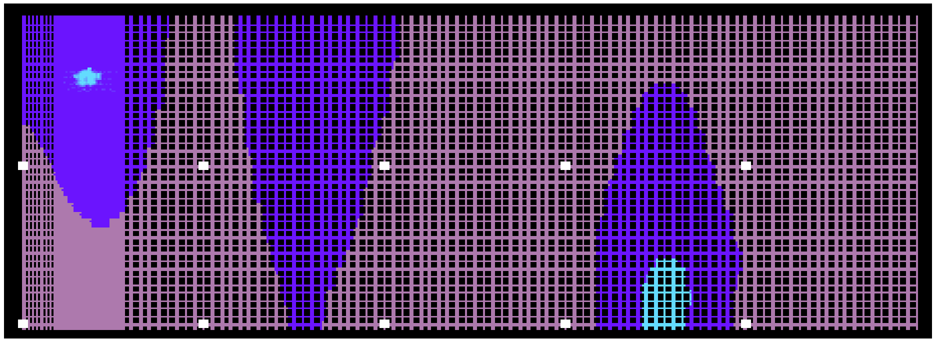
- External Power Domain



- Internal Power Domain



- Ground Domain



Switch Optimization Problems

- Power switch placement
- Power switch sizing
- Power switch removal
  - Specify constraint as voltage drop on switch
  - Based on static analysis result
  - Remove redundant switches as many as possible
- Power switch ramp-up scheduling

Switch Removal Example

- Nominal voltage: 1.08V
- Before removal
  - Switch number: 312
  - Maximal voltage drop across switch: 3.512mV
  - Minimal voltage drop across switch: 0.234mV
  - Average voltage drop across switch: 1.393mV
  - Worst voltage drop in internal net: 4.405mV(0.407%)

Switch Removal Result

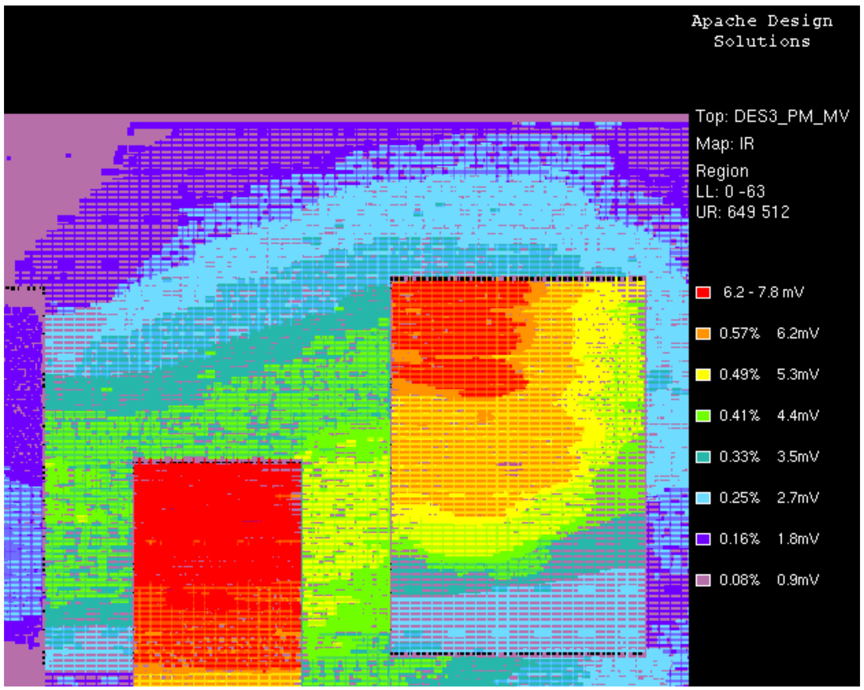
After Removal

IR-drop Constraint On switch	Removed Switches Number	Area/ Leakage Reduction	Max. IR Switch (mV)	Min. IR Switch (mV)	Avg. IR Switch (mV)	Wst. IR Internal Net (mV)
3.52mV	11	3.52%	3.512	0.354	1.443	4.405
4mV	173	55.4%	3.799	2.596	3.103	5.315
5mV	203	65.1%	4.902	3.153	3.953	7.941
6mV	212	67.9%	5.727	3.425	4.307	22.51
N/A	N/A	N/A	3.512	0.234	1.393	4.405

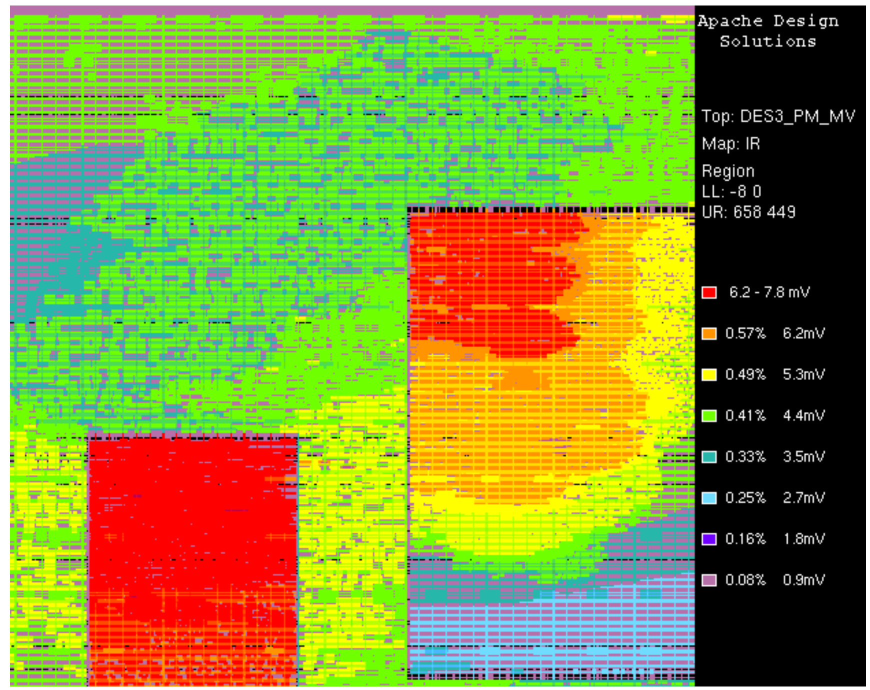
Before Removal

Switch Removal Result

Initial IR Map



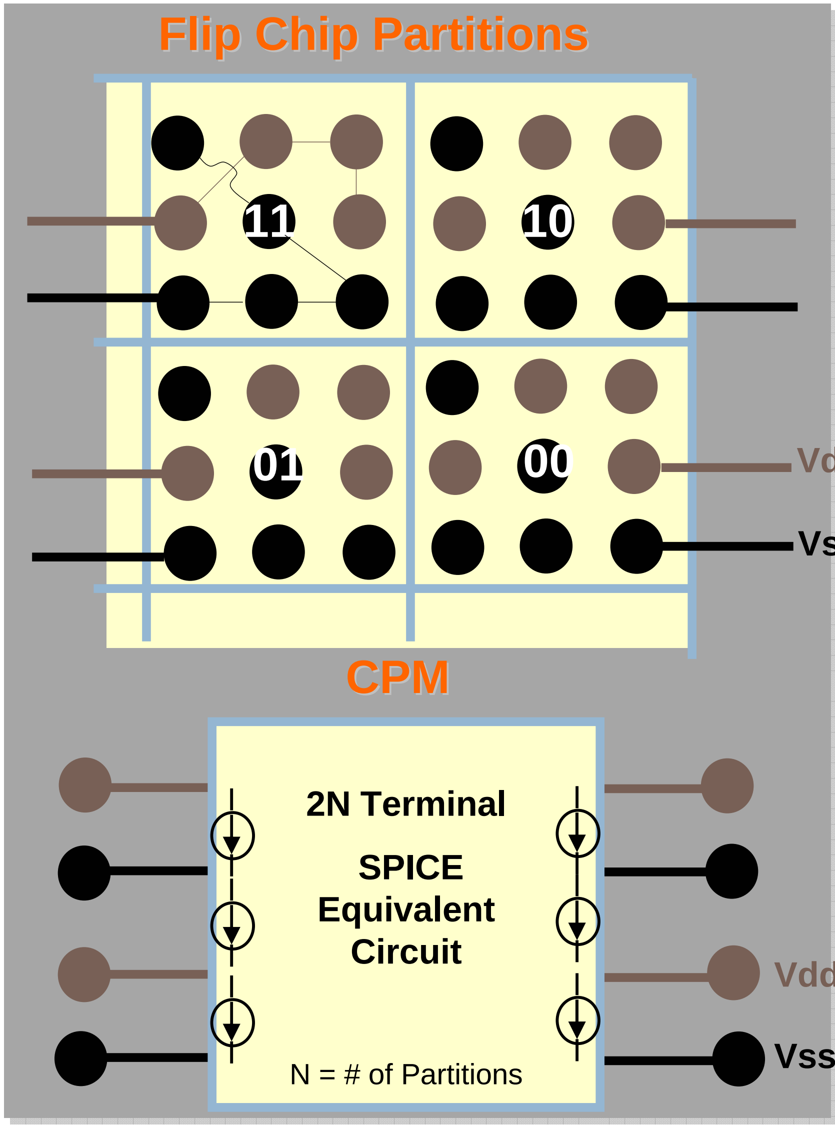
IR Map with constraint = 4mV

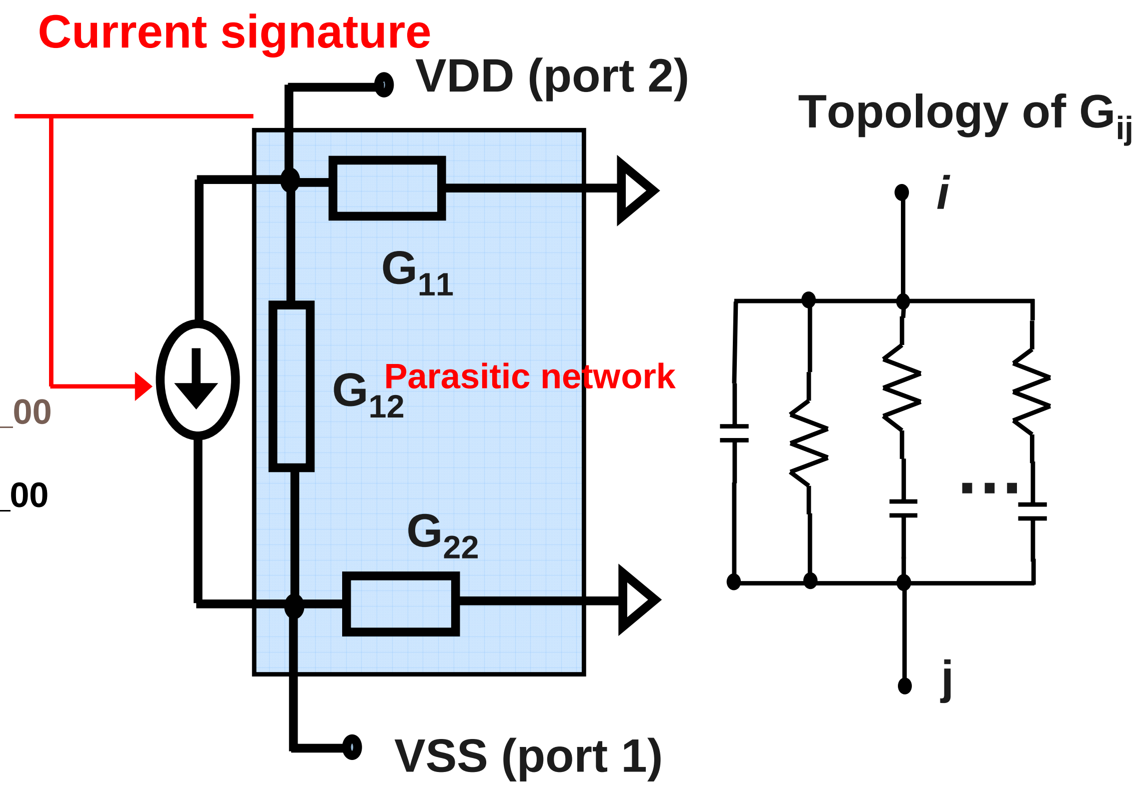


Why Early CPM?

- CPM is a compact and accurate SPICE model for the full-chip power distribution network
- CPM can be seamlessly integrated for package/board co-design
- Early CPM helps in pad placement planning and early package selection
- Different types of CPM can be generated
  - DC current model (static analysis)
  - Spatial and temporal current model (dynamic analysis)

CPM Equivalent Circuit for Flip Chip

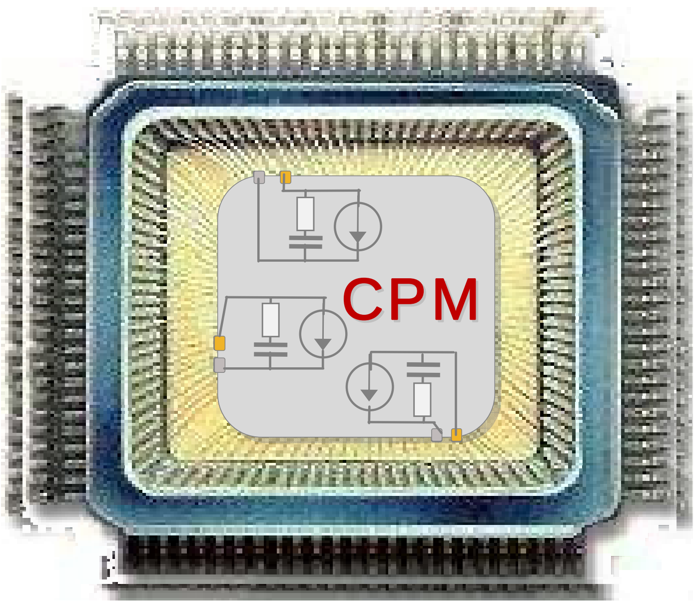




Two-port example shown for simplicity

How does it work?

Prototyping Flow



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2. Define associated power
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4. Define the PG Pads

⇒ **Run your Static Analysis**

FAO
What If?

5. Define Frequencies or Current profile
6. Assign On-Die Decoupling

⇒ **Run your Dynamic Analysis**

⇒ **Create your 1st Chip Power Model**

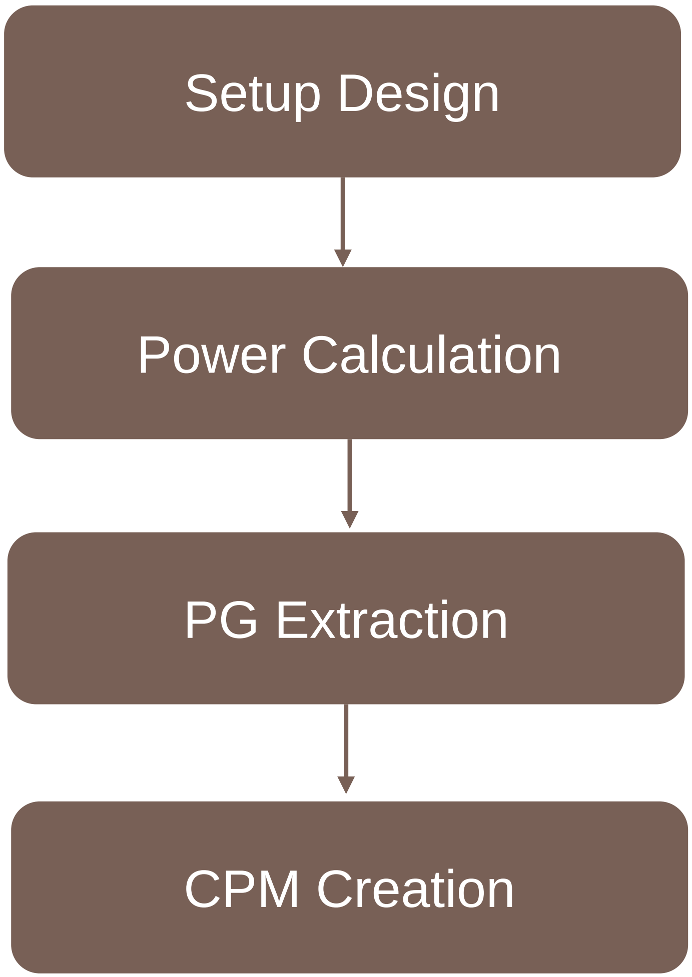
⇒ **Time & Freq Domain Analysis**

FAO
What If?

Front End
P&R
Tape Out

Project's Time Line

Early Analysis and CPM Flow



- No package parasitic are used in the simulation (Chip power model is package independent)
- No separate dynamic simulation required
- CPM internally performs dynamic simulation for capturing the current signature
- CPM dynamic simulation run time might be higher than regular dynamic simulation time

Application of CPM in Global Power Integrity

- Global PDN target impedance
- IC-Package resonance analysis
- Dynamic voltage noise budgeting at board and package level
- Package and board optimization
- System in package (SiP)
- EMI analysis

Summary

- Early Static Analysis
  - Plan and verify power distribution network
- Early Dynamic Analysis
  - Explore different scenarios
    - Transitions from one state to another
    - Multi-cycle analysis
  - Early package design
    - Chip power model creation
    - Package response for on-die current transition

Thank You!