Welcome to ISPD 2009

ACM International Symposium on Physical Design March 29 – April 1 2009, San Diego CA

















Conference Chair: Gi-Joon Nam

Technical Program Chair: Prashant Saxena

ISPD 2009 Technical Program

- Strong technical program
 - Over 60 submissions
 - 21 accepted papers
 - 11 invited talks
- Major topics include layout planning, nanotechnology, analog design, regular fabrics, manufacturability, clock network synthesis, routing and post-si prediction and debugging
- ISPD is a workshop in spirit
 - Questions are encouraged
 - Interruptions are OK, but speaker can defer until later
 - Please give your name and affiliation when asking questions

ISPD 2009 Housekeeping

Presenters:

- Please sign-in on the sheet near the exit
- Check-in with your session chair 15 minutes before your slot
- Keep on time
- Default is that we post pdfs of slides after the conference on the website; if this is not OK with you please let your session know

Session Chiars:

- Keep your session on time
- Know your presenters

ISPD 2009 Housekeeping

- Please turn your cell phones to silent mode
- □ Wear your badge to meals it's your ticket
- All meals will be served during the conference
 - Room Rio Vista Salon E
- Internet access
 - Wireless network is *NOT* available in the conference room
 - It should be available in lobby area and in your room

ISPD 2009 Acknowledgements

- □ IEEE and ACM
 - IEEE/CEDA for sponsoring the contest
- ☐ Corporate sponsors
 - Cadence Design Systems
 - IBM Research
 - IEEE/CEDA
 - Sun Microsystems
 - Synopsys
 - SpringSoft
 - Tela Innovations

ISPD 2009 Acknowledgements





































InTime Software





More thanks

- The volunteers who make this conference possible
 - Prashant Saxena, technical chair
 - Yao-Wen Chang, publication chair
 - Jiang Hu, publicity chair
 - Steering Committee
 - □ David Z. Pan (Chair), Patrick Groeneveld, Malgorzata Marek-Sadowska, Patrick Madden and Ruchir Puri
- A special thanks to Cliff Sze, for organizing the clock network synthesis contest
- And the technical program committee

The Technical Program Committee

Ameya Agnihotri (Magma)

Yao-Wen Chang (NTU)

Chris Chu (Iowa State U)

Yegna Parasuram (Mentor)

Lars Hagen (Cadence)

Jiang Hu (Texas A&M)

Andrew Kennings (U of Waterloo)

Cheng-Kok Koh (Purdue U)

Jens Lienig (Dresden U)

Rob Mains (SUN)

Igor Markov (U of Michigan)

David Newmark (AMD)

Hidetoshi Onodera (Kyoto U)

Rajendran Panda (Freescale)

Prashant Saxena (Synopsys)

Ankur Srivastava (U of Maryland)

Cliff Sze (IBM Research)

Martin Wong (UIUC)

Linda Wu (AtopTech)

Hannah Yang (Intel)

Evangenline Young (Chines U of HK)

Clock Network Synthesis Contest

- □ Dr. Cliff Sze from IBM Research in Charge
- □ 27 teams signed up; 12 survived
- □ 5th ISPD contest; inaugural clock network synthesis contest
- Session 7: Clocking and the ISPD'09 Clock Synthesis Contest
 - Tues: 3:40 5:05 pm
- http://www.ispd.cc/contests/

Best Paper Award — Previous ISPDs

- **2004**
 - FastPlace: Efficient Analytical Placement using Cell Shifting, Iterative Local Refinement and a Hybrid Net Model, by Natarajan Viswanathan and Chris Chu
- 2005
 - Multilevel Generalized Force-Directed Method for Circuit Placement, by Tony Chan, Jason Cong and Kenton Sze
- **2006**
 - Robust Extraction of Spatial Correlation, by Jinjun Xiong, Vladimir Zolotove and Lei He
- □ 2007
 - Variability-Driven Formulation for Simultaneous Gate Sizing and Post-Silicon Tunability Allocation, by Vishal Khandelwal and Ankur Srivastava
- **2008**
 - Optimizing Non-Monotonic Interconnect Using Functional Simulation and Logic Restructuring, by Stephen M. Plaza, Igor L. Markov and Valeria Bertacco

Best Paper Award – ISPD 2009

- □ 3 candidates
 - A New Algorithm for Simultaneous Gate Sizing and Threhosld Voltage Assignment, by Yifang Liu and Jiang Hu
 Session 2
 - Transistor-Level Layout of High-Density Regular Circuits, by Yi-Wei Lin, Malgorzata Marek-Sadowska and Wojciech Maly
 - ☐ Session 5
 - Synthesizing a Representative Critical Path for Post-Silicon Delay Prediction, by Qunzeng Liu and Sachin Sapatnekar
 - ☐ Session 9

Best Paper Award – ISPD 2009

- Synthesizing a Representative Critical Path for Post-Silicon Delay Prediction
- Qunzeng Liu and Sachin Sapatnekar from University of Minnesota
- Session 9, Paper 1

IEEE/CEDA Announcements

- Early Career Award
 - To recognize an individual who has made substantial contributions to the area of EDA in the early stages of his/her career
 - Eligibility: members of the IEEE whose highest educational degree was awarded within 8 years of the nomination
- A. Richard Newton Award
 - To recognize a person or persons for an outstanding technical contribution via a paper
 - Eligibility: journal or conference refereed papers in the EDA field and in print for 10+ years
- ☐ Deadline: May 15. Award presented at ICCAD
- For more info: www.c-eda.org

Keynote Talk

Dr. Carl J. Anderson (IBM): One Look into the Future of CMOS Chip Design