Physical Design Issues in Biofluidic Microchips

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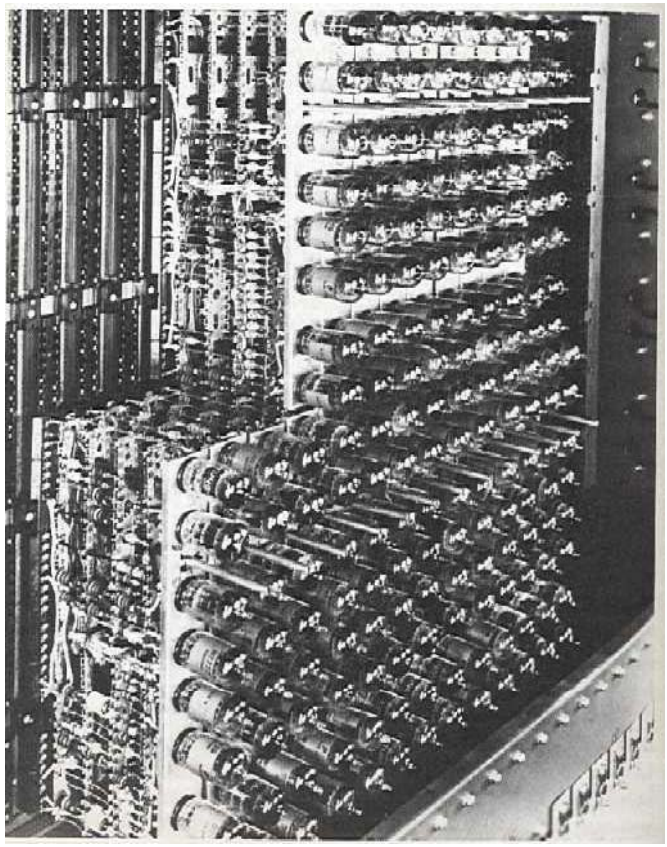
M E M S

Carnegie Mellon

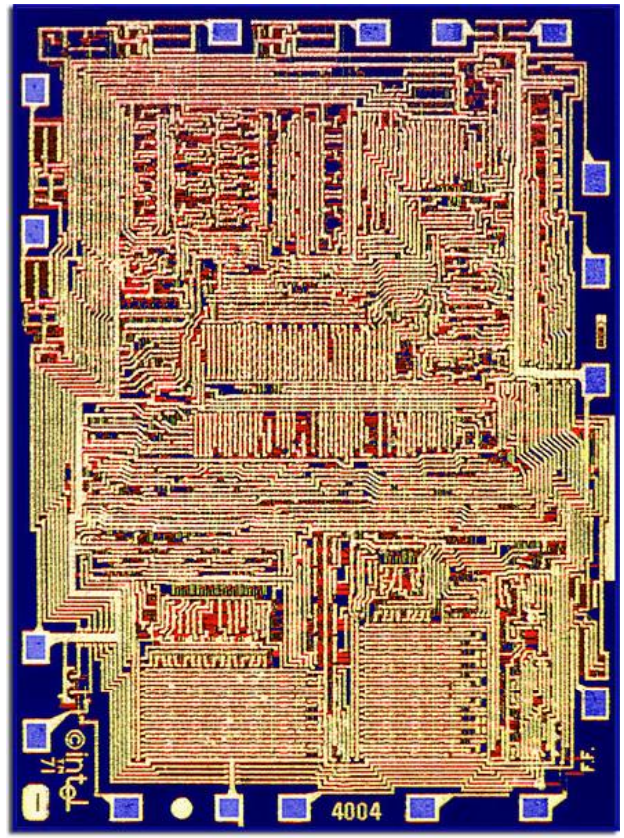
ISPD, April 16, 2008

Tubes to Chips: ICs

- Driven by Information Processing needs



IBM 701 calculator
(1952)



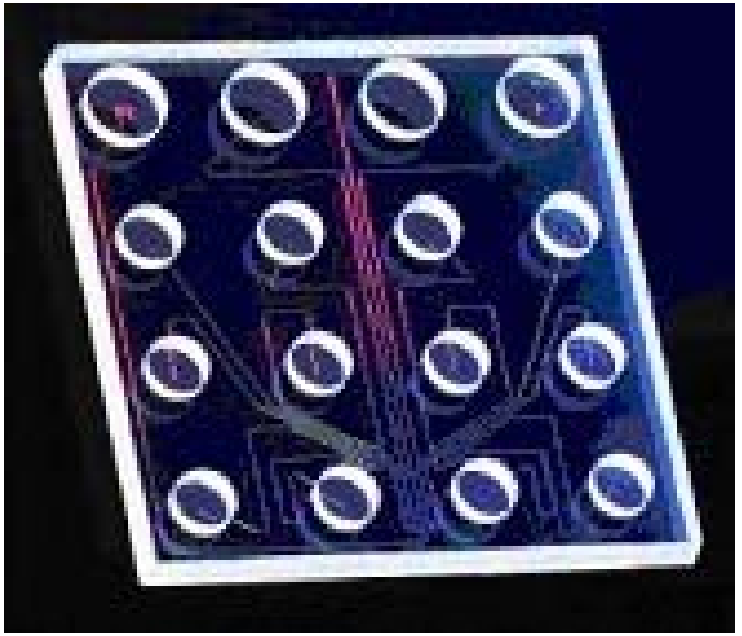
Intel 4004 Calculator IC
(1971)

Tubes to Chips: BioChips

- **Driven by Biomolecular Analysis needs**

Image from Barnard College Archives

Test tubes & Beakers (1950)



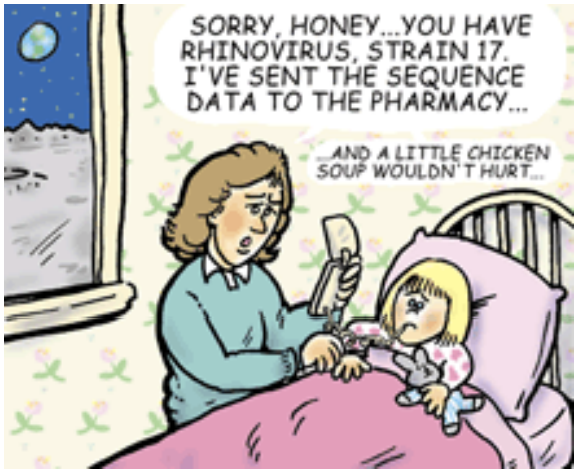
Agilent DNA analysis Lab on a Chip (1997)

Portable Analysis

- New knowledge of molecular basis of biology
  - e.g. Human Genome Project
  - Massively parallel analysis infrastructure
- Integration and miniaturization will drive biomolecular analysis instrumentation

Biomolecular "mainframes"

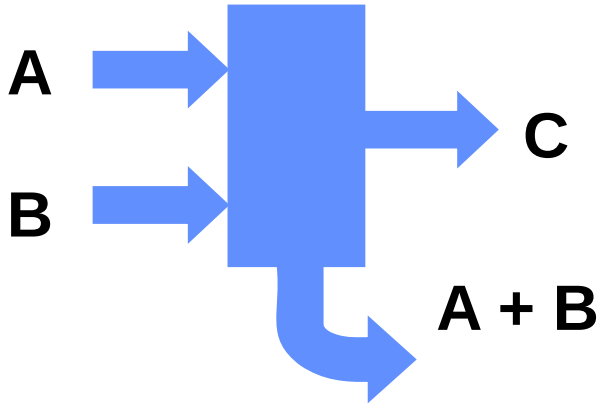
Spock with Tricorder Sensor + computer



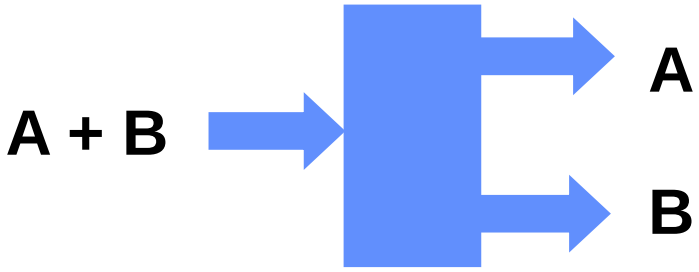
Burns Science 2002

Typical Biological Lab Functions

- **Synthesis**



- **Analysis**



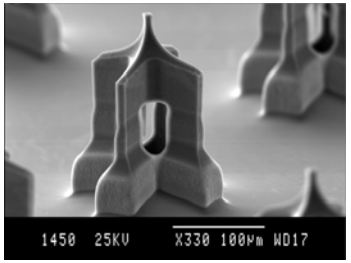
Mixing

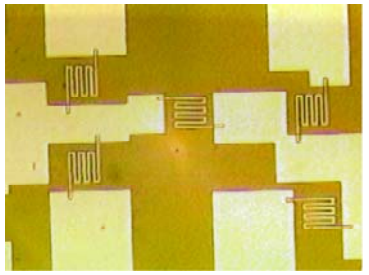
Reaction

Separation

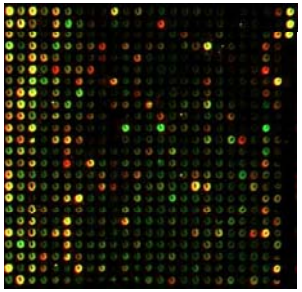
Microdevice Technology Summary

- **BioMEMS**



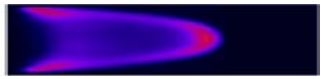


- **BioChips**

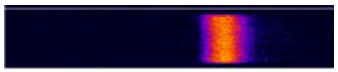


- **Lab-on-a Chip**
  - **Droplet**

  - **Channel**
    - **Pressure**

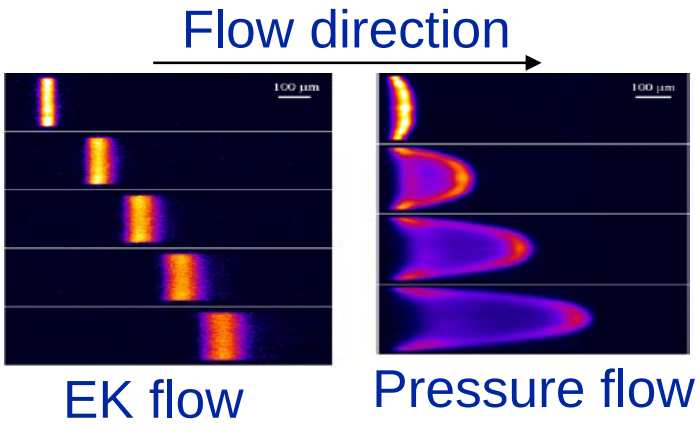


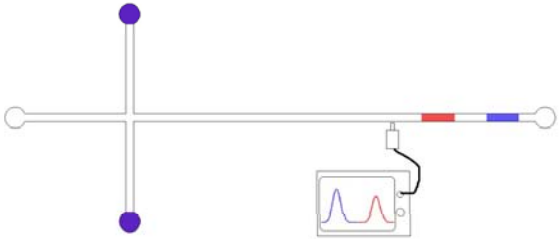
    - **Electrokinetics**

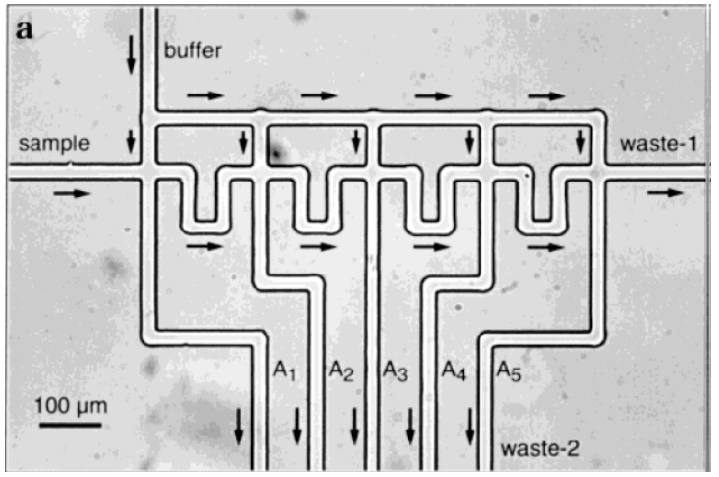


Channel-based LoC: EK drive

- **What is Electrokinetics ?**
  - **Voltage driven flow**
- **Why Electrokinetic flow?**
  - **Plug velocity profile**
  - **Portable kV sources**
  - **EK flow can be used for electrophoresis**
  - **EK flow already used in complex designs**





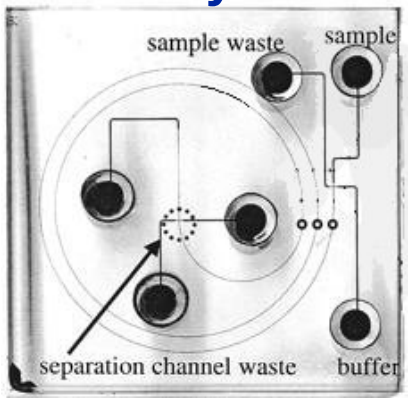


Serial Mixer ORNL

Microdevice Technologies: LoC

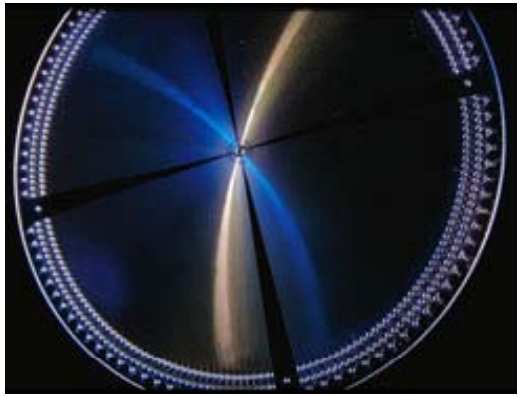
- Miniaturized Bio-chemical Lab-on-a-Chip
- Individual functional units demonstrated
  - Analyzer, Reactor, …
- Research driven by integration
  - Design aids needed to handle complexity!

Amino-Acid Analysis



ORNL

DNA Analysis

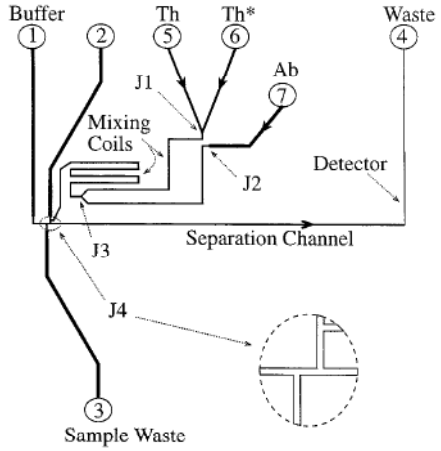


U. C. Berkeley

Chemical Synthesis

U. Hull

Immunoassay



U. Alberta

Outline

- Introduction
- Motivation for Design Automation
- Design Hierarchy
- Multi-function System Simulation
- Multi-plex Physical Synthesis
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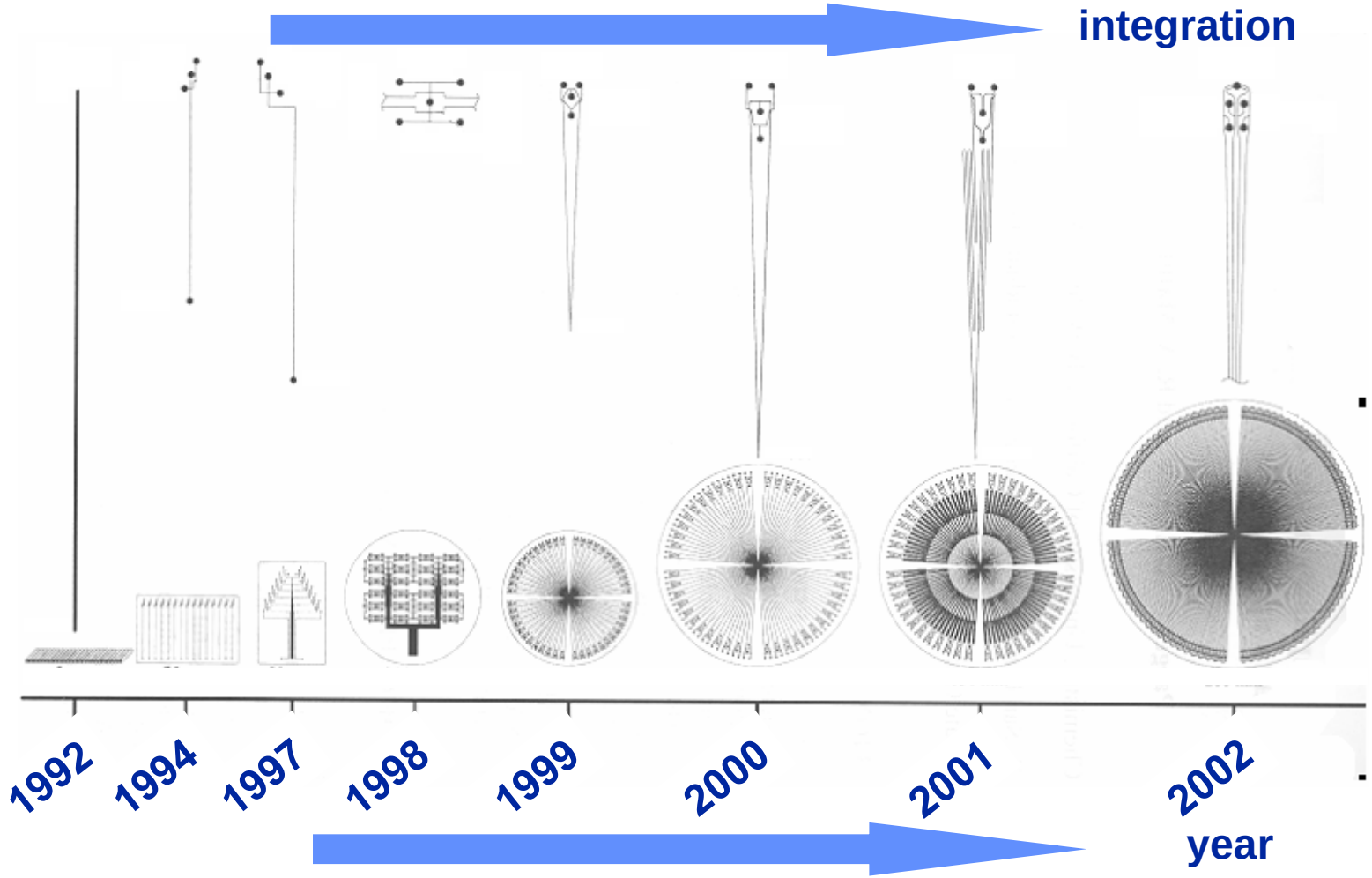
Multiplex Lab-on-a-Chip

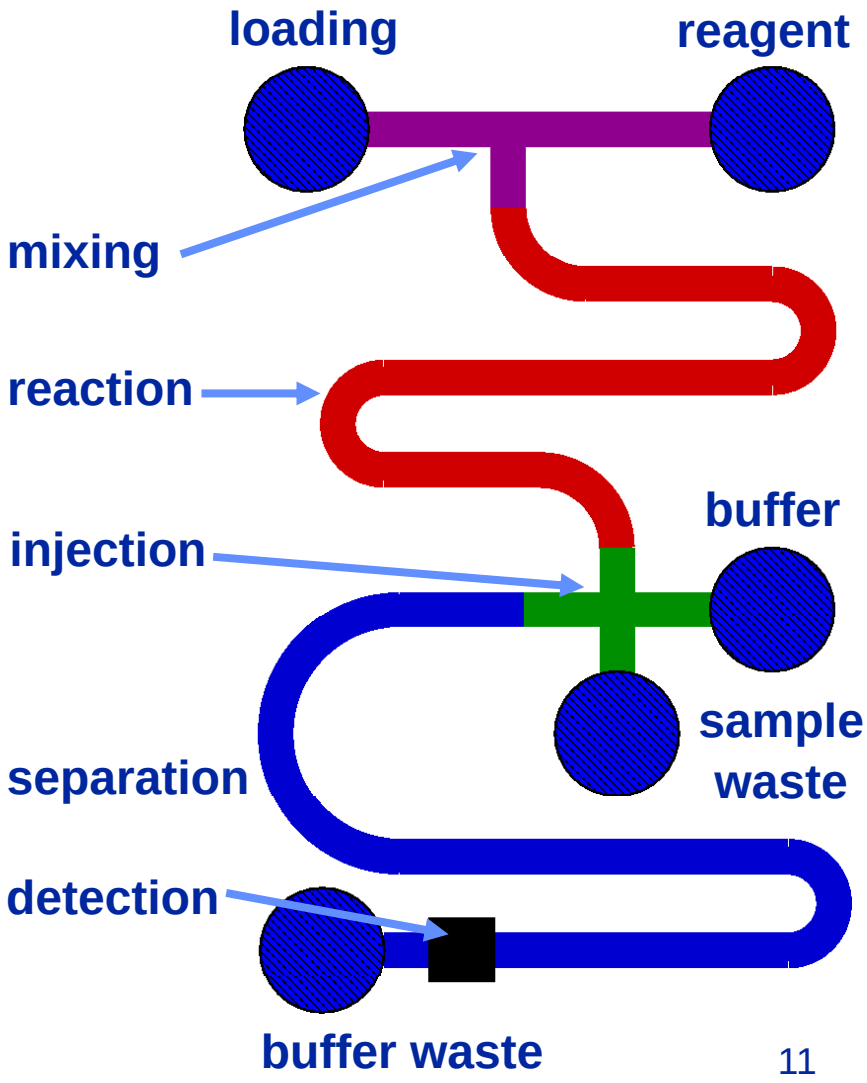
- **Same subsystem, integrated for redundancy, combinatorial experiments**



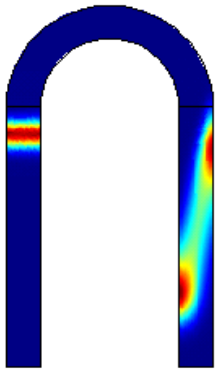
Multifunction LoCs

Example: Immunoassay

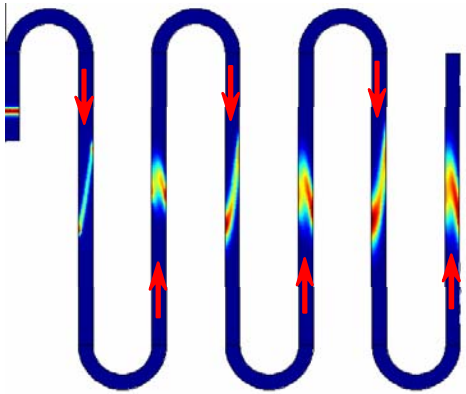
1. Load sample {Ag*, Ag}
2. Mix with reagents {Ab}
3. Rxn: Ag* + Ab → Ag*-Ab
4. Inject sample plug
5. Separate analytes
6. Detection
   { [Ag*,Ag], Ab, Ag*-Ab}



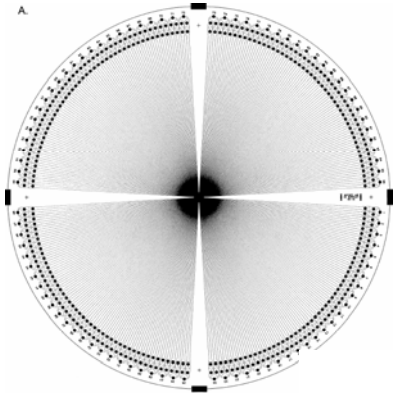
Complexity Hierarchy



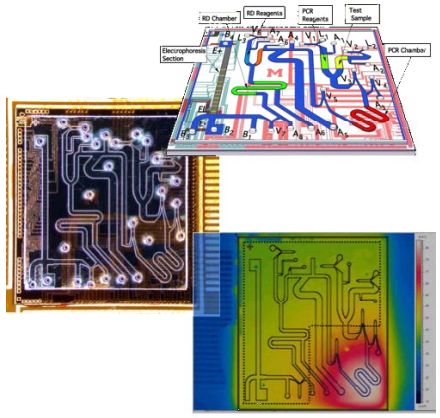
Element



Functional Component



Subsystem



System

Increasing Integration

Outline

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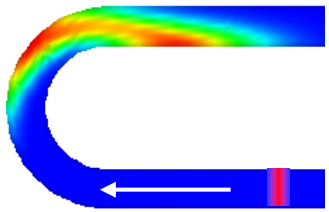
Simulation Techniques

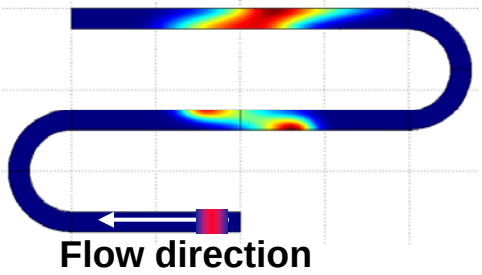
- **Computational fluid dynamics**

One single turn

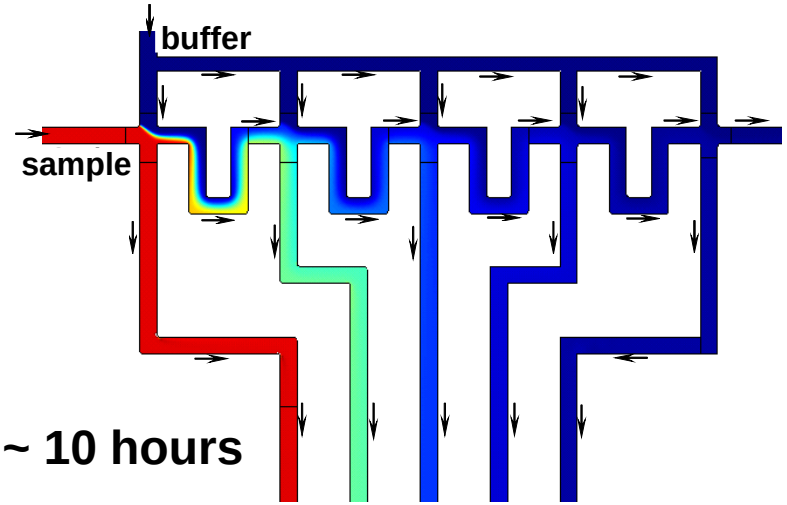


~ 10 Hours

Complimentary turns

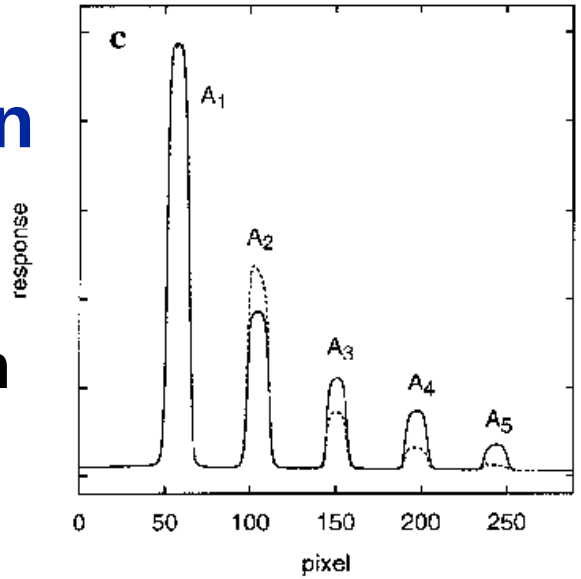


2~3 days



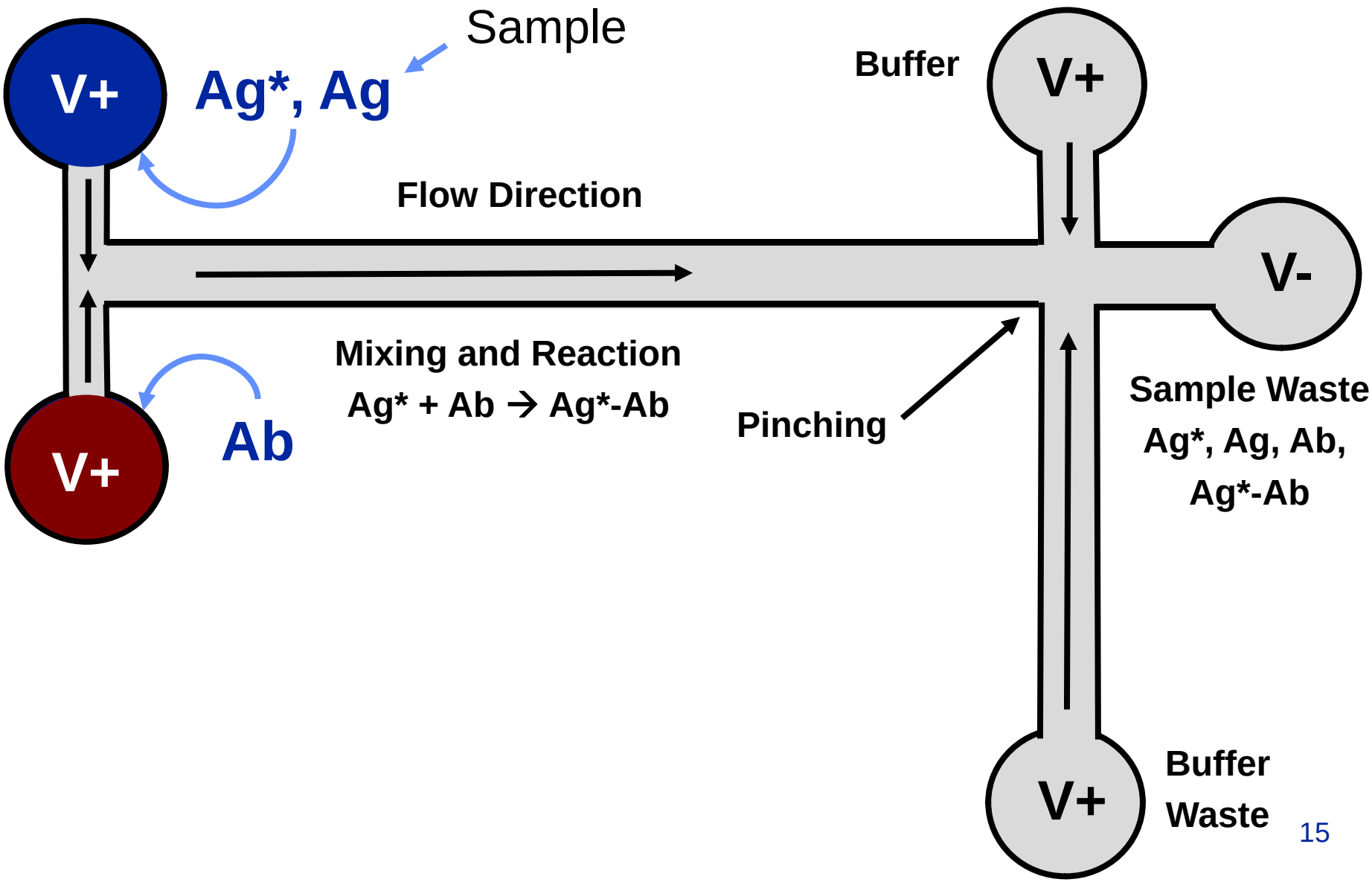
~ 10 hours

- **Reduced order models**
- **Hierarchical decomposition and parameterization**
  - **Capture geometric effects**
  - **Amenable for use in design**

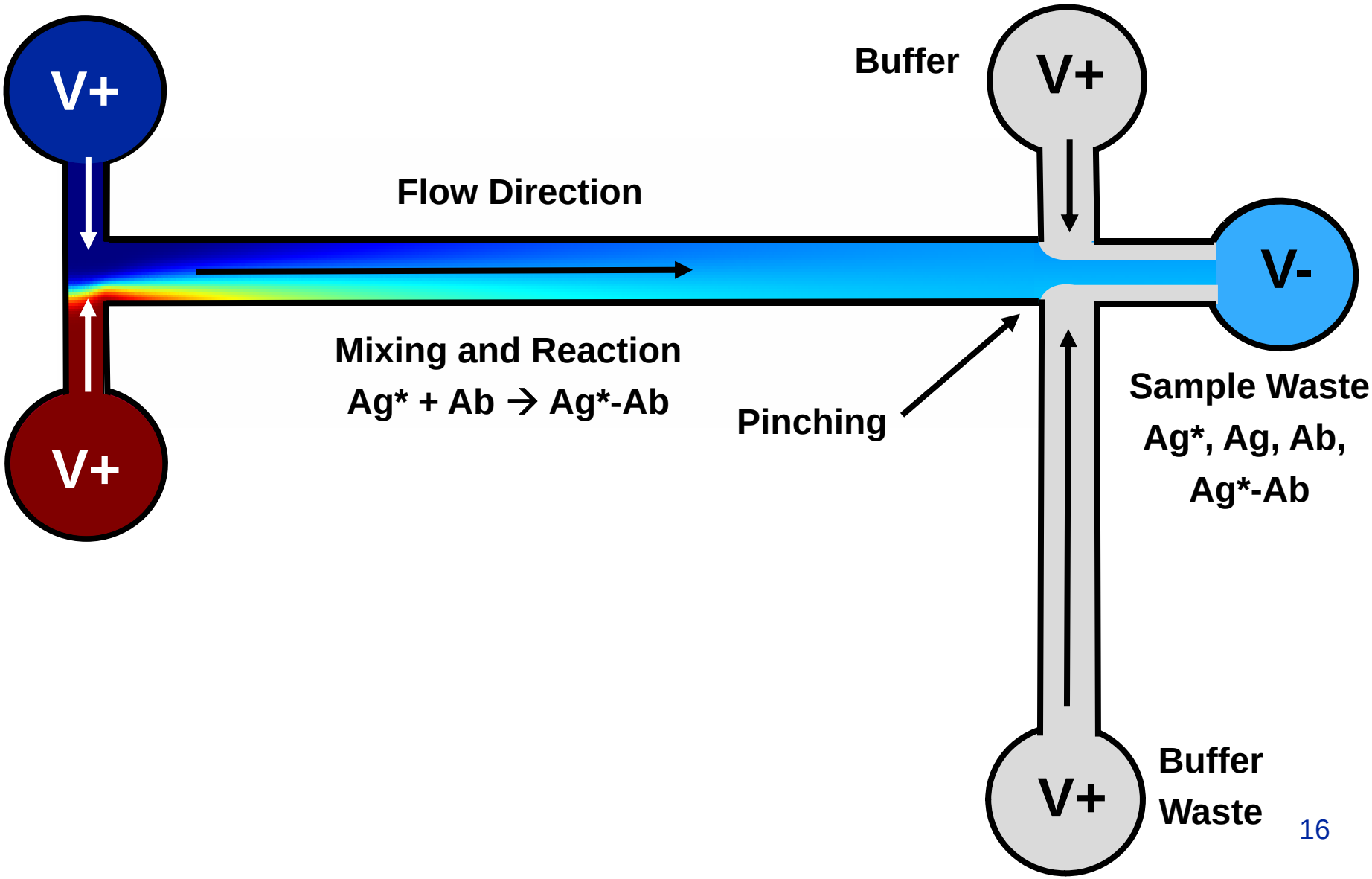


Serial Mixer (ORNL)

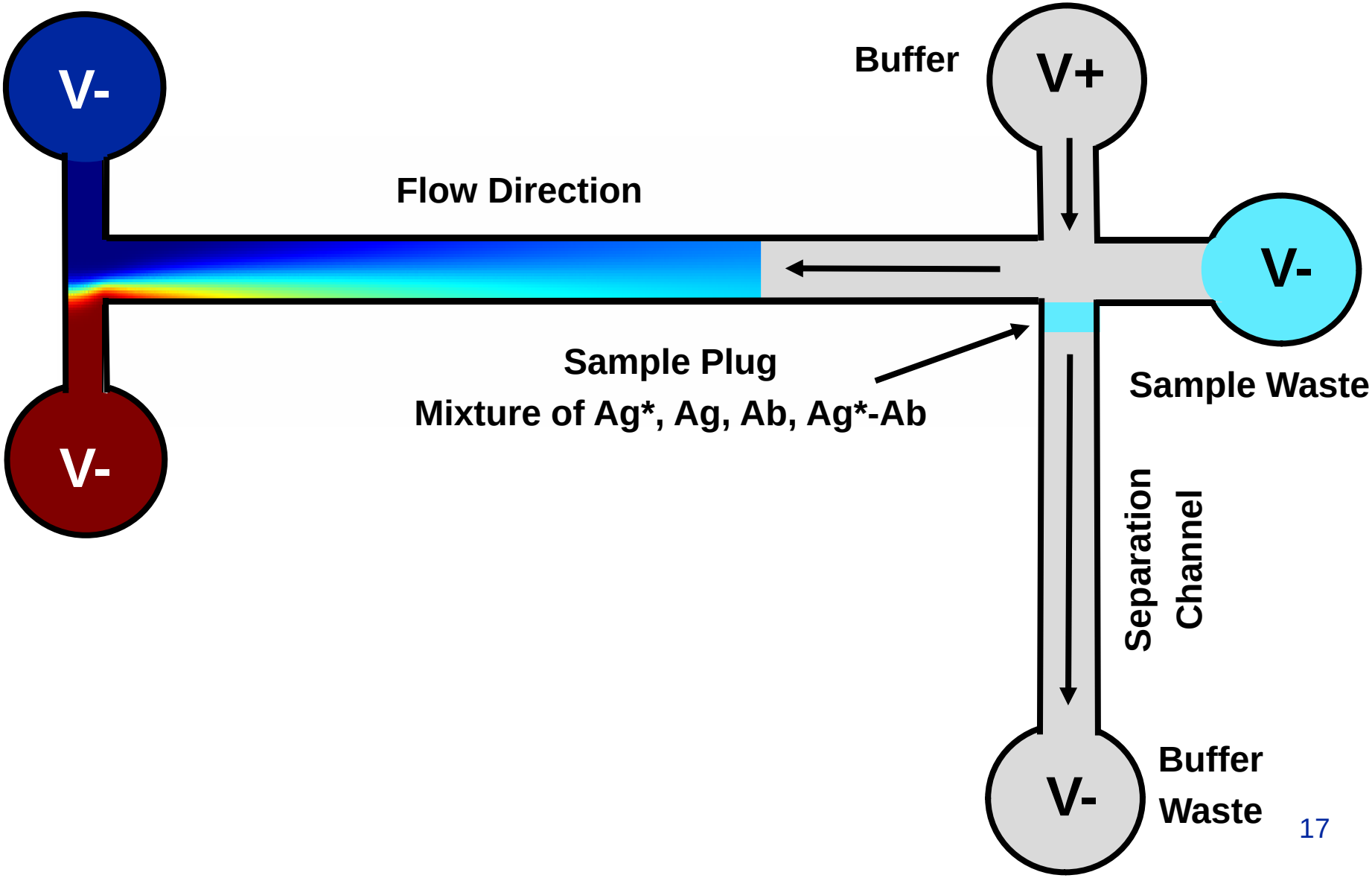
Hierarchy Example: Immunoassay



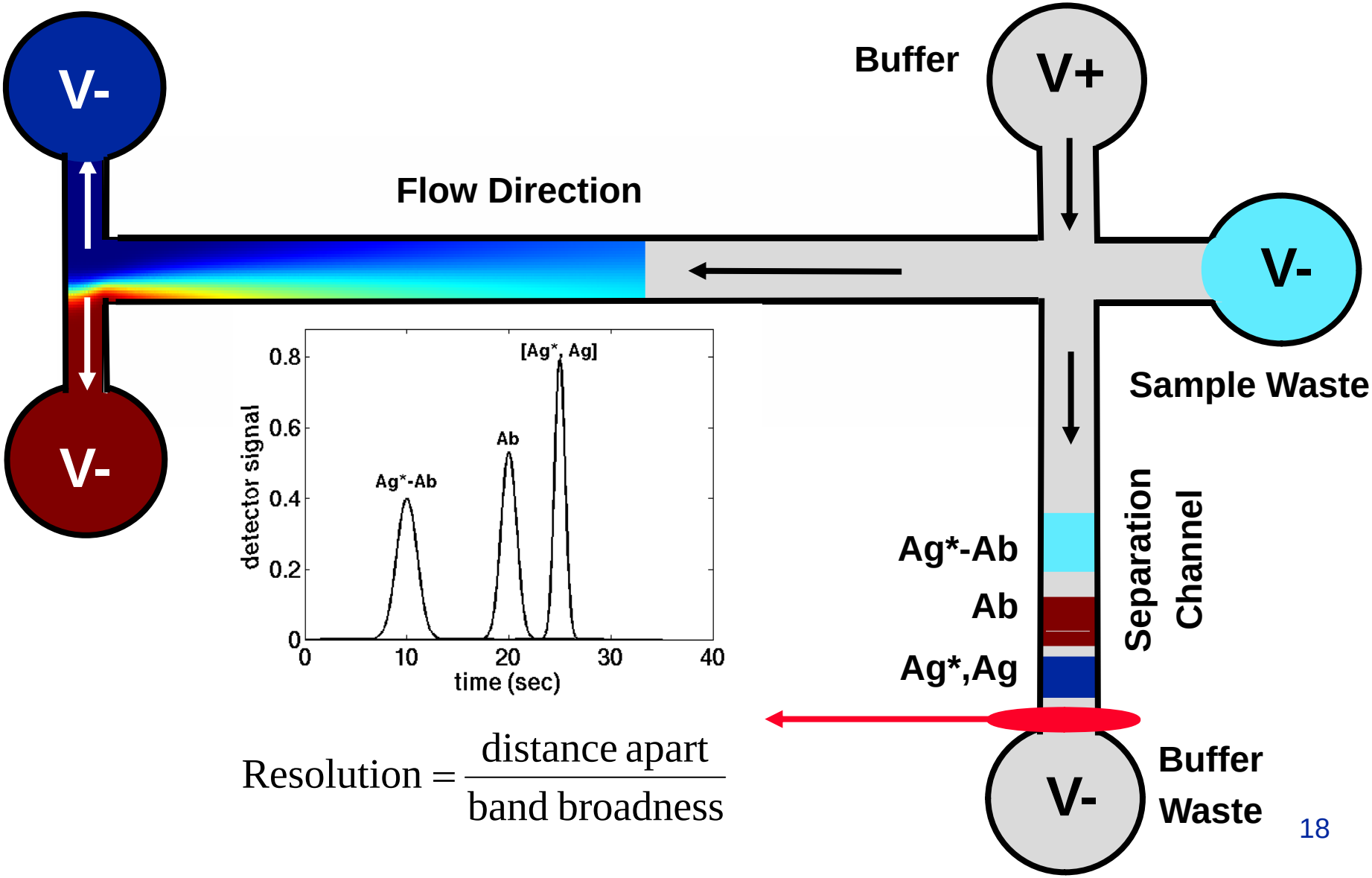
Synthesis Phase: Steady State



Analysis Phase: Transient



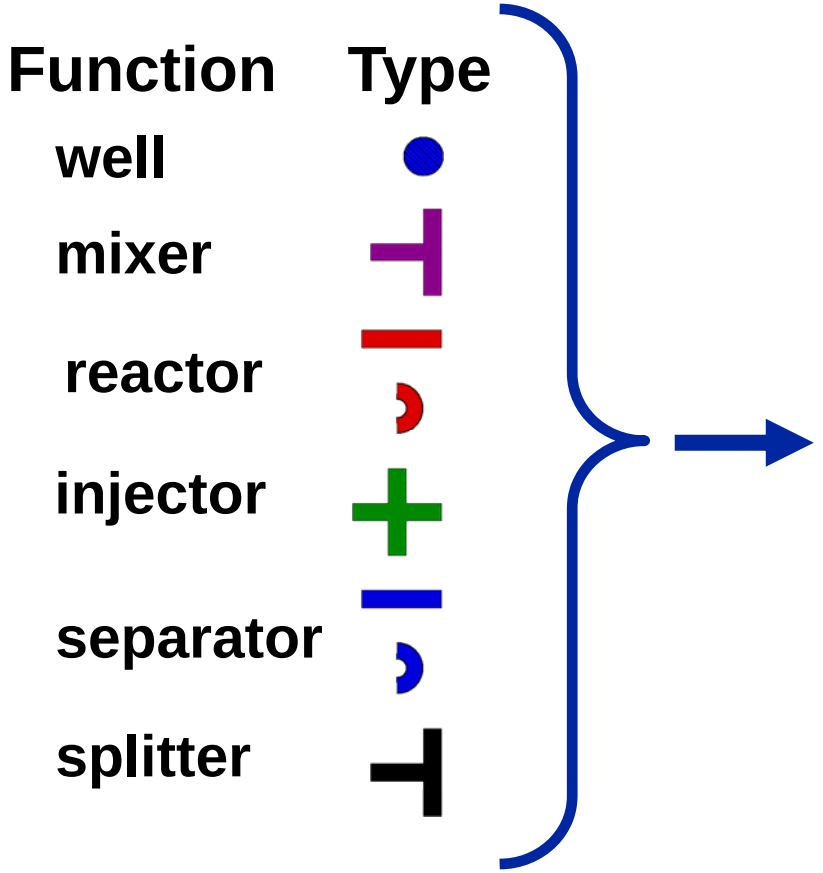
Analysis Phase: Transient



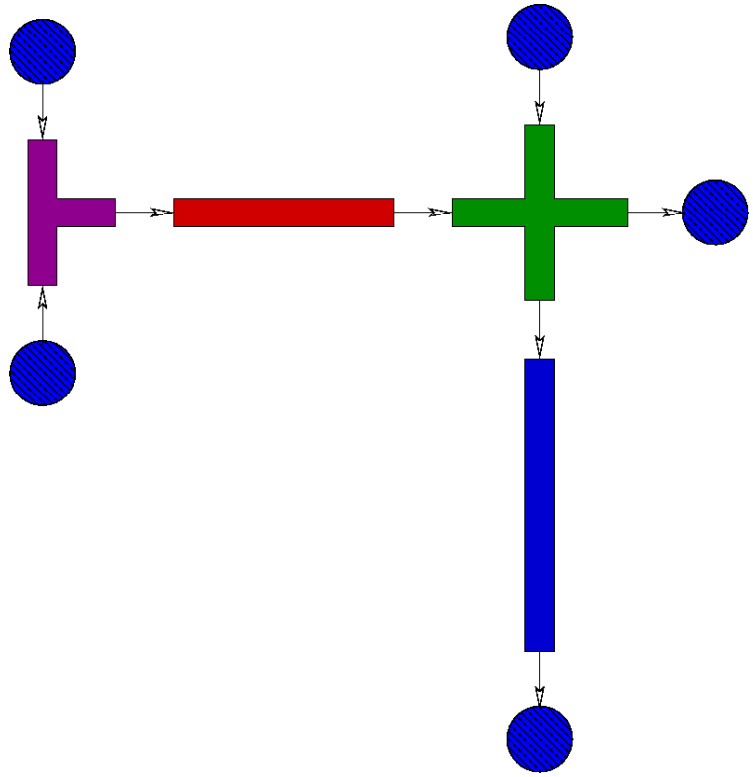
$$\text{Resolution} = \frac{\text{distance apart}}{\text{band broadness}}$$

Component Library

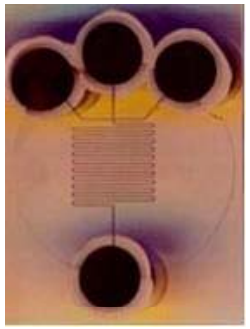
Library of LoC Unit Operations

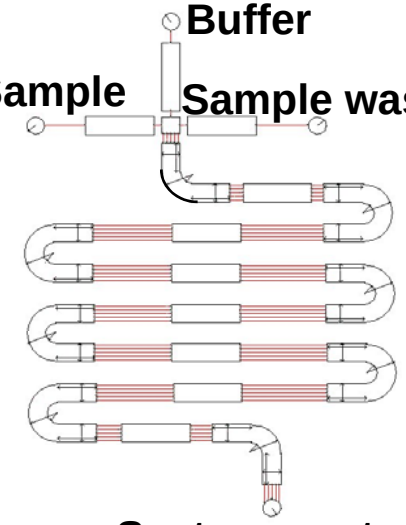


Compose Topology

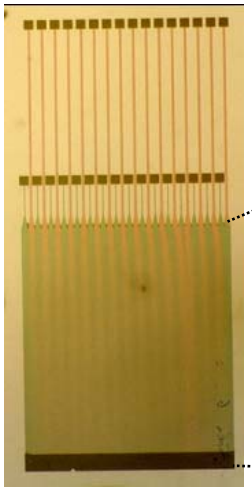


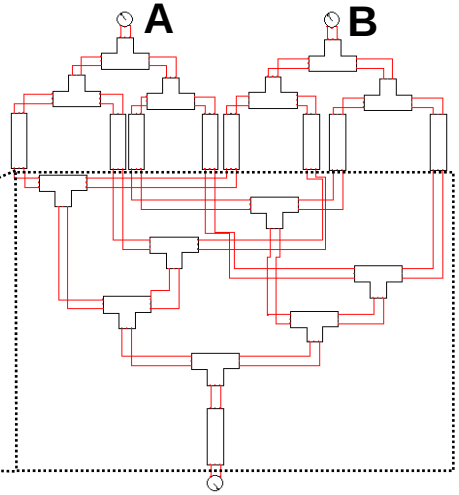
Composition Examples



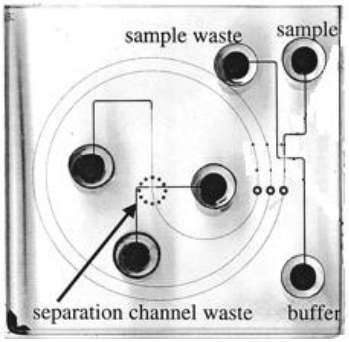


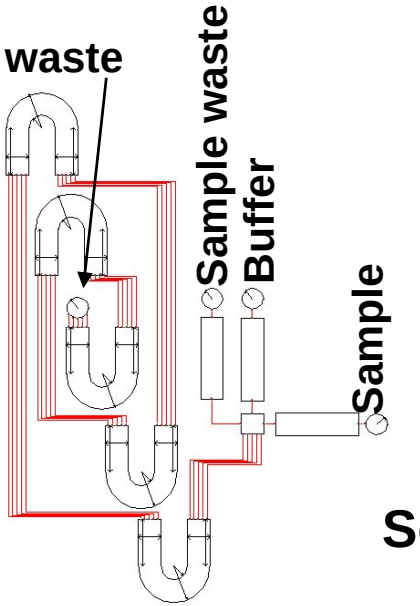
Serpentine separation chip (ORNL)



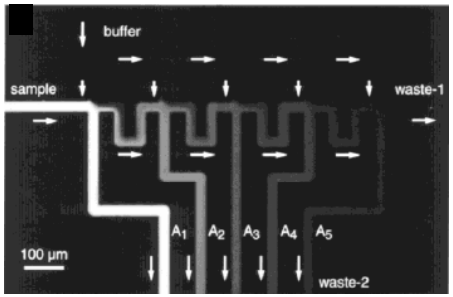


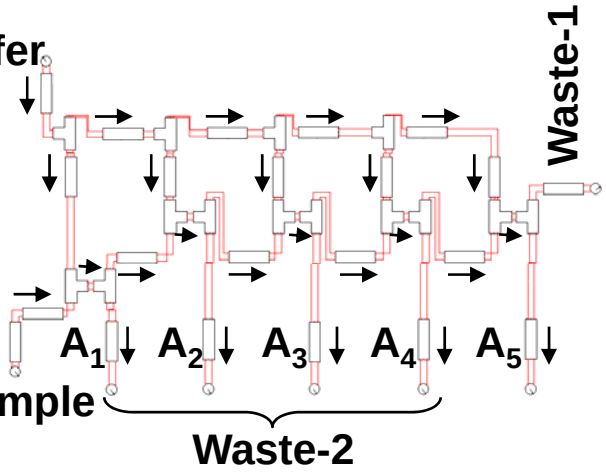
Multi-stream mixer (M. Koch, et al.)





Spiral chip (ORNL)





Serial Mixing network (S.C. Jacobson, et al.)

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- Component Models
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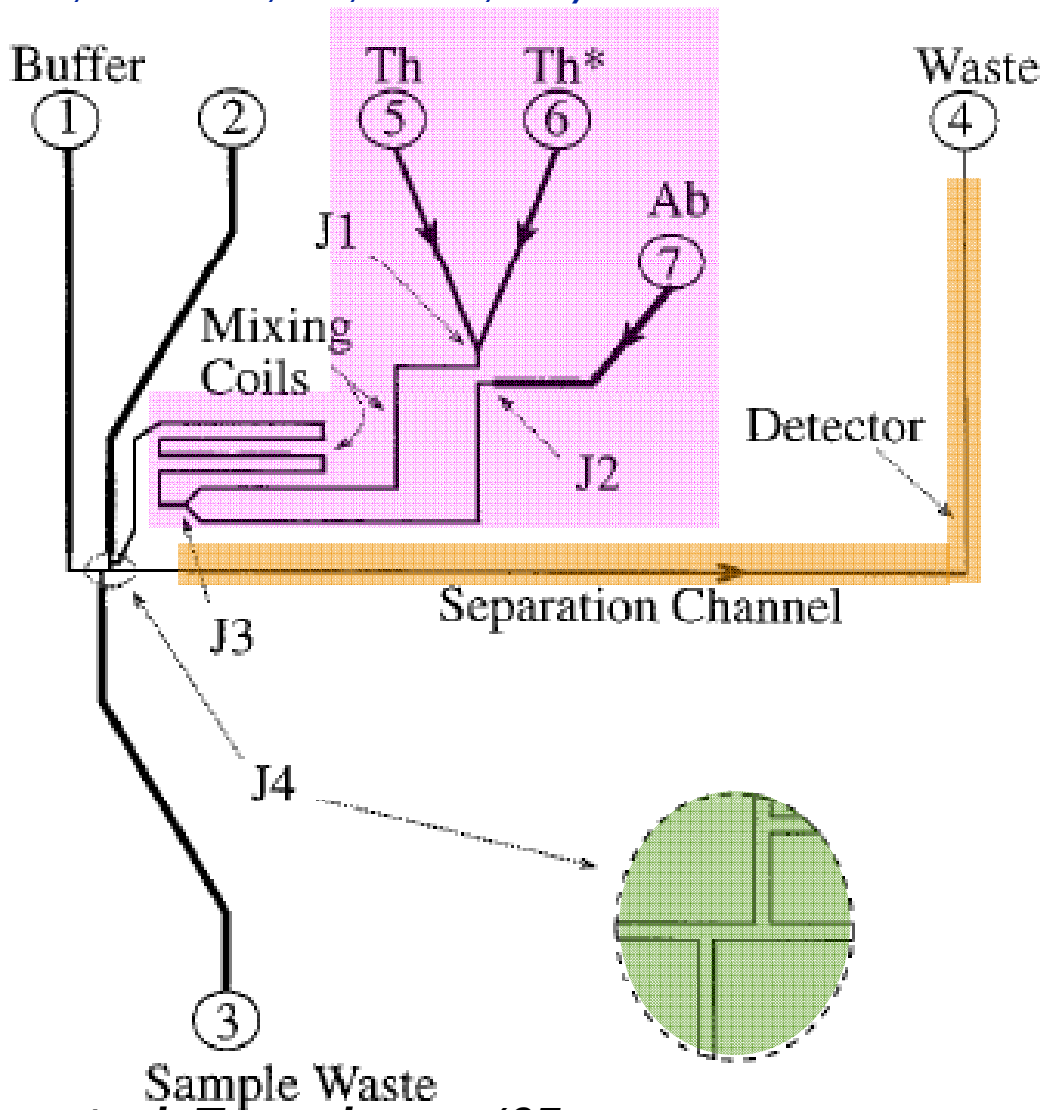
Simulating a Multifunction Design

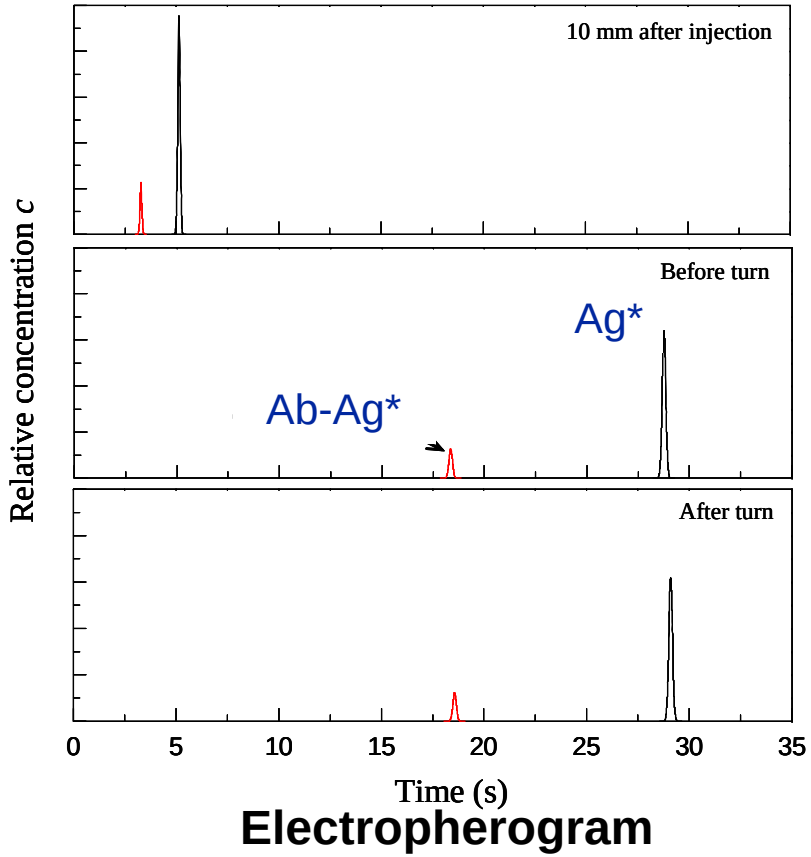
(Cheim, Clin. Chem., *44:3*, 591-598, 1998)



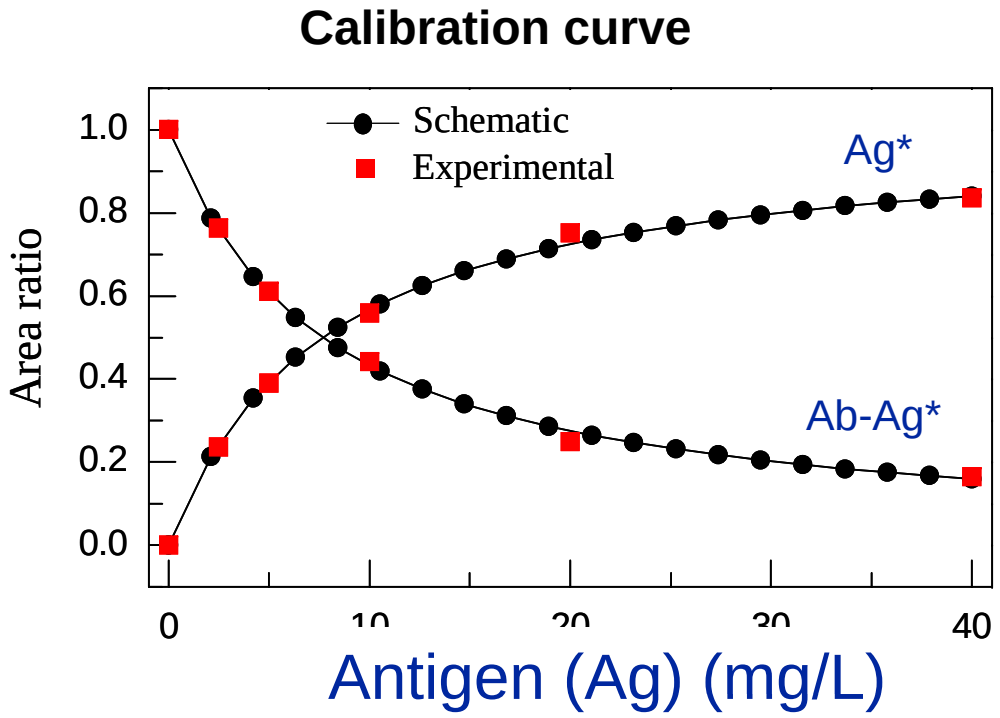
- **Real Immunoassay Chip from U. Alberta**
- **Operation**
  - **Mixing/Dilution**
  - **Reaction**
  - **Injection**
  - **Separation**
  - **Detection**

Wang et. al. Transducers '05

Simulation Results



Electropherogram



- **Ag↑ ⇒ unreacted Ag* ↑ ⇒ Ab-Ag* ↓**
- **Simulation matches experiment**
- **Simulation time is a few CPU seconds**

Wang et. al. Transducers '05

Optimizing the design: NLP

$$x_0$$

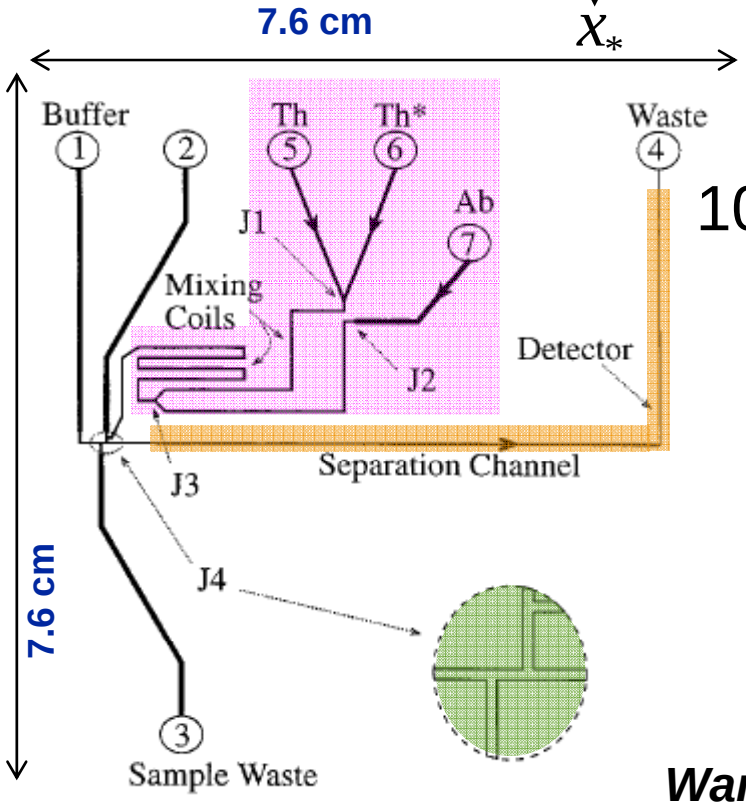
$$\begin{aligned} obj: \quad & \min f(y_i) \\ s.t. \quad & g(y_i) < 0 \\ & h(y_i) = 0 \end{aligned}$$

x_i →

← y_i

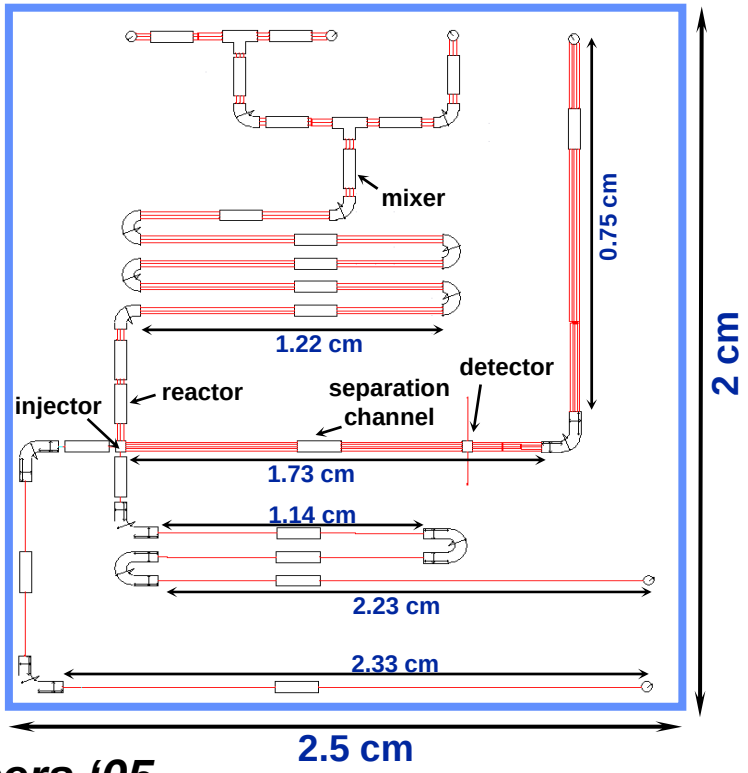
$$y_i = SIM\,(x_i, PARAMS\,)$$

$$x_*$$



10x less space

Same perf



Wang et. al. Transducers '05

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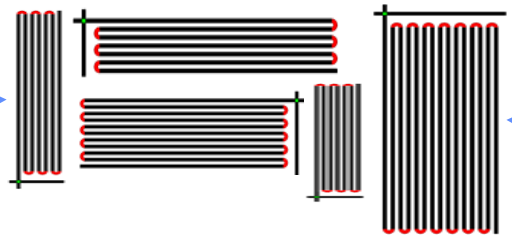
Multiplex Physical Synthesis

Family of subsystems



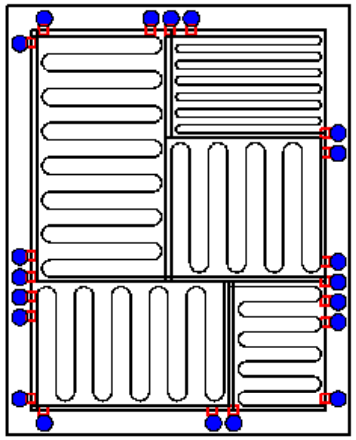
Input: Design Specs

- **Overall Chip Dimensions**
- **Species/Buffer properties**
- **Operational constraints**
- **Chip fabrication**
- **Subsystem performance**

Simultaneously determine:

- **placement**
- **dimensions**
- **# of sections**
- **voltage**

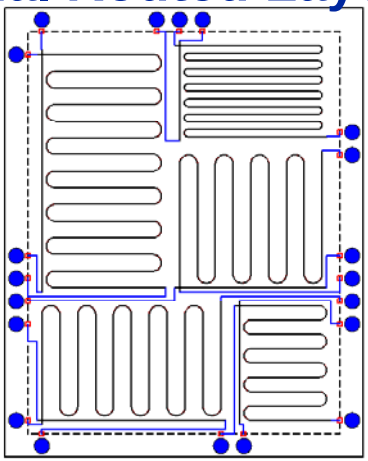
Intermediate Placement



Route subsystems to wells:

- **single layer, planar**
- **min. length, bends**

Final Routed Layout

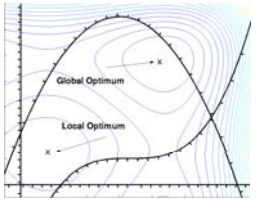


Pfeiffer et. al., TCAD '06

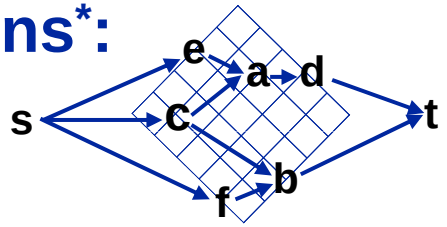
Placement Features

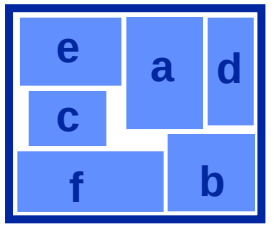
- **Subsystem optimization:**

NLP →



- **"System-on-Chip" extensions*:**



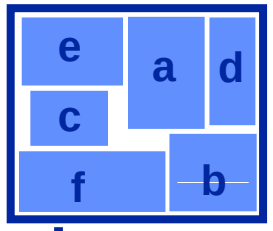


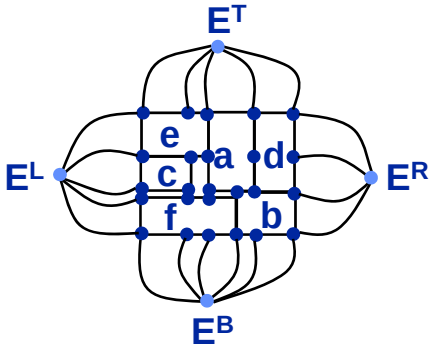
* Murata, H. et al., IEEE Trans. on CAD. 1996

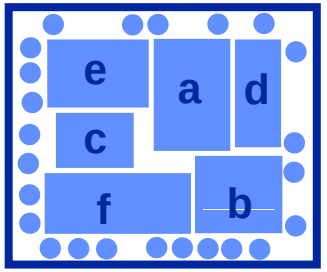
- **Orientation:**

and

- **Well placement:**

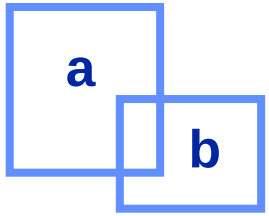




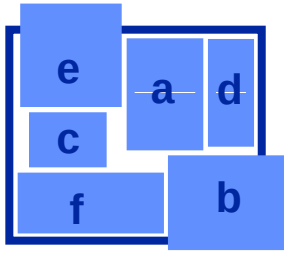


- **Overlap constraints:**

Never →



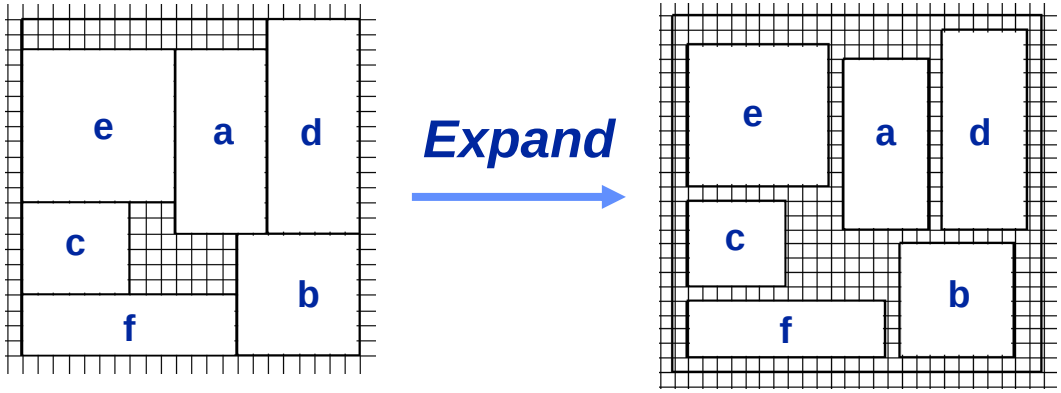
Penalty →



Pfeiffer et. al., TCAD '06

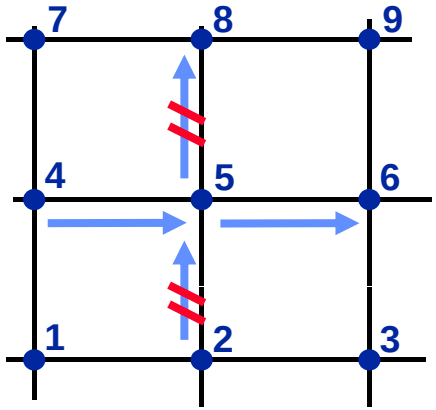
Routing Features

- **Routing grid graph*:**



* Lengauer, T., Combinatorial Algs. for IC Layout, 1990

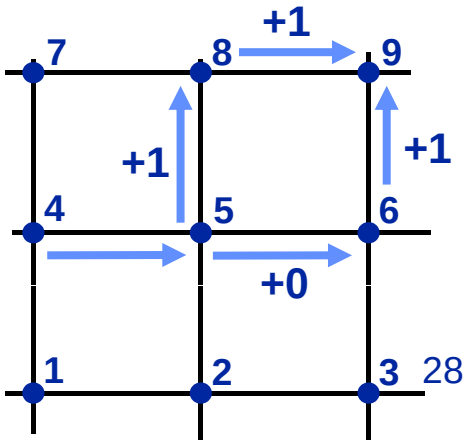
- **Node constraints:**



flows in = flows out
1 flow in/out of node
(single layer, planar)

- **Bend reduction:**

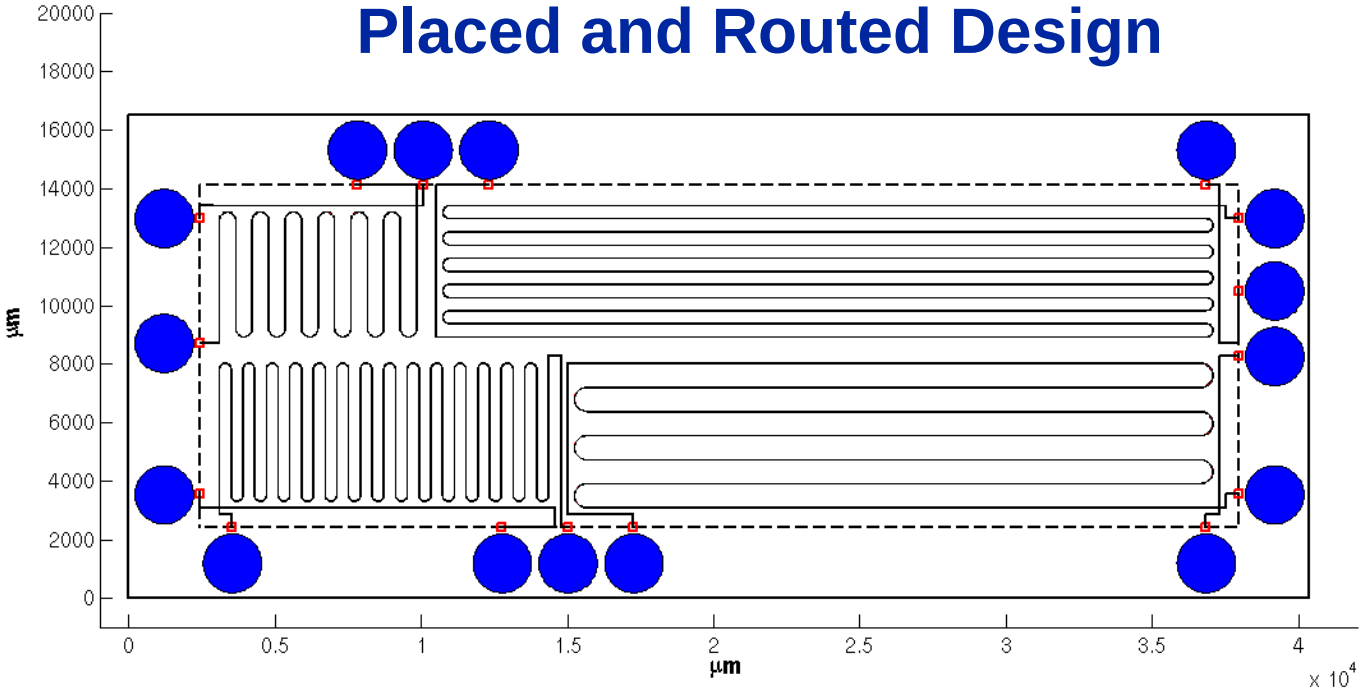
penalize bends
favor straight paths



Pfeiffer et. al., TCAD '06

Multiplex Synthesis Example

Placed and Routed Design



	P&R By Hand	Automated	Improvement
Time	**5+ hrs.**	**Place: 20 min** **Route: 3 min** **Total: 23 min**	**> 10X faster**
Dimensions	**1.67cm x 8.8cm**	**1.61cm x 3.79cm**	**~ 2.5X smaller**

Pfeiffer et. al., TCAD '06

Summary

- Lab on a Chips *integrate* bioanalysis functions
- Hierarchically decomposition used for development of fast, accurate, reusable, parameterized models
- Relatively few types of band profile on a chip
  - Profile representation to simplify PDE into ODEs
- Models are reuseable
- Separation models integrated with P&R algorithms for simultaneous model based placement followed by routing
- Focus still at ‘circuit’-level, need to consider architecture, protocol optimization

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  - **Prof. Steinar Hauan (ChE)**
  - **Prof. Qiao Lin (ME, now at Columbia Univ)**
- **Students**
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