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Stress Aware Layout Optimization

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Outline

- Introduction & motivation
- Simulation at device level
- Guidelines to improve performance via layout
- Applying guidelines to standard cell layouts
- Conclusions and future work

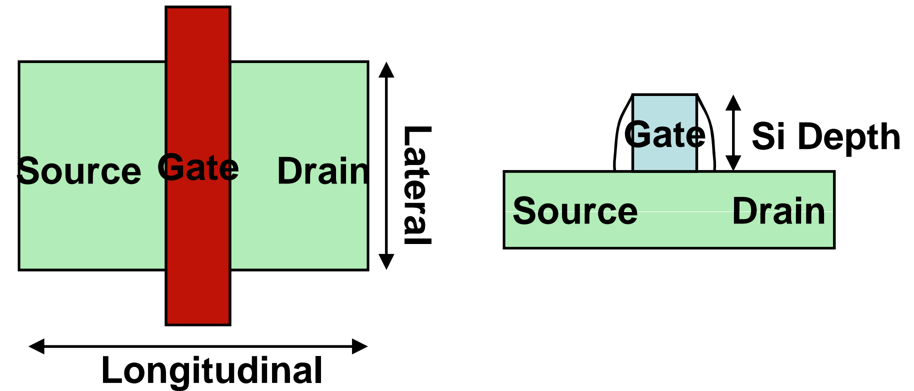
Introduction

- Maintaining performance and reliability with scaling is difficult
  - Can no longer scale tox, VDD, V_{th} as aggressively as L
  - Mobility degradation due to higher effective fields

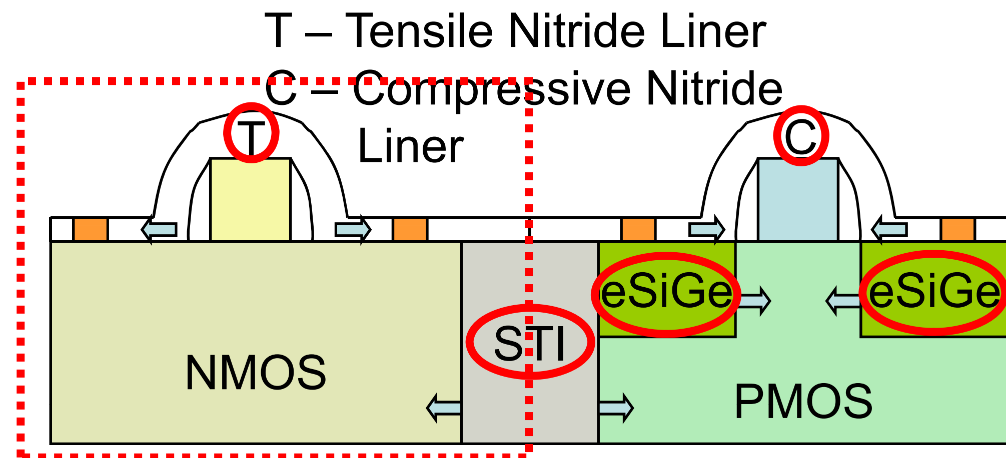
- Introduce mechanical stress in channel to enhance carrier transport
  - Alters valence and conduction bands
  - Changes effective carrier mass and/or band scattering rates
  - Increase in carrier mobility results in higher performance and leakage

Introduction

- NMOS and PMOS have different desired stress in different directions
- Stress generated due to thermal and lattice mismatch
- Four main sources of stress
  - Shallow trench isolation
  - Embedded SiGe
  - Dual-stress nitride liner
  - Stress memorization technique

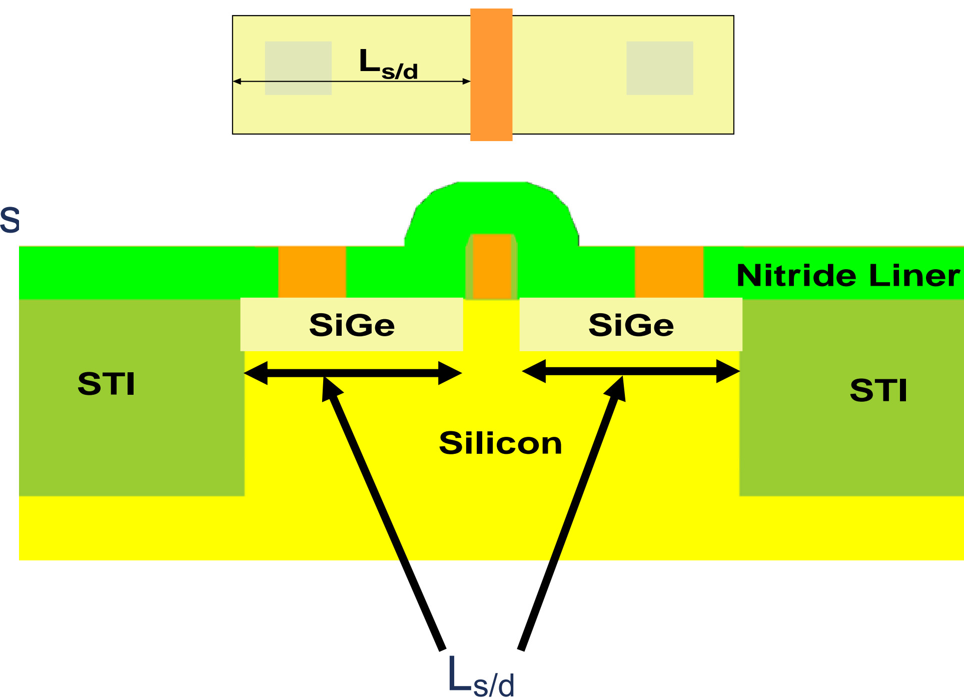


	NMOS	PMOS
Longitudinal	Tensile	Compressive
Lateral	Tensile	Tensile
Si Depth	Compressive	Tensile



Dependence of Channel Stress on Layout

- Amount of stress transferred has a strong dependence on layout
  - Longer active area (higher $L_{s/d}$) – more SiGe, STI pushed away
  - Contacts away from channel – more stress due to nitride, no contacts - higher stress
  - SMT – uniform, not considered in this analysis
- Two devices with same W, L can differ significantly in performance
- We study this dependence and suggest layout guidelines to enhance channel stress



Previous Work

- Focus on modeling stress due to various sources
- No comprehensive model that considers all layout dependent sources
- Extensive research and modeling focused on STI
  - Accurate device level modeling (included in BSIM4)
  - Efficient white-space management placement algorithms
  - BUT: Contribution of STI to stress induced in channel is minor compared to other sources
- No research has focused on new standard cell library design exploiting stress, while considering all layout dependent sources

Comparison to V_{th} reduction

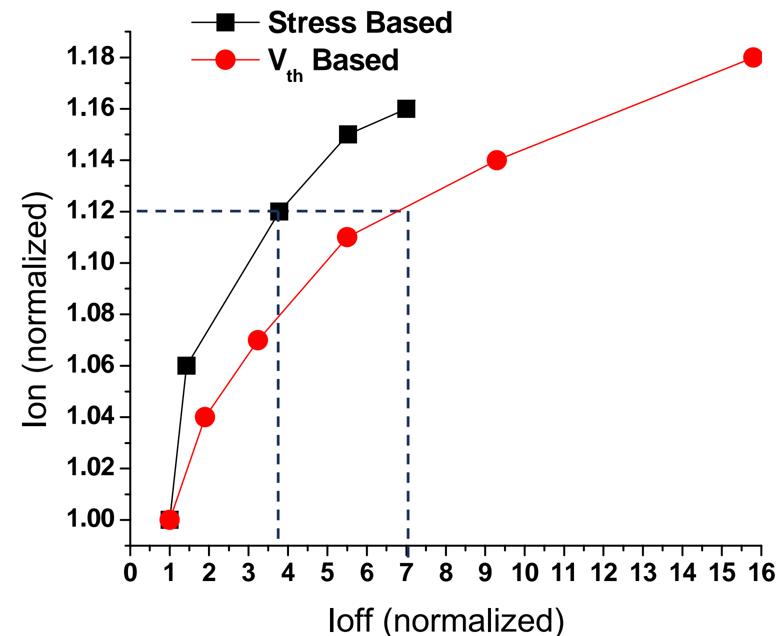
- Mobility enhancement -
  - Saturation current – sub-linear dependence
  - Leakage current – linear
- V_{th} reduction
  - Saturation current – almost linear
  - Leakage current – exponential
- Mobility enhancement shows a better tradeoff
  - In 65nm, stressed PMOS achieves 12% Ion improvement with ~½ leakage penalty of V_{th} reduction

$$I_D = \frac{\mu_0}{[1 + U_0(V_{GS} - V_T)]} \cdot \frac{C_{ox}}{2aV} \cdot \frac{W}{L_{eff}} \cdot (V_{GS} - V_T)^2$$

$$V = \frac{1 + v_c + \sqrt{1 + 2v_c}}{2} \qquad v_c = U_1((V_{GS} - V_T)/a)$$

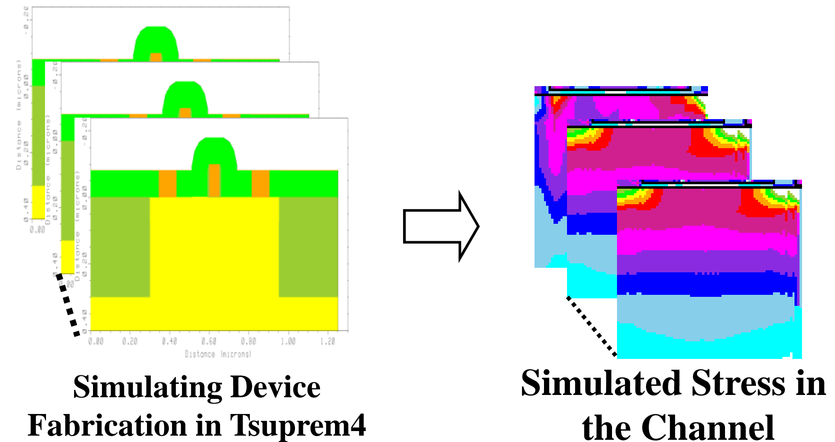
$$I_{sub} = A \cdot e^{\frac{1}{nv_T} \cdot (V_G - V_S - V_{th0} - \gamma' V_S + \eta V_{DS})} \cdot (1 - e^{(-V_{DS})/v_T})$$

$$A = \mu_0 C'_{ox} \frac{W}{L_{eff}} v_T^2 e^{1.8} e^{-\frac{\Delta V_{th}}{\eta v_T}}$$



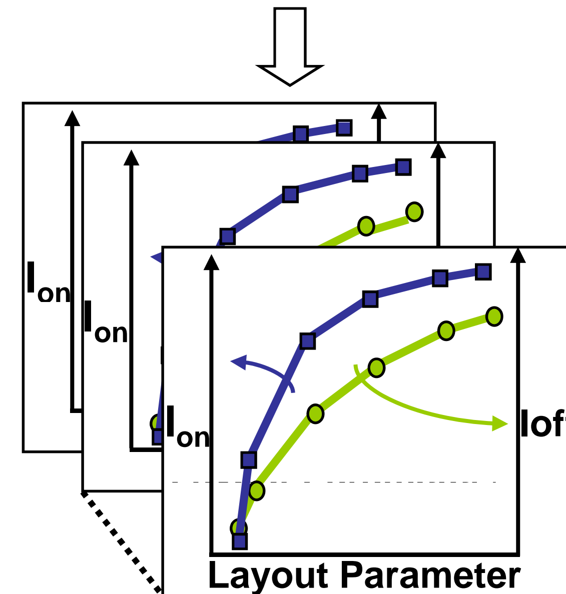
Simulation Flow

- Tsuprem4 for simulating device fabrication
- Stress values imported into Davinci → solves stress-based equations
- Resulting drain currents consistent with published results [IBM65, IEDM05]
- Based on simulation, analyze layout dependencies to develop guidelines



Simulating Device Fabrication in Tsuprem4

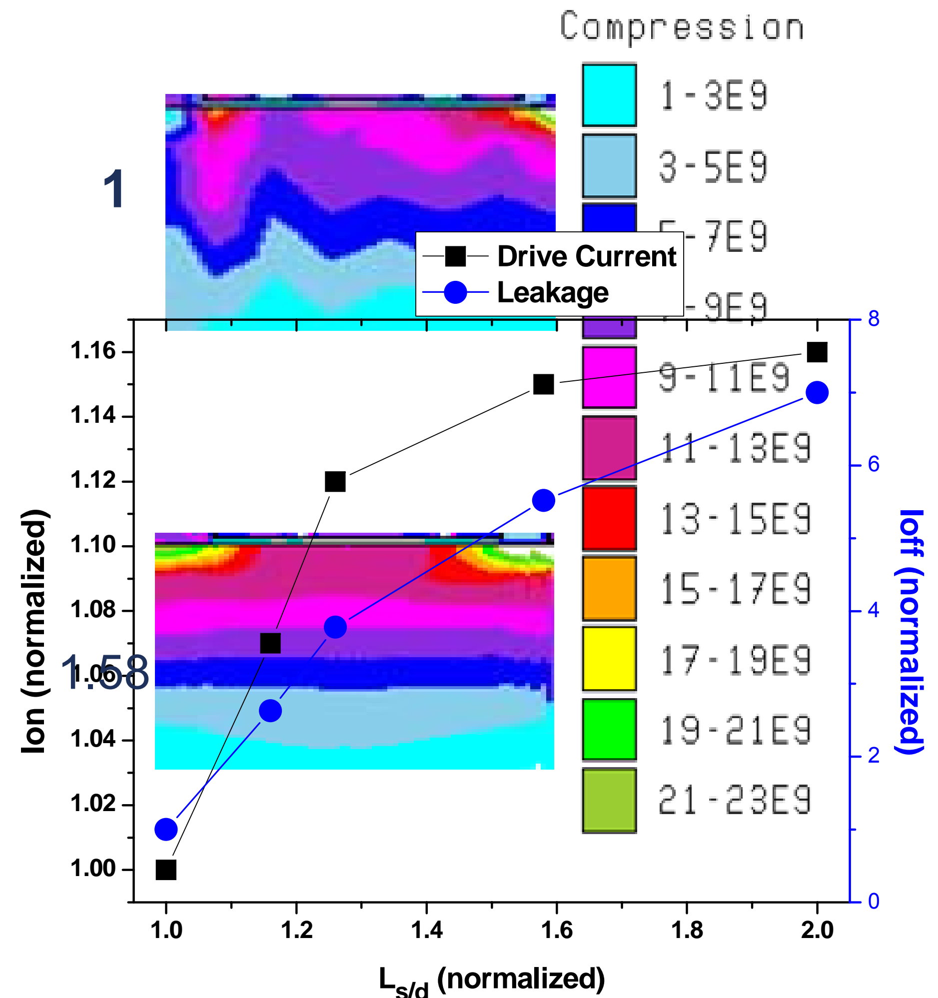
Simulated Stress in the Channel



Dependence on Layout Parameters using Davinci 3D TCAD Tool

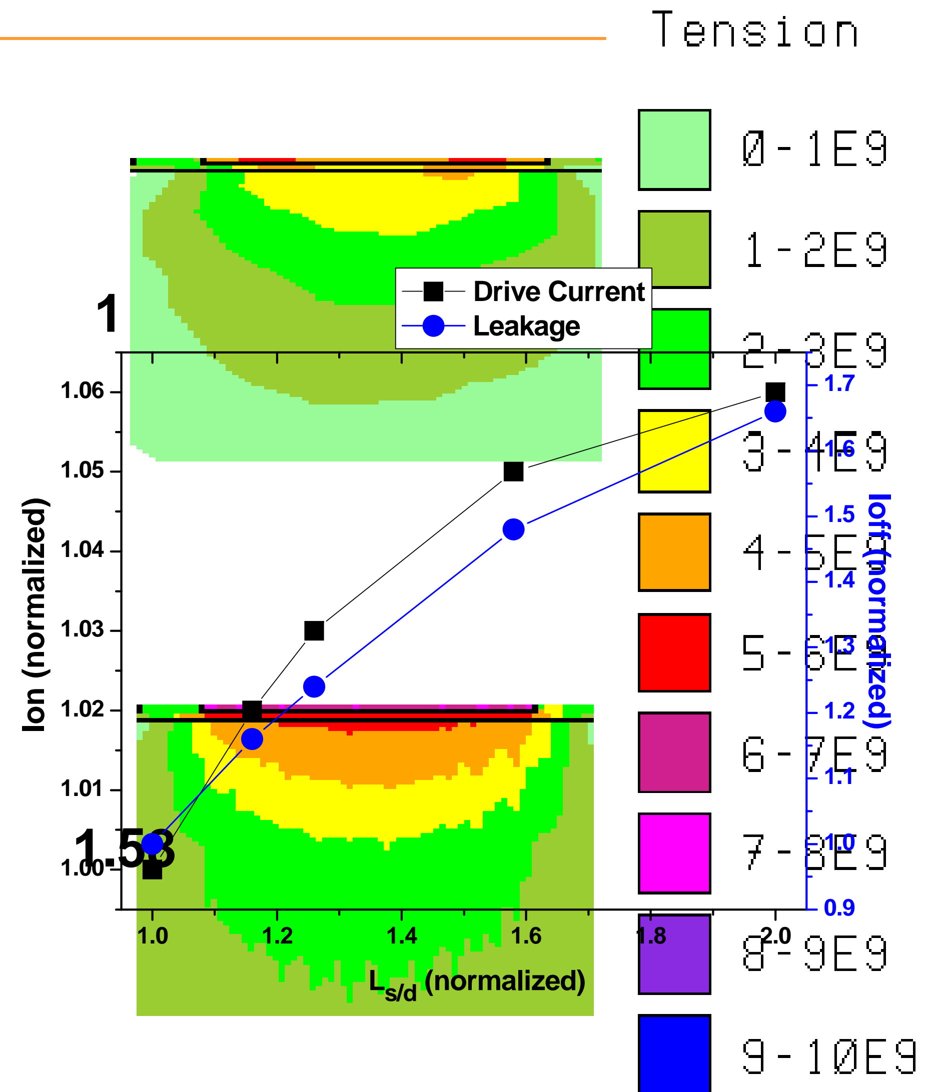
Simulation for Isolated Device - PMOS

- Vary source/drain length ($L_{s/d}$)
- 12% performance increase for 3.8X increase in leakage
  - Superior tradeoff to Vth reduction
  - Leakage tradeoff better for lower power libraries
- Ion gains saturate beyond $L_{s/d}$ of 1.6
- Ion gains sensitive to contact placement
  - 2.6% of improvement
  - No contact – 4% higher Ion



Simulation for Isolated Device - NMOS

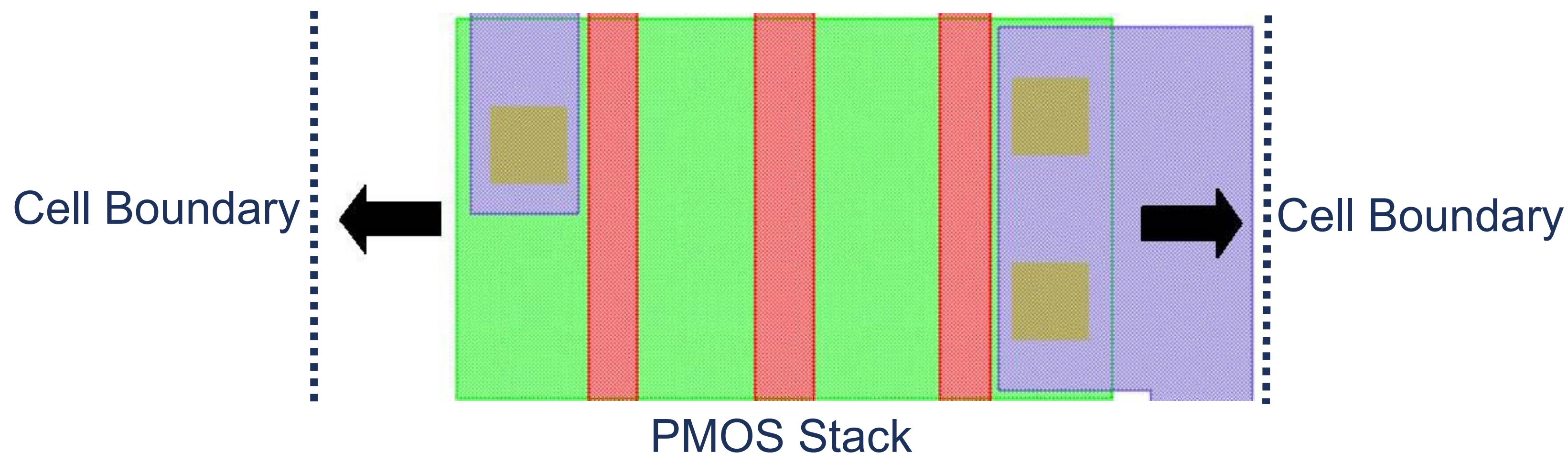
- 5% performance increase for 1.5X leakage increase
- Less sensitive than PMOS
  - Increasing only longitudinal nitride stress
  - Moving away STI, not as effective as eSiGe increase
- Contact placement becomes more important
  - No contact – 2% higher Ion



Layout Guideline 1

"Increase the active area in a given cell to fill up the entire cell width while obeying DRC rules"

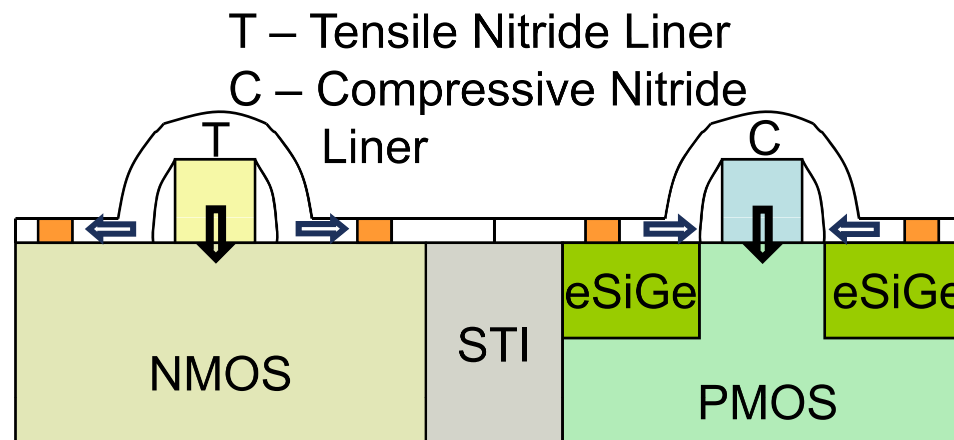
- Most readily applied to compact pull-up and pull-down networks
  - Ex: PMOS stack in NOR, NMOS in NAND
- Increases S/D capacitance – apply to cells with larger output loading
- Can apply to cells to create slightly larger high performance versions



Layout Guideline 2

"Move contacts away from gate polysilicon as much as possible"

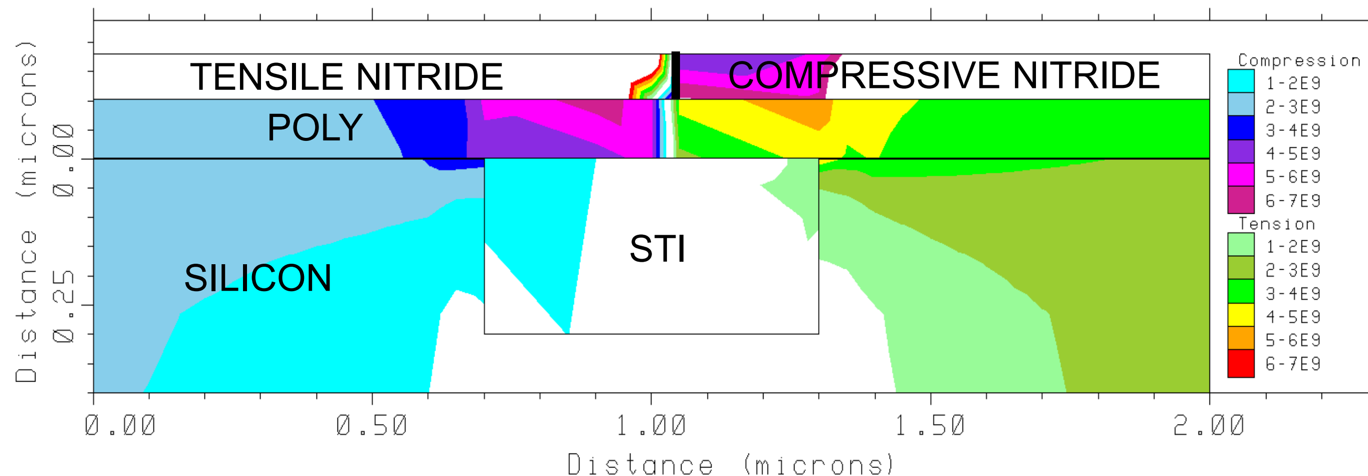
- Nitride transfers stress in two ways: vertically through the gate, longitudinally
- Increases longitudinal component
- Limited improvement – due to increasing only one component
- Increases S/D resistance - typically very small increase (<5Ω)



Layout Guideline 3

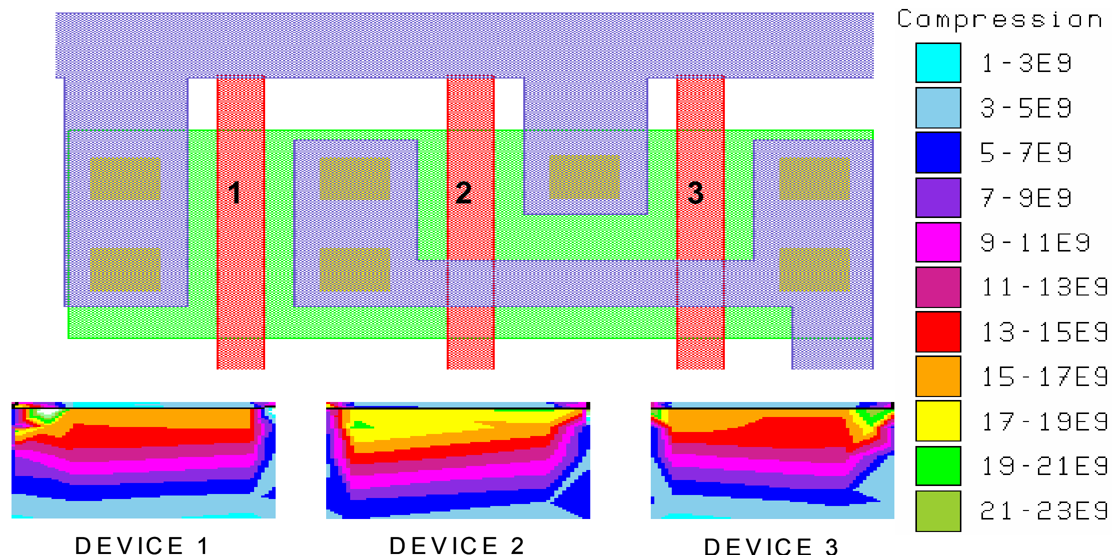
"In the lateral direction, move PMOS closer to tensile/compressive nitride interface and NMOS away from it"

- Curious behavior at interface – compressive stress under tensile nitride and vice versa
- Both NMOS and PMOS need tensile stress in this direction
- Space readily available for transistors with smaller widths
  - Ex: X1 variants of various gates



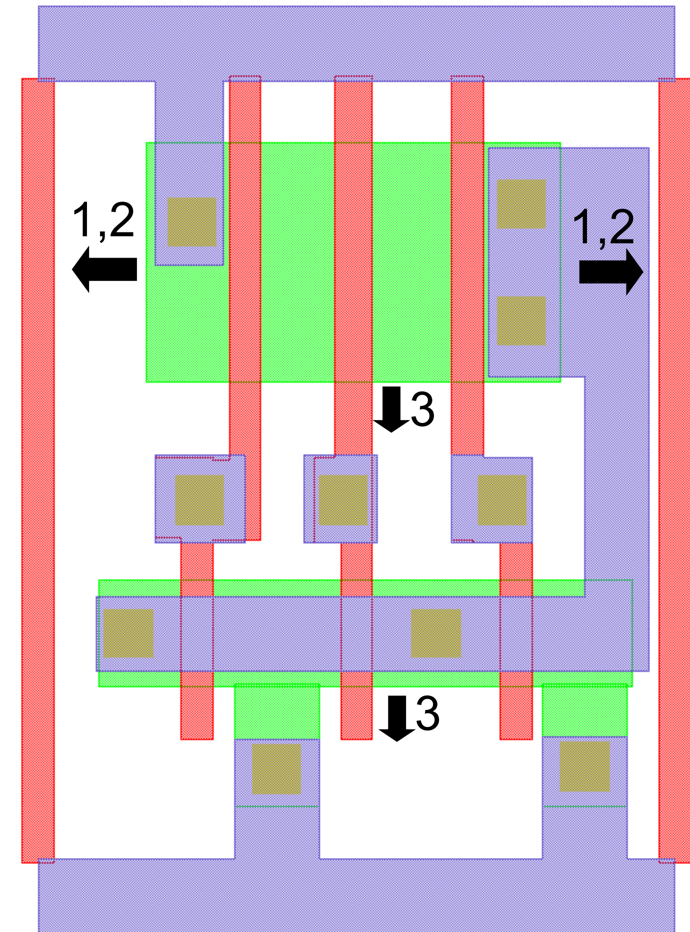
Position Dependence of Stress

- “Center” devices in denser layouts have higher channel stress
- NMOS: STI pushed away
- PMOS: more eSiGe, more stress, as SiGe has higher contribution as compared to STI
- Can result in design issues, noise margin degradation, speed issues for certain dynamic circuits, etc.



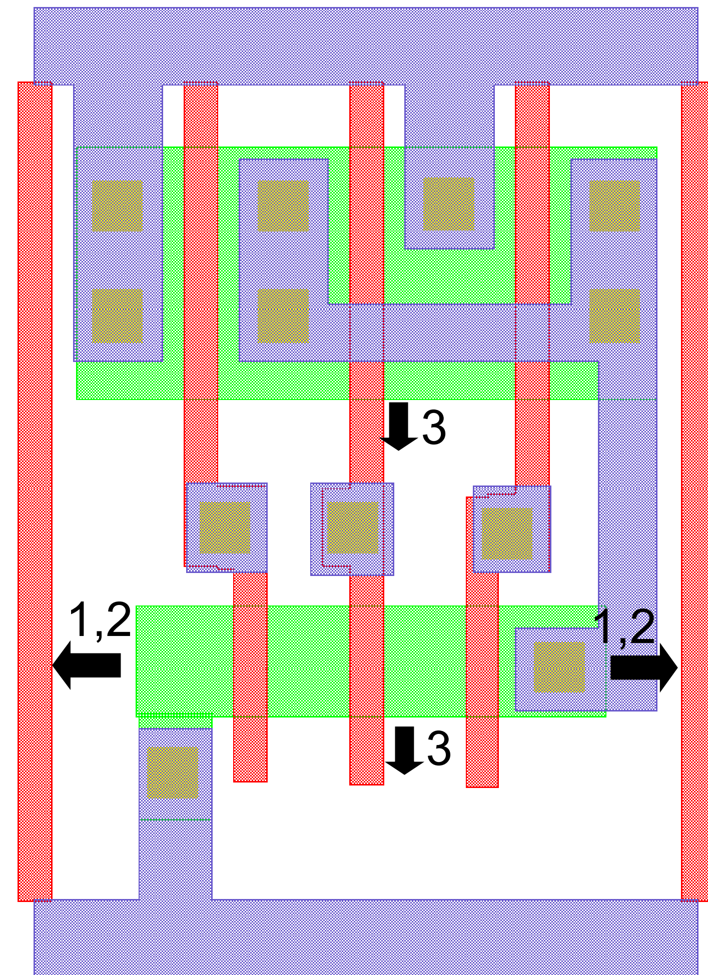
Applying guidelines to a 3 Input NOR

- Apply guideline 1 - ~22% increase in PMOS active area
- Apply guideline 2 – Move contacts away from PMOS after increasing active area
- Apply guideline 3 – move PMOS and NMOS as shown
- Drive current enhancement - ~13.5% for PMOS, ~3% for NMOS



Applying guidelines to a 3 Input NAND

- Apply guideline 1 - ~20% increase in NMOS active area
- Apply guideline 2 – Move contacts away from NMOS after increasing active area
- Apply guideline 3 – move PMOS and NMOS as shown
- Drive current enhancement - ~1.5% for PMOS, ~7% for NMOS
- Lower improvements because nitride transfers stress vertically and longitudinally



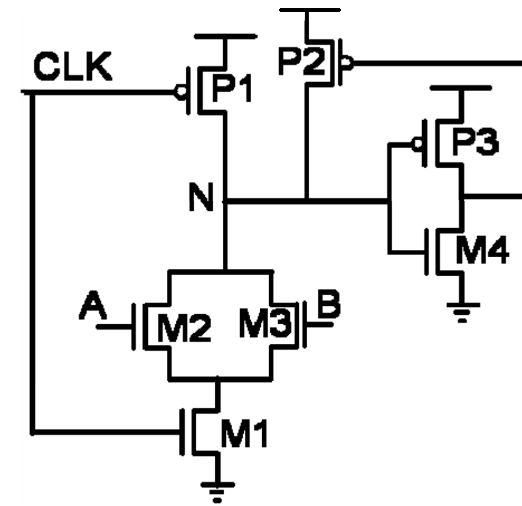
Results

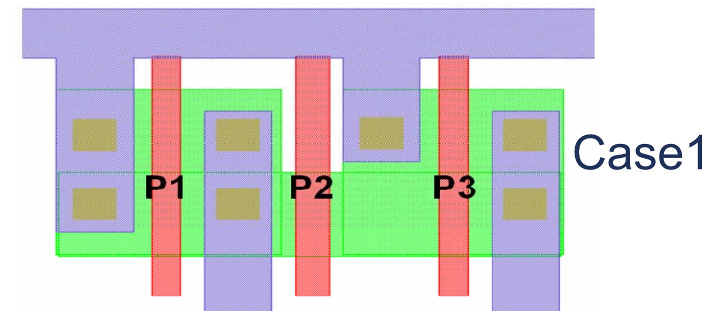
Cell	Stress-based drive current improvement		Stress-based leakage increase		V_{th}-based leakage increase for same performance gain		Capacitance increase (FO4 loading)
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	
NOR3	3%	13.5%	1.22X	4.02X	1.31X	9.20X	2.74%
NOR2	3%	7.5%	1.22X	2.24X	1.31X	3.52X	1.92%
NAND3	7%	1.5%	1.98X	1.10X	2.36X	1.53X	1.85%
NAND2	4.5%	1.5%	1.45X	1.10X	1.68X	1.53X	1.30%

- Very small increase in capacitance due to the application of guideline 1 (<2.74%)
- Lower leakage vs. V_{th} reduction – advantage is more pronounced for larger delay improvements
- Better improvements for 3-input gates than 2-input gates (larger scope for applying guideline 1)

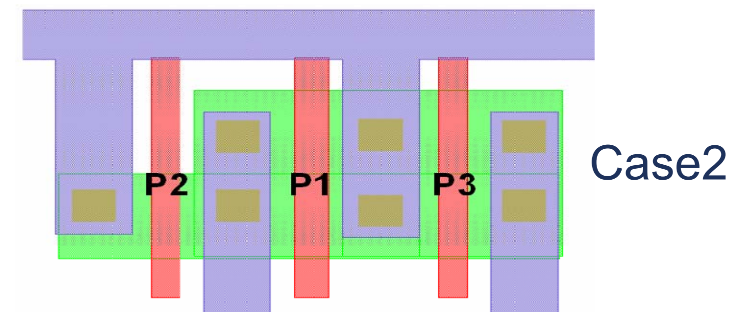
Position Dependence - Example

- Domino implementation of 2-in OR
- Two different layout positions for P2 (keeper)
- 8% difference in drive current for the two configurations
- Keeper fights evaluate tree – performance loss for Case 1
- Time to discharge N increases by 12% in Case 1
- Performance loss can worsen for more aggressively sized circuits





Case1



Case2

Conclusions and Future Work

- We propose standard cell layout guidelines for optimizing stress-based performance enhancement
- Studied the dependence of stress-based improvement on layout parameters and identified key parameters
- Device performance can be improved with no area increase for most gates
- Substantial improvements for lower leakage vs. reduced V_{th}
- Ongoing and future work
  - Circuit-level, block-based, stress-enhanced optimization algorithm
  - Modeling the dependence of induced stress upon different layout parameters

Thank You