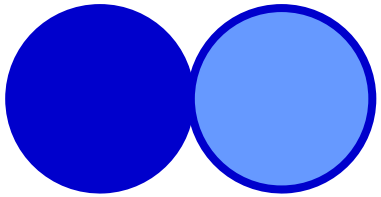
Statistical Timing Analysis Considering Spatially and Temporally Correlated Dynamic Power Supply Noise



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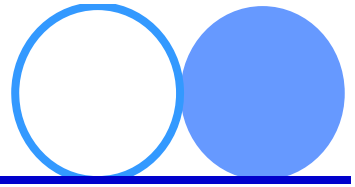
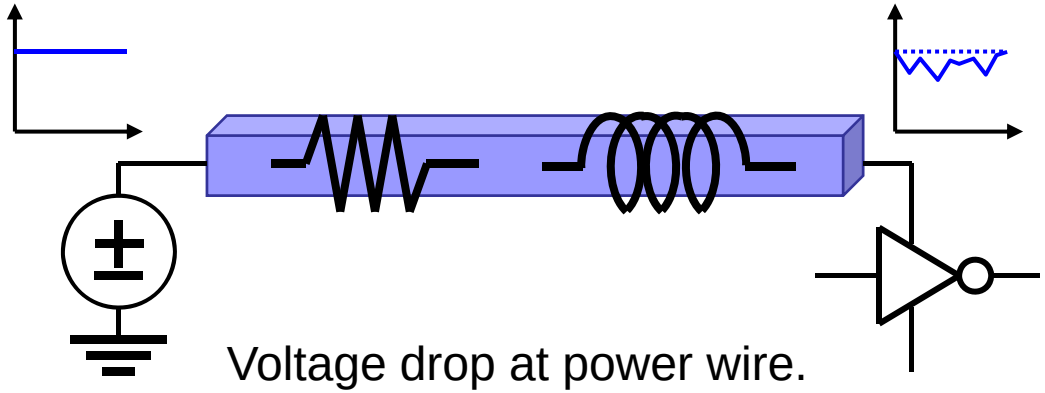
Agenda



- Background and objective
- Statistical modeling of power supply noise
- SSTA with statistical model of power supply noise
- Experimental results
- Conclusion

Background



Voltage drop at power wire.

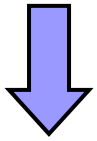
- Power supply noise is becoming more influential on timing due to
  - increasing current consumption,
  - decreasing power supply voltage.

Demand for timing analysis considering power supply noise.

Objective

- Conventional analysis method
  - Dynamic analysis
    - Analysis with test patterns.
      => Combination space of test patterns is tremendous.
  - Static analysis
    - Analysis with constant voltage drop.
      => Irrelevant voltage drop leads to optimistic or excessively pessimistic estimation.

Exact worst-case delay cannot be obtained practically.

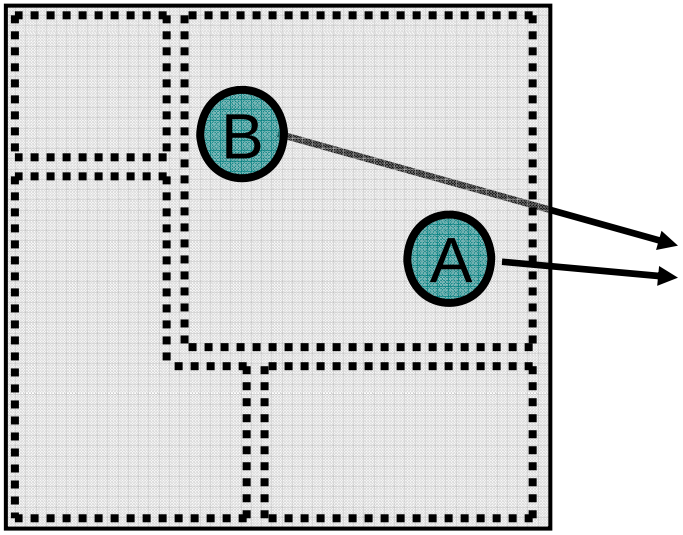


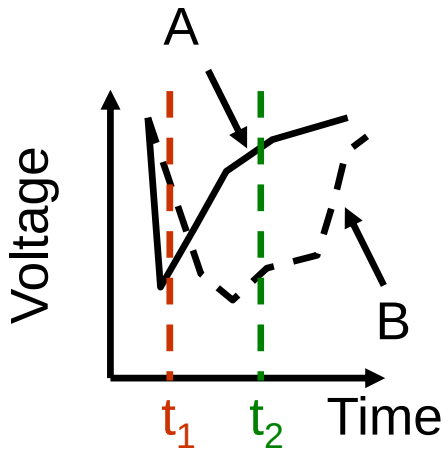
Propose a **statistical** timing analysis method that gives reasonable worst-case timing.

Difficulties of noise aware timing analysis

- Cell position (spatial)
- Switching timing (temporal)

} affect gate delay.





temporal difference

t_1: delay(A) ≫ delay(B)

t_2: delay(A) ≪ delay(B)

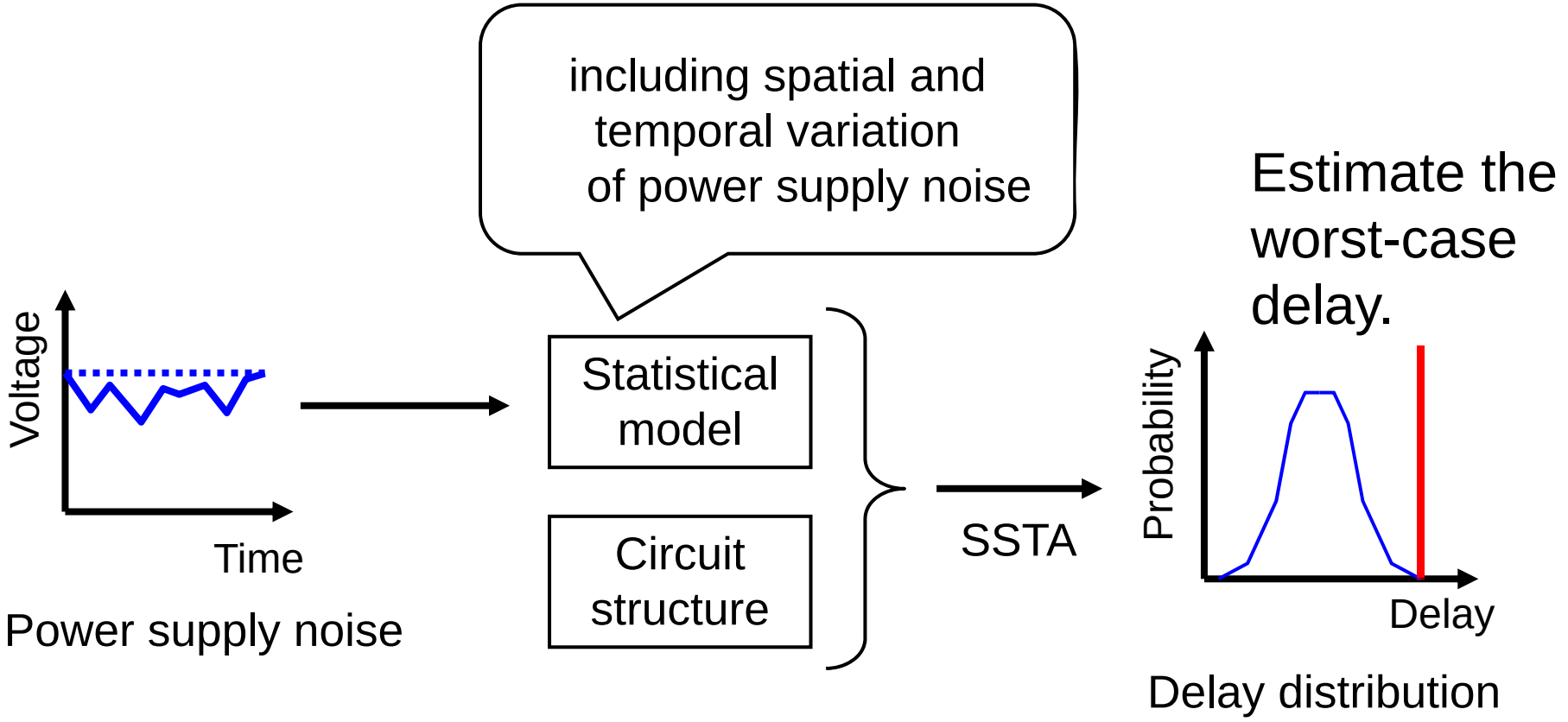
spatial difference

A: delay(t_1) > delay(t_2)

B: delay(t_1) < delay(t_2)

Position of critical paths and
spatial and temporal variation
must be considered simultaneously.

Proposed approach (Overview)



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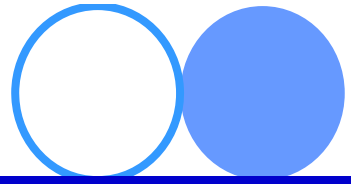

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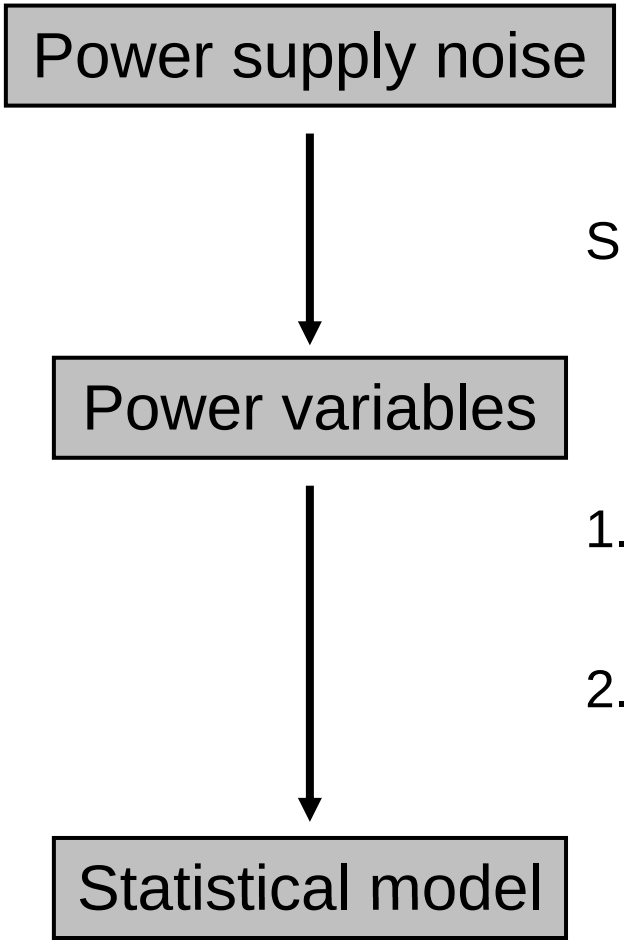
Modeling flow

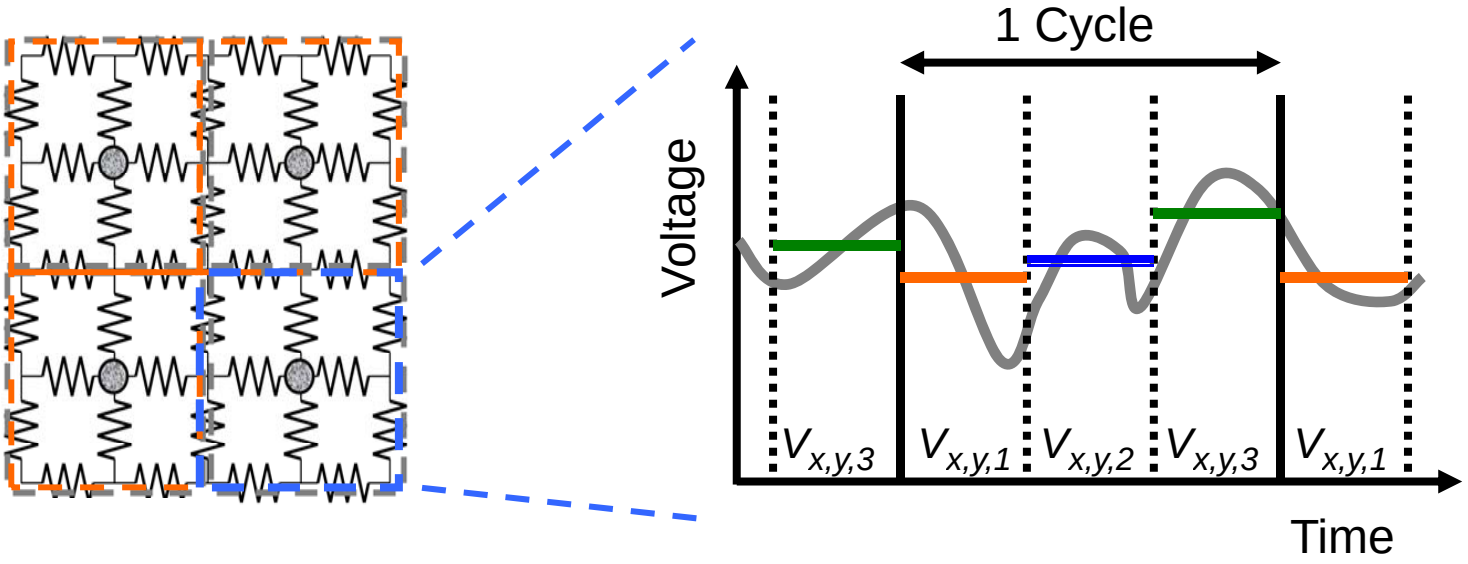


Spatial and temporal division.

1. Gaussianization: if necessary
   improve Gaussianity of the variables.
2. Orthogonalization:
   transform the correlated variables
   into the uncorrelated variables.

Spatial and temporal division

remove spatial and temporal continuity
for variable assignment



ex) divide a clock cycle into 3 time spans.

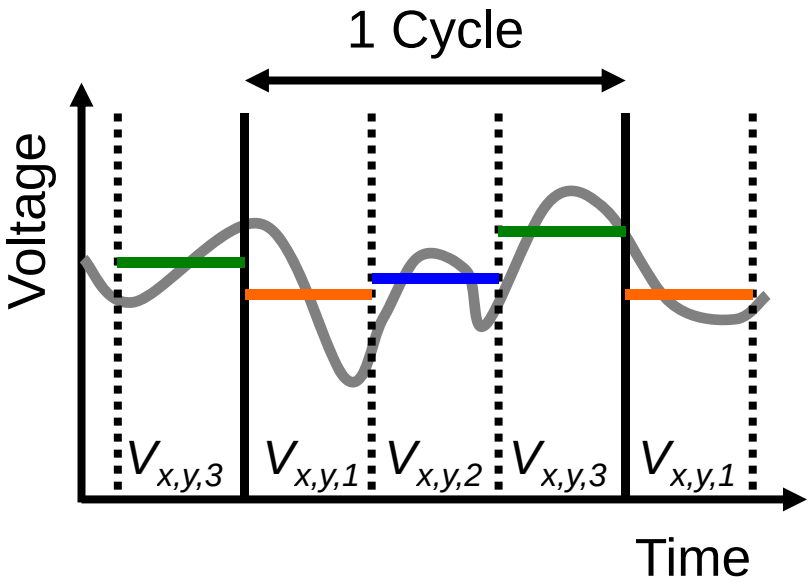
spatial division

choose a representative value for each partition.

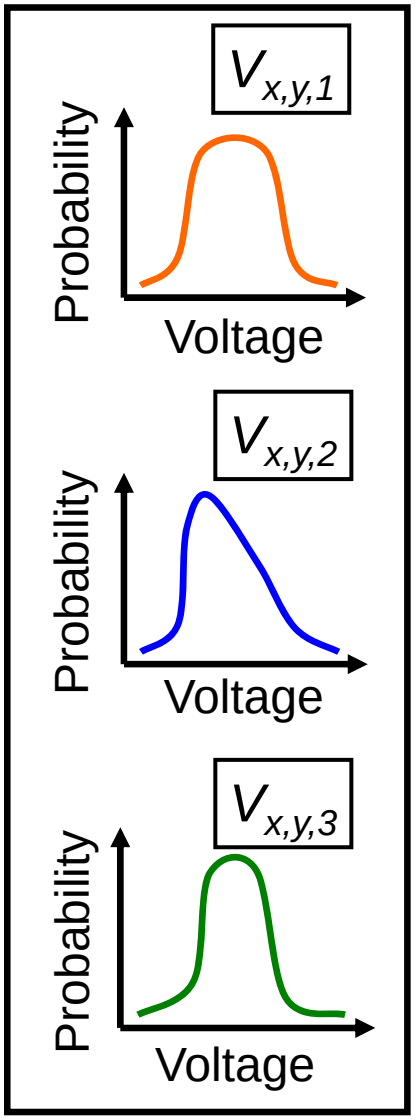
temporal division

use average voltage in each span.

Assigning variables and obtaining distribution



different clock cycle
=> different sample

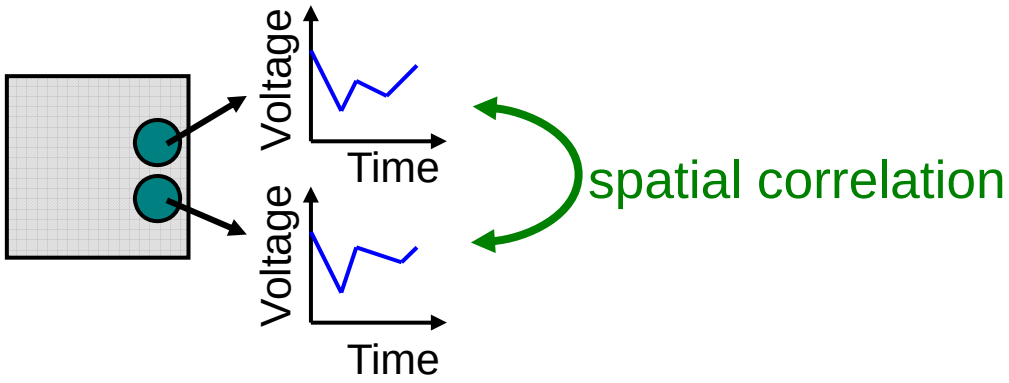


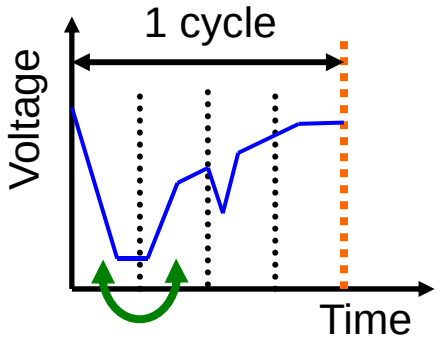
Data set of power variables

calculate average, standard deviation and correlation coefficient

can model spatial and temporal variation.

Correlation of power variables

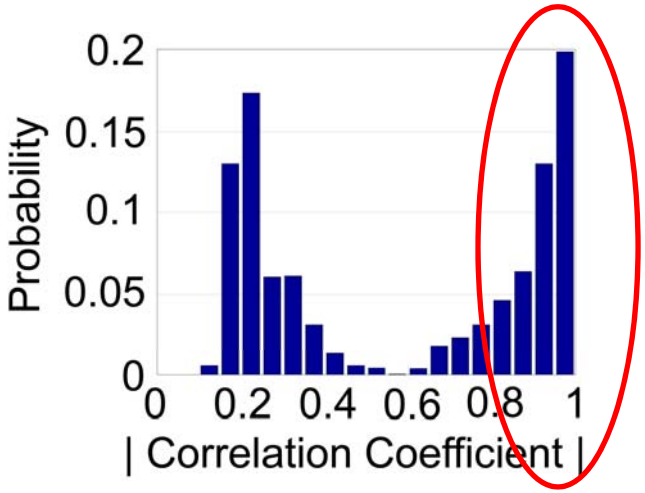




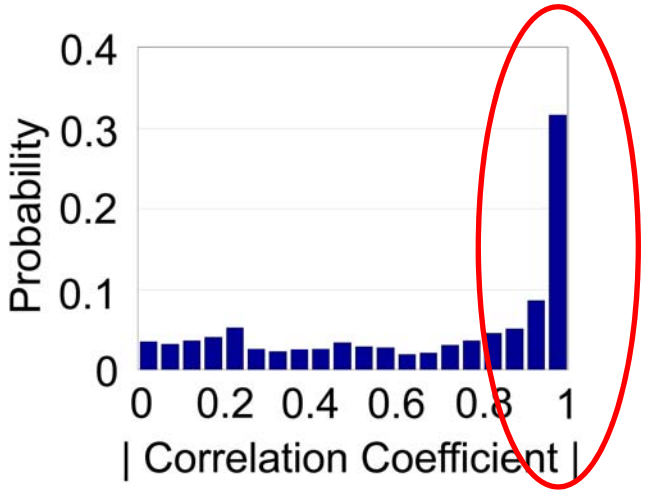
temporal correlation

Voltage drop tends to be similar.

Voltage drop lasts awhile.



spatial correlation



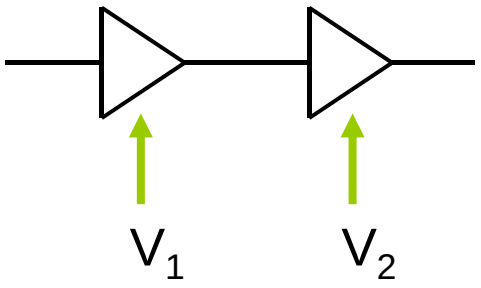
temporal correlation

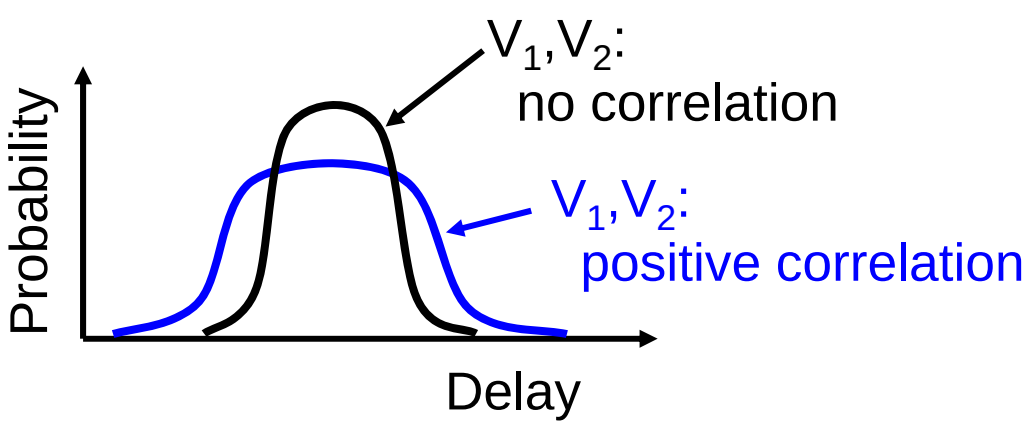
Correlation of power variables is strong.

Correlation's effect on delay

Correlation between variables affects delay distribution.

ex) SUM operation





Delay calculation considering correlation is inevitable.

⇕

Computationally expensive.

Orthogonalization

- Orthogonalization by principal component analysis (PCA)
  - Delay calculation considering correlation is facilitated [1].
  - Compact statistical model is derived when strong correlation exists.
  - Compatibility with SSTA developed for manufacturing variability [1].

$$z_i = \mu_i + \left(\sum_{j=1}^{k} \sqrt{\lambda_j} e_{ij} pc_j \right) \sigma_i$$

$$\approx \mu_i + \left(\sum_{j=1}^{k'} \sqrt{\lambda_j} e_{ij} pc_j \right) \sigma_i \quad \text{(compact, } k' \ll k\text{)}$$

- z_i : original variable
- μ_i : average of z_i
- σ_i : standard deviation of z_i
- λ_j : jth largest eigenvalue
- e_{ij} : jth eigenvector corresponding to z_i
- pc_j : jth principal component (PC)
- k, k' : number of PCs

[1] H. Chang, et. al., "Statistical Timing Analysis Under Spatial Correlations," *IEEE TCAD*, Vol. 24, No. 9, Sep. 2005.

Gaussianization

PCA assumes Gaussian distribution.

⇔ Some variables might be different from Gaussian.

⇩

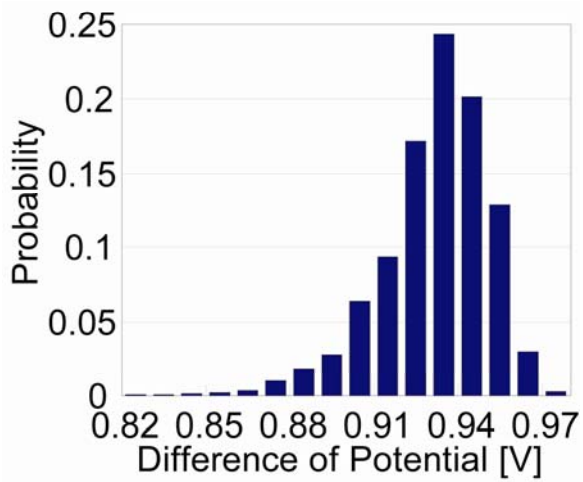
improve Gaussianity of the variables before PCA.

Box-Cox transformation

$$z' = \begin{cases} \frac{z^{\Lambda}-1}{\Lambda} & (\Lambda \neq 0) \\ \log(z) & (\Lambda = 0) \end{cases}$$

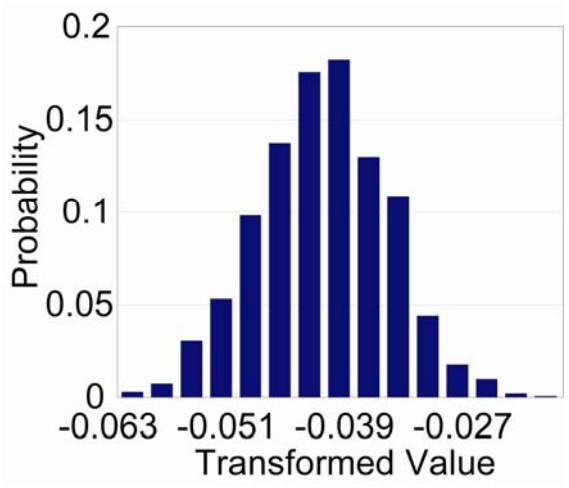
Λ: Every variable has the optimum value individually.

original distribution



Box-Cox transformation

transformed distribution



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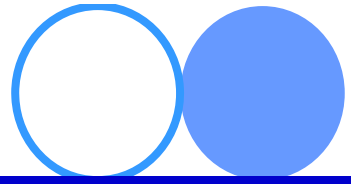

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Gate delay calculation

canonical gate delay model
considering power supply noise.

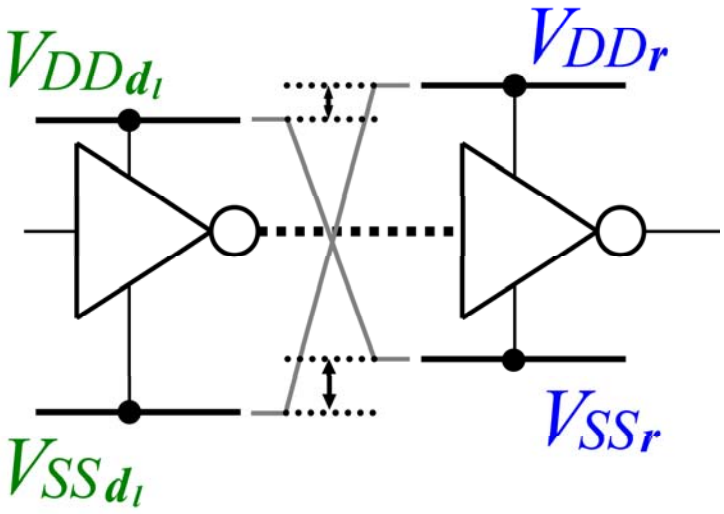
$$d_r = \mu_r + \sum_{j=1}^{k'} \sqrt{\lambda_j} A_{r,j} pc_j$$

$$A_{r,j} = \sigma_{V_{\mathrm{DD}r}} \frac{\partial d_r}{\partial V_{\mathrm{DD}r}} e_{(V_{\mathrm{DD}r}),j} + \sigma_{V_{\mathrm{SS}r}} \frac{\partial d_r}{\partial V_{\mathrm{SS}r}} e_{(V_{\mathrm{SS}r}),j}$$

receiver side

$$+ \sum_l \left(\sigma_{V_{\mathrm{DD}d_l}} \frac{\partial d_r}{\partial V_{\mathrm{DD}d_l}} e_{(V_{\mathrm{DD}d_l}),j} + \sigma_{V_{\mathrm{SS}d_l}} \frac{\partial d_r}{\partial V_{\mathrm{SS}d_l}} e_{(V_{\mathrm{SS}d_l}),j} \right)$$

driver side



$\sigma_{V^{**}}$: standard deviation of V^{**}

$\frac{\partial d*}{\partial V**}$: sensitivity of V^{**} to d^*

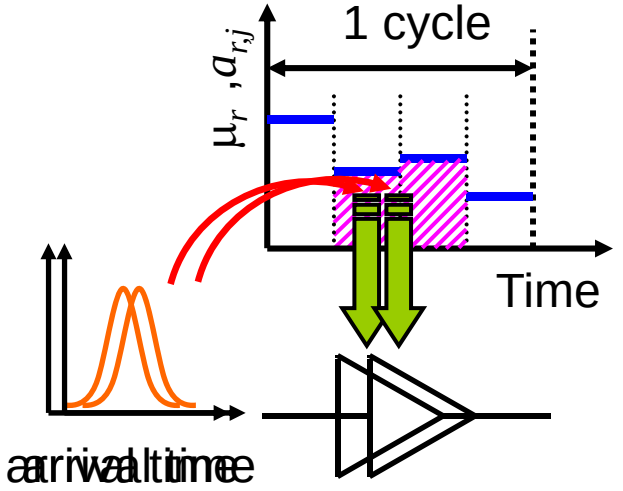
$e_{(V^{**}),j}$: jth eigenvector corresponding to V^{**}

How are these parameters(μ_r, $A_{r,j}$) decided?

Parameter calculation

- Parameters of canonical delay model must consider not only cell position but also switching timing,
  - Parameters are set based on arrival time.

If switching timing crosses over the boundary of two time spans.
=> calculate weighted-average of two spans.



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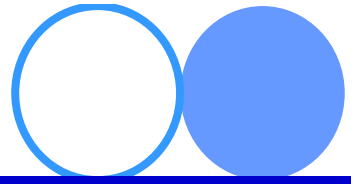

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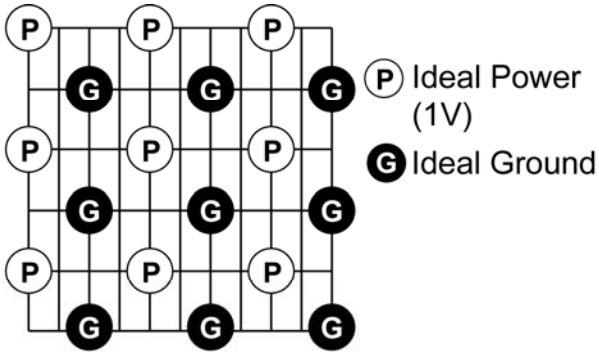
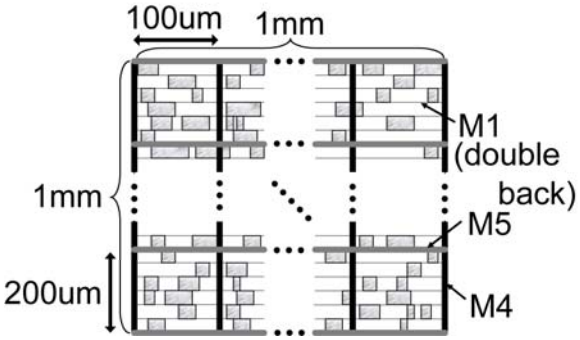
  - Accuracy of proposed SSTA
  - SSTA with reduced model
  - SSTA considering power supply noise and manufacturing variability
- Conclusion

Experimental conditions

- noise generators,
  - two circuits,
    - FPU[2] (90nm process, 39k gates),
    - tiny64 processor[2] (90nm process, 20k gates),
  - size: 1mm x 1mm,
  - input vector: random, 2000 clock cycles,
- circuits for timing analysis,
  - ISCAS85 (5 circuits),
  - 64-bit multiplier,
  - ALU,
  - H-tree (evaluation of clock jitter),

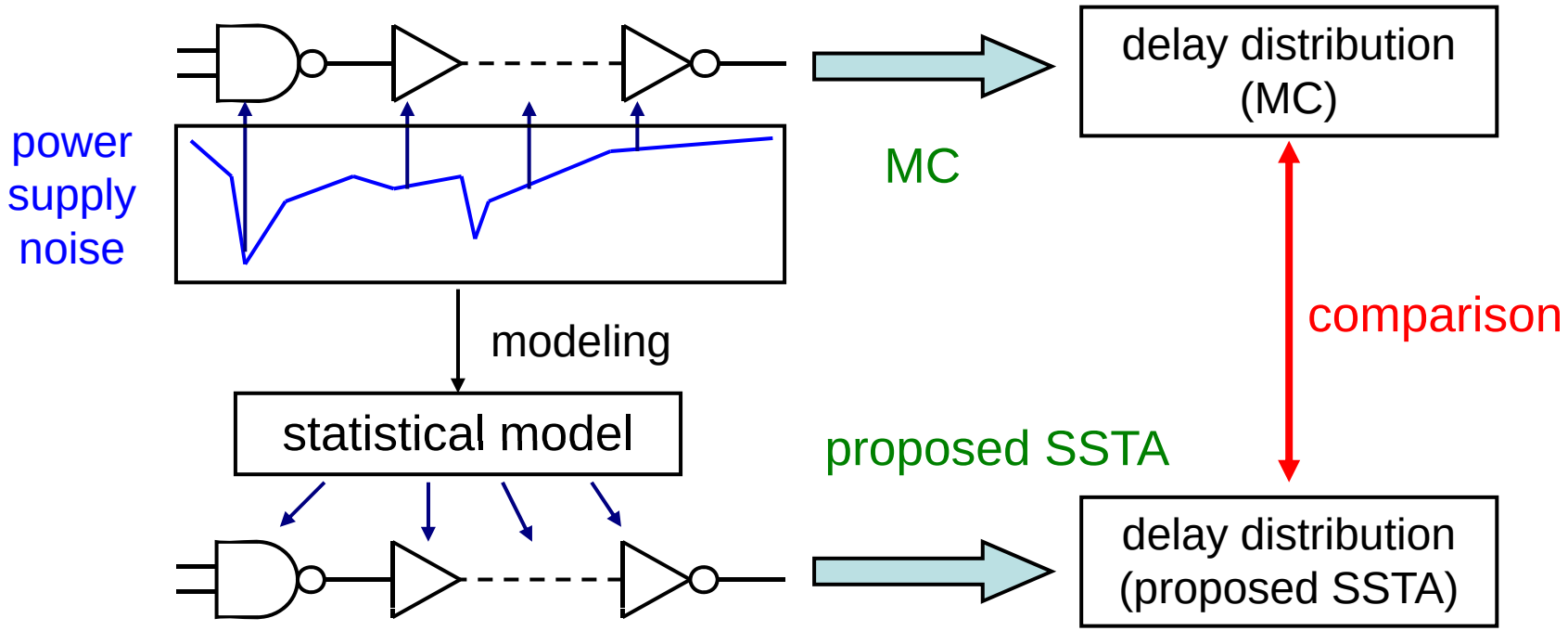




[2] OPENCORES.ORG, http://www.opencores.org/.

Procedure of accuracy evaluation

compare proposed SSTA and Monte Carlo STA (MC) using the same noise information given to PCA.



- SSTA includes errors that originate from
  - discretization,
  - PCA for incomplete Gaussian distribution,
  - SSTA operation.

Accuracy of proposed SSTA

circuit	# cells	$\frac{\lvert SSTA - MC \rvert}{MC}$	
		avg (%)	sd (%)
c432	232	0.478	4.21
c1355	329	1.27	29.4
c1908	387	0.472	24.1
c6288	3382	0.370	9.15
c7552	2070	0.172	13.8
multiplier	41629	0.0969	7.23
ALU	14655	0.216	2.87
H-tree	7	0.576	10.8
average	-	0.456	12.7

noise generator: FPU
spatial division number: 10x10
temporal division number: 10

- Proposed SSTA estimates the delay accurately.
- Estimation errors without Box-Cox transformation (avg: 0.465%, sd: 14.4%), => non-Gaussianity was not significant but Box-Cox transformation improved results slightly.

Evaluation of variable reduction

Evaluate accuracy and CPU time with
the reduced number of principal components (PCs).

noise generator: tiny64 circuit: multiplier

spatial division number: 10x10 temporal division number: 10
=> total 2000 variables (power + ground) @ Opteron 2.4GHz

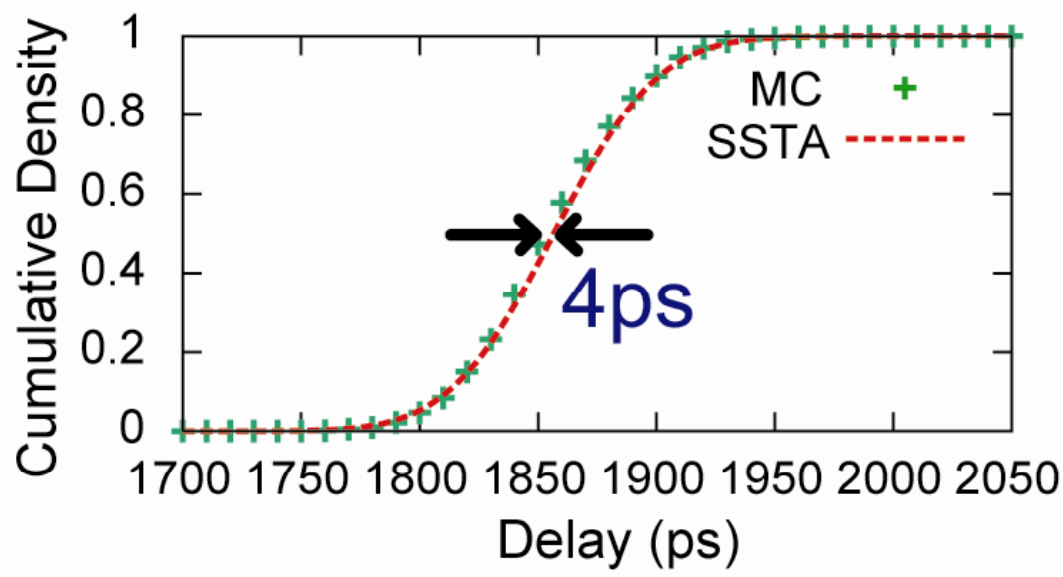
PCs reduction

# PCs	avg (ps)	sd (ps)	CPU time (ms)	reduction rate of CPU time (%)
1	1843	0.384	164	98.6
2	2708	3.16	166	98.6
4	2708	3.71	180	98.5
8	2708	4.07	205	98.3
16	2708	4.09	238	98.0
2000	2708	4.09	11800	0

reduce CPU time largely with little loss of accuracy.

SSTA result both for power supply noise and manufacturing variability

Proposed SSTA has a compatibility with SSTA developed for manufacturing variability.
=> can perform SSTA considering manufacturing and supply voltage fluctuation simultaneously.



noise generator: FPU
circuit: multiplier
spatial division number: 10x10
temporal division number: 10
Vth variation: σ = 25mv

SSTA considering both variabilities has a possibility to reduce timing margin.

Conclusion

- Proposed SSTA can consider dynamic power supply noise with PCA.
  - Errors of proposed SSTA
    - average: 0.456%,
    - standard deviation: 12.7%.
  - SSTA with the partial model reduced CPU time more than 98% almost without loss of accuracy.
  - Proposed SSTA can be performed considering manufacturing and supply voltage fluctuation simultaneously.

Calculation with switching transition

calculate weighted-average of the parameters corresponding to input and output transition timing.

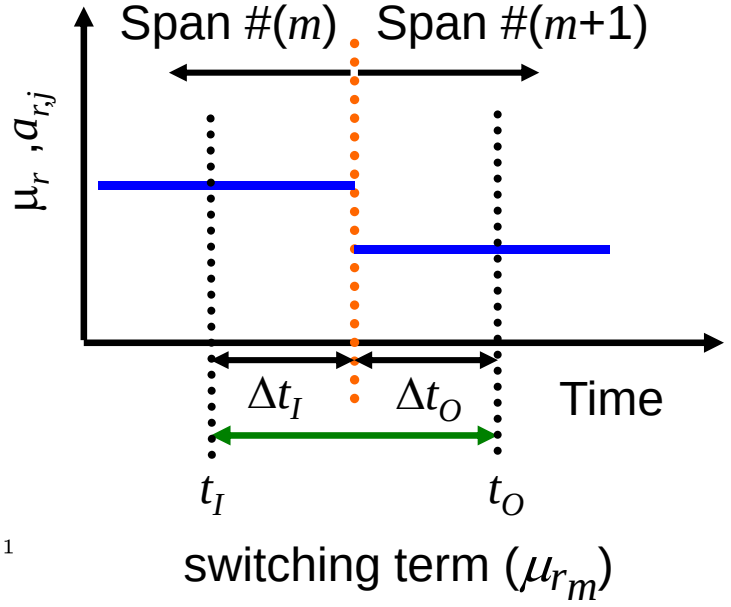
1. estimate t_O with the use of μ_{r_m}.

$$t_O = t_I + \mu_{r_m}$$
$$(\Delta t_I + \Delta t_O = \mu_{r_m})$$

2. calculate weighted-average based on Δt_I and Δt_O .

average $$\mu'_r = \frac{\Delta t_I}{\Delta t_I + \Delta t_O}\mu_{r_m} + \frac{\Delta t_O}{\Delta t_I + \Delta t_O}\mu_{r_{m+1}}$$

coefficient $$a'_{r,j} = \frac{\Delta t_I}{\Delta t_O + \Delta t_O}a_{r_m,j} + \frac{\Delta t_O}{\Delta t_I + \Delta t_O}a_{r_{m+1},j}$$



switching term (μ_{r_m})

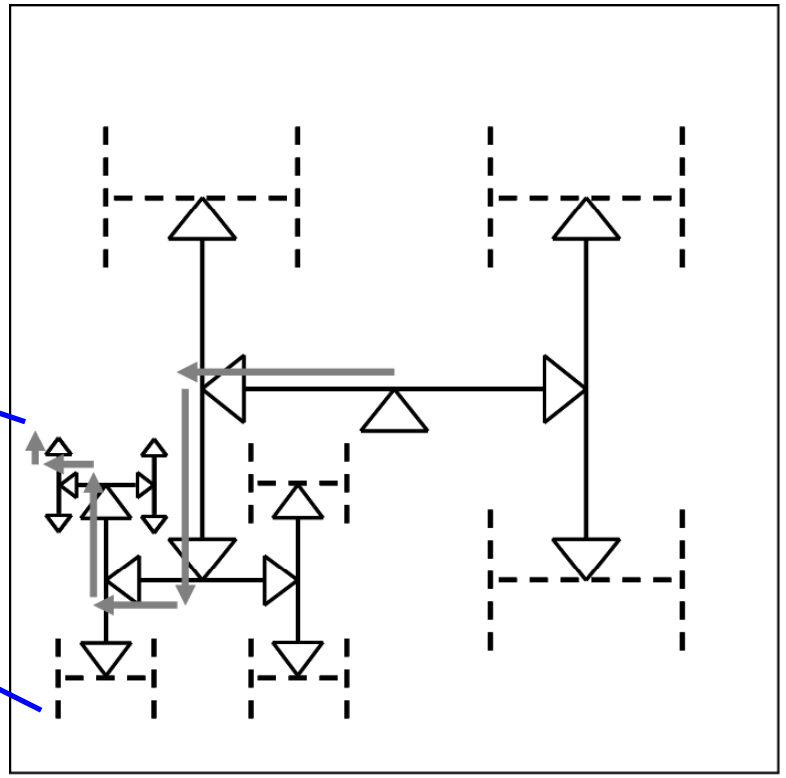
Circuit delay is calculated according to conventional SSTA.

Clock Skew Analysis

Easily perform
by application of
clock jitter analysis.

$$jitter_1 = \mu_1 + \sum_{j=1}^{k'} a_{1,j}\, pc_j$$

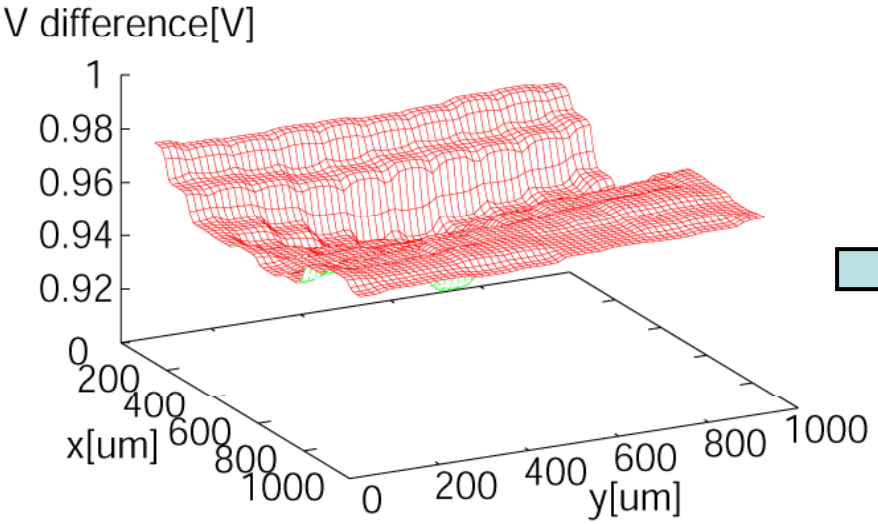
$$jitter_2 = \mu_2 + \sum_{j=1}^{k'} a_{2,j}\, pc_j$$



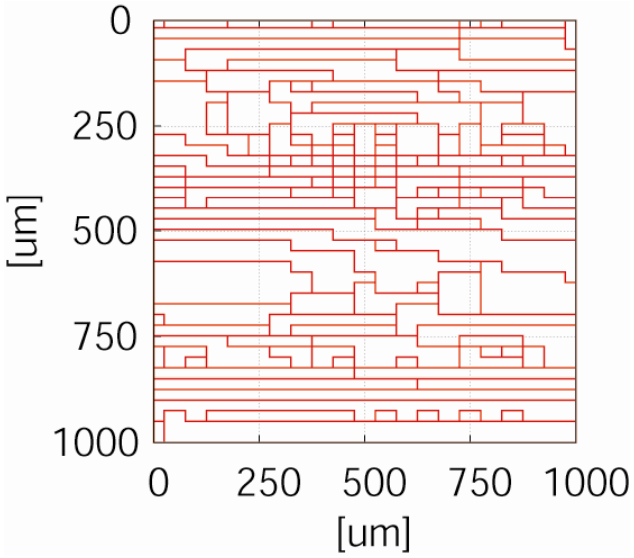
$$skew_{1,2} = (\mu_1 - \mu_2) + \left\{ \sum_{j=1}^{k'} (a_{1,j} - a_{2,j}) pc_j \right\}$$

Adaptive spatial discretization

Power supply noise has
- heavily fluctuating area.
  - => fine division
- calm area.
  - => coarse division



Spatial distribution of FPU noise (average).



Adaptive discretization of FPU noise.