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Fast Interconnect Synthesis with Layer Assignment

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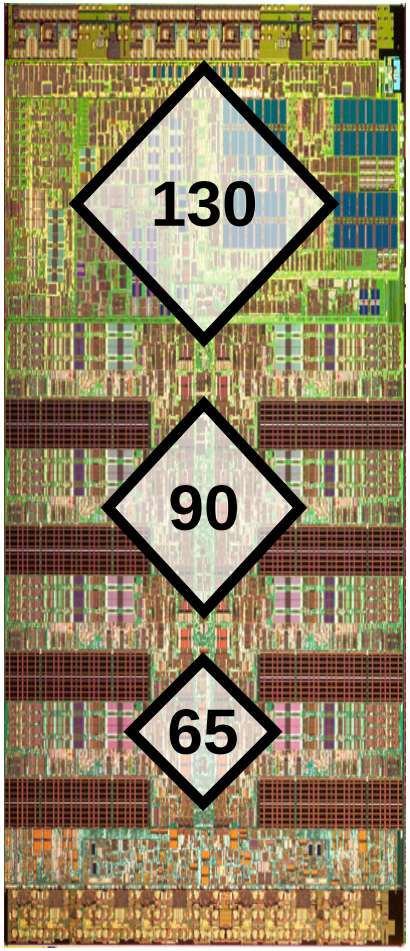
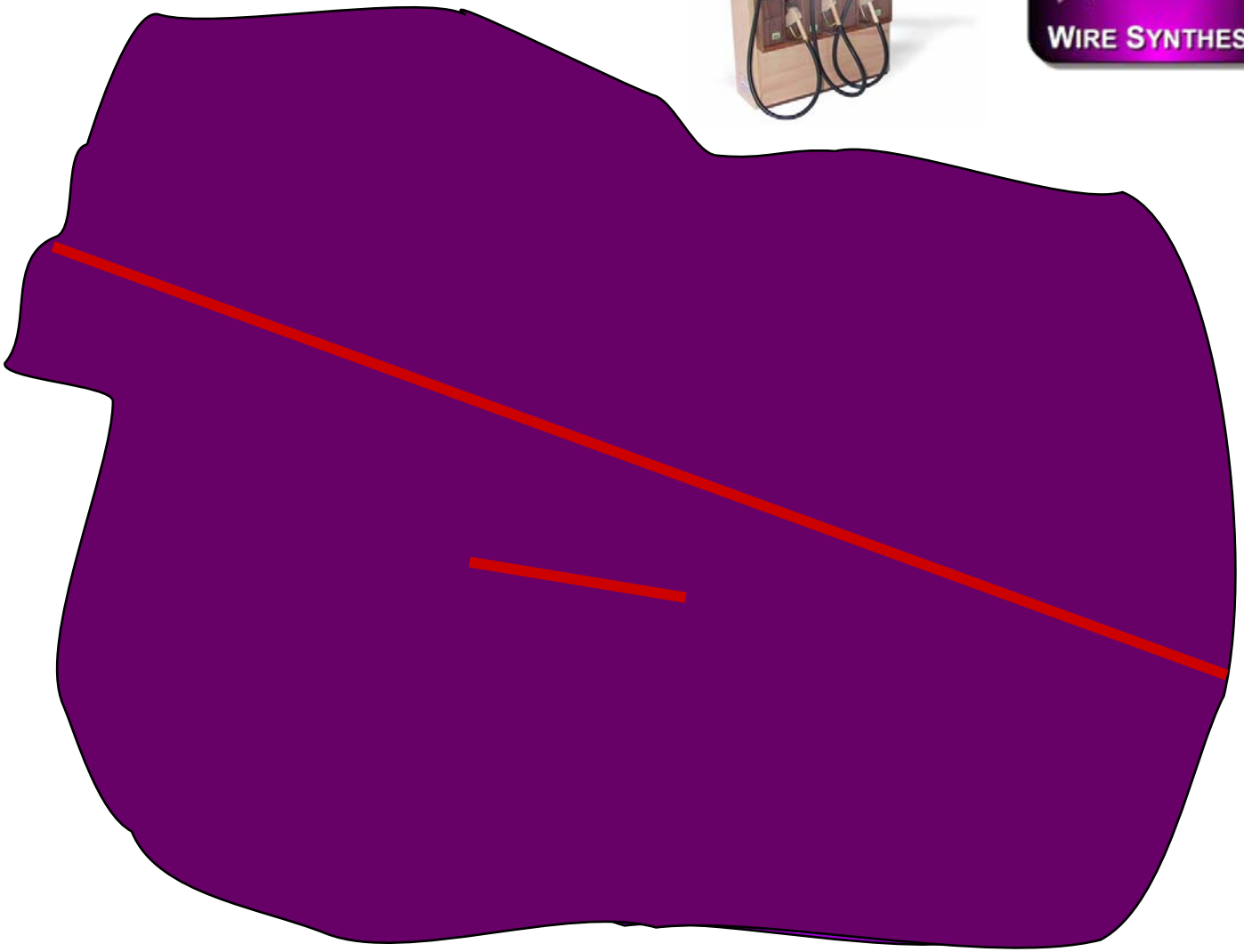
Extending the Driving Analogy





Fat Metal Wires Are Freeway Overpasses

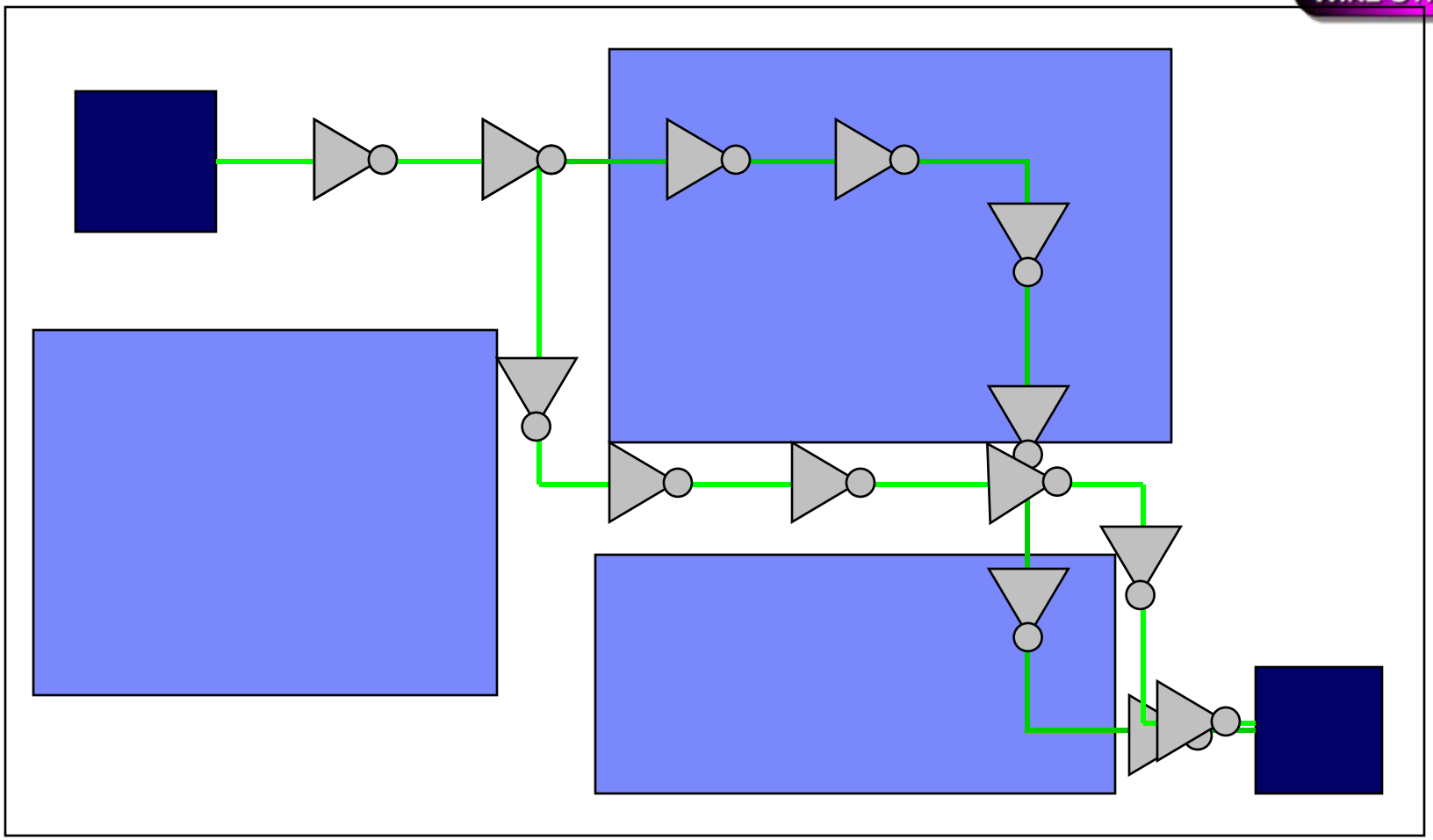
In Summary . . .

- **Advancing technology == period of city expansion**
- **More transistors == bigger city**
- **Latches == gas stations**
- **Streets == interconnect**
  - Local streets == thin metal wires
  - Freeways == fat metal wires
- **Time to cross city == time of flight on cross chip wire**

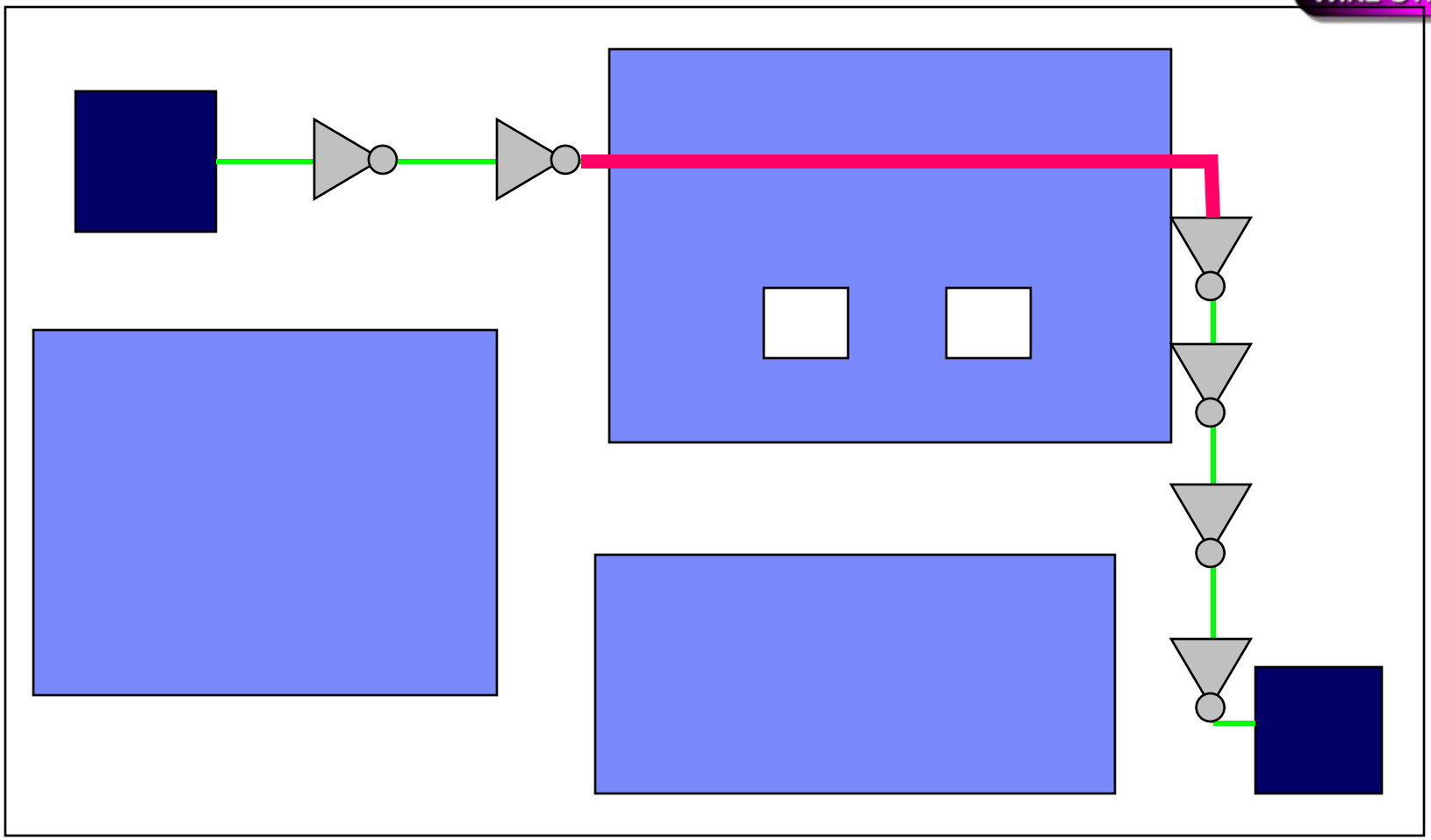
Like all analogies, this one eventually breaks down.

David Letterman

What is Wire (Interconnect) Synthesis?



What Does Wire Synthesis Really Mean?



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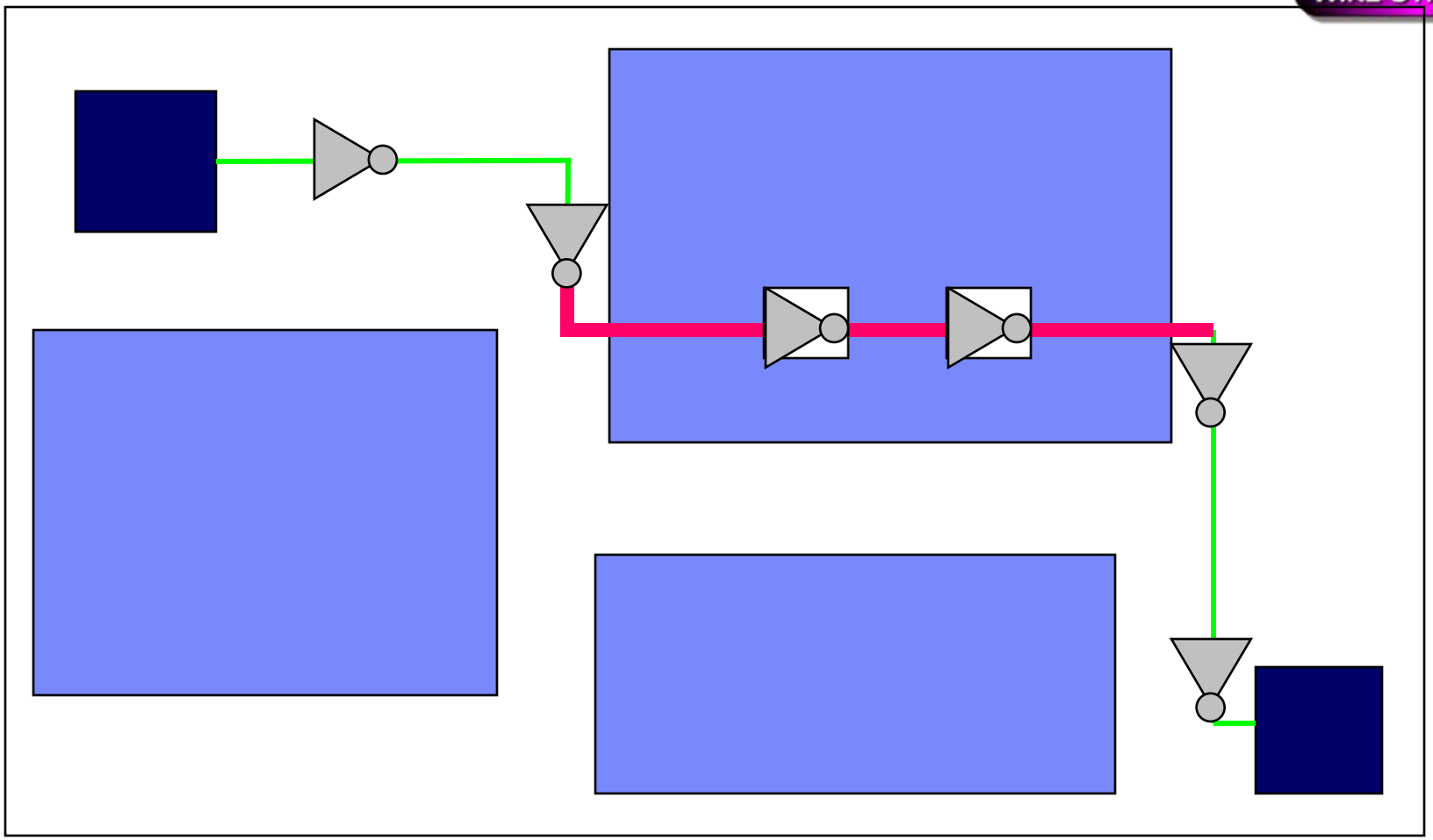
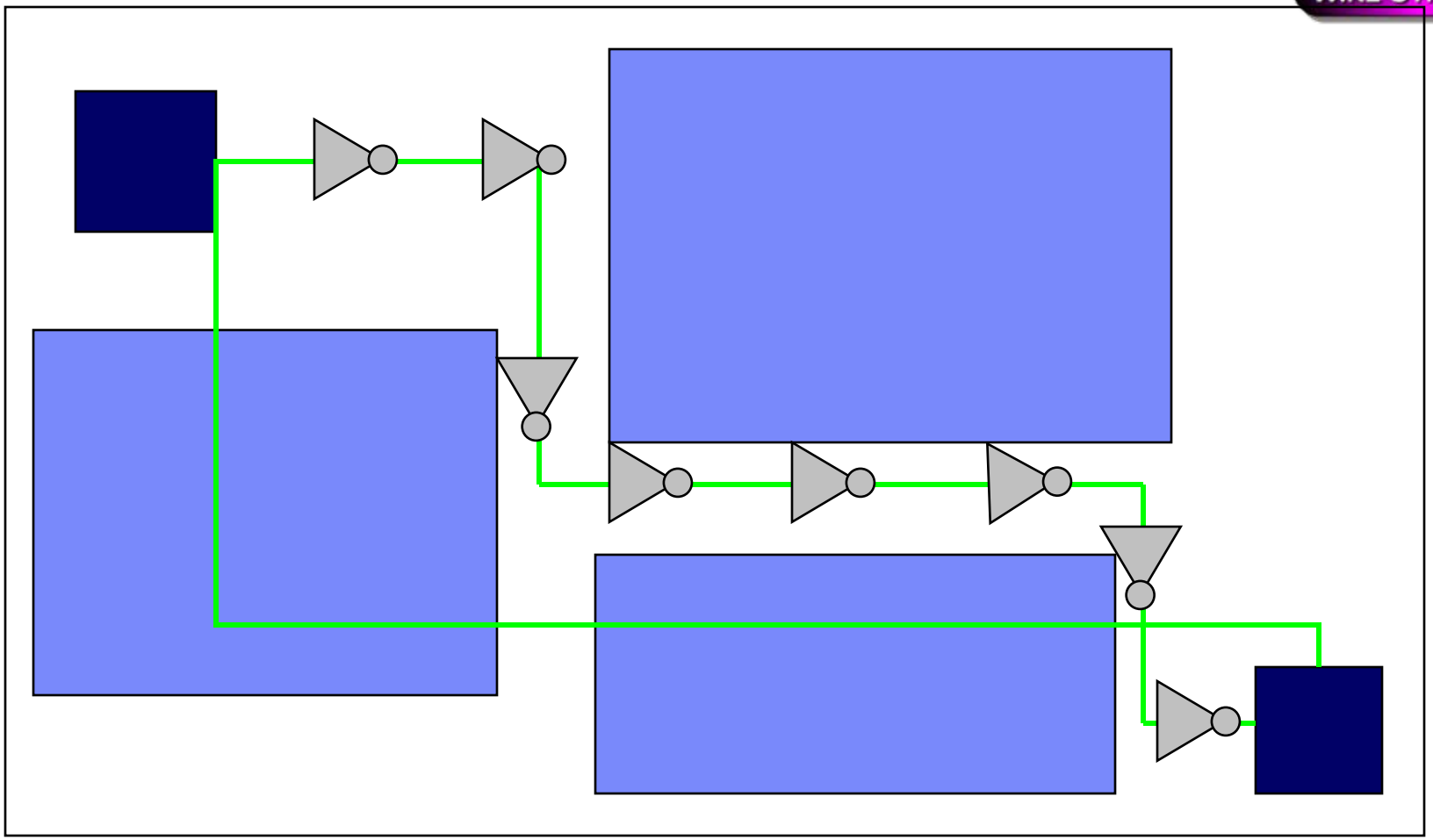


WIRE SYNTHESIS

Buffering Restricts Global Routing

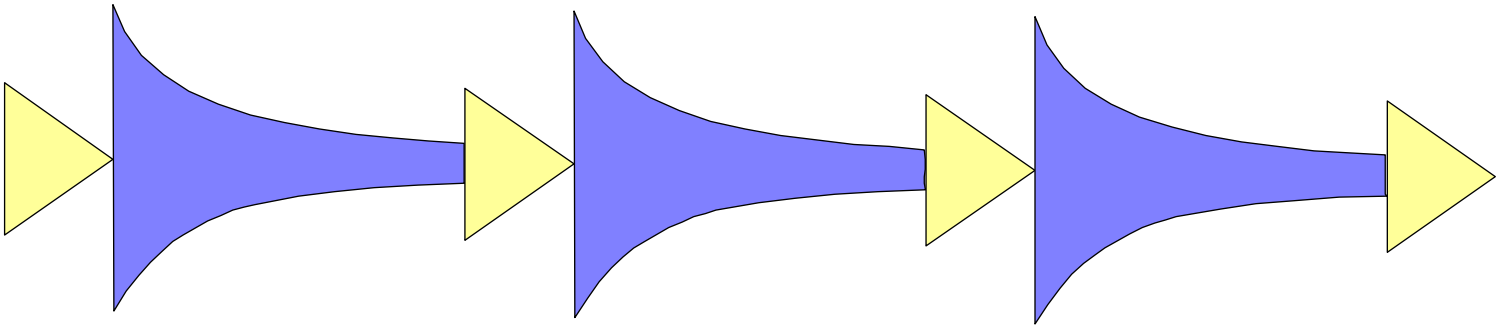


Wire Synthesis Definition for a Single Net

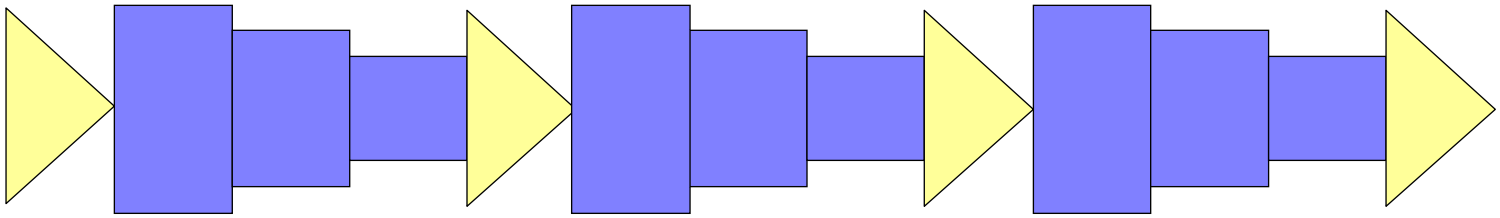
- **Global route of the net**
- **Size / locations of buffers/inverters**
- **Wire widths / layer assignments of sub-nets**
- **Environmental Awareness**
  - Blockages
  - Holes
  - Local placement congestion
  - Local routing congestion

Wire Synthesis in the 1990s

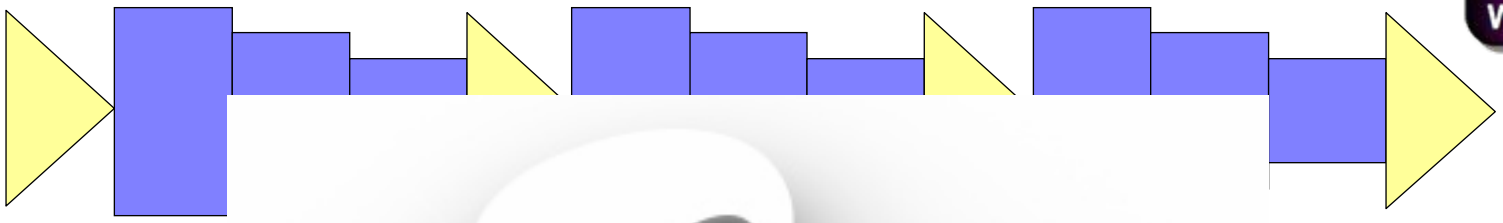
Optimal Wire Shape



Simultaneous Buffering and Wire Tapering



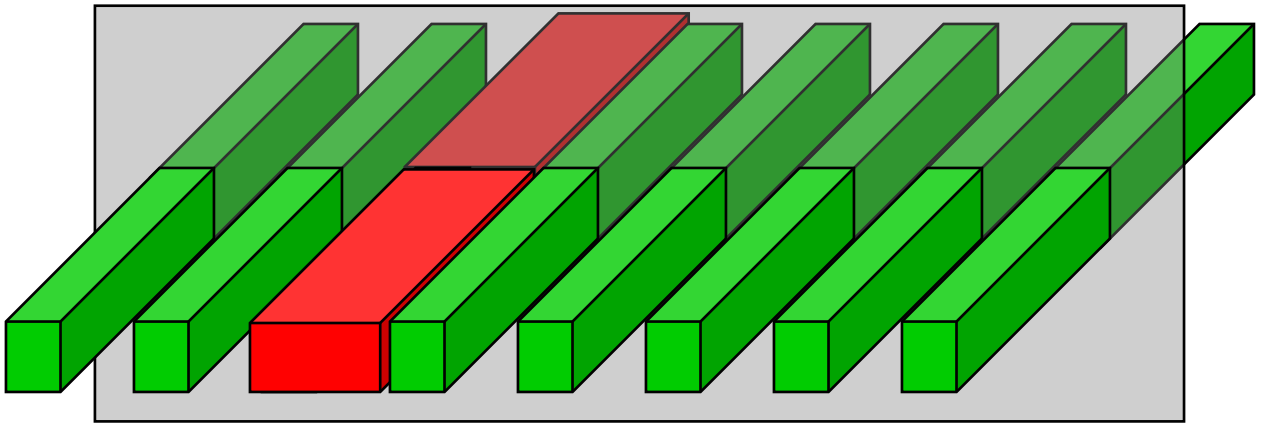
Was Wire Tapering Worthwhile?



- Route well if at all
- Even

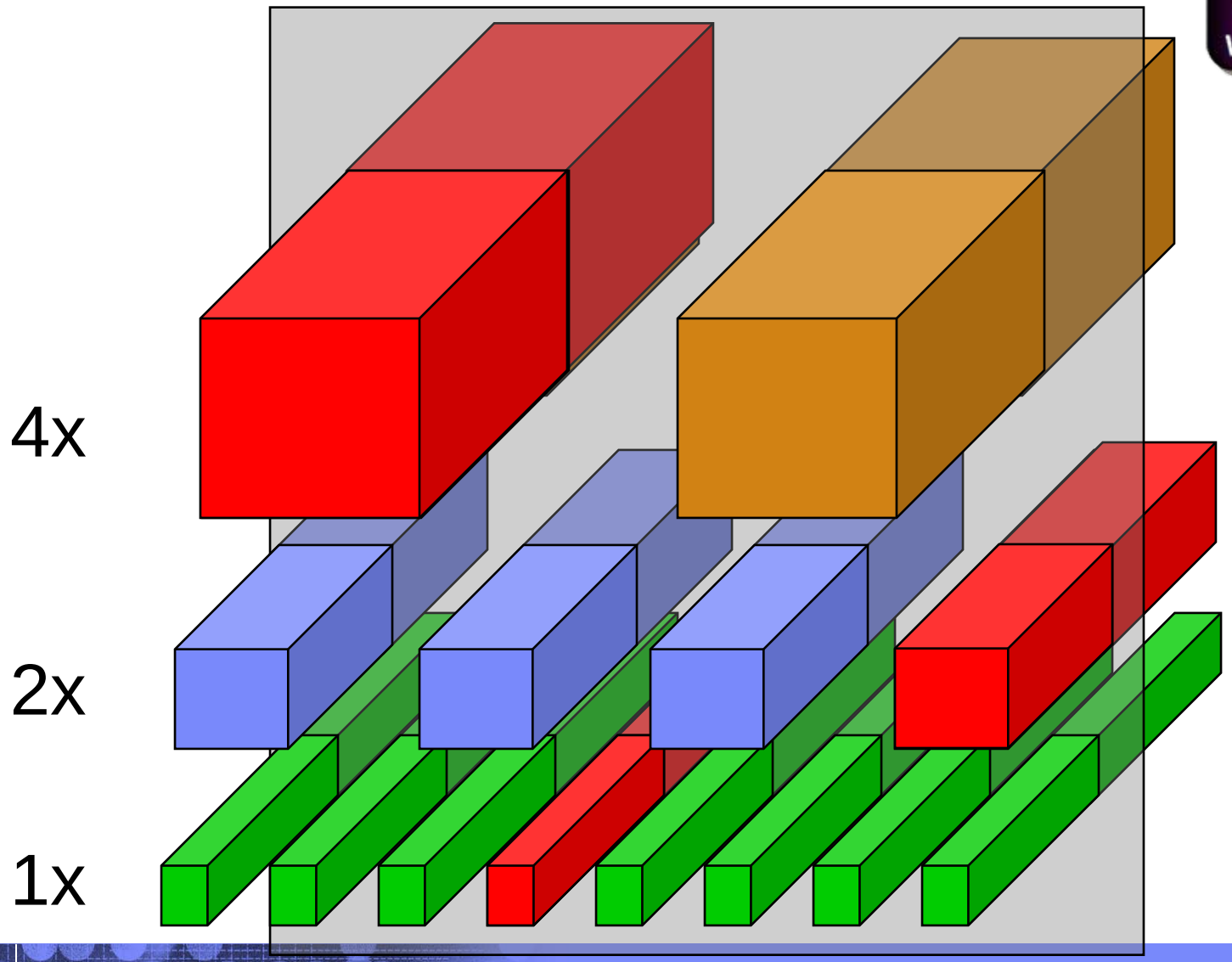
- With to tapering
- Theoretical formula: 3.5% difference in optimal cases

1990s Uniform Wire Sizing in Optimization



- **Need to be conservative for routability**

Performing Layer Assignment



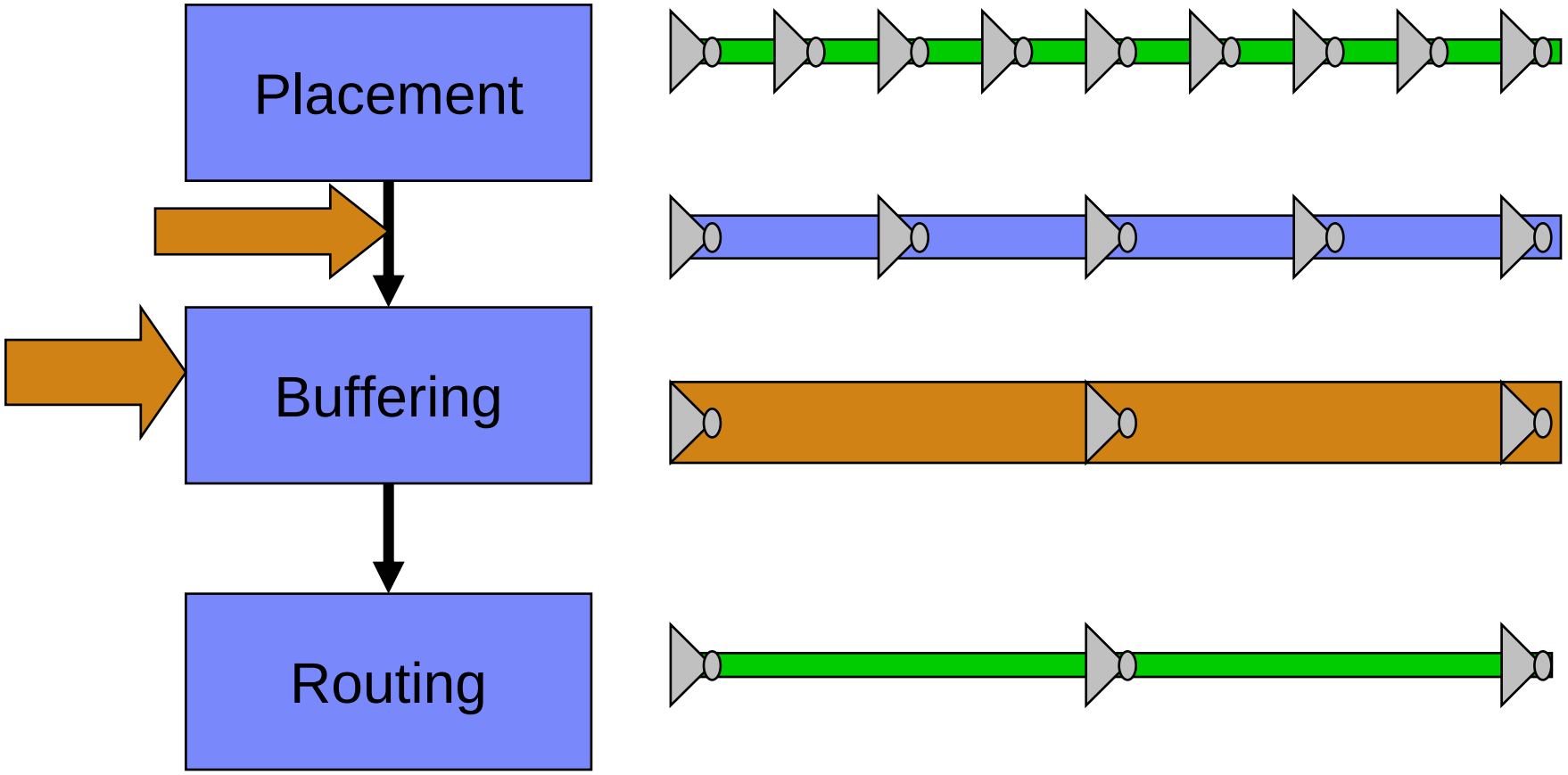
Resurrecting the Dead

- **Traditional wire sizing == making wider lanes**
- **Layer assignment == freeway overpasses**

"The rumors of my death have been greatly exaggerated".

Mark Twain

Where Does Layer Assignment Belong?



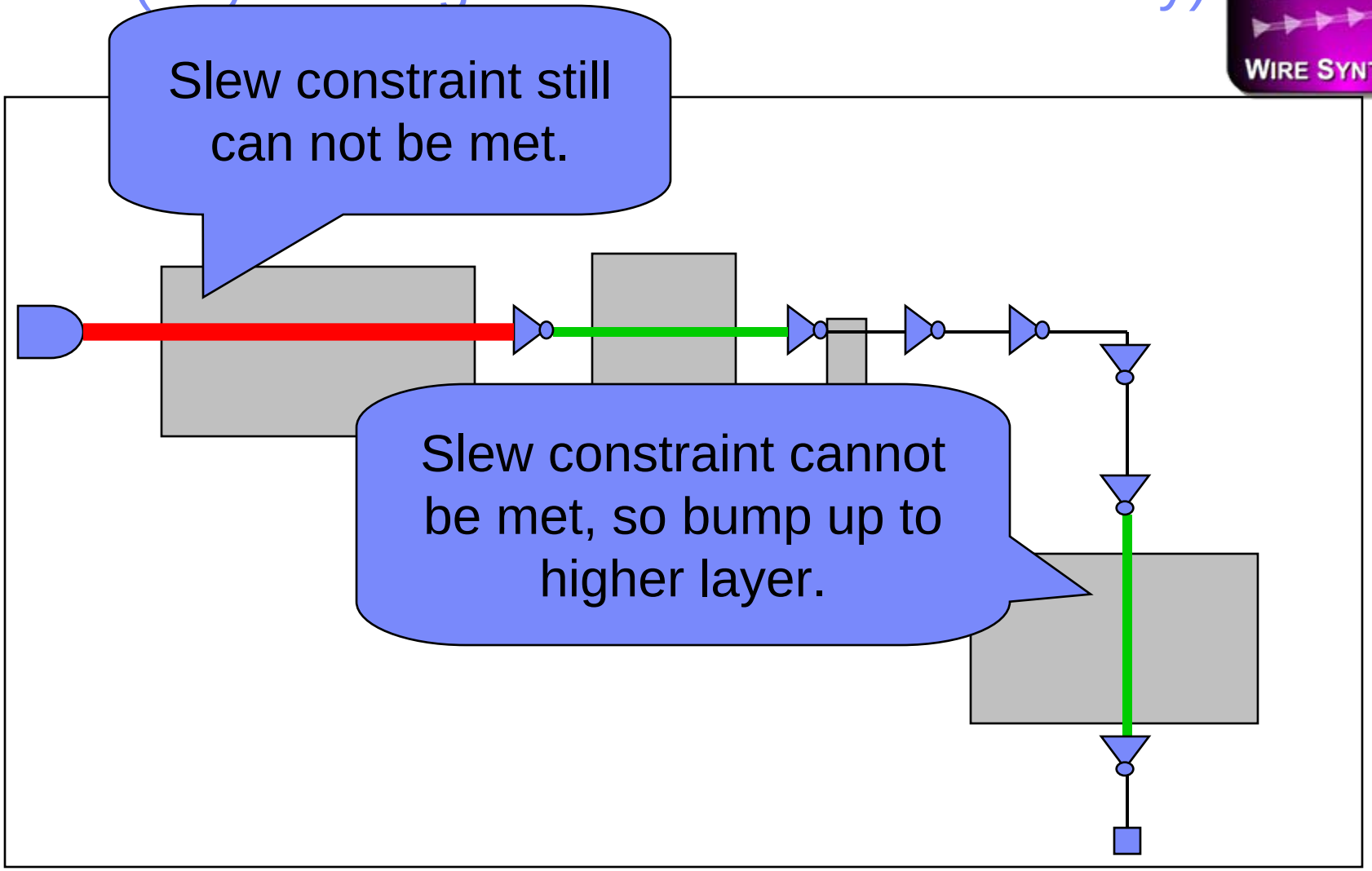
Buffering + Layer Assignment Objectives

- **Fix slew violations**
- **Optimize timing for critical nets**
- **Minimize routing constraints == minimize thick metal**
- **Exact formulation depends on router**
  - Hard constraints
  - Soft constraints

Fixing Slew Violations

- **Problem formulation:**
  - Given routing topology
  - Perform buffering and layer assignment to fix slew violations
  - Minimize usage of thick metal
- **Main purpose: cross over blockages**
- **Idea: when crossing a blockage, if the slew constraint cannot be met, bump the wire up to thicker metal**

LASR (Layer Assignment with Slew Recovery)



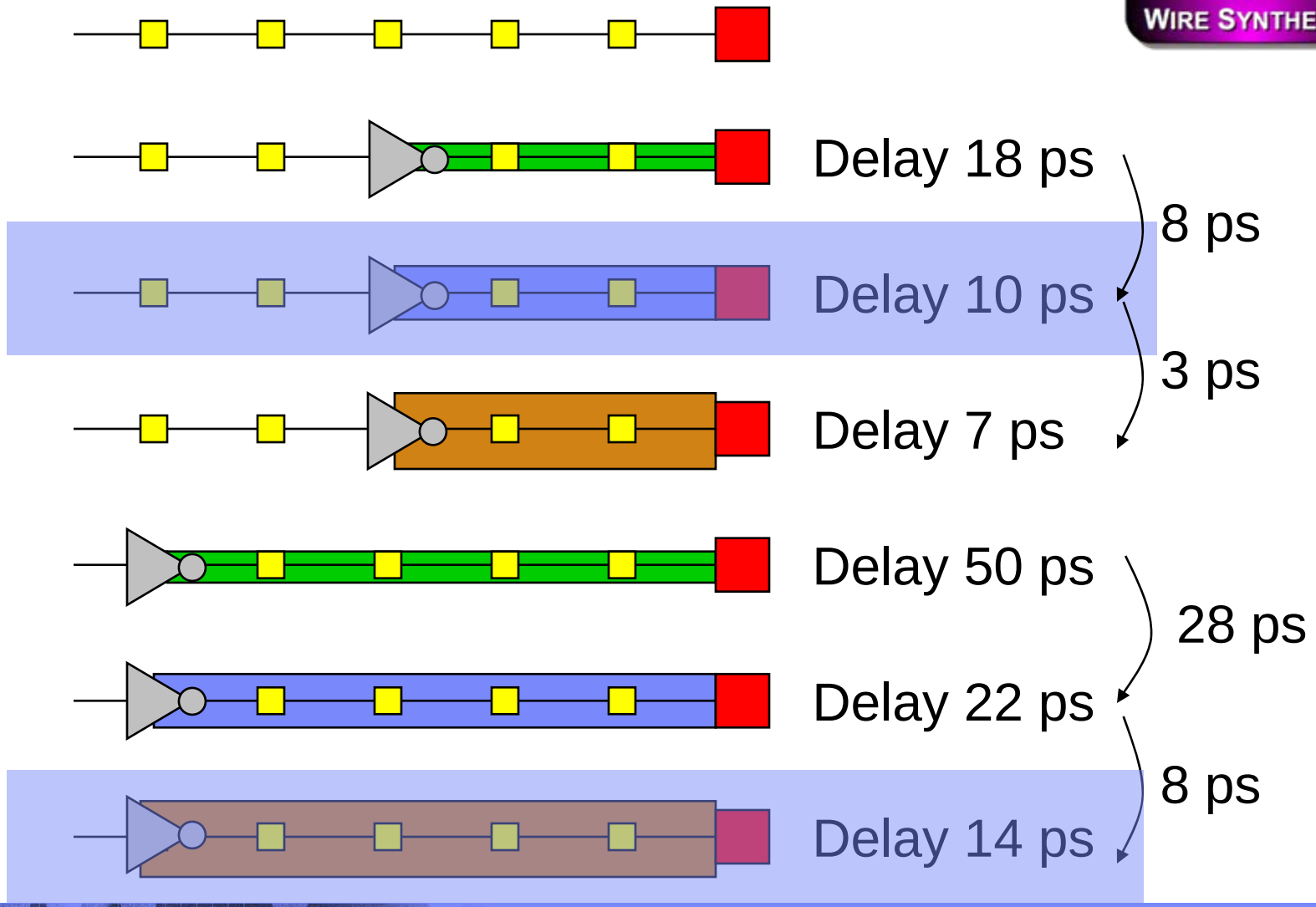
LASR Details

- **Default mode is thinnest metal**
- **Compute delay/slew for each available metal layer during bottom-up optimization**
- **When inserting a buffer, check for slew violation**
- **If slews for all buffers fail, use next thickest metal and regenerate buffer solutions**
- **Runtime cost is negligible**

Fixing Timing Violations

- **Problem formulation:**
  - Given routing topology
  - Perform buffering and layer assignment to fix optimize slack
  - Use thick metal only for significant benefit: need X ps improvement to justify jumping to next metal layer
- **Main purpose: cross over blockages**
- **Idea: Use traditional Van Ginneken's algorithm, but add *X* ps penalty for each additional metal layer.**

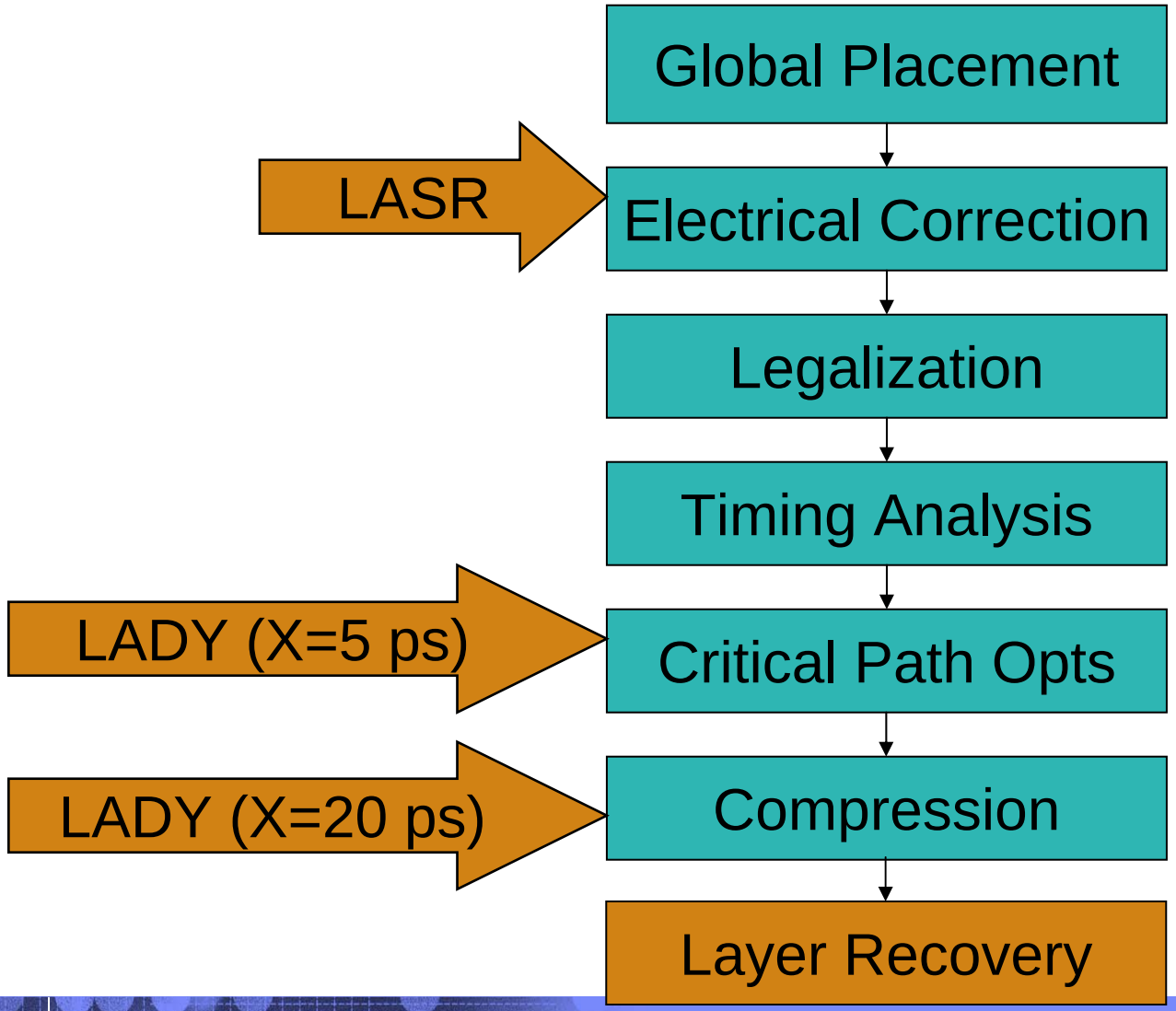
LADY Example (X = 5 ps)



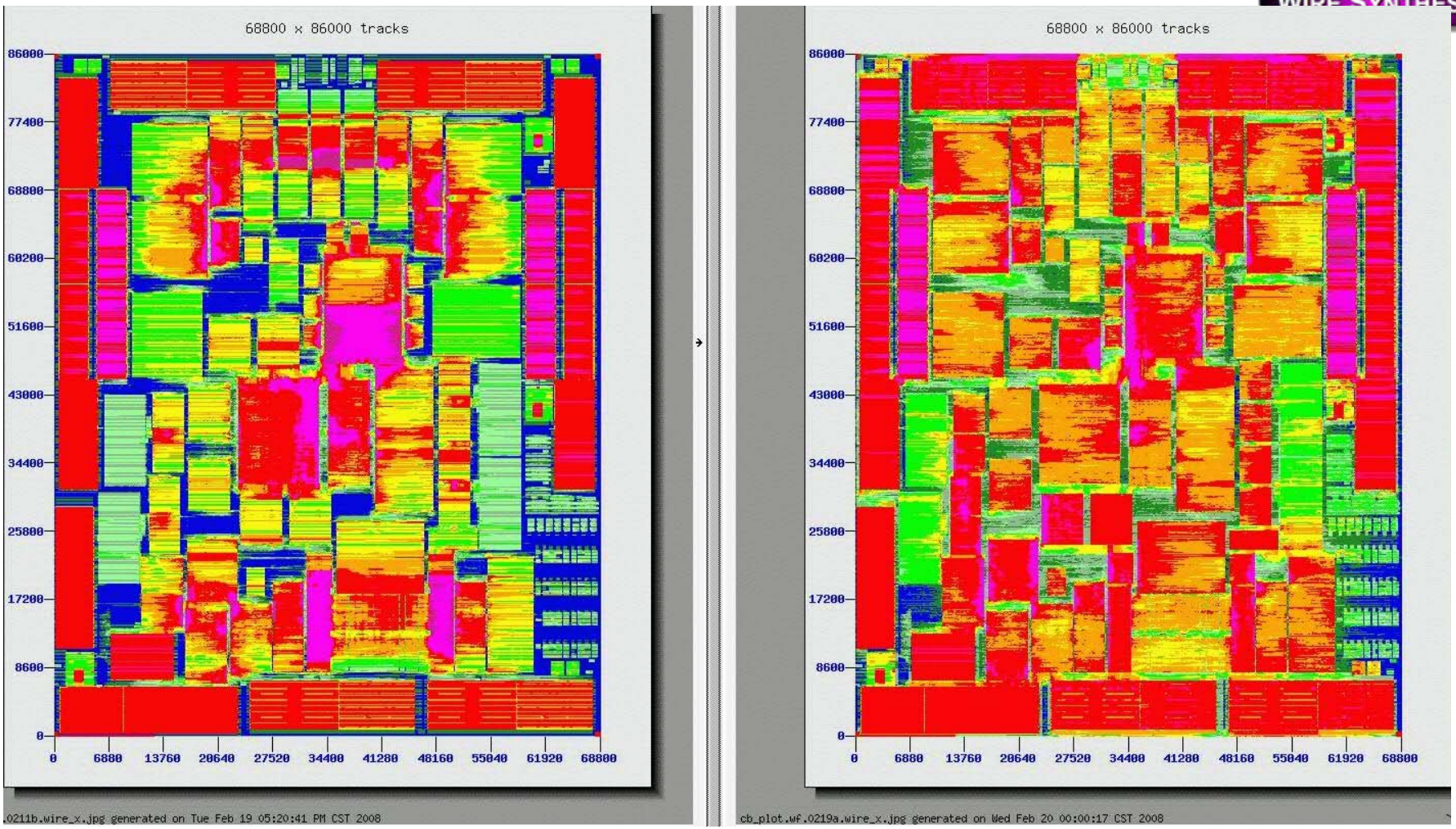
LADY Details

- **Instead of having k candidates, there are km candidates, where m is #metal layers**
- **When generating candidates add appropriate penalty to each candidate**
- **Overall number of candidates stays same**
- **Runtime impact minimal: about 10%**
- **Extensions:**
  - Different costs for each layer jump
  - Different costs for horizontal and vertical

Layer Assignment in Physical Synthesis



It's Still Not Enough



Wire Synthesis is Back

- **Original formulations hindered routability**
- **New metal layers are here for the taking**
- **Two new extensions to van Ginneken**
  - LASR for slew
  - LADY for delay
- **Wiring stacks are getting more complex**
  - 8 metal layers for 65 nm
  - 10 metal layers for 45 nm

New Problems in Wire Synthesis

- **Global allocation of layers to nets**
- **Fast global router that understands layer constraints**
- **Detection of too much thick metal usage and recovery**
- **Routing congestion mitigation algorithms**
- **Use of other wire codes (isolated, double)**
- **Handling metal pair mismatches (e.g., 3 layers of 2x)**
- **Some use of low-vt buffers**
- **Integration with latch relocation**

Food for Thought

“The best path through life is the highway”.

Henri Frederic Amiel