Manufacturing Challenges and their Implications on Design

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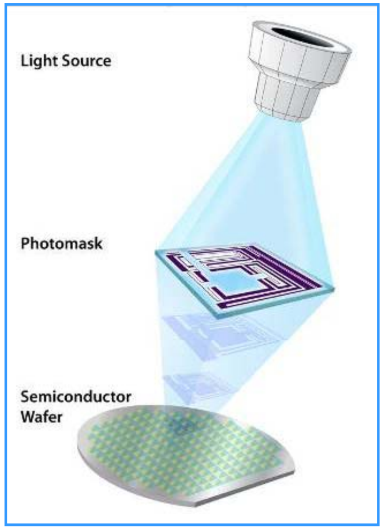
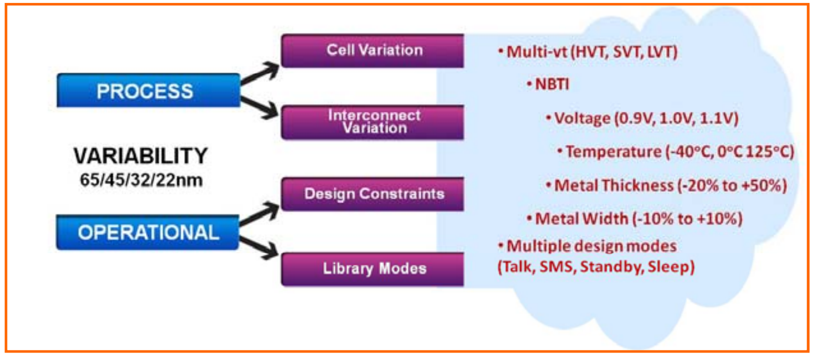
Mentor Graphics®

45nm/32nm Design Challenges

MANUFACTURING VARIATIONS



PROCESS & DESIGN VARIATIONS



LARGE DESIGNS

	NUMBER OF GATES	APPLICATIONS
5 mm x 5 mm	16 Million	▪ Consumer Electronics ▪ DSP ▪ Wireless Mobile
10 mm x 10 mm	50 Million	▪ Set-top Boxes ▪ Networking
15 mm x 15 mm	140 Million	▪ Graphics ▪ Microprocessors ▪ Networking

LOW POWER

Mentor Graphics

The Evolution of Signoff

PRE-TAPEOUT

130nm
- DRC

90nm
- DRC
- Critical Feature Analysis

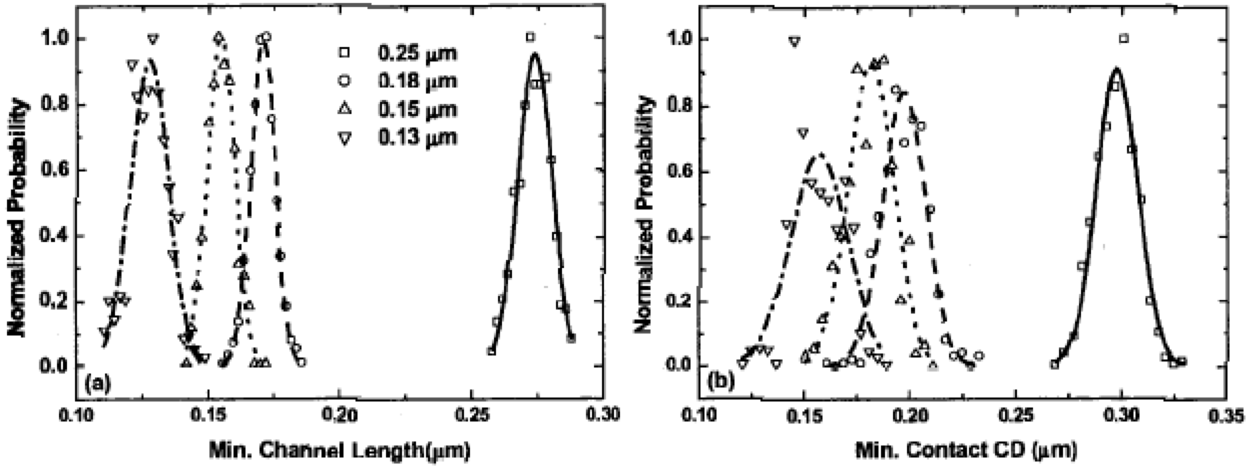
65nm
- DRC
- Critical Feature Analysis
- Critical Area Analysis
- Litho-friendly Design

45nm
- DRC
- Critical Feature Analysis
- Critical Area Analysis
- Litho-friendly Design
- Litho-aware Silicon Modeling

32nm

Variability vs. Yield, Cause vs. Effect

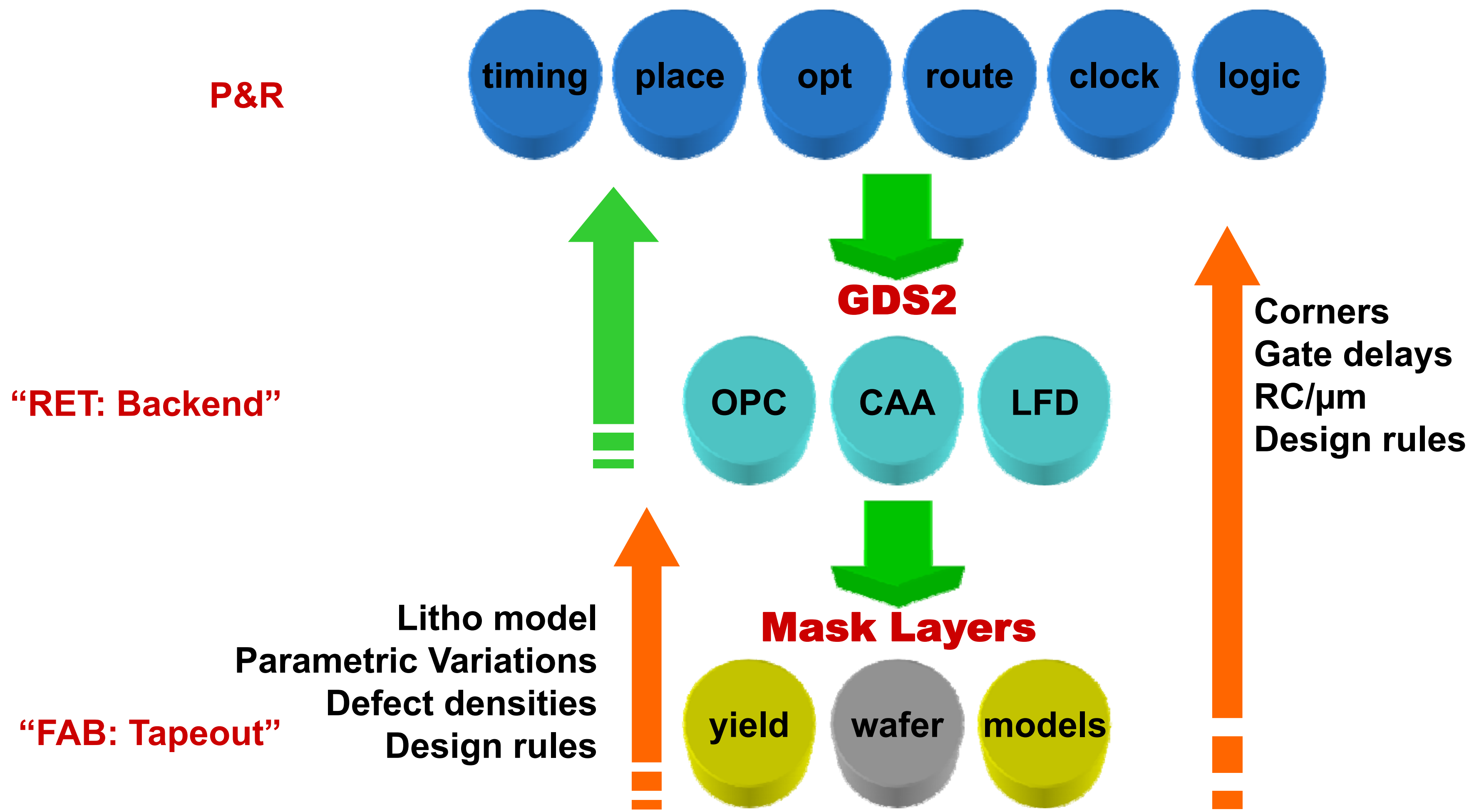
- **Variability: spread in process/layout parameters and is inherently caused by the litho-process**



- **Yield: measure of success-rate in fabrication process**

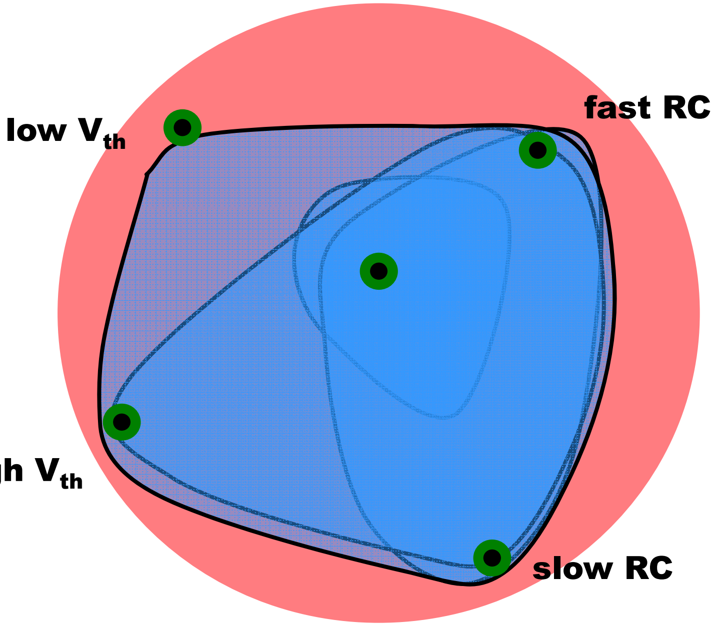
- **Yield-failure: limiting case of variability.**
  The effect of a high-σ event!

P&R, RET and Fabrication



How does robust optimization address variability?

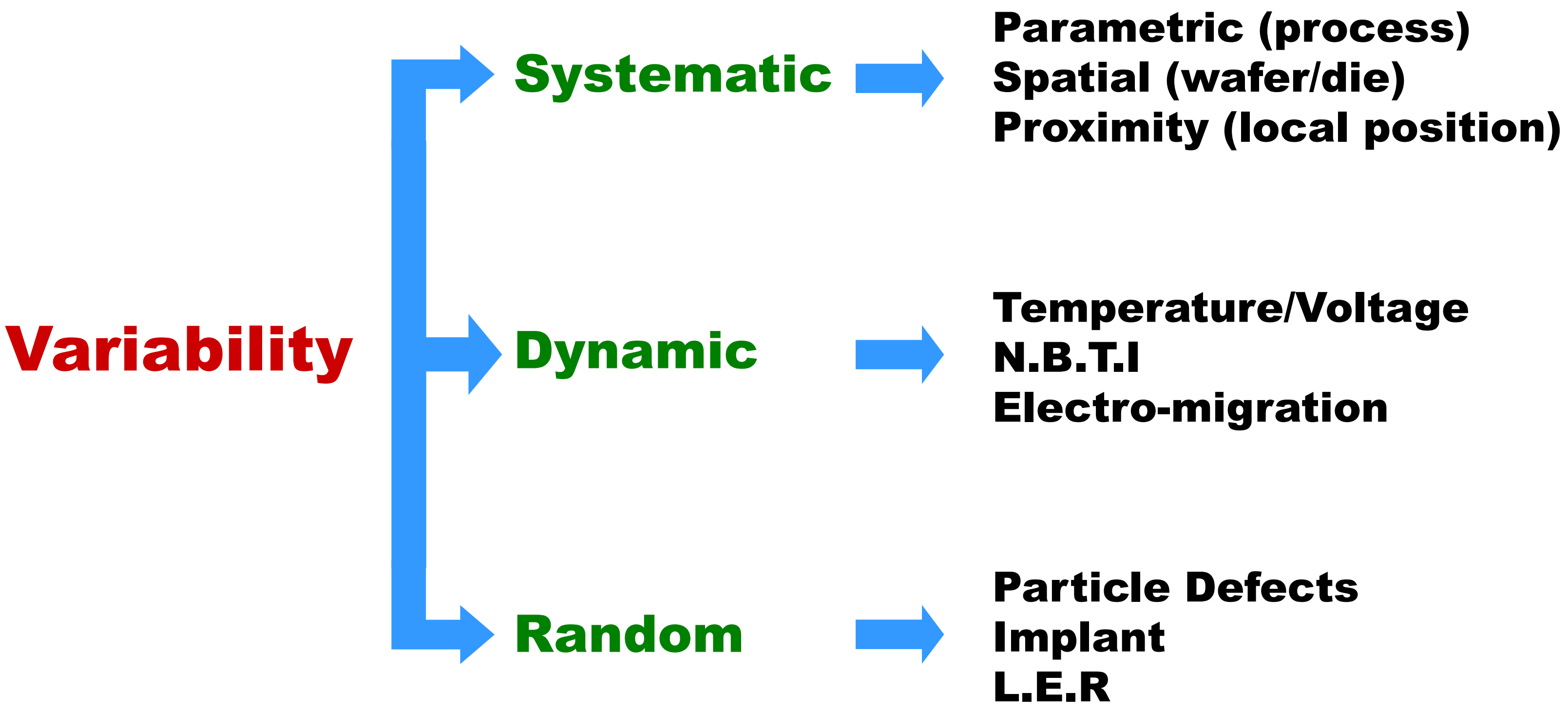
Fab & Test Universe



Typical optimization centered around nominal process

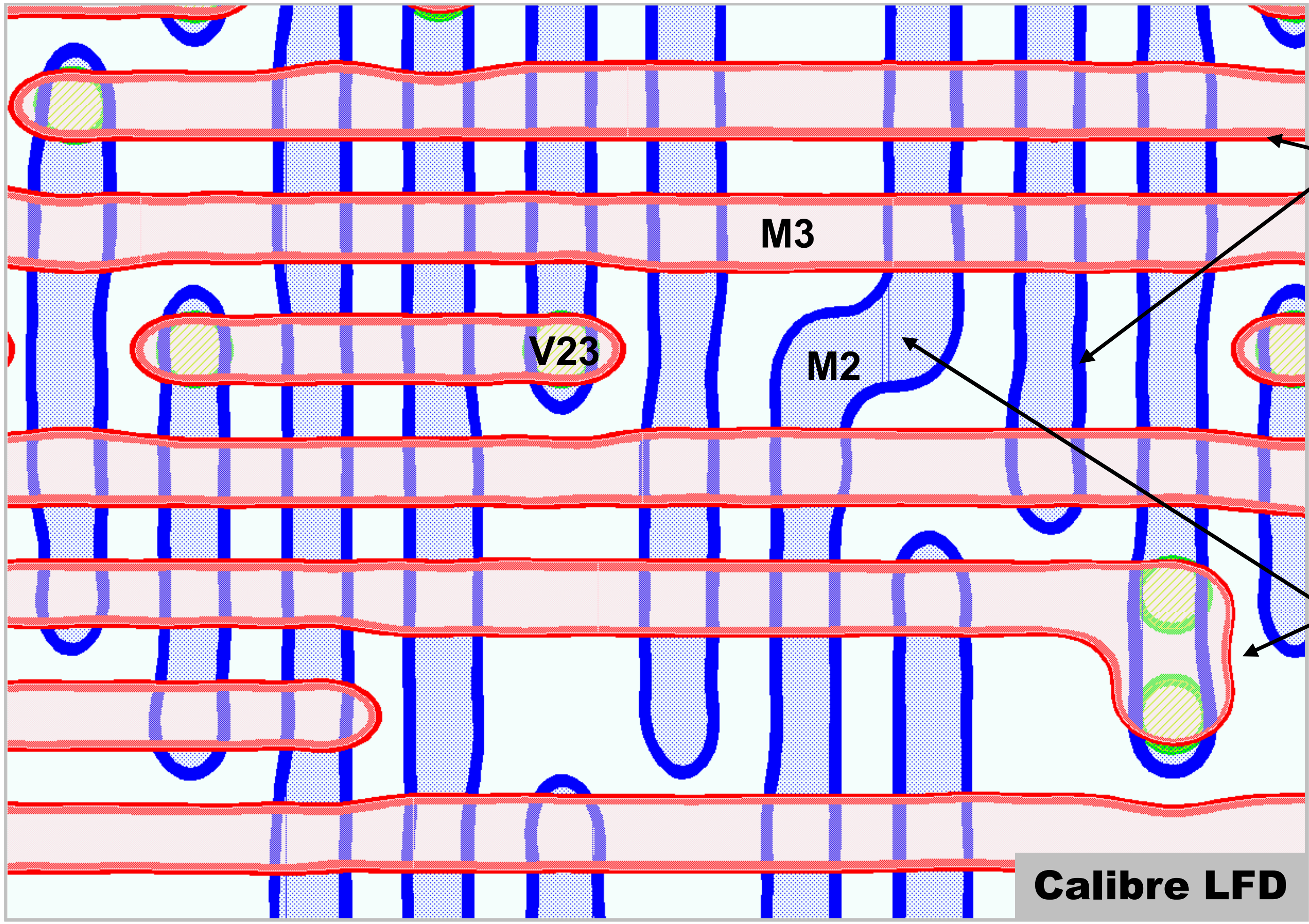
Robust optimization seeks to cover larger process conditions

Taxonomy



What can be addressed by P&R?

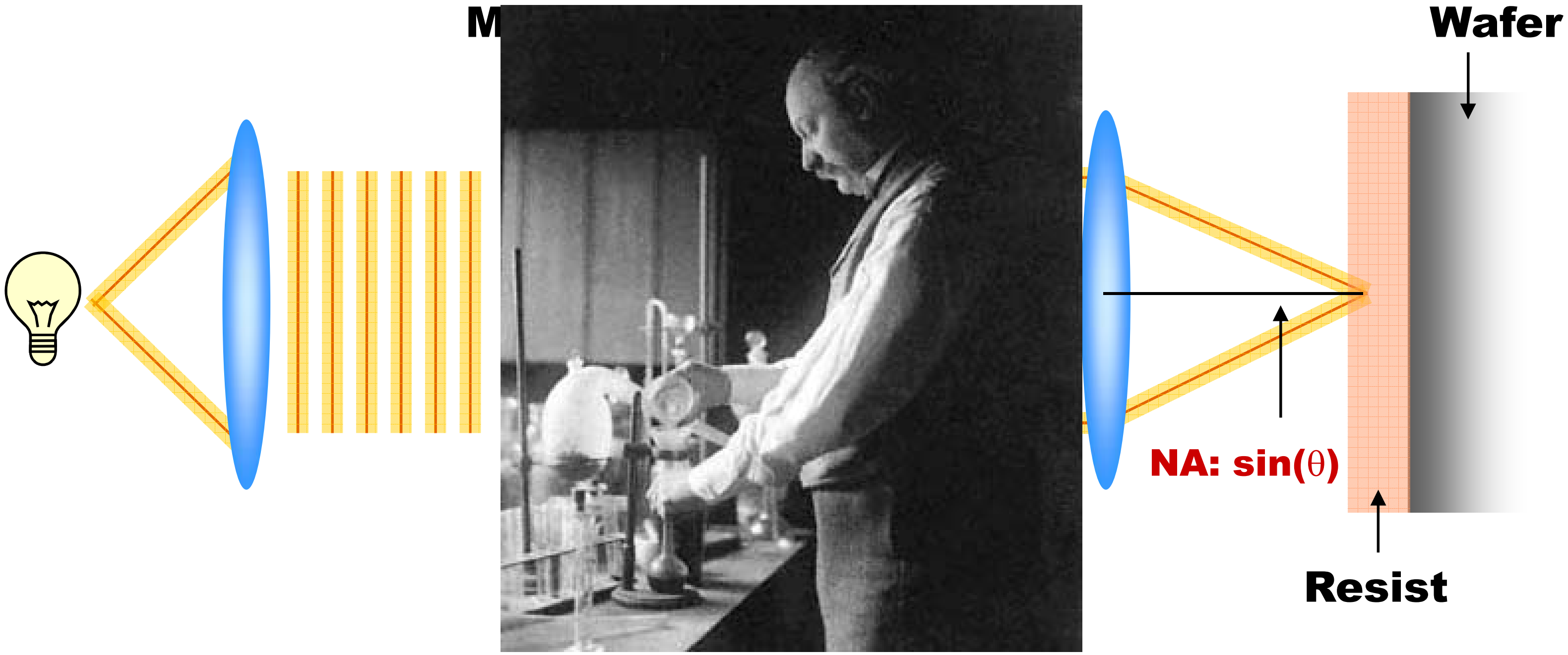
Example → Systematic Parametric Variation: PV-Bands



The bands represent a range of simulations across Dose, Defocus, and Mask-Bias

Drawn != Actual

Understanding Lithography is the first step

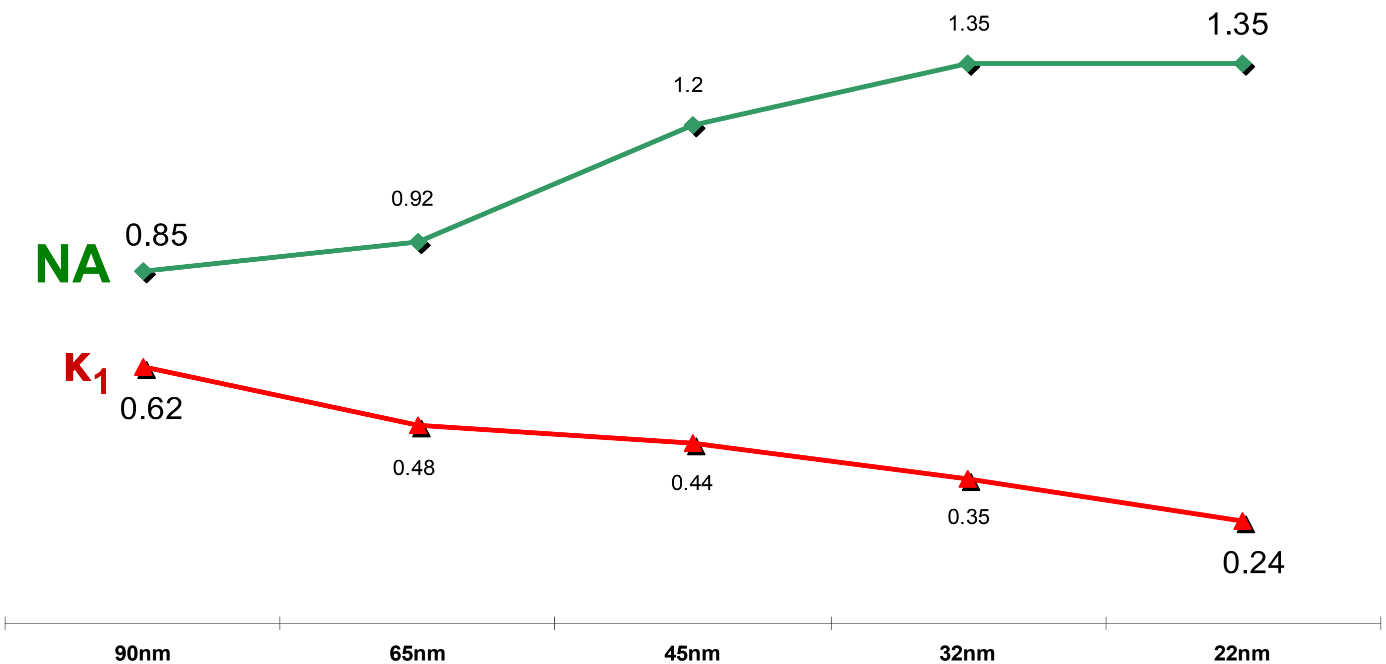


$$\text{Critical\_dimension} = \kappa_1 * \lambda / \text{Numerical\_Aperture}$$

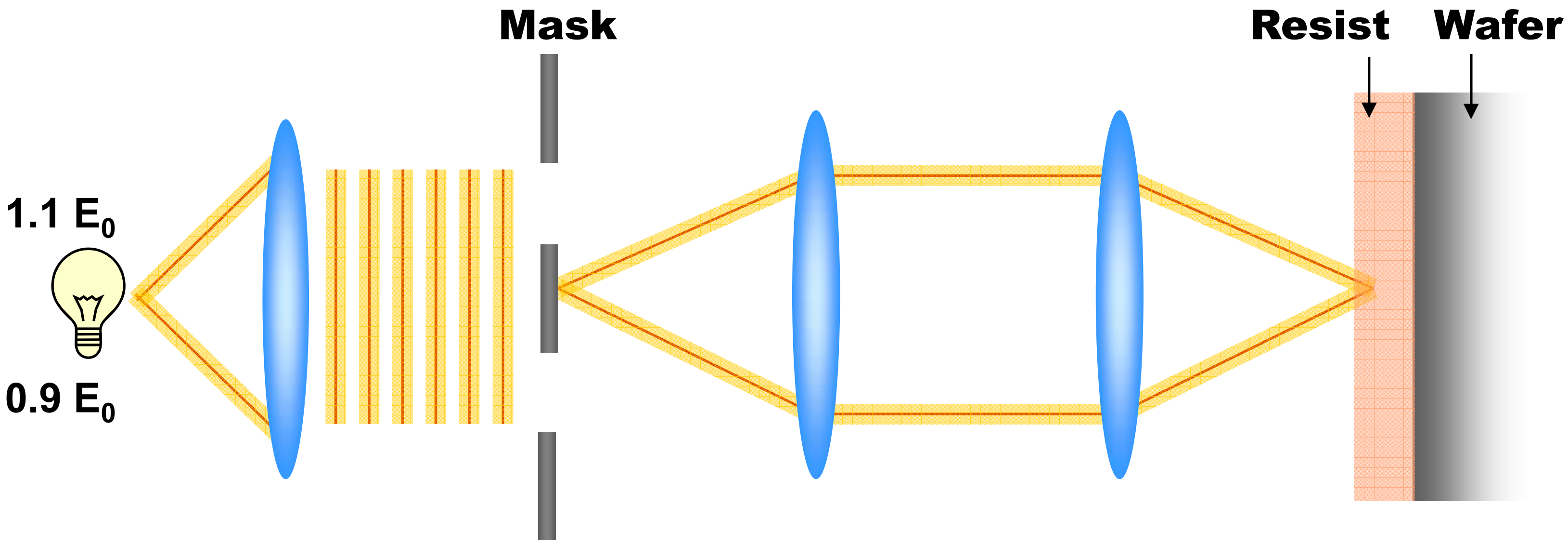
How is sub-λ possible?

- **λ = 193nm; sin(θ) ≤ 1 → CD ≥ 193nm**

$$CD = k_1 * \lambda/NA$$



Optics: Initial Source of Variability



Exposure Latitude

Mask Bias

Focus

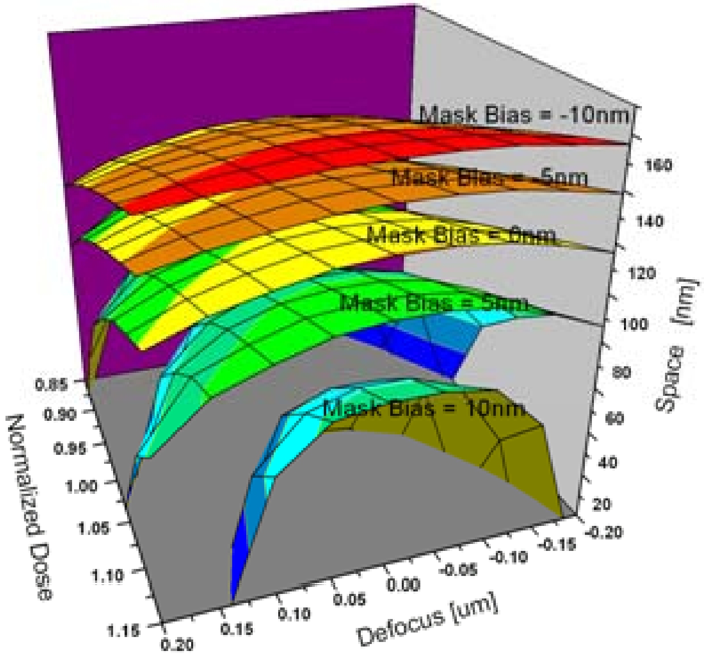
$\sigma(CD_{image})$ limits $\sigma(E_0)$

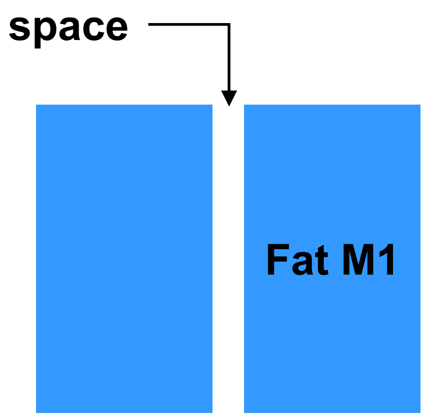
$\sigma(DOF)$ limited by $\sigma(CD_{image})$

$\sigma(CD_{image})$ limits $\sigma(CD_{mask})$

The variance of CD_{image}, Exposure, Masks and Focus are coupled

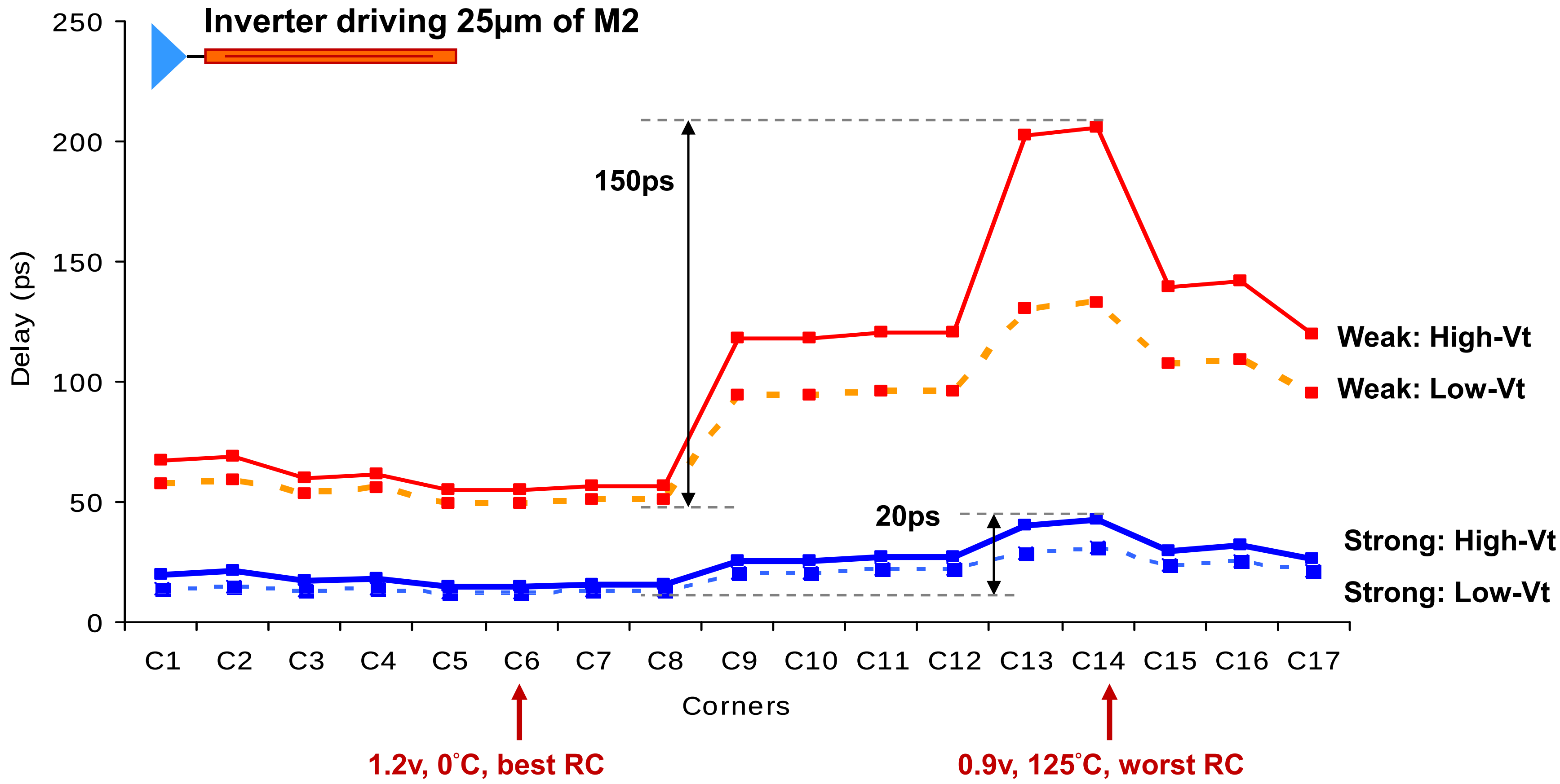
Parametric Variability in Lithography





Variability is a measure of the change in the image over changes in Dose, Focus and Mask-Bias

Variability through Timing Corners

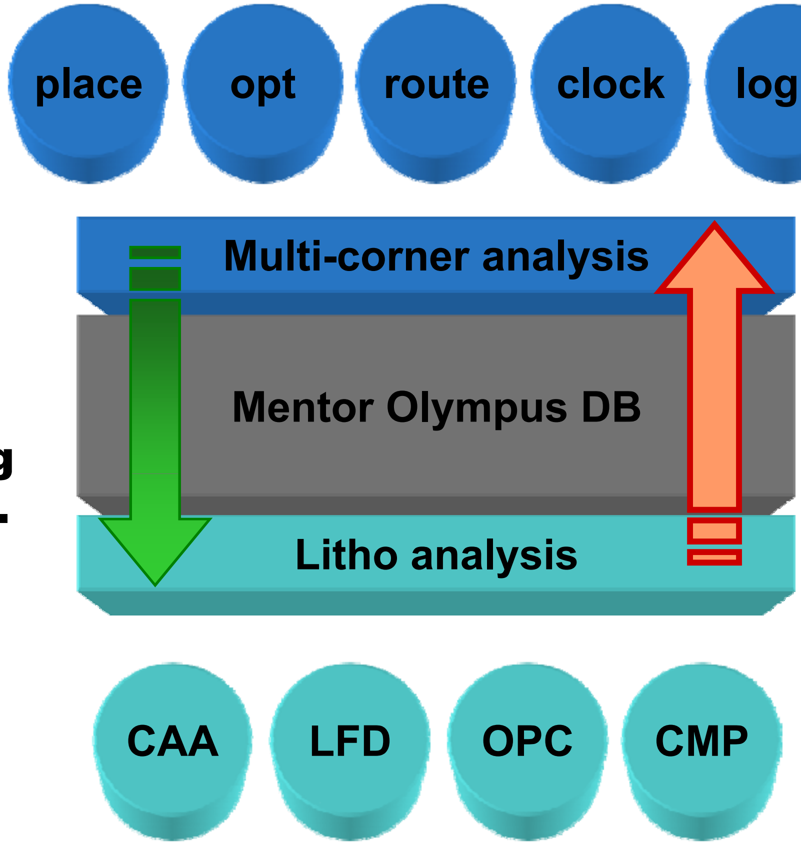


Each corner is a full chip timing → tighten the range

Robust P&R for DFM

Timing aware

Metal Fill
Fast DRC
Wire Spreading
Double Via Ins.



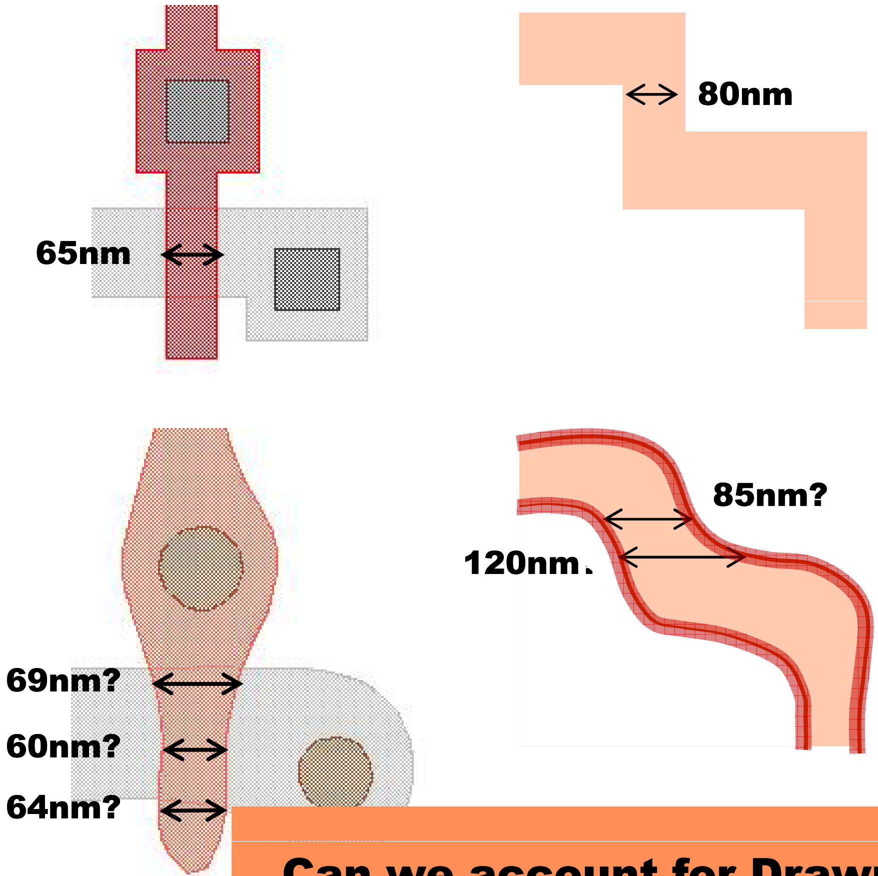
Litho Errors
Advanced Rules
CAA / Yield
CMP Maps

Litho aware

Variability

- **Systematic** → Parametric (process); Spatial (wafer/die); Proximity (local position)
- **Dynamic** → Temperature/Voltage; N.B.T.I; Electro-migration
- **Random** → Particle Defects; Implant; L.E.R

Systematic vs. Parametric



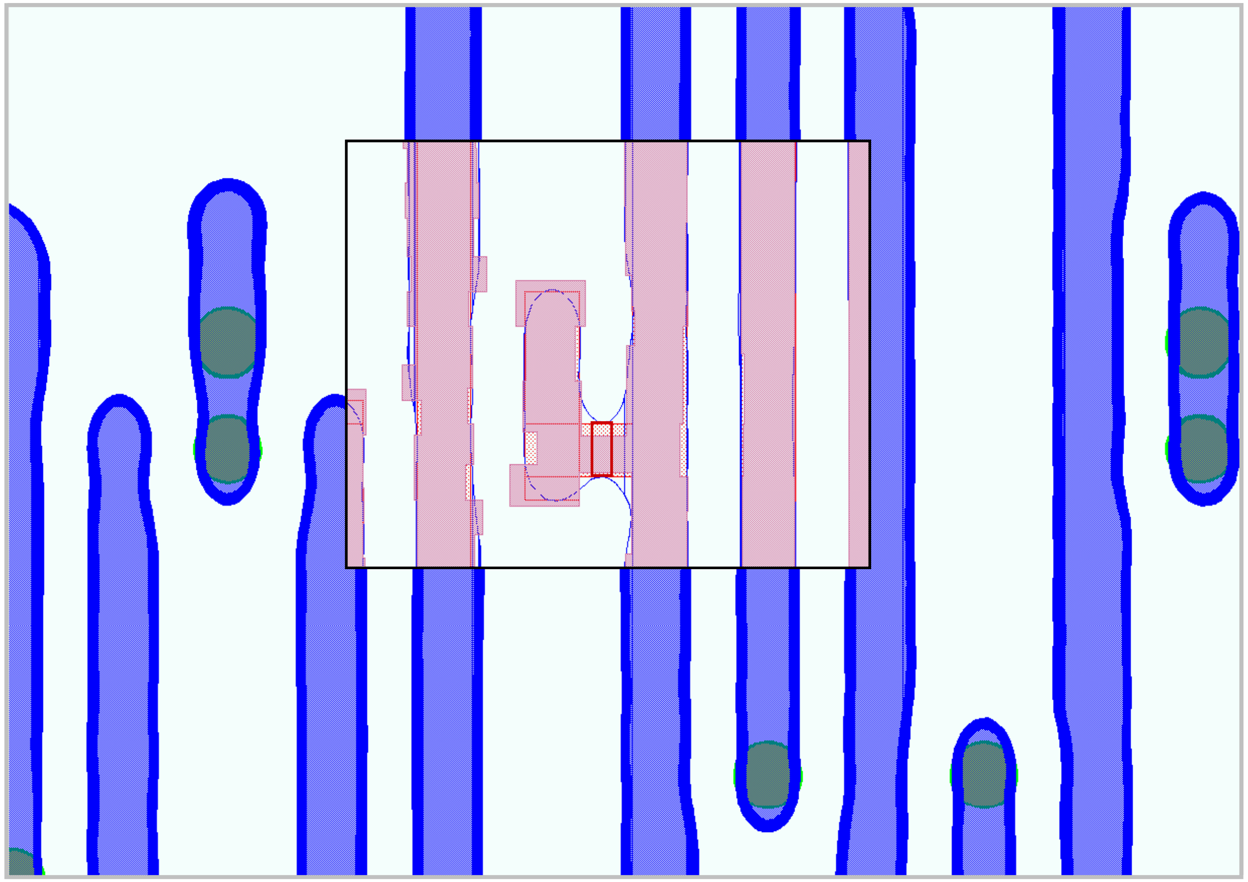
Actual Shape Can be Simulated

Systematic → Drawn - Actual

Parametric → σ(Actual)

Can we account for Drawn Shapes in Routing?

Metal Pinching (Min-Width)



M2 bridge with litho error

Pinched (but still ok)

PV-band violation

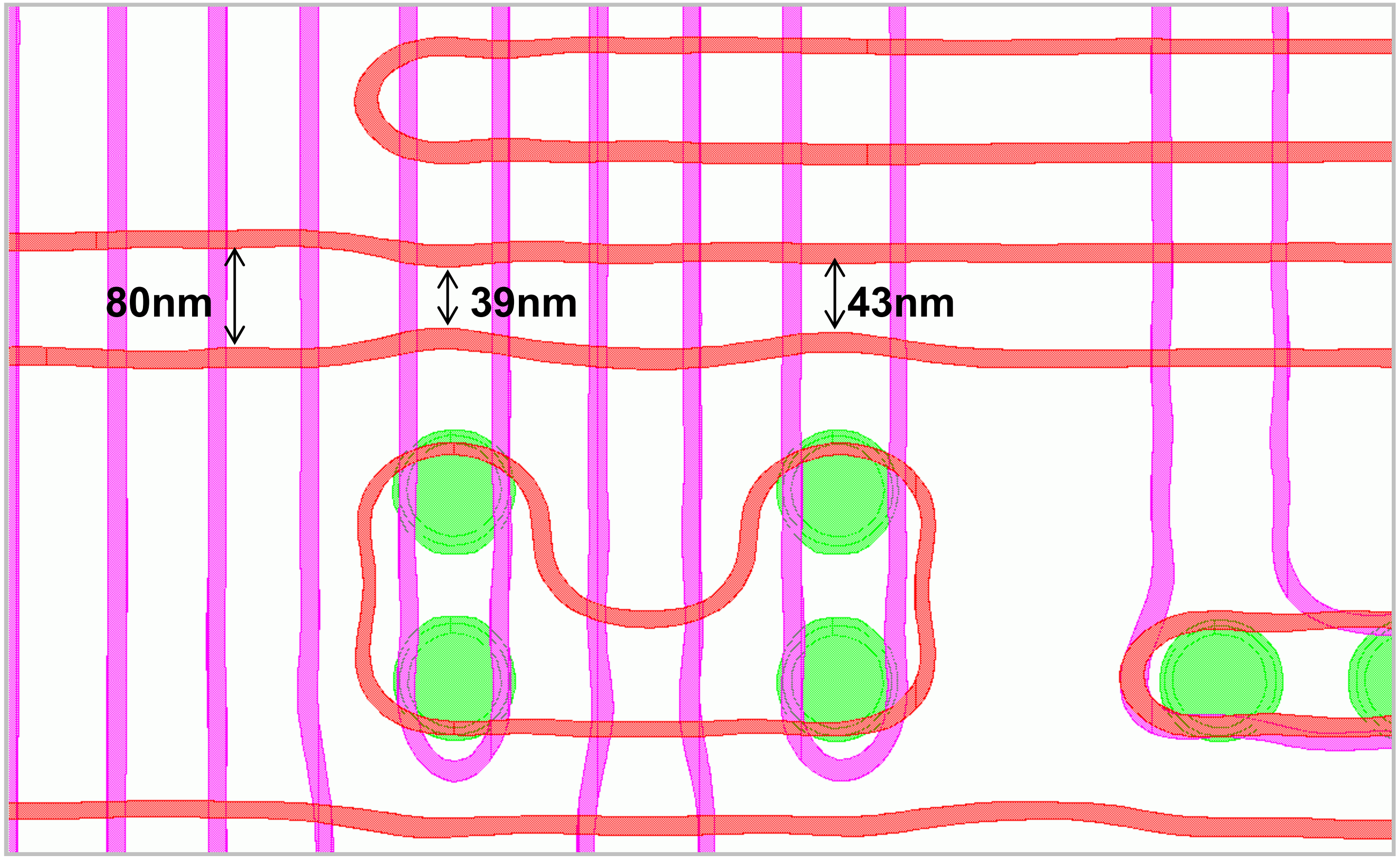
OPC: nominal case

Rather than make OPC solve for all Process windows, we could make the M2 jog wider

Density based width variation

Modeled in RC extraction

Double vias can be a double edged sword

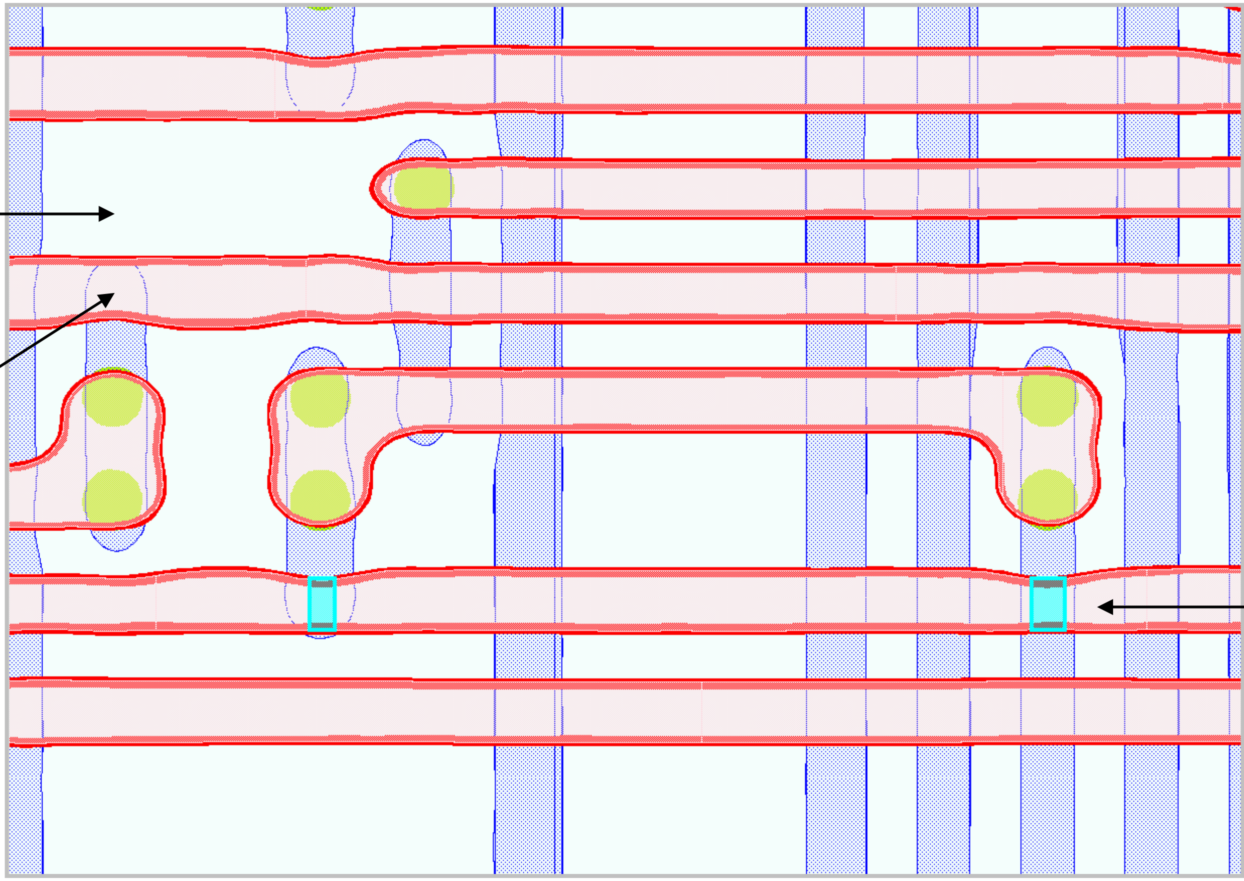


Increased contact reliability ⇔ Decreased metal reliability

Locality != adjacency

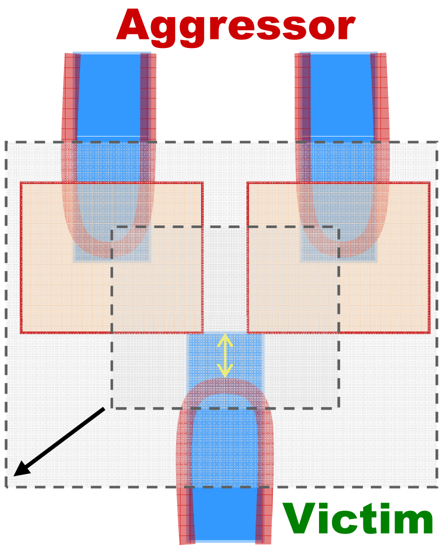
Space allows the other side to compensate

Symmetry suggests this should be an error



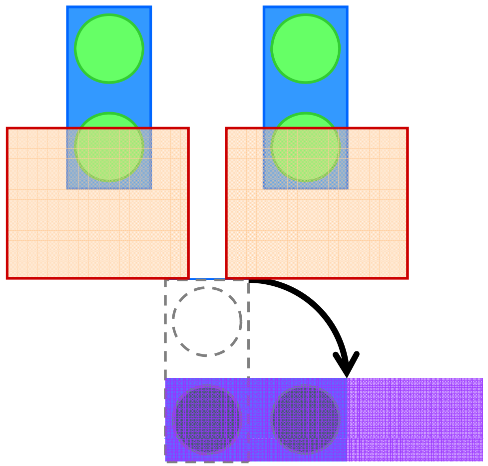
M3 min-width violation

Robust repair of Litho-Errors

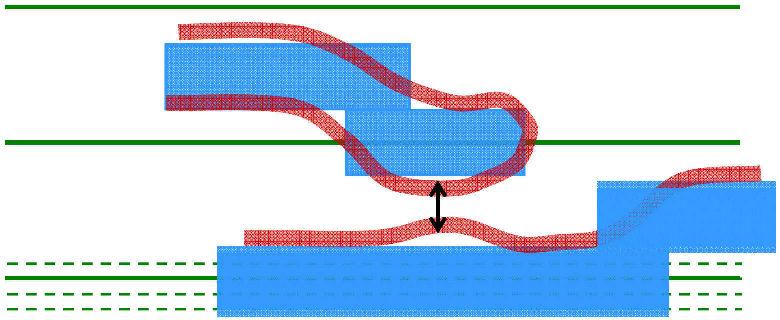


Zones

Expand
to fix error

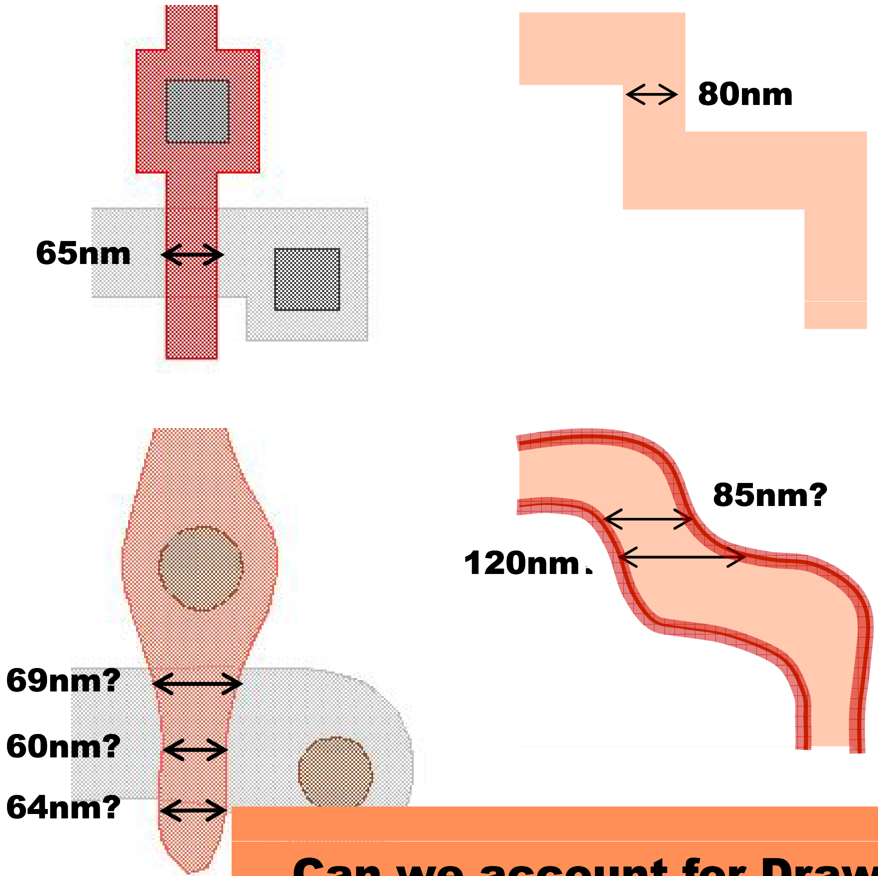


Rotate (if possible)



Use a fine grid to resolve violation

Systematic vs. Parametric



Actual Shape Can be Simulated

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Parametric → σ(Actual)

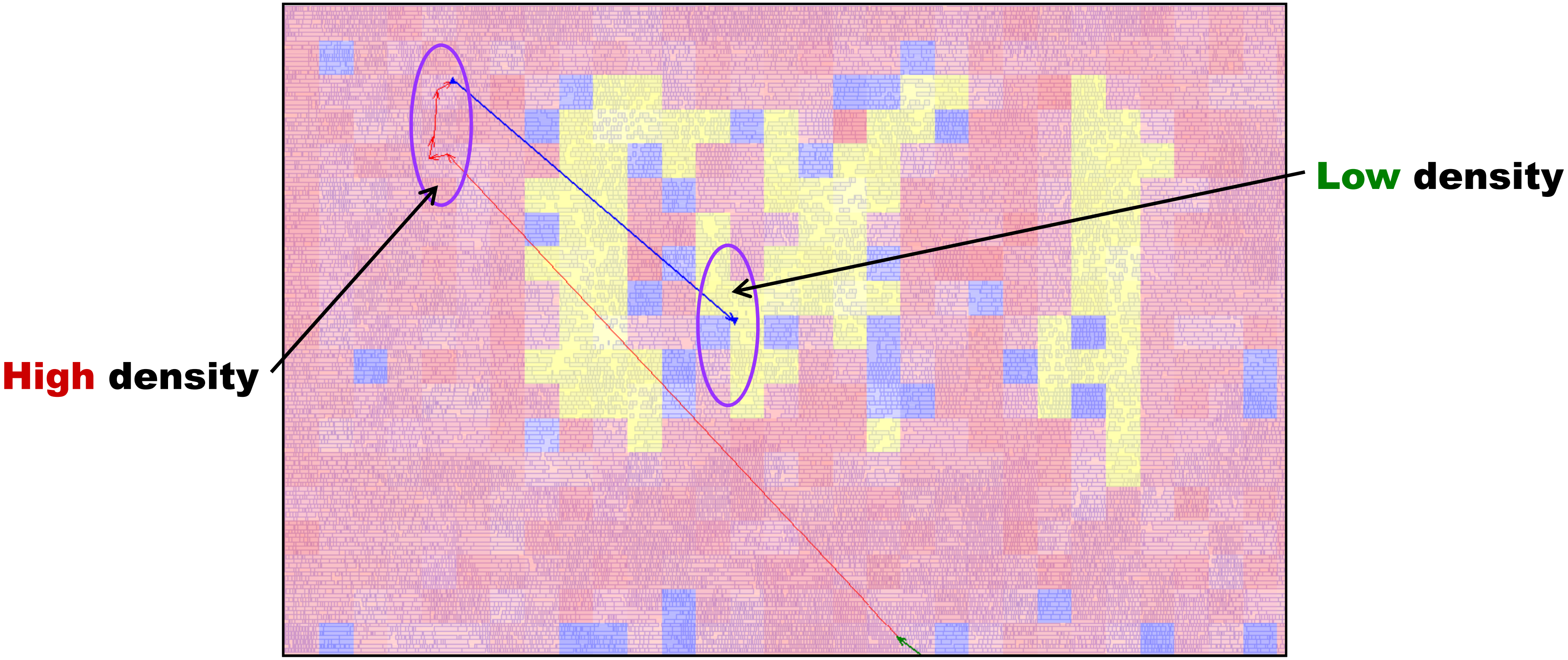
Can we account for Drawn Shapes in Timing?

OCV → Margins → "Fudge-factor"

- "OCV Margin" factor of ~20%
  - This factor masks
    - Location based variation
    - L/Weff variation
    - IR-drop etc..

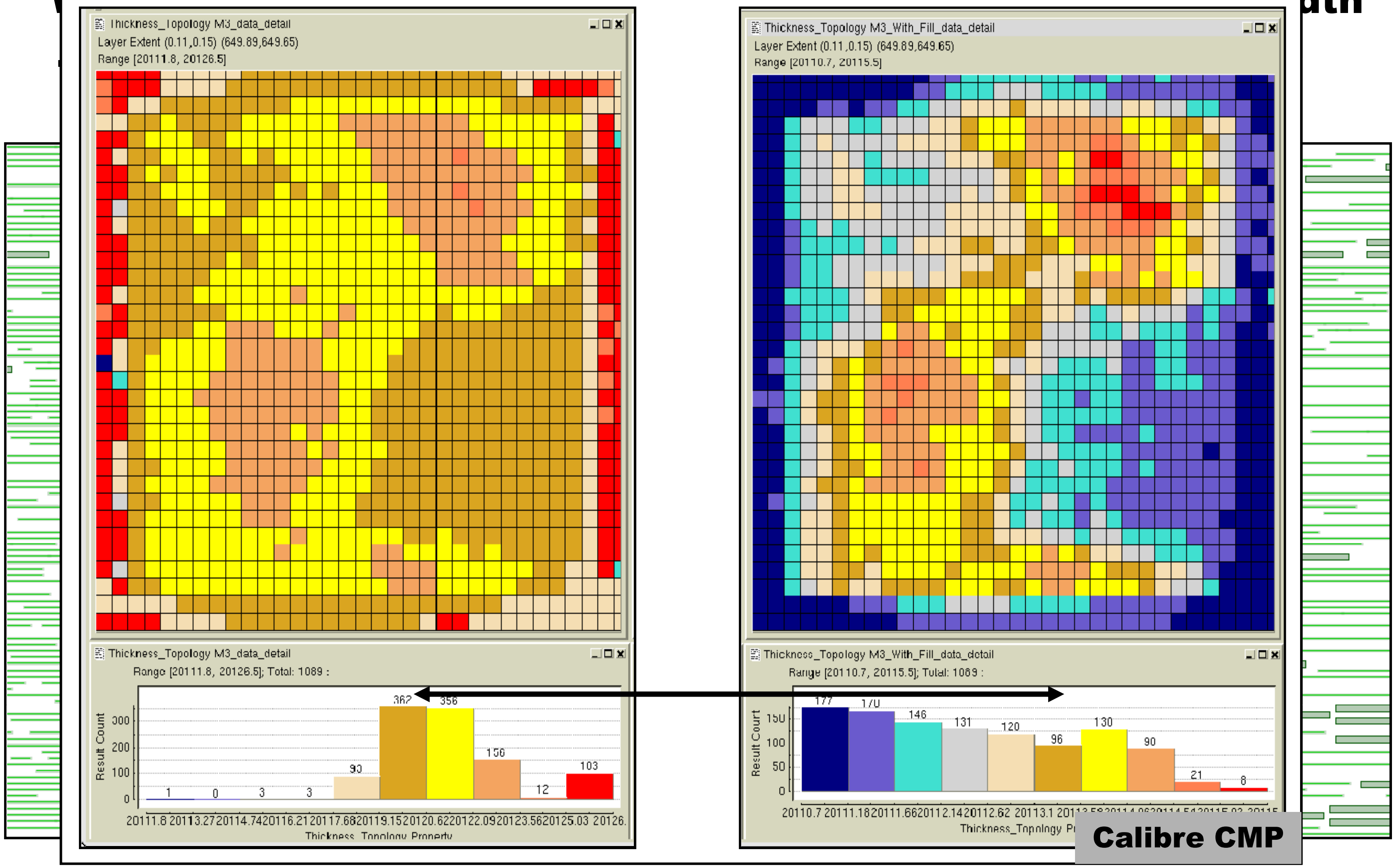
- Robust OCV → model each factor

Systematic Density-based Variation for a Timer



High cell density → increased $\sigma(L_{eff})$
Proximity(Density) Based OCV

Parasitic Variation and Chemical Mechanical Polishing



Taxonomy

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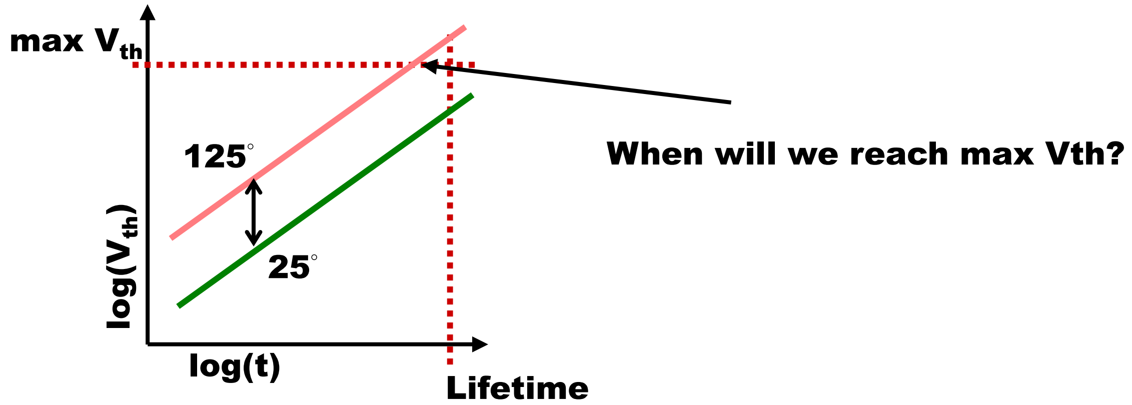
  - Electro-migration
- **Random**
  - Particle Defects
  - Implant (V_{th})
  - L.E.R

Dynamic Variation

- **Time/state dependent**
- **Eg: Negative Bias Temp Instability (NBTI)**



"*A comprehensive model of PMOS NBTI degradation*", M. Alam.

- **A °K map + target conditions are needed**
  - **Also supports delay dependence on IR-drop**

Taxonomy

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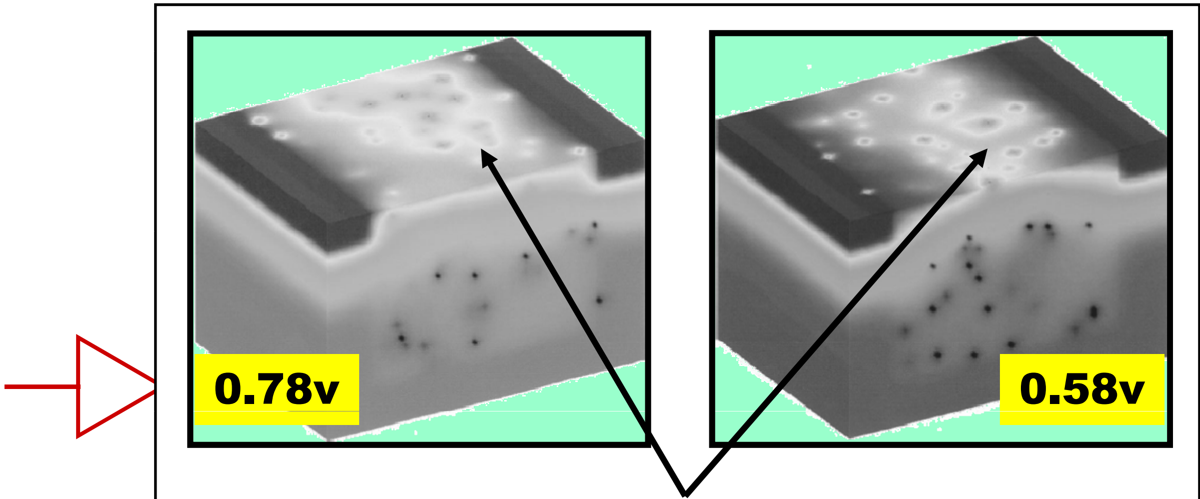
Random variation along timing-path

- $\sigma(V_{th}) = K / \sqrt{W \cdot L}$
  - Due to variation in number and distribution of dopant atoms in the channel

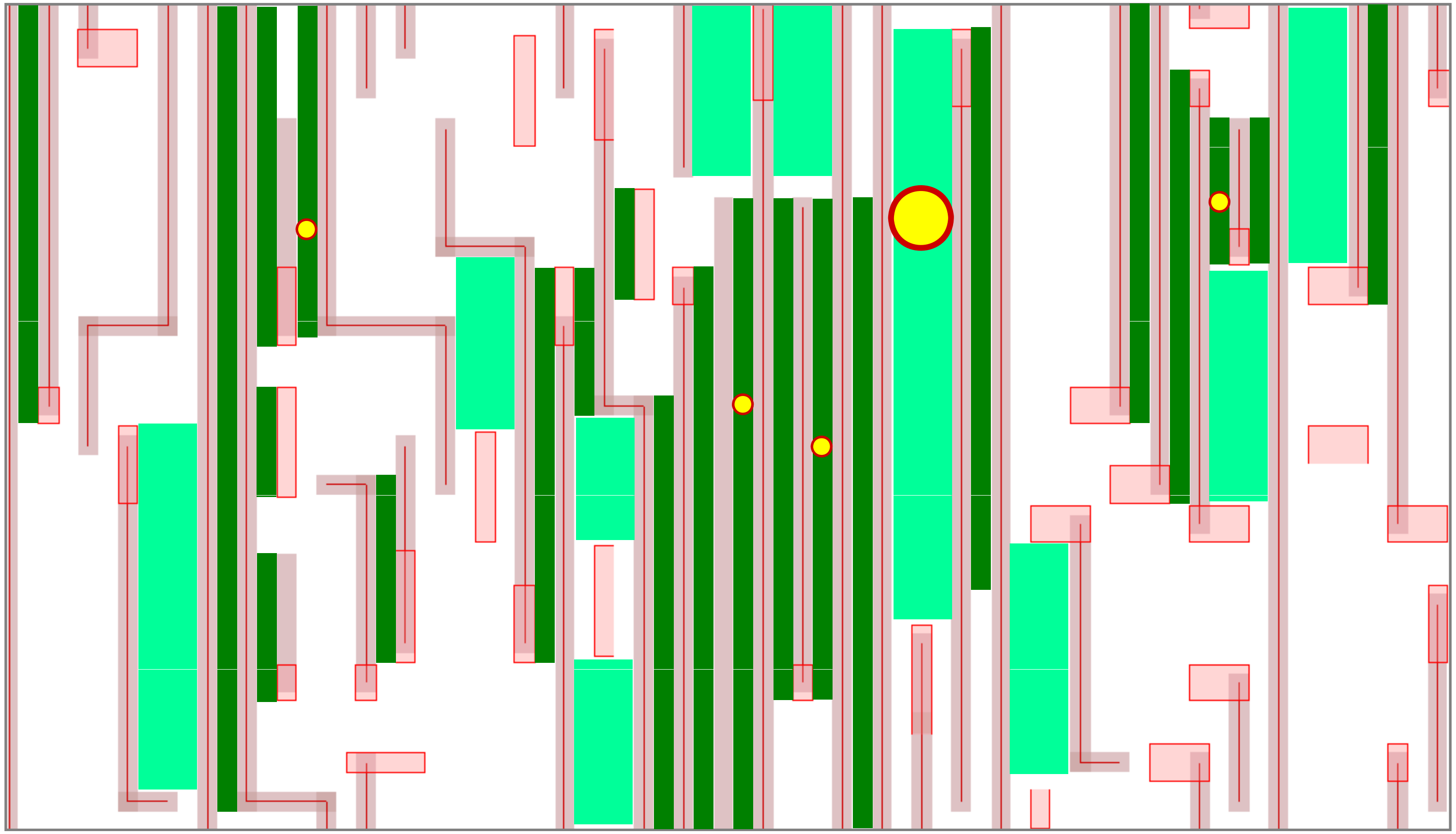


Different distribution!
Same number of atoms

$\sigma(V_{th})*\sqrt{5}$
$\sigma(V_{th})*\sqrt{2}$

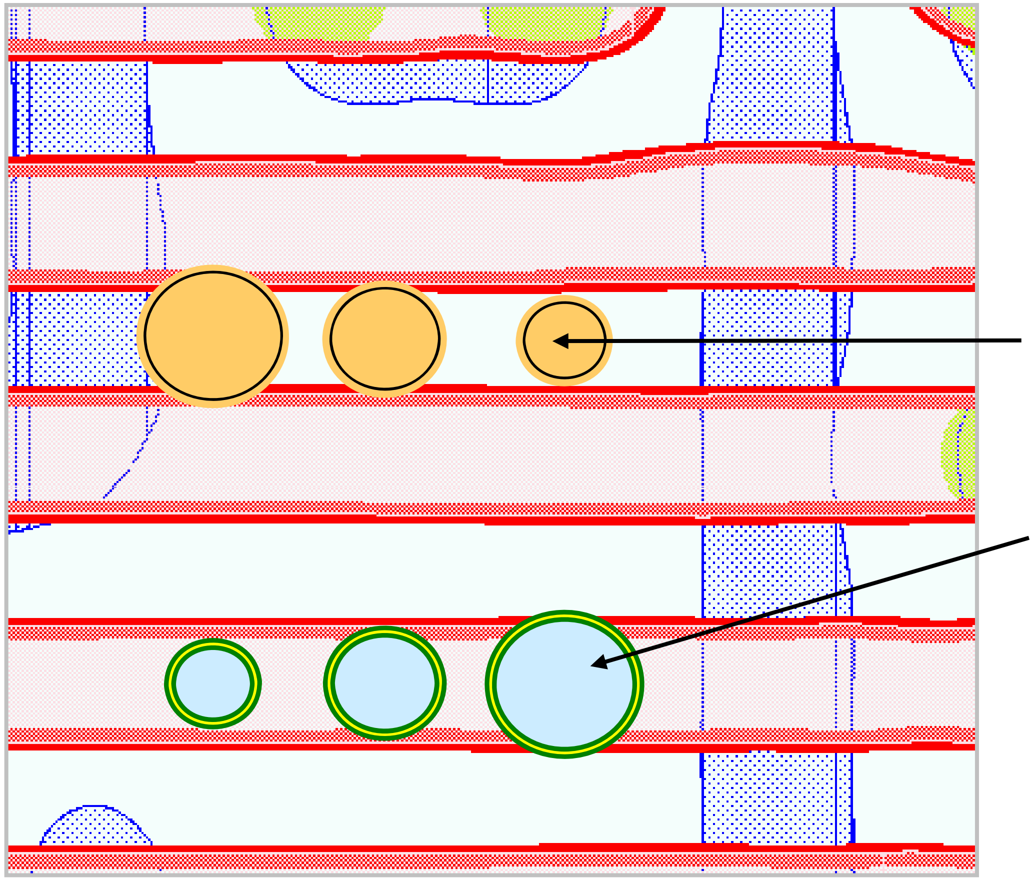
On clock trees, even a small difference in path-depth matters.

Random Fault: Critical Area Analysis



$$C.A = \int_0^\infty P(r) \cdot A(r)\, dr$$

CAA: How is A(r) to be determined?



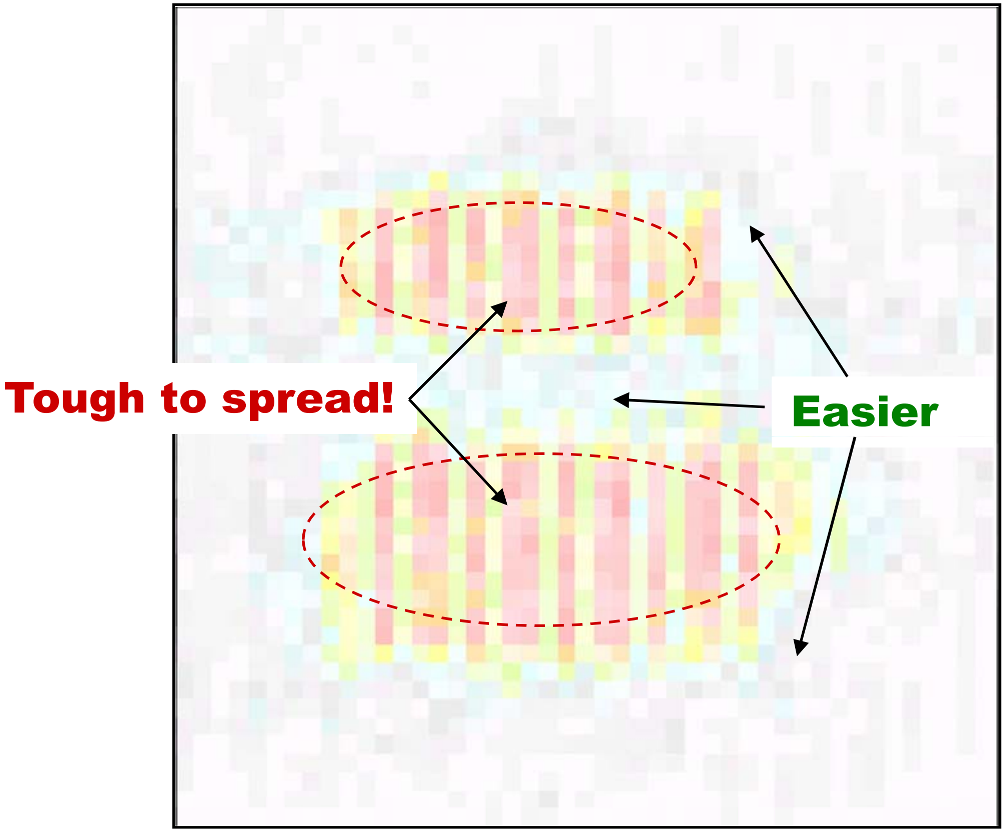
Shorts:
PV-Bands → 3 possible A(r)

Opens:
PV-Bands → 3 possible A(r)

Conservative: Inner band for opens and Outer band for shorts

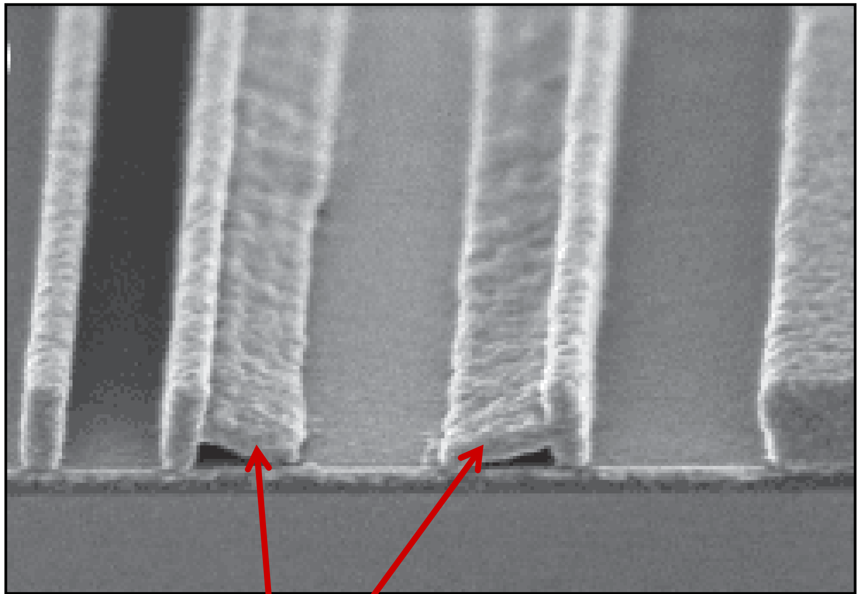
Improving CAA score

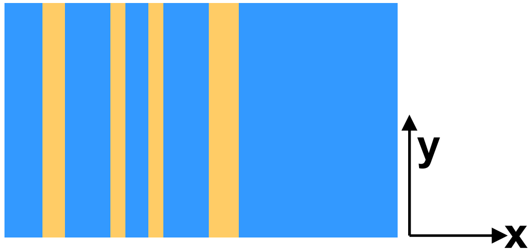
$$C.A = \int_0^\infty P(r) \cdot A(r)\, dr$$

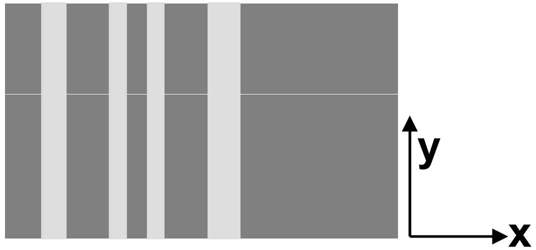


Improve A(r) by wire-spreading or wire-sizing

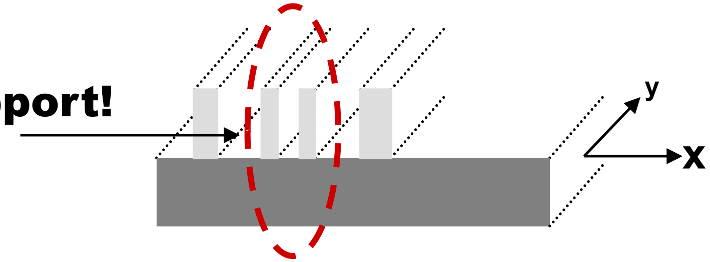
Random Fault: Pattern collapse





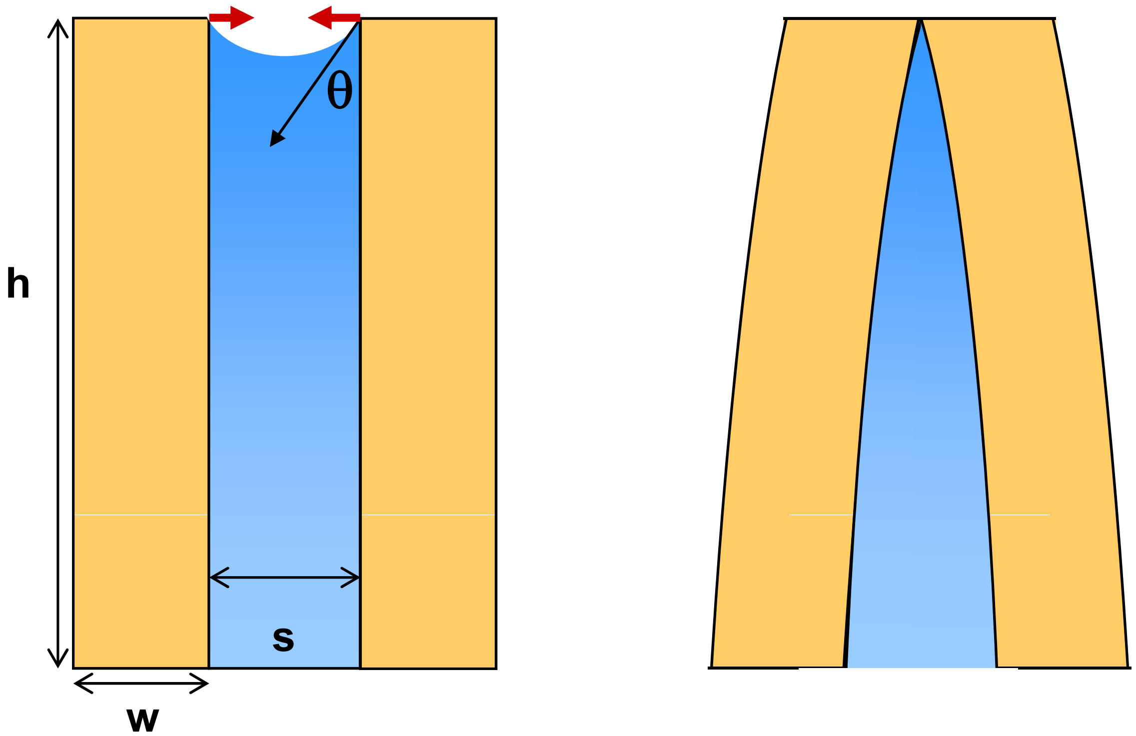


High aspect ratio, without side support!



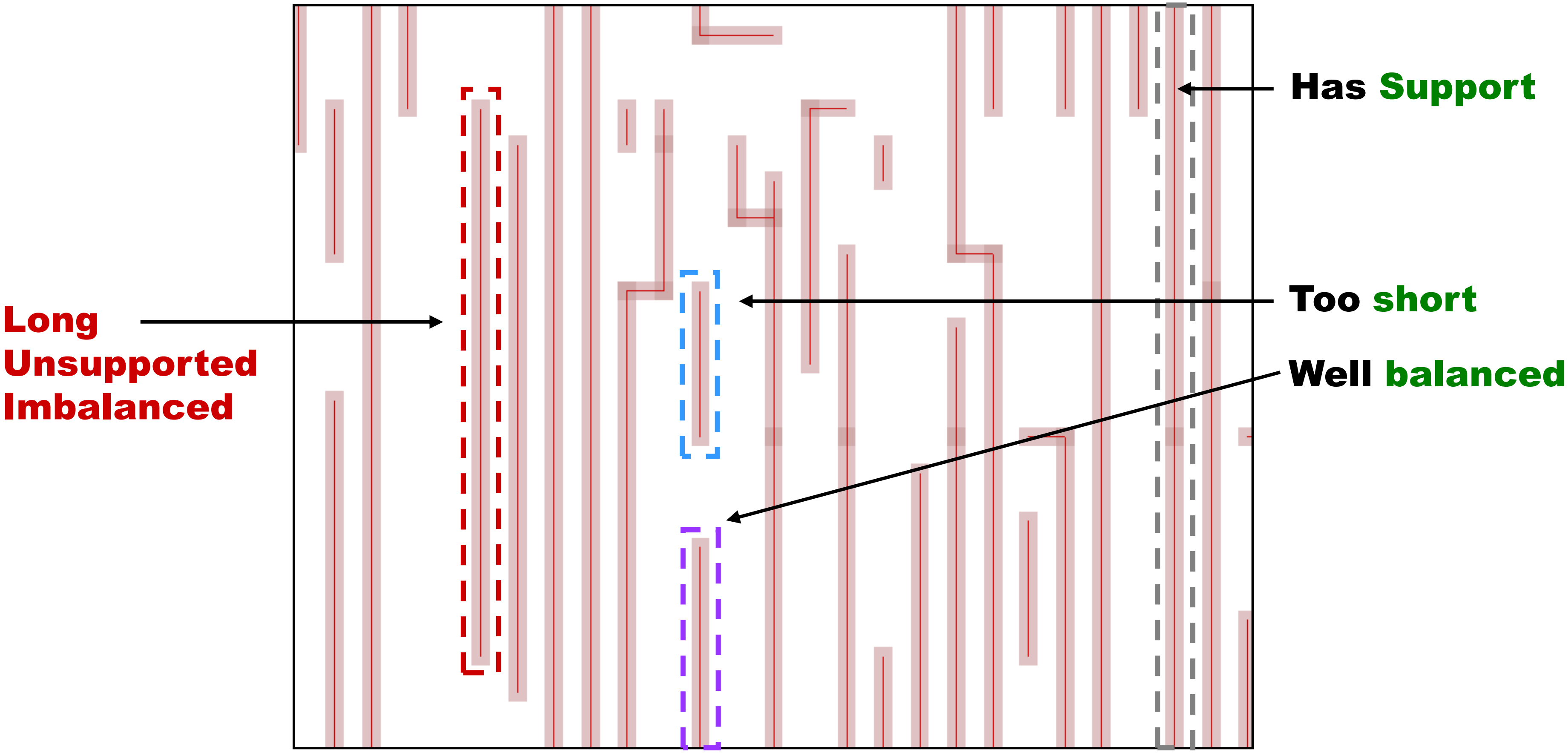
Pattern collapse

Capillary effect



Young's Modulus used to determine snapping point

Potential For Collapse?



Wire-spreading → prevent collapse

Conclusion

Variability

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  - Particle Defects
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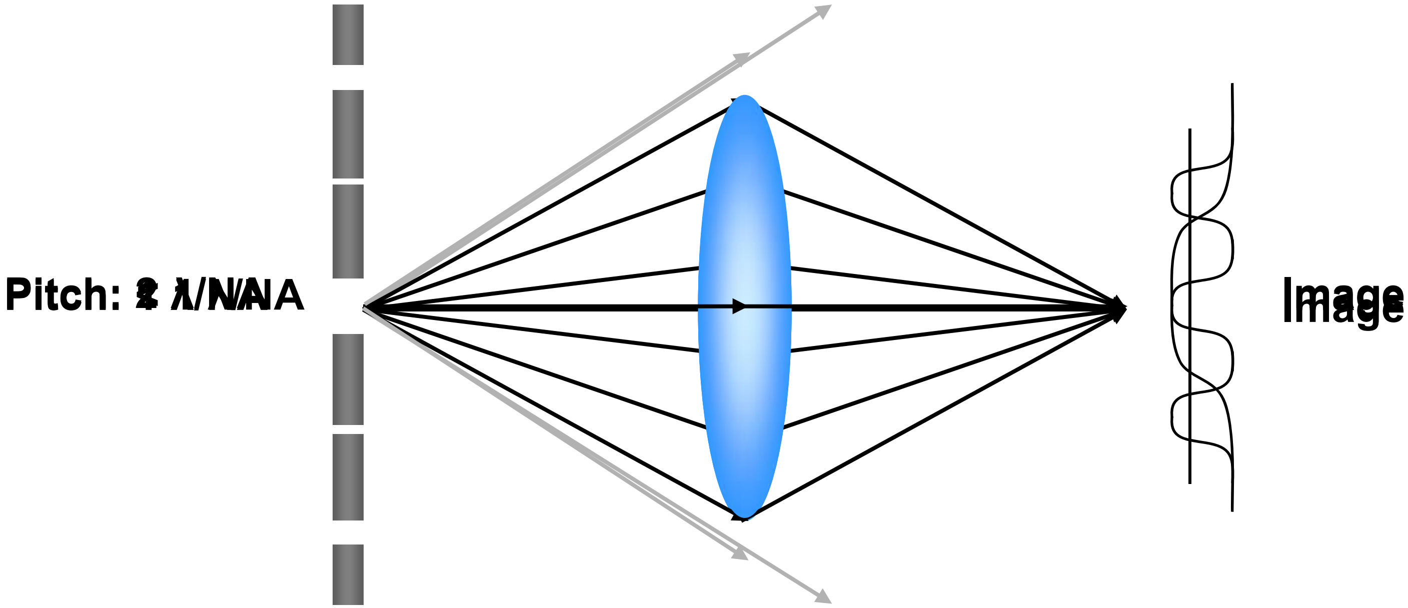
Proper models are key to addressing variability

Acknowledgements

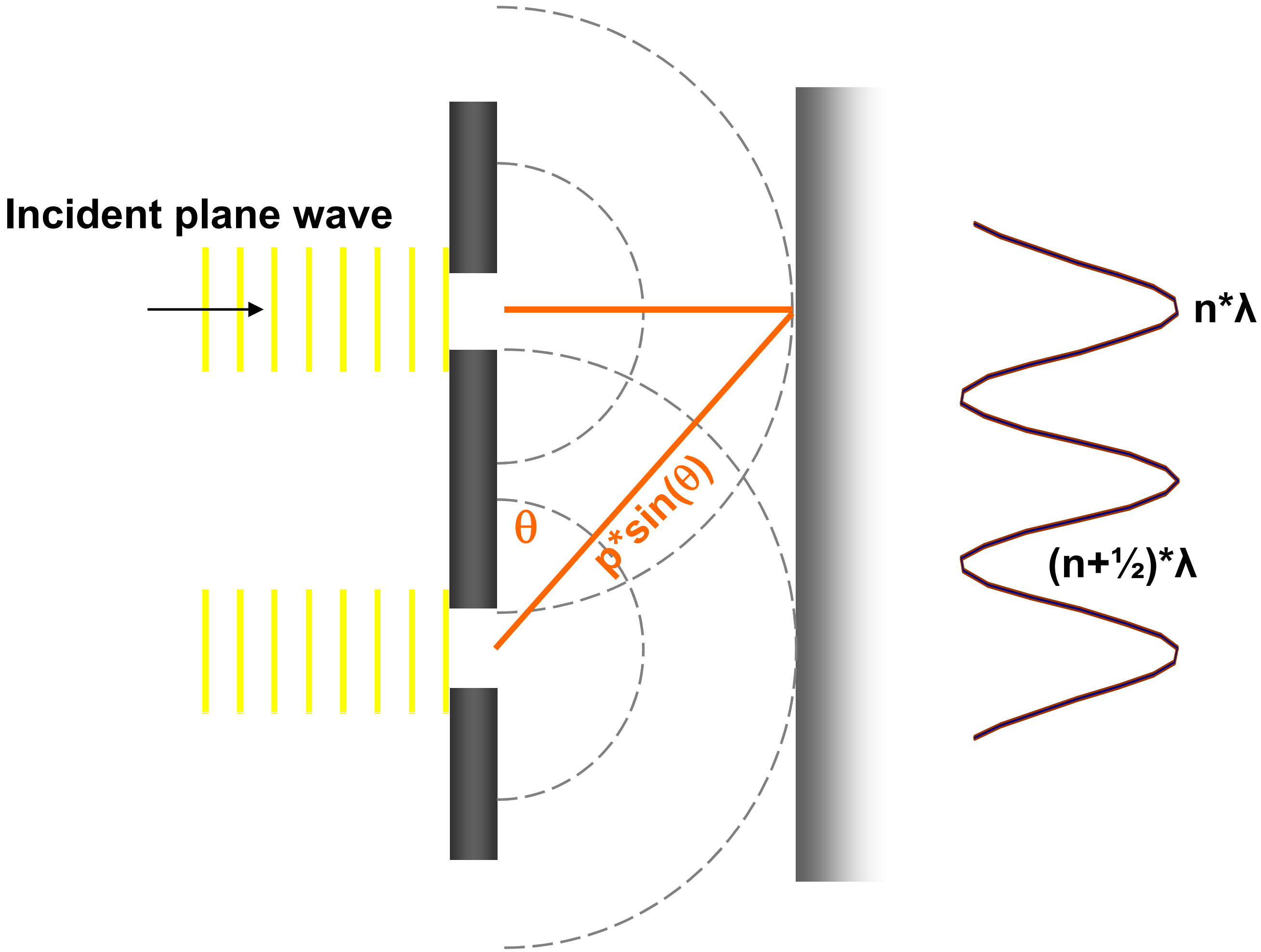
- Andres Torres
- Alex Volkov
- Shankar Krishnamoorthy

Resolution lower-bound

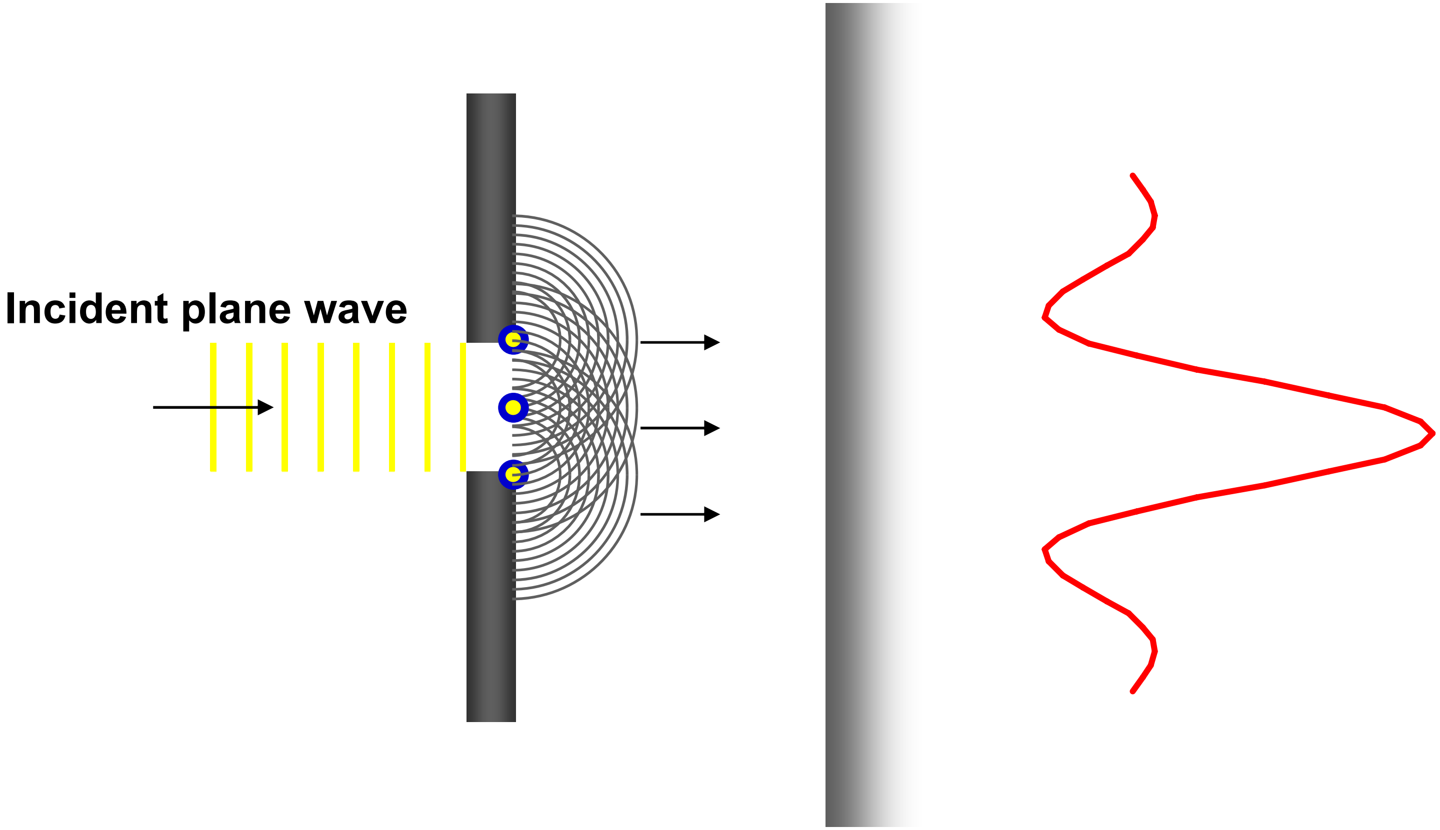


The lens is a low pass filter!
It will suppress frequencies below CD^{-1}

Interference



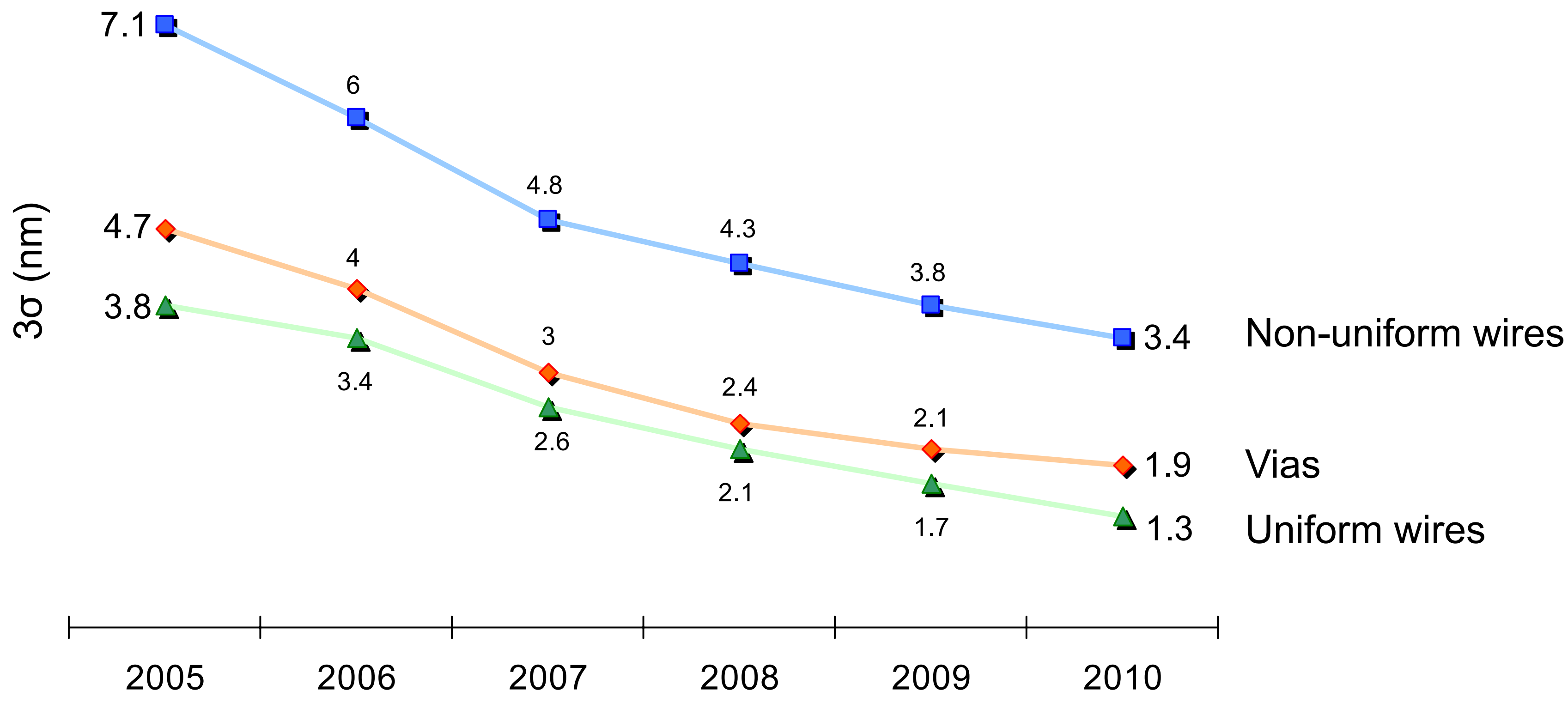
Diffraction



Constructive: n*λ

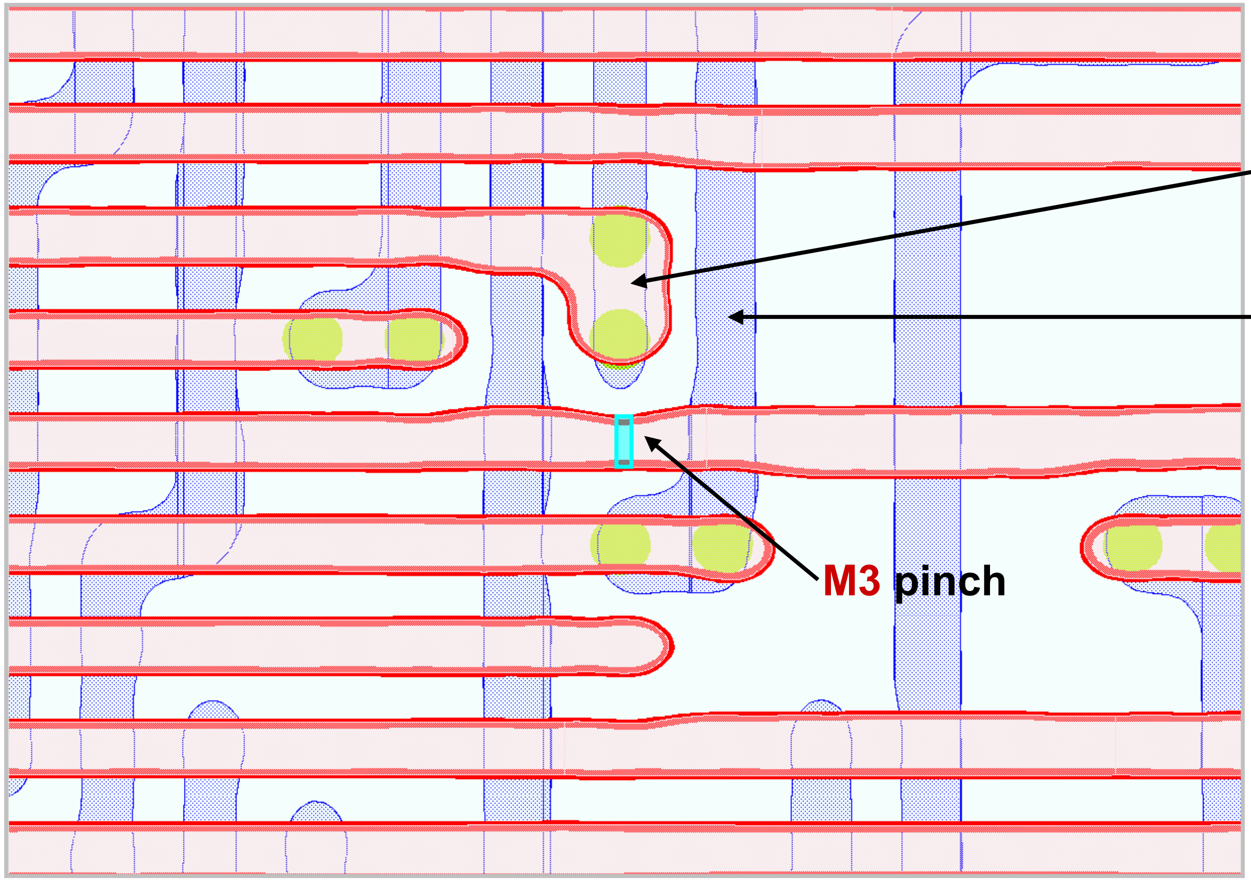
Destructive: (n+½)*λ

Sub-λ stressed by need for increased control

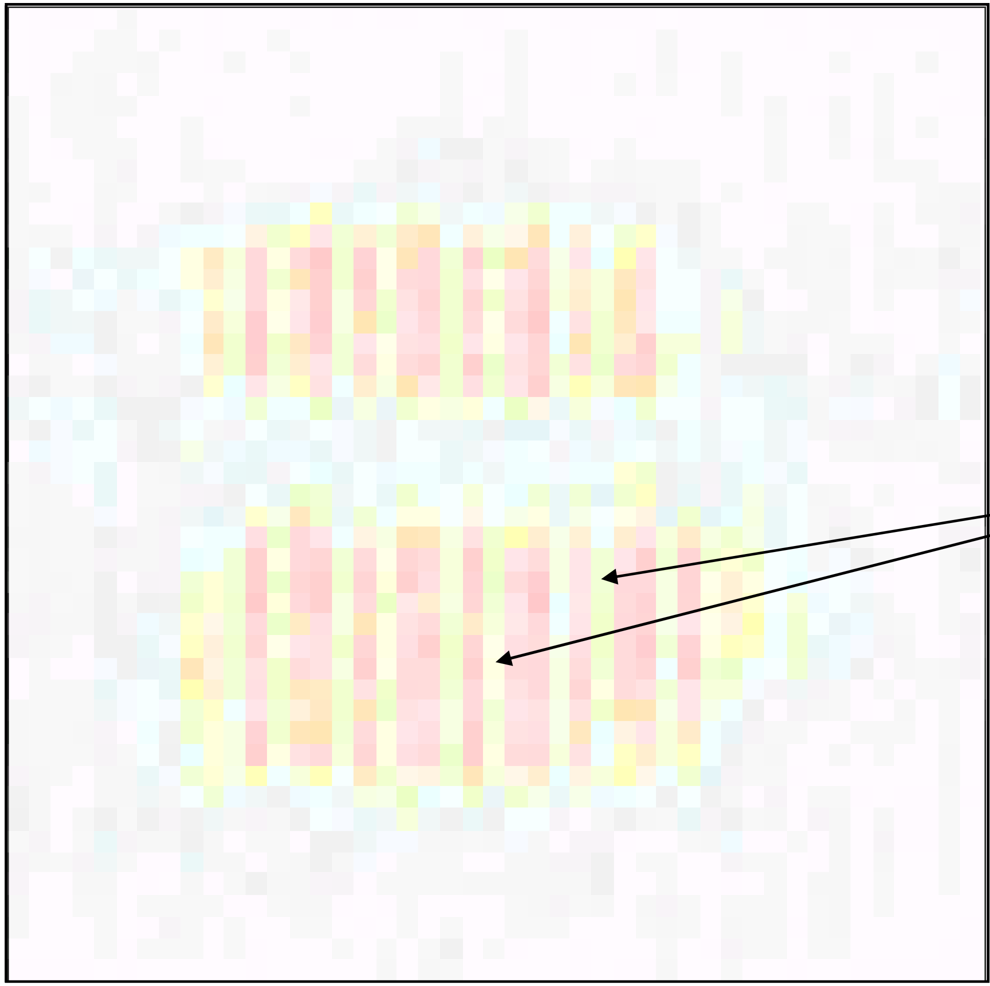


Variance is larger due to non-uniformity

Contacts vs. Metal



CAA on 45nm design



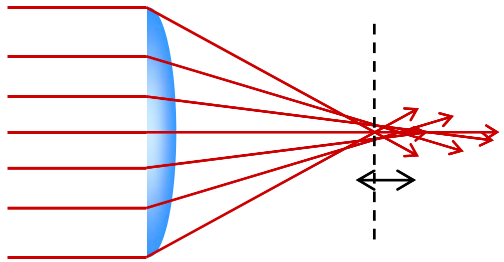
Metal 2

Metal 3

Metal 4

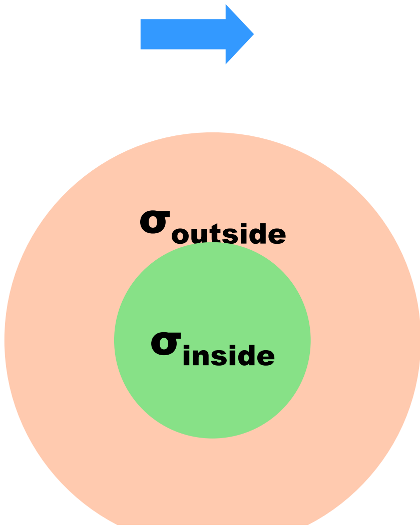
Stripes due to power lines

O.C.V: Systematic variation for a Timer



Spherical aberration → Focus

Resist Coating, CMP Planarity → Etch Thickness



$\sigma_{outside} > \sigma_{inside}$

Chips inside have less variation → they sort into faster bins!
Location Based OCV

CAA: How is P(r) determined?

- **Inline Particle Detectors shine a laser on the wafer and detect scattered light**
- **Scattering intensity is proportional to particle size**