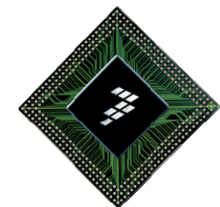
April 14, 2008

Variations, Margins, & Statistics



2008 ISPD

Patrick McGuinness

Freescale Semiconductor

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Variations, Margins, & Statistics

- Variations
- Margins
- Statistical STA
- Statistical STA Flow Benefit
- Variation-aware Timing Flow

"Facts are stubborn, but statistics are more pliable." ~ Mark Twain

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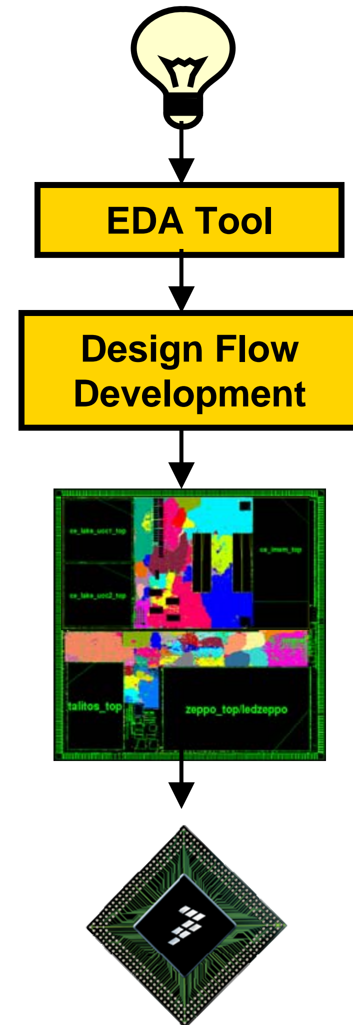
Perspective

- IC design & manufacturing - Freescale
- Design flow development
- Adopting Statistical STA to improve design-for-variability & reduce margins



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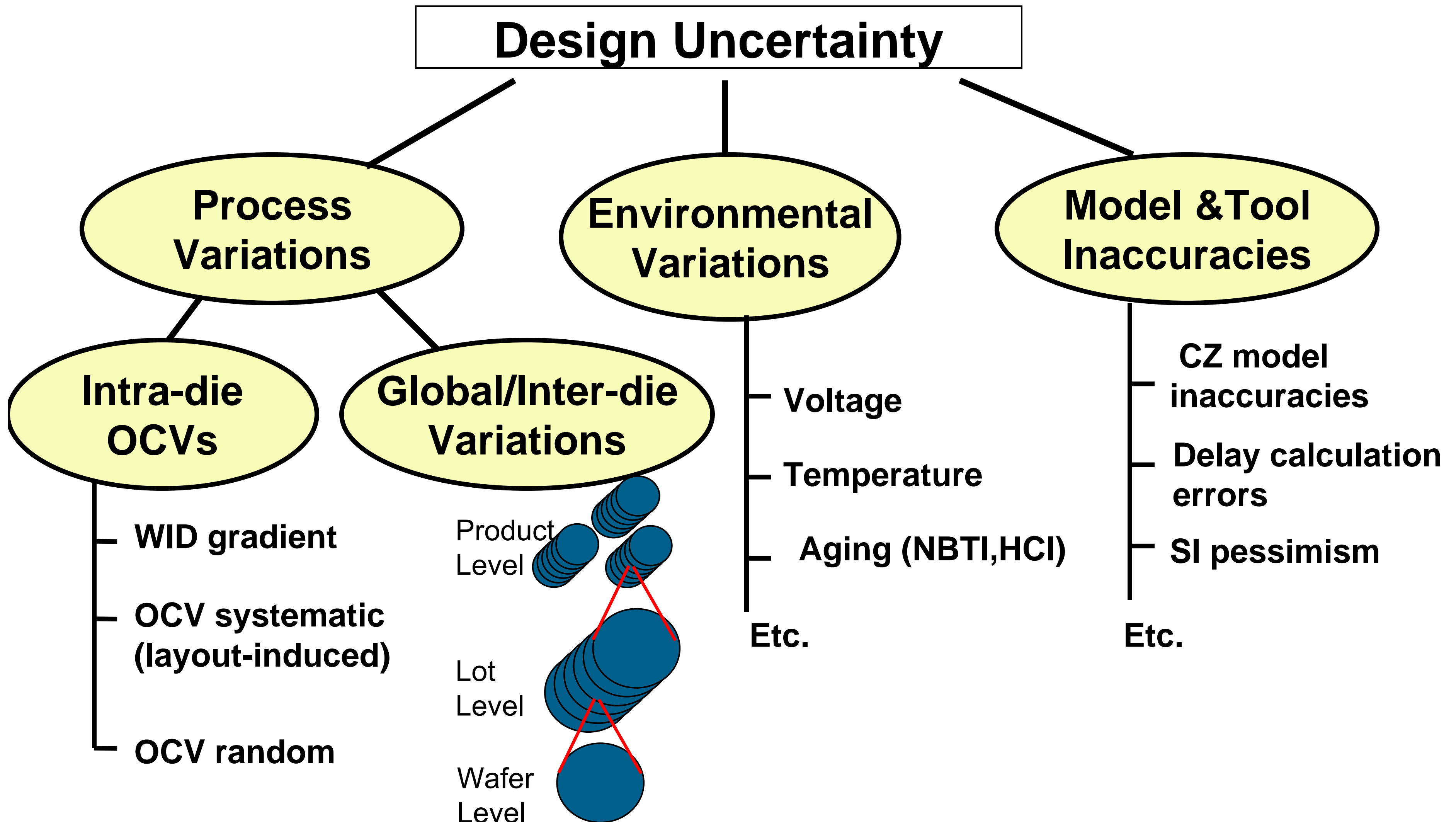
Design Uncertainty



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Process Variations & Trends

Scope	Trend	Description / Sources
Global	Important, stable	• Lot-to-lot, wafer-to-wafer changes in focus, dose, etch, etc. Wafer-level non-uniform gas flow, focus, resist coat, etc. • Process tool change impact on metal layers.
OCV WID gradient	Small (.3%/mm 3σ)	• ACLV of transistors due to non-uniform processes on die.
OCV systematic (layout-induced)	Increasing complexity & impact	• Layout-dependent lithography interferences, varies Leff and metal width. • Layout-dependent stress effect, impacts mobility. • Well proximity effect. • CMP-induced metal thickness variations, eg., dishing, erosion.
OCV random	LER & RDF increasing	• Random dopant fluctuation (RDF), line edge roughness (LER). • Metal-layer line-edge roughness.

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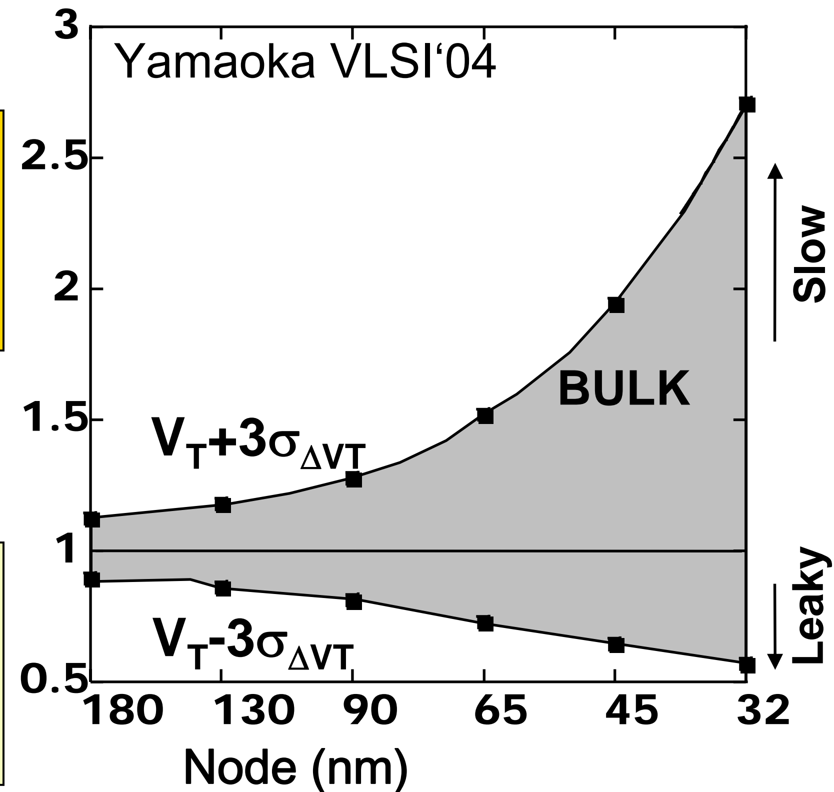
Random device variation

V_T Variability is increasing

- **2X from 65nm to 32nm [ITRS]**
- **Random Dopant Fluctuation**



Mismatch variation @65nm:

Skew 3-σ = +/- ~11%

Paired 22-stage 65nm ring oscillators

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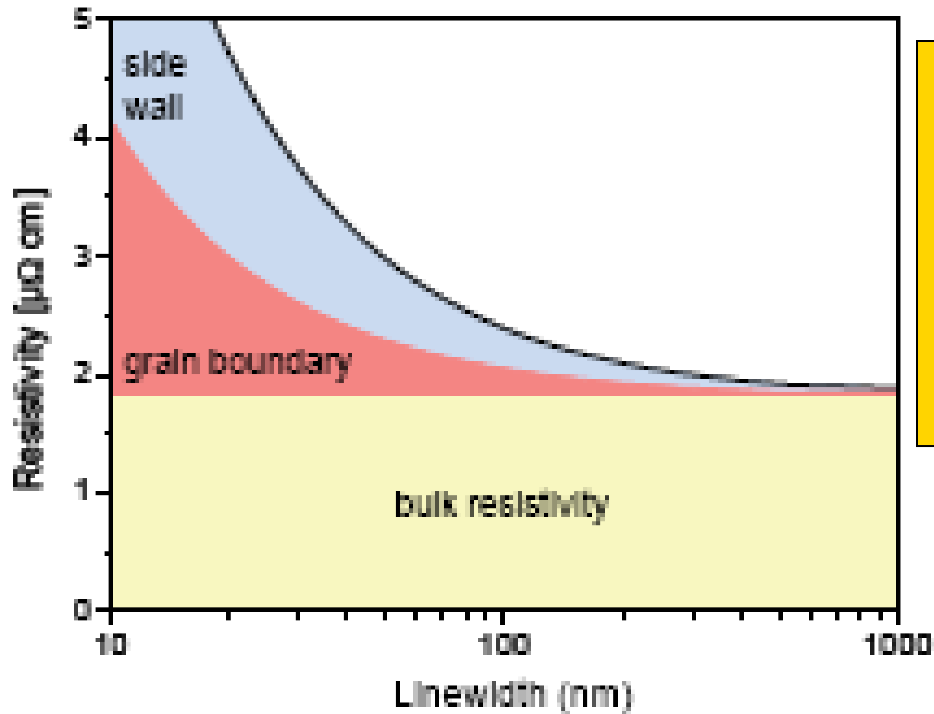
Resistivity Rampup

Resistivity (ρ) increases exponentially as width decreases under 100nm



- Induces skewed Resistance variation
- Higher R
- Higher R variation

ITRS 2007 Roadmap

Figure INTC1 Cu Resistivity

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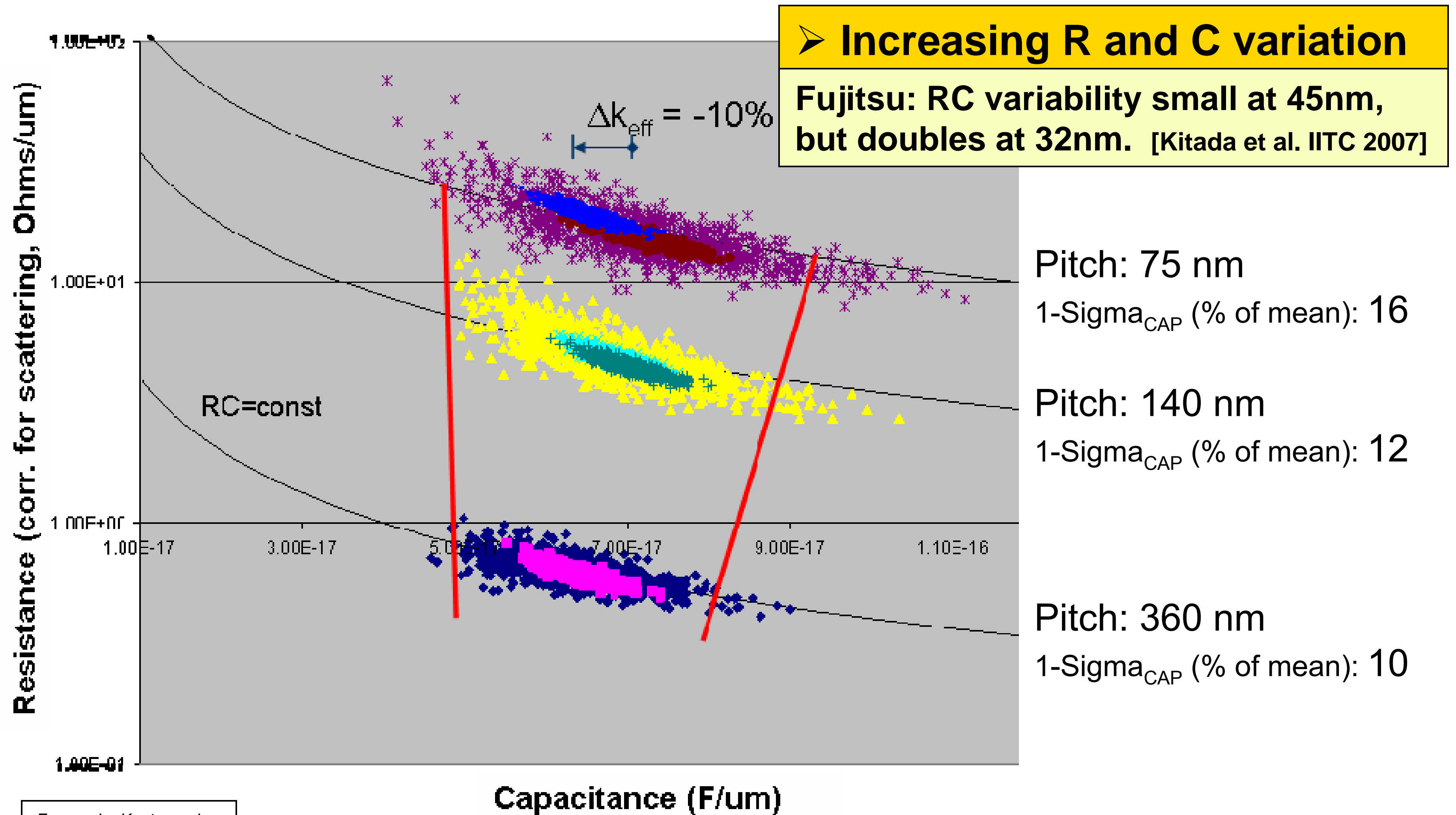
Interconnect Variation Trend



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Resistance variation components

Ave: 3.694
Std: 0.3339
Var: 0.1115
#Points: 1281
MS: 0.00664
Weight factor for MS: 1
Weighted MS: 0.00664
Variance from this level alone: 0.00664
Data Grouped by SubGrp:
Ave: 3.69
Std: 0.3242
Var: 0.1051
Ave Var of Groups: 0.006618
#Points: 144
MS: 0.003707
Weight factor for MS: 8.896
Weighted MS: 0.03297
Variance from this level alone: 0.00296
Ave: 3.491
Std: 0.4538
Var: 0.2059
#Points: 13665
MS: 0.06035
Weight factor for MS: 1
Weighted MS: 0.06035
Variance from this level alone: 0.06035
Data Grouped by Wafer_ID:
Ave: 3.494
Std: 0.3867
Var: 0.1495
Ave Var of Groups: 0.06135
#Points: 404
MS: 0.01655
Weight factor for MS: 33.82
Weighted MS: 0.5598
Variance from this level alone: 0.01476
Data Grouped by Lot_ID:
Ave: 3.483
Std: 0.3605
Var: 0.13
Ave Var of Groups: 0.01343
#Points: 57
MS: 0.13
Weight factor for MS: 239.7
Weighted MS: 31.16
Variance from this level alone: 0.1276
Total variance from Mean Sums: 0.2027
data from C45 SGPC's was normalized to units Ohm/um.

ANOVA (C45 data):

Mismatch 3.12 %

OCV 1.26 %

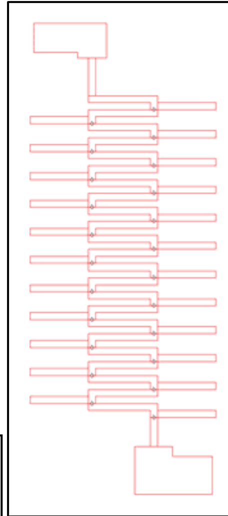
Local <5%

Die-2-Die 28.4 %

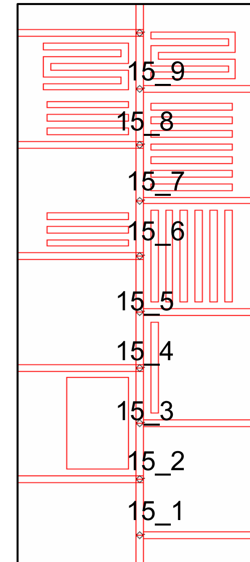
Wfr-2-Wfr 6.95 %

Global 95%

Lot-2-Lot 60.1 %



Dense vs ISO:
Mismatch=29%
of total variation (C90)



Measured structure:
M1 line, 1.0 um long, 0.12 um wide, OPC.
Avg: 0.529 +/- 0.085 Ohm

- **Global is dominant R variation factor**
- **Layout-induced systematics matter (litho, CMP)**
- **Ignore local/mismatch**

Freescale: Kastenmeier

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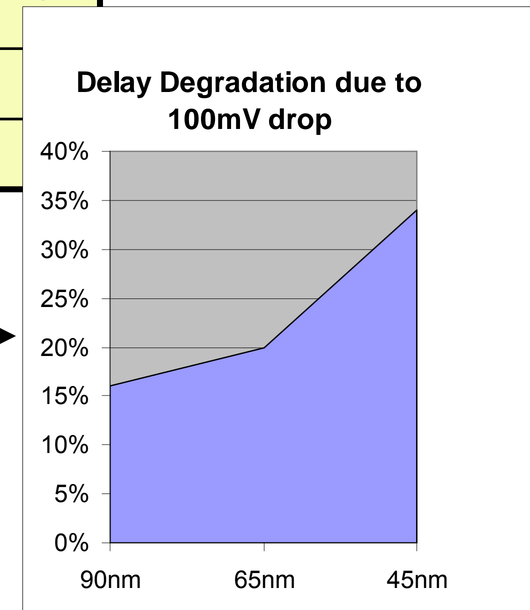
Environmental Variations

Scope/Type	Description
Operating - Voltage	Device dependence on voltage due to IR drop.
Operating - Temperature	Dependence of transistor operation on temperature.
	Dependence of Metal R and C on temperature.
Operating - Clocks	Clock jitter, due to PLL and clock generator process variations.
OCV – Aging	Negative bias temperature instability (NBTI). Hot Carrier (HCI).
Operating - SOI	SOI history effect, varies substrate bias.
Operating	Different well voltage due to (dynamic) well biasing.



Trends:

- **Voltage: Increasing sensitivity/impact**
  - V drop causes quadratic timing degradation
- **Temperature: inversion effect - V_T vs mobility**
- **NBTI increasing**

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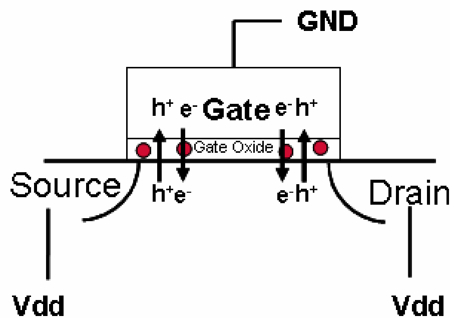
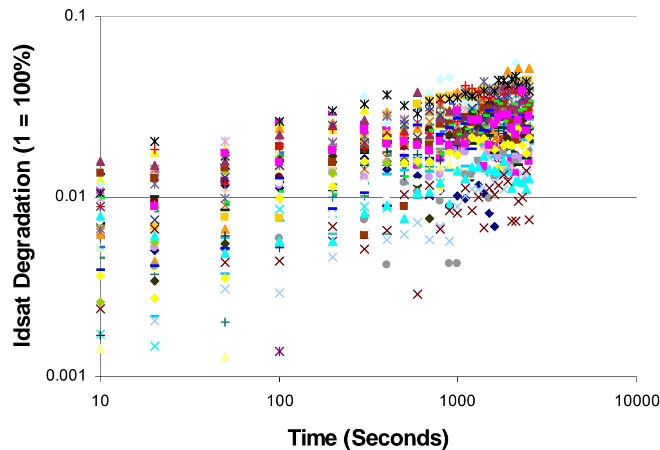
NBTI Variability



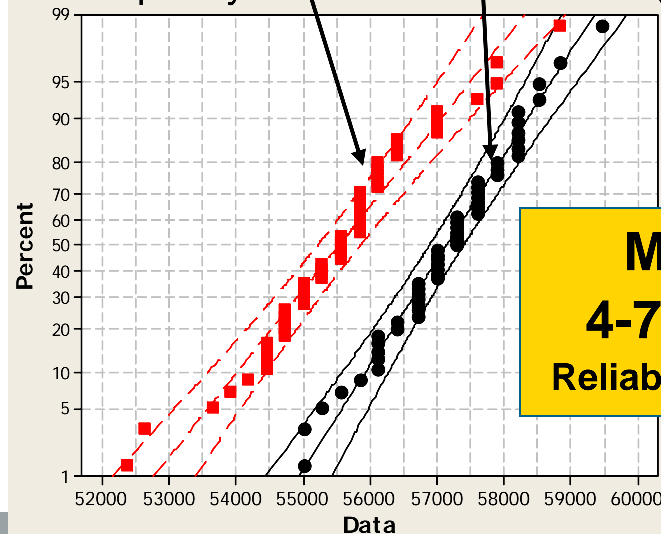
NBTI: Negative Bias temperature instability

- Increase in gate V_T from trapped charges
- **PMOS only**
- **Switching activity-based**
- **Statistical effect**
- Result: Frequency degradation with wider distribution



Freescale C90 stress test data

Frequency before and after burn-in (mimics NBTI)



Margin hit:
4-7% for NBTI
Reliability (0.1% failure)

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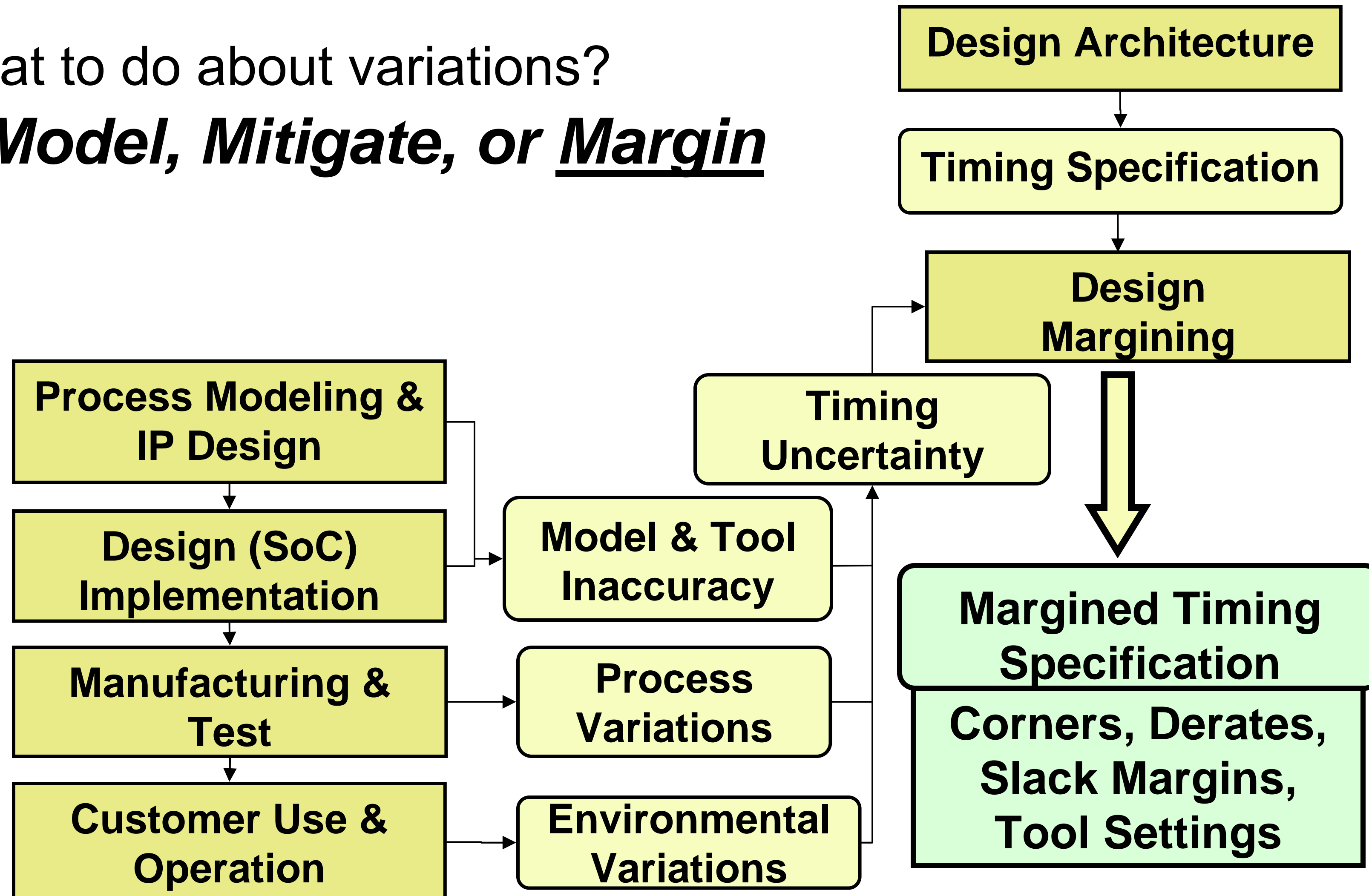
Margins

What to do about variations?

Model, Mitigate, or Margin



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► Corner explosion …

- More Modes, e.g., multi-voltage (DVFS)
- Temperature Inversion: need both cold and hot T
- More Extraction corners: RCmax, Cmax, RCmin, Cmin, RCtyp, Xtlk, …

Example 65nm recommendation:

Setup: {4 extraction corners} x {2 device corners} = 8 corners / mode
Hold: {4 extraction corners} x {3 device corners} = 12 corners / mode

► Margins and derates ramping up

- Random variation, voltage & interconnect skew effects

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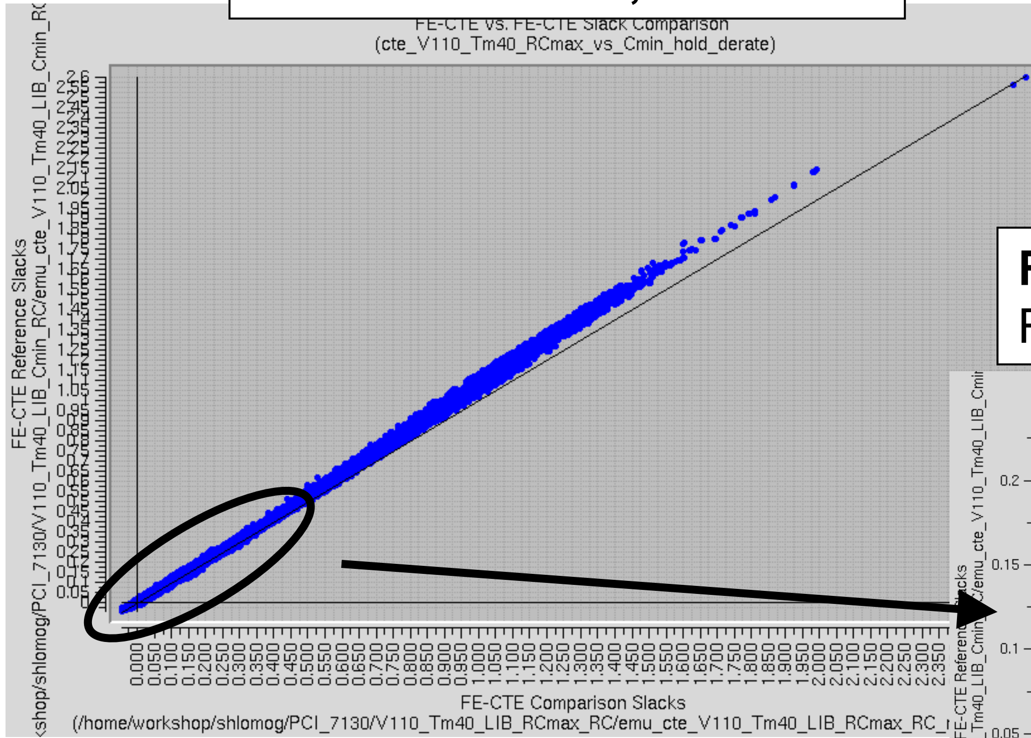
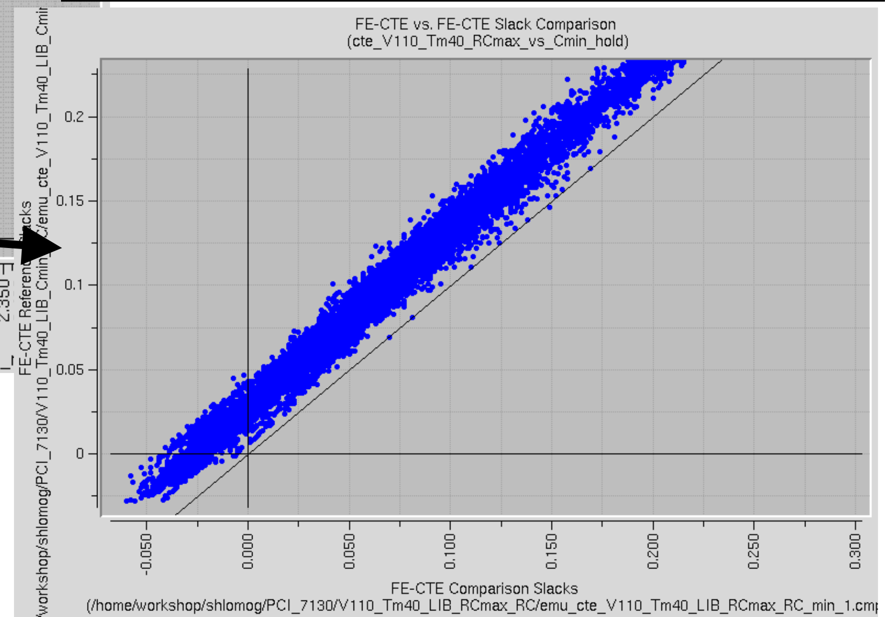
We Can Cut Corners … For a Price

RCmax vs. Cmin, no derate



RCmax vs. Cmin, with derate 1.5%
RCmax 'covers' Cmin with derate



Freescale C65 data

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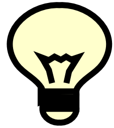
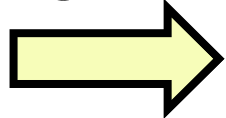
Variation-Aware Flow Challenge



Use Statistical STA to model variations



Reduce timing margins

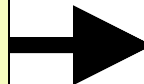
Challenge: An effective Statistical STA *flow*

- Not just tool: methodology, collateral, models, etc.
- Validate "Return on Flow Investment"

  "Does adoption benefit justify the effort/cost?"

For each parameter/feature:
Can we measure, model, build in tool and validate?

What's the impact?



Model The Big Stuff,
Margin The Small Stuff

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Statistical STA – A “normal” configuration

Parameterized block-based & path-based Statistical STA

$$D = \mu + \sum_{i=1}^{n} a_i \Delta X_i + a_{n+1} \Delta R$$

μ = mean delay

ΔX_i = Variation for X_i param

ΔR = Random variation

a_i = Gate sensitivities

- ► Sensitivity-based (delay, slew)
- ► Linear (Gaussian) parameters
- ► Block-based max operation preserves linear model
- ► Linear algorithm

In:	**Out:**
► **Device Globals & Random** ► **Interconnect (W, T, ILD / layer)** **“Keep SSTA Normal”**	• **No within-die gradient** • **No Voltage and Temp vars, V and T are corners (for now)** • **No non-gaussian**

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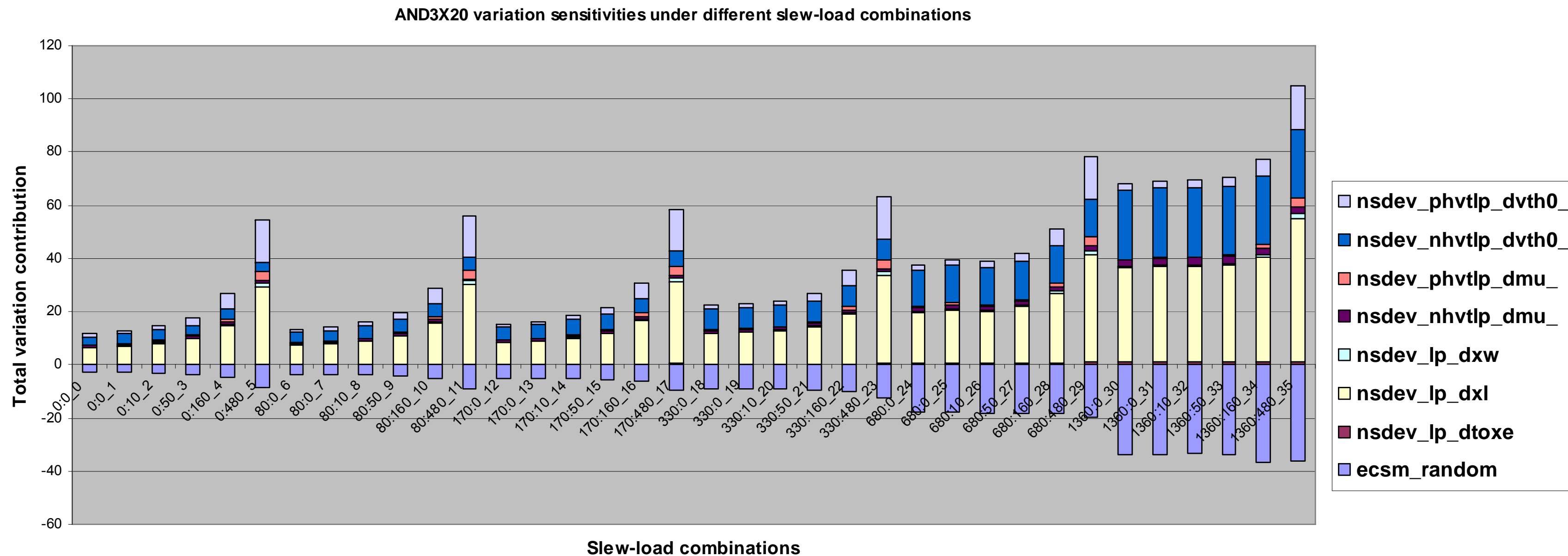
Cell Level Sensitivities Contribution



Freescale C65 data

Major device variation components: Random, Leff, Vt

- **Relative contributions of parameters changes (P-loaded vs N-loaded)**
- **Random and other variations increase with increase slew/load (7X diff)**

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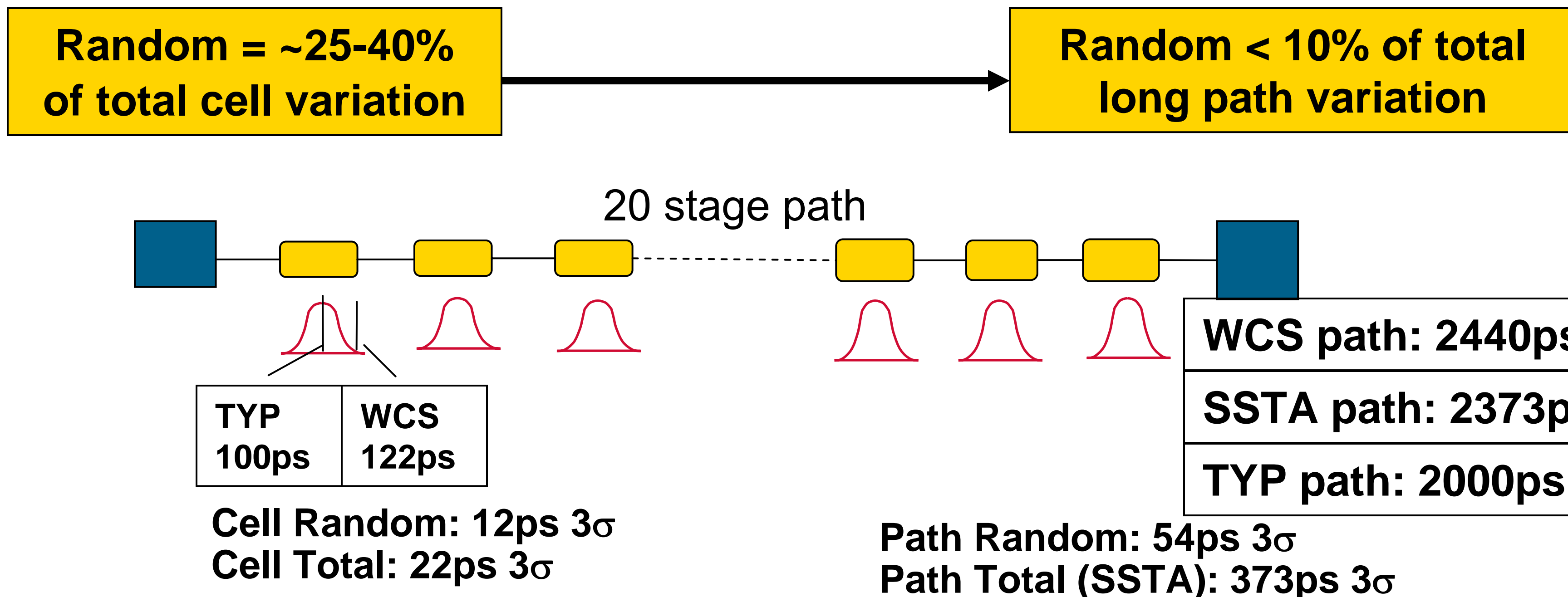
Device Corner Pessimism

DSTA corners are pessimistic

Real path variation is not a linear sum of cell variation

- Each independent global variation accumulates at linear rate
- Independent global variables are combined with RSS
- **Random variation accumulates at root-sum square (RSS) rate**



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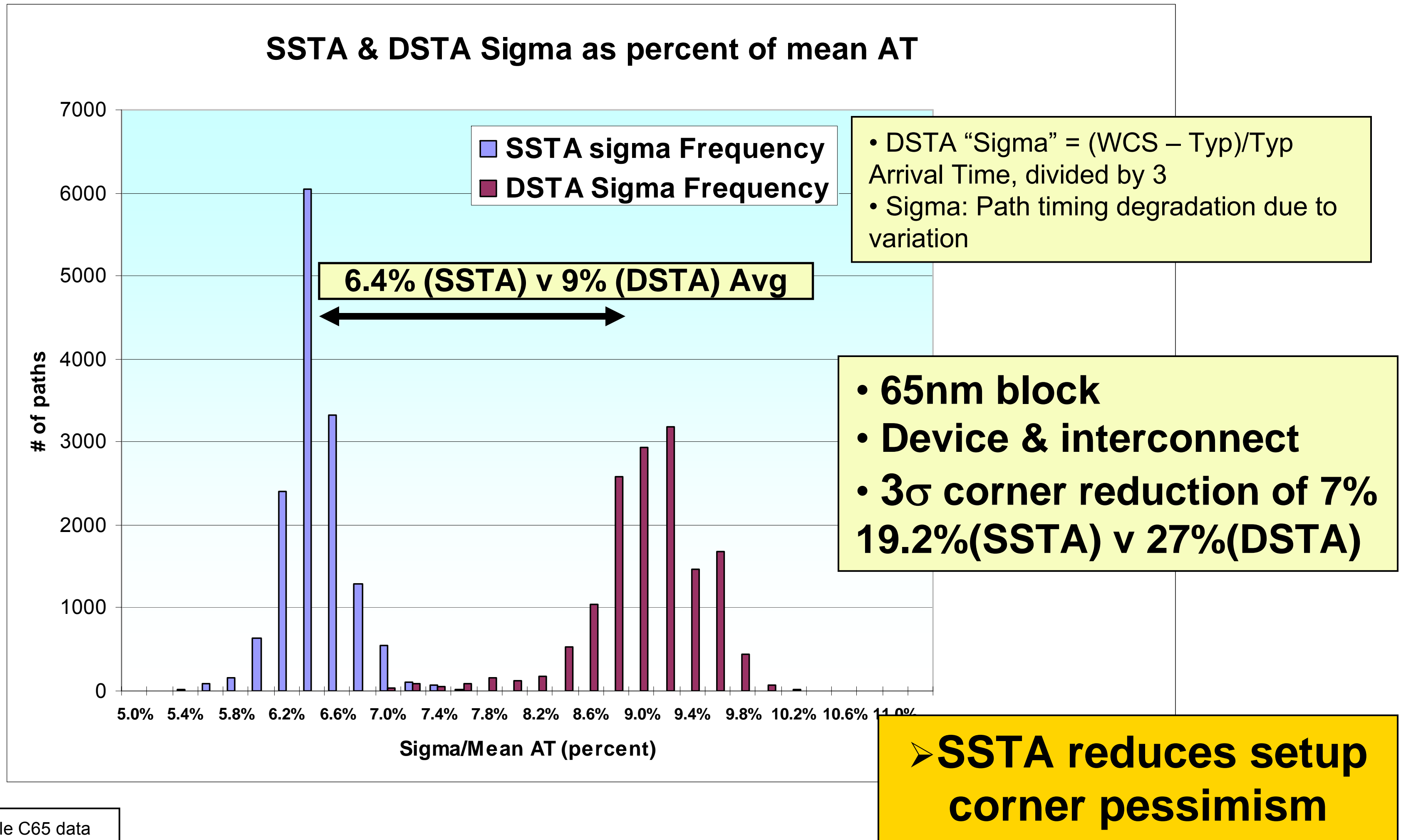
Corner Pessimism – SSTA v DSTA



Freescale C65 data

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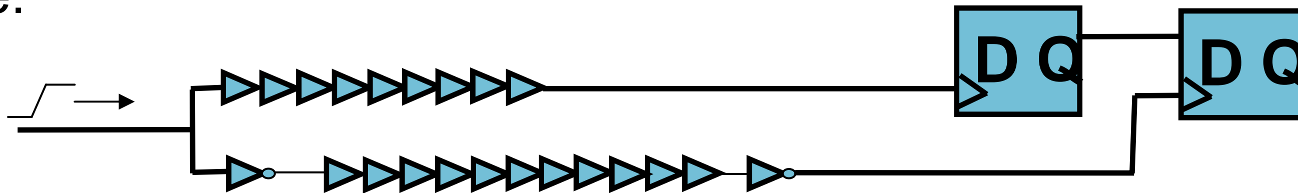
Device OCV Correlations and Sensitivities

Random & independent global variation-induced skew

- Uncorrelated global variations cause skew in non-common paths

Example:



Launch sensitive to PMOS, capture path sensitive to NMOS

- Random variation skew

> ➢ **SSTA measures skew impact from random and non-correlated global variations.**
> ➢ **DSTA cannot – hold margin and design risk.**

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Interconnect Model vs Reality

Reality: Interconnect metal layers vary independently

- Mx-My variance correlations of ~0.2 to 0.5 [Freescale data],

Reality: Worst-delay corner is context-dependent [Fukuoka, ISPD07]

- Shorter nets C-dominated, longest nets RC-dominated
- "Worst-case" Cmax is not taking longest paths to real worst-case

> - **Uniform metal corner extraction model is wrong**
> - **SSTA and sensitivity-based extraction is better**

- **Net variation impact on typical path AT: 3σ = ~2.5%**

- **Metal layer independence skew effect**
  - M2/M3 metal skew testcase in 65nm: **3σ skew of 13%**

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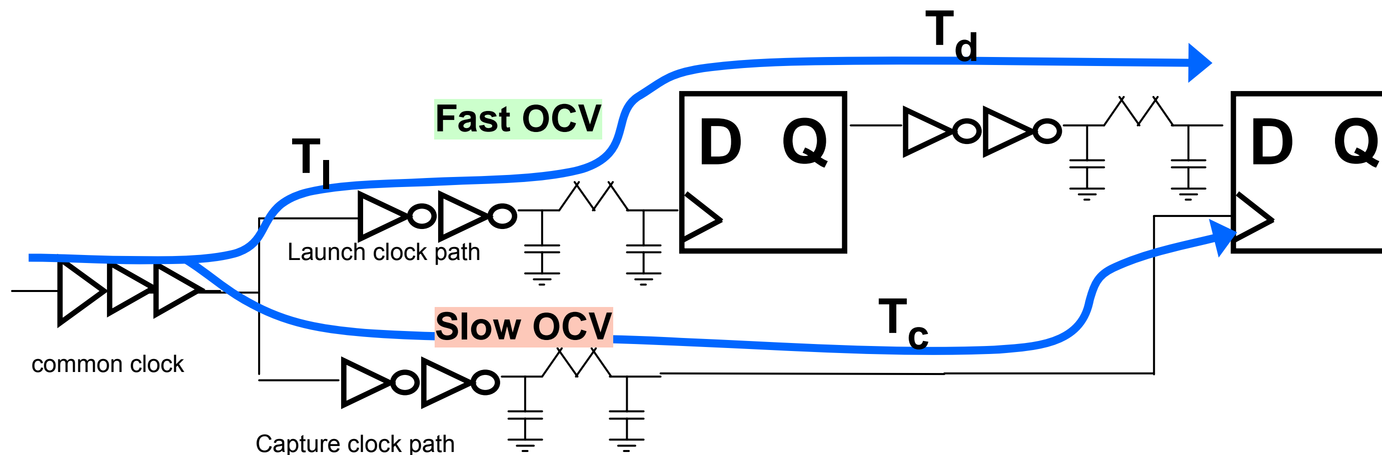
Hold Derate Reduction

Hold dominated by clock path skew

- **Low-power SoC w/ power gating, V domains, hard IP, CTS**
  - **Hampers variation-mitigation**
- **Hold margin derate @ 65nm: 16%**

SSTA:

- **OCV random variation-induced skew (3-5%)**
- **Non-correlated metal layer and global skew (0-3%)**



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Statistical STA - Return on Flow Investment

Cost:	Benefits:
➢ Collateral (CZ) ➢ Model support ➢ Tool runtime ➢ Tool memory ➢ Flow complexity	➢ Reduce hold margin • Model device OCV and metal skew ➢ Interconnect corner reduction ➢ Reduce corner pessimism ➢ Model NBTI ➢ Path timing distributions ➢ Precise yield/timing tradeoffs ➢ Variability-sensitivity reduction

"The rumors of my death are greatly exaggerated." - Mark Twain

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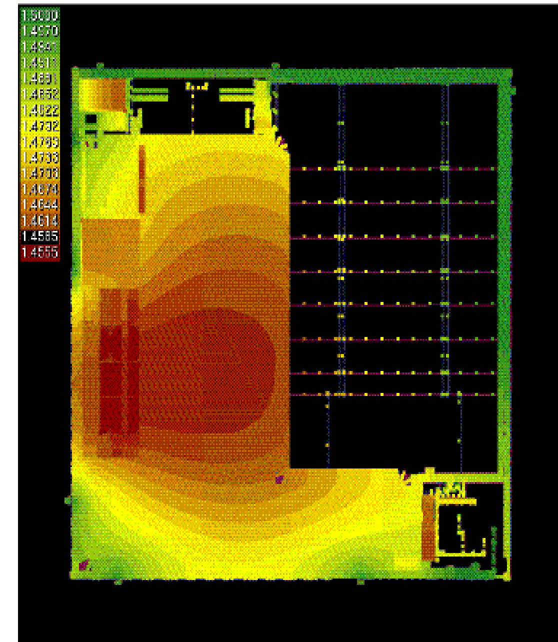
What about Voltage?

Voltage variation solutions

- **Model Voltage range as OCV in SSTA**
  "Don't treat statistically what you can model deterministically"
- **IR drop instance-based timing**
  - What about voltage variation/uncertainty?

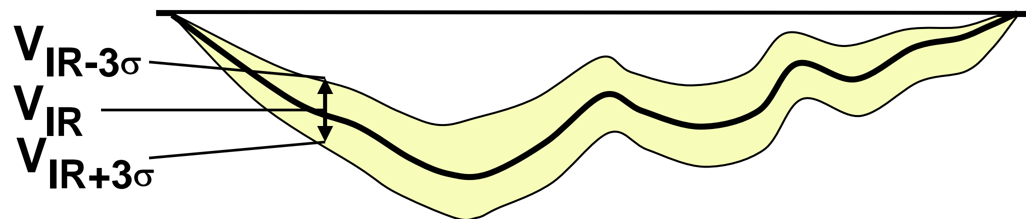


Combined Solution:

- **Measure $V_{IR\text{-}drop}$ per instance**
  - Can be temporal, activity-based
- **Spatially correlated V variation**

Up to 5% hold derate for V drop skew

45nm: 33% timing hit for 100mV drop



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Activity Profile-based Operating Condition

"PVT" is obsolete

► *P, V, T : Device, not global, conditions*

Switching-activity-dependent Analyses:

► Voltage IR Drop, Thermal Analysis, NBTI, Statistical Leakage

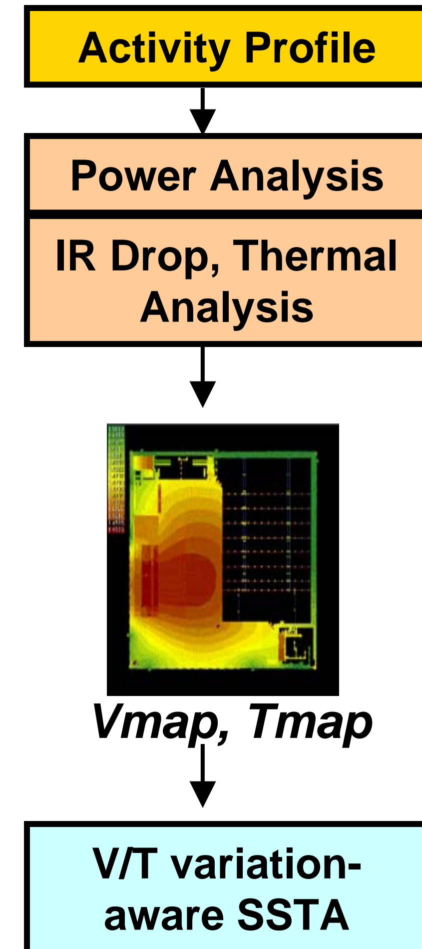
Activity Profile:

► Represents switching activity

► "Corners" – Max Power/Activity, Sleep, Typical

New Operating Condition:

(Activity Profile, process parameters, Derived Vmap, Derived Tmap)



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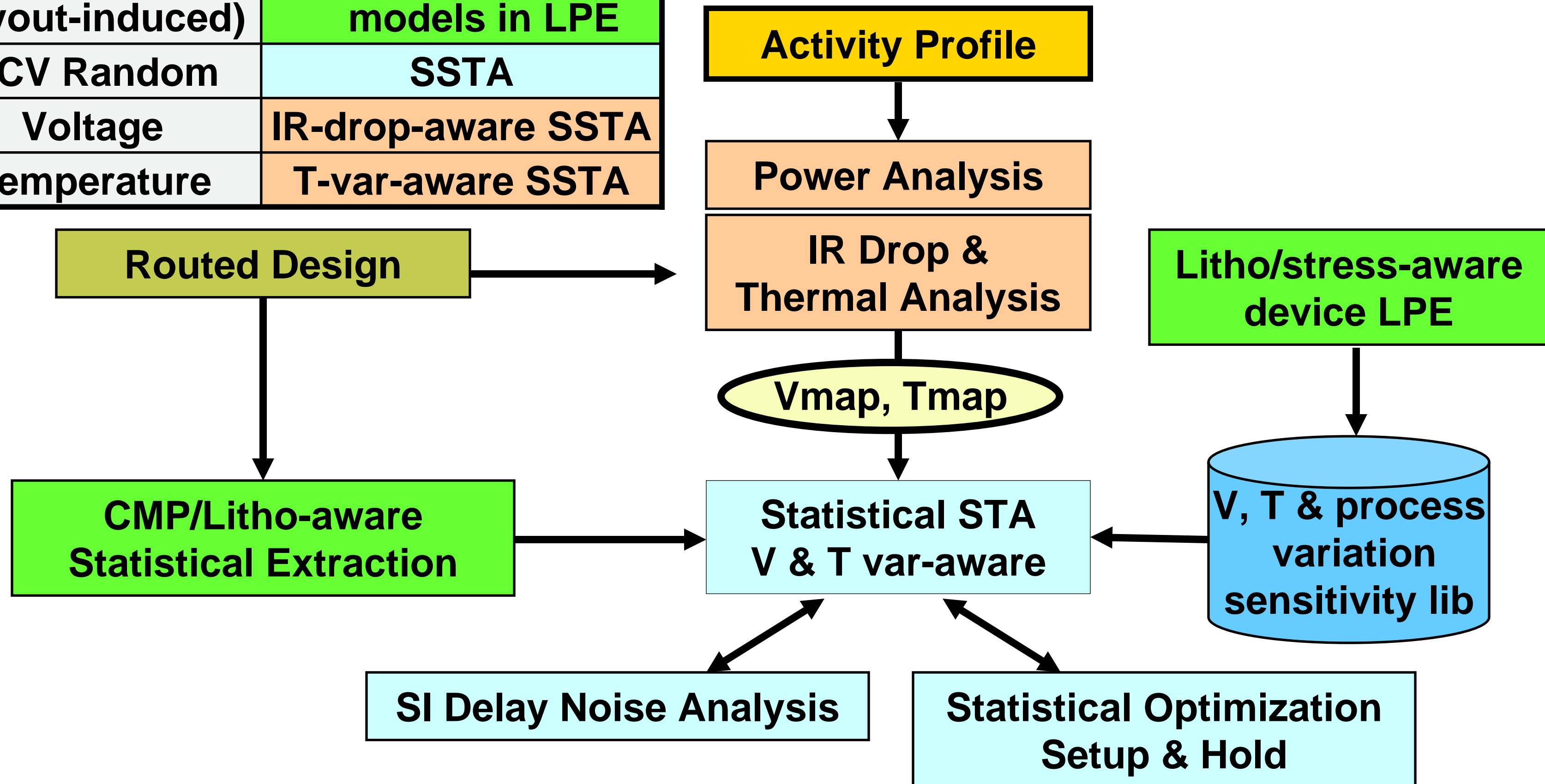
Variation-Aware Timing Flow

Variation	Solution
Global	SSTA
OCV systematic (layout-induced)	CMP, litho, stress models in LPE
OCV Random	SSTA
Voltage	IR-drop-aware SSTA
Temperature	T-var-aware SSTA



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Design-for-Reality

The Big Stuff we must model …
The Small Stuff we can margin away

Variation is Big Stuff!

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Close

Thank you!

Acknowledgement

I acknowledge Freescale colleagues for their assistance and contributions: Andrew Hoover, Terence Liang, Bernd Kastenmeier, Shuling Wang, Arijit Dutta, Hazem Zawaideh, and other members of the Statistical STA working group.

Moral: "Always do right. This will gratify some people and astonish the rest." ~ Mark Twain

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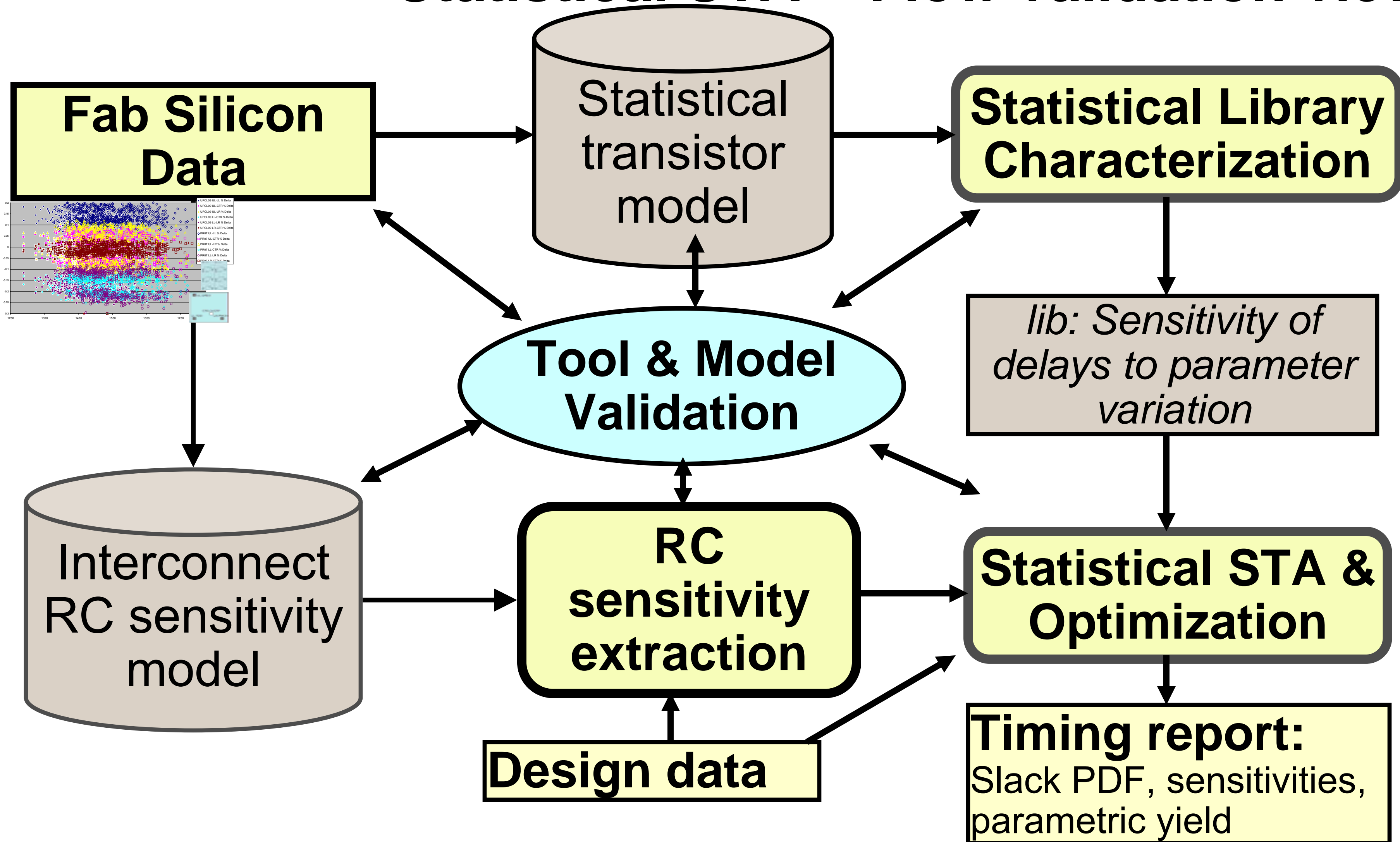
Statistical STA - Flow validation view



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