Metal-Density Driven Placement for CMP Variation and Routability

ISPD-2008

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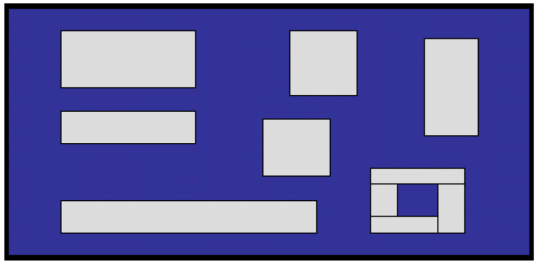
April 14, 2008

Outline

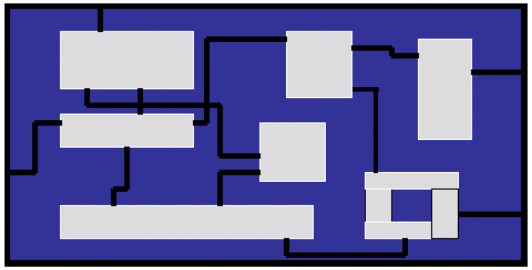
- Introduction
- Review of NTUplace3
- Metal-density driven placement
- Experimental results
- Conclusion

Placement

- Fundamental VLSI problems
  - Placement
  - Routing
- Significant impact on VLSI
  - Wirelength
    - Performance
  - Routability
    - Routing complete rate
  - Manufacturability
    - Topography variation after CMP



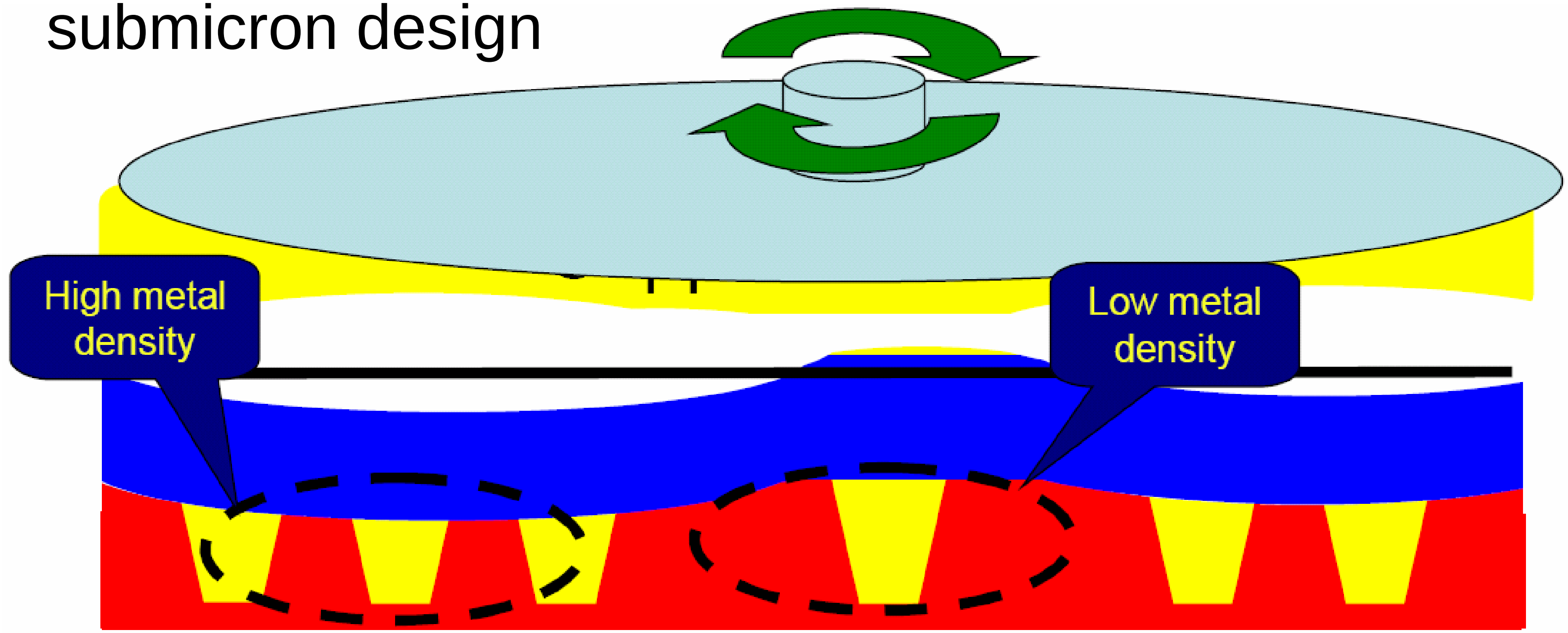
Placement



Routing

Chemical Mechanical Polishing (CMP)

- CMP: Key multilevel metallization technique in deep submicron design



- CMP variation
  - Performance degradation due to increase resistance
  - Printability issues due to non-uniform surface (depth-of-focus)
  - Systematic variation due to non-uniform metal density distribution (dummy fills)

Placement Objectives

- Placement is a fundamental VLSI physical synthesis problem
  - Wirelength-driven placement
  - Timing-driven placement
  - Routability-driven placement
  - Cell-density driven placement

Metal-density has never been considered!

Metal-Density Driven Placement

- Metal-density driven routing was studied by Cho et al., in ICCAD-2006.
  - The average CMP variation is reduced by 7.5%.
  - Metal density is highly related to placement since the metal density optimization in routing is often limited by pin locations.
- Effectively distributing pins and cells into a placement region with metal density consideration can provide better flexibility for routing, leading to better wire density topography.

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NTUplace3

- T.-C. Chen, Z.-W. Jiang, T.-C. Hsu, H.-C. Chen and Y.-W. Chang, "A high-quality mixed-size analytical placer considering preplaced blocks and density constraints" [ICCAD-2006]

- NTUplace3
  - Handles preplaced blocks and density constraints
  - Is based on the multilevel framework
  - Uses an analytical model
  - Obtained the best average placement quality based on the results reported in [Viswanathan et al., DAC-2007] (Was tied with RQL.)

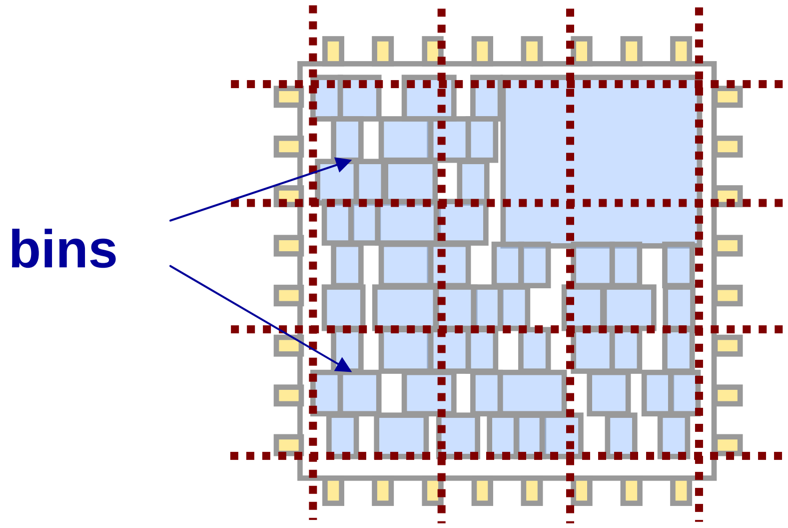
Placement with Density Constraint

- Given the chip region and block dimensions, divide the placement region into bin grids
- Determine (x, y) for all movable blocks

min W(x, y) -- wirelength function

s.t. 1. $\text{Density}_b(x, y) \le \text{MaximumDensity}_b$ for each bin b

2. No overlap between blocks

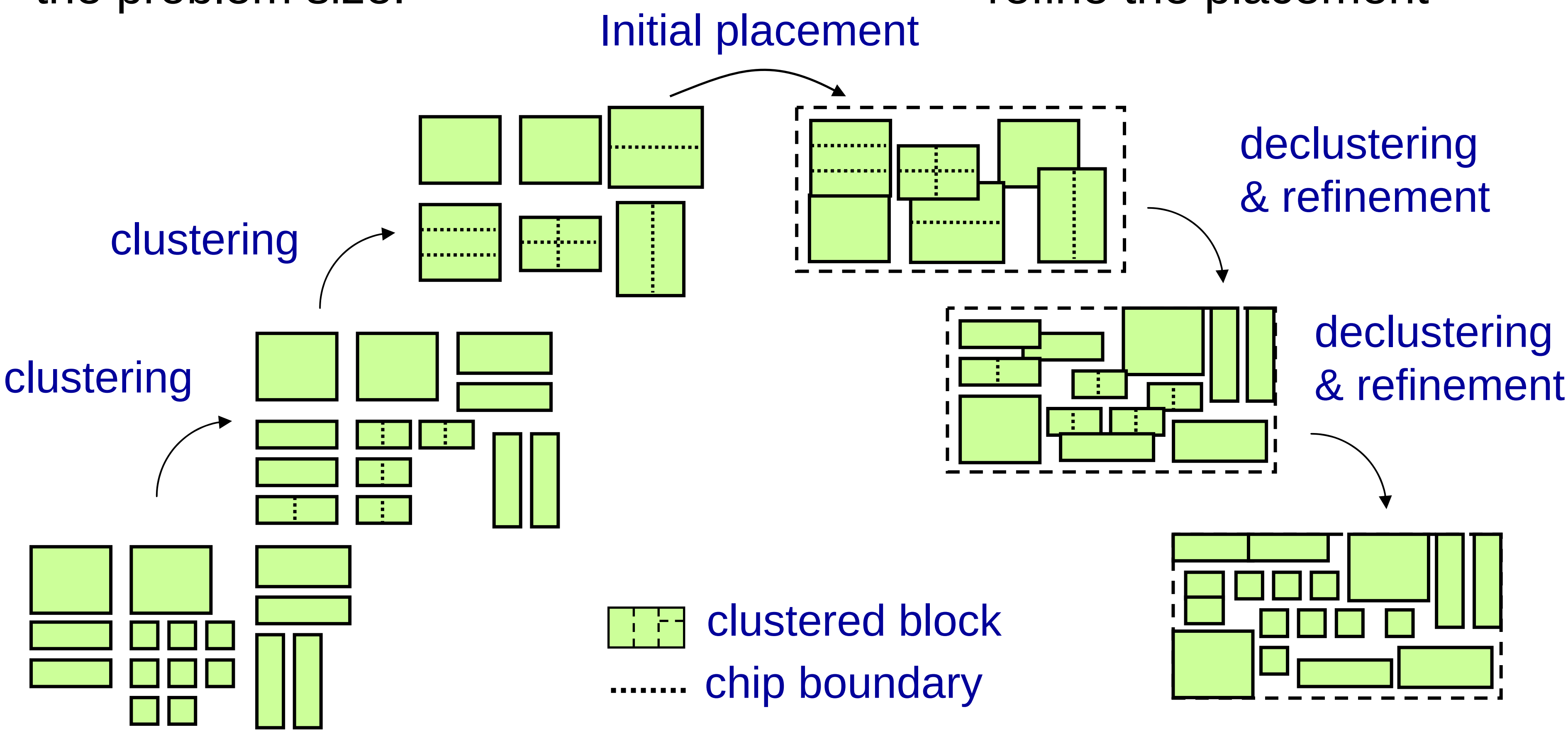


$$\text{Density} = \frac{A_{block}}{A_{bin}}$$

Multilevel Global Placement

Cluster the blocks based on connectivity/size to reduce the problem size.

Iteratively decluster the clusters and further refine the placement



Analytical Placement Model

- **Global placement problem (allow overlaps)**

$$\textbf{min} \quad W(x, y)$$
$$\textbf{s.t.} \quad D_b(x, y) \le D_b^{max}$$

Minimize HPWL

D_b: density for bin *b*

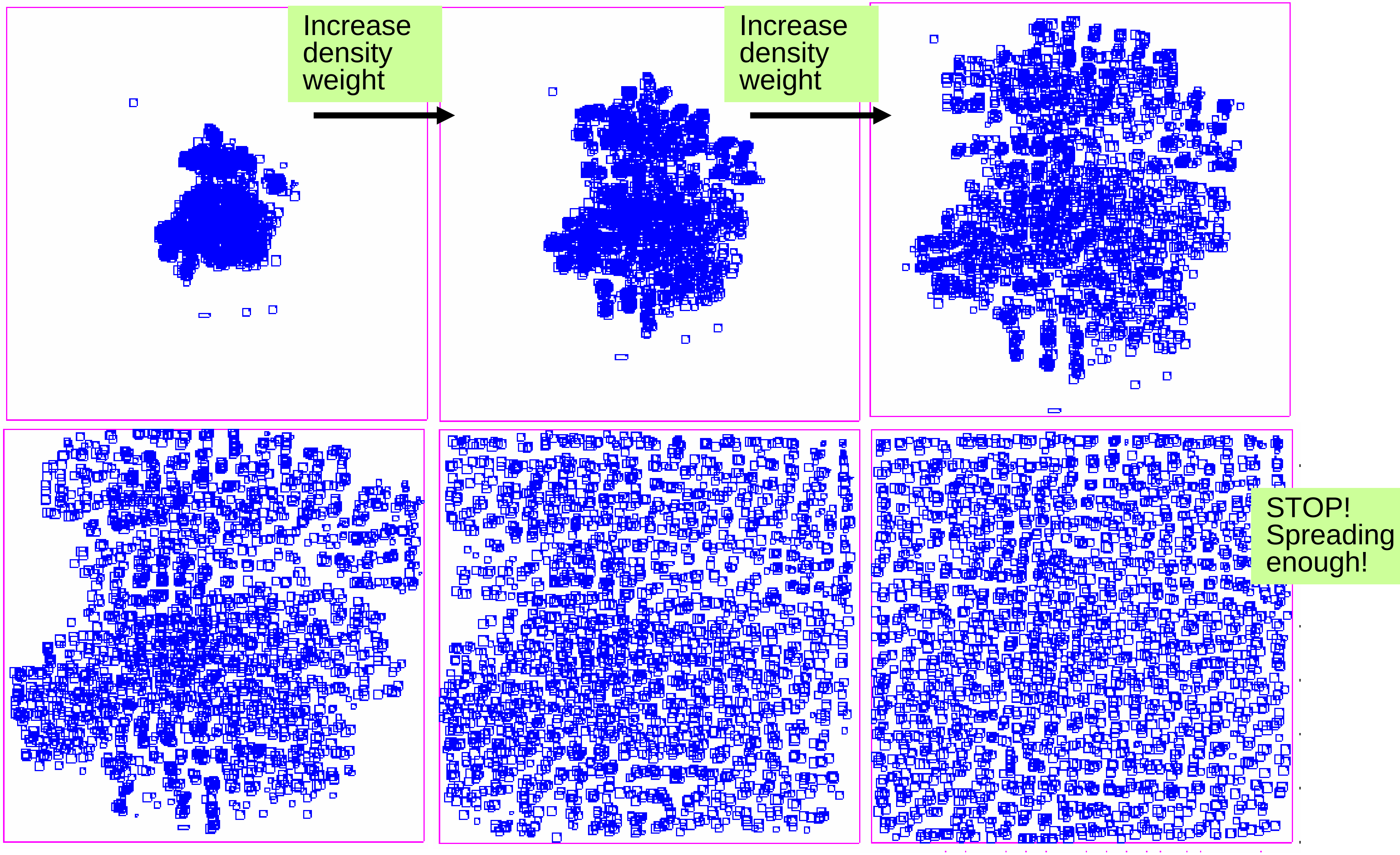
D_b^{max}: max density for bin *b*

- **Relax the constraints into the objective function**

$$\textbf{min} \quad W(x, y) + \lambda \sum (D_b(x, y) - D_b^{max})^2$$

  - Use the gradient method to solve it
  - Increase λ gradually to find the optimal (x, y)

Placement Process



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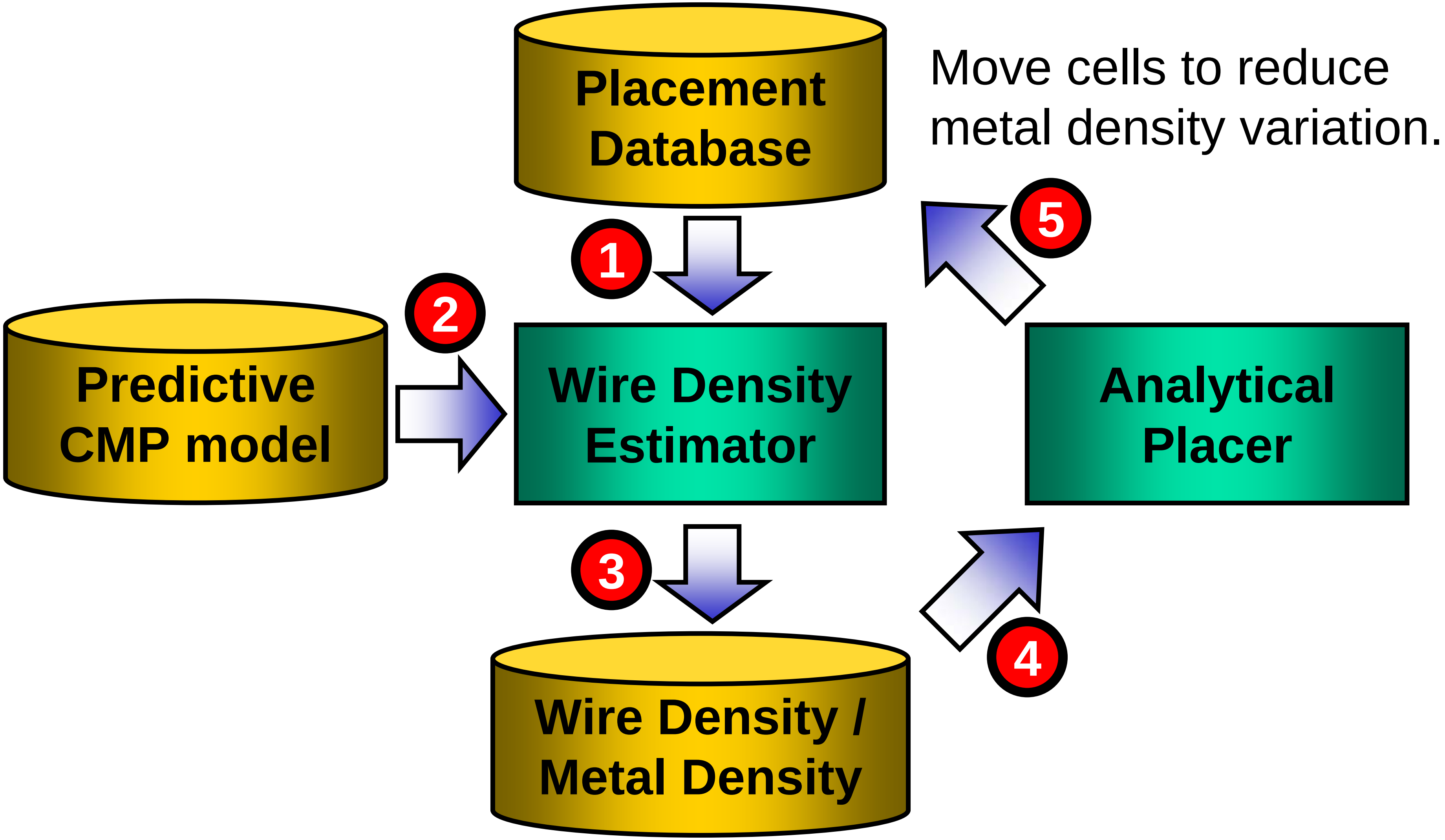
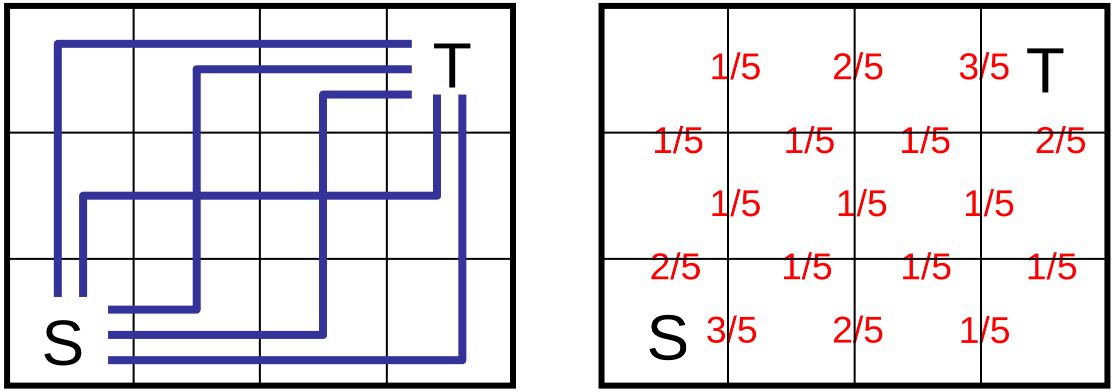
Framework



Placement Database
Move cells to reduce metal density variation.
5
1
2
Predictive CMP model
Wire Density Estimator
Analytical Placer
3
4
Wire Density / Metal Density

Wire Density Estimator

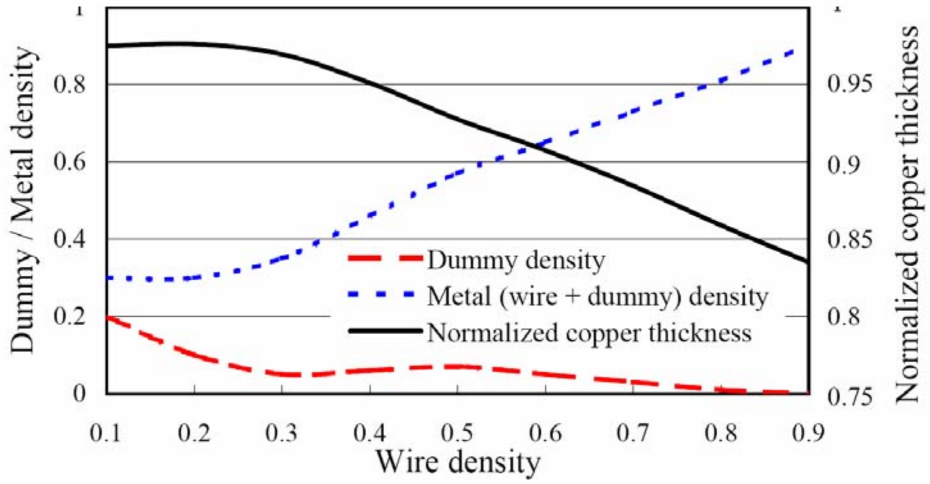
- Wire density of a bin is computed by the number of track go through the bin boundary and the internal routing in the bin.
- To predict the predict track usage, we decompose multi-terminal nets into Steiner trees using FLUTE. [Chu, ISPD04]
- Track usage is estimated by the probabilistic routing model. [Lou, Thakur, and Krishnamoorthy, TCAD02]



Predictive CMP Model

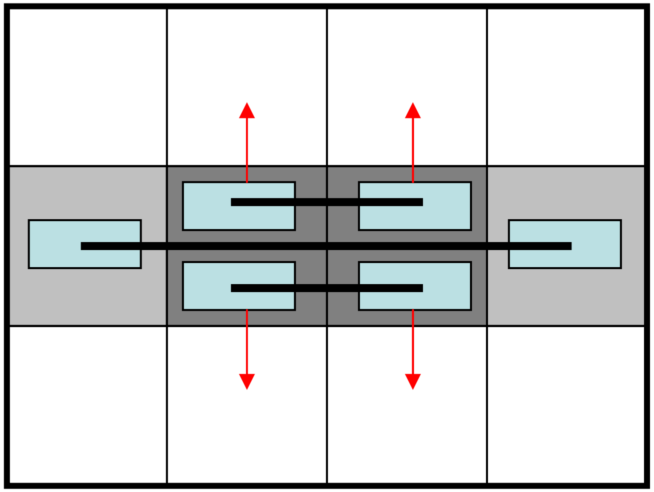
- A fast CMP model is desired
  - Use the predictive CMP model [ICCAD-2007]
- Cu thickness is systematically dependent on metal density

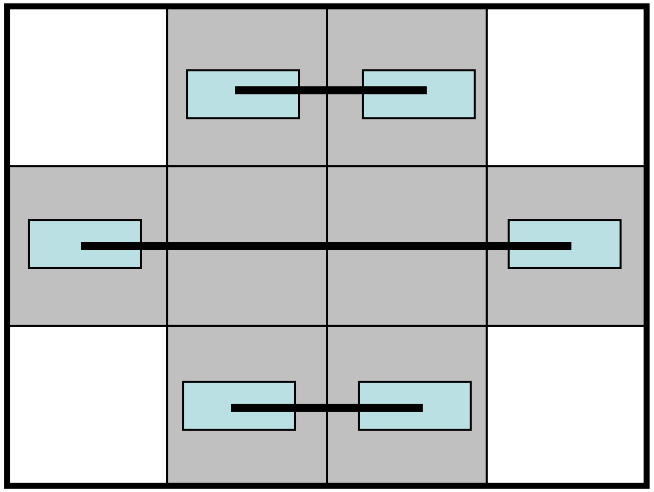
$$Cu\_Thickness = \alpha * (1 - \frac{Metal\_density^2}{\beta})$$



- Metal density = wire density + dummy fill density
- Wire density → Dummy fill → Metal density

Concept of Reducing Metal Density





- Move cells out from high metal-density regions.
- Add forces to blocks in high metal-density regions.
- Result in more uniform metal density.

Metal-Density Driven Placement Formulation

- **min** W
  s.t. $D_b \leq D_b^{max}$
  $M_b^v \leq M_b^{v,max}$
  $M_b^h \leq M_b^{h,max}$

M_b^v metal density in the vertical routing layer

M_b^h metal density in the horizontal routing layer

- Relax all constraints to objective function may cause instability of the solver and may not converge to a feasible solution.

$$\textbf{min} \quad W + \lambda_1 \Sigma (D_b - D_b^{max})^2 + \lambda_2 \Sigma (M_b^v - M_b^{v,max})^2 + \lambda_3 \Sigma (M_b^h - M_b^{h,max})^2$$

- Instead, we solve the following equation to ensure the stability:

$$\textbf{min} \quad W + \lambda \ \Sigma (D_b - D'^{max}_b)^2$$

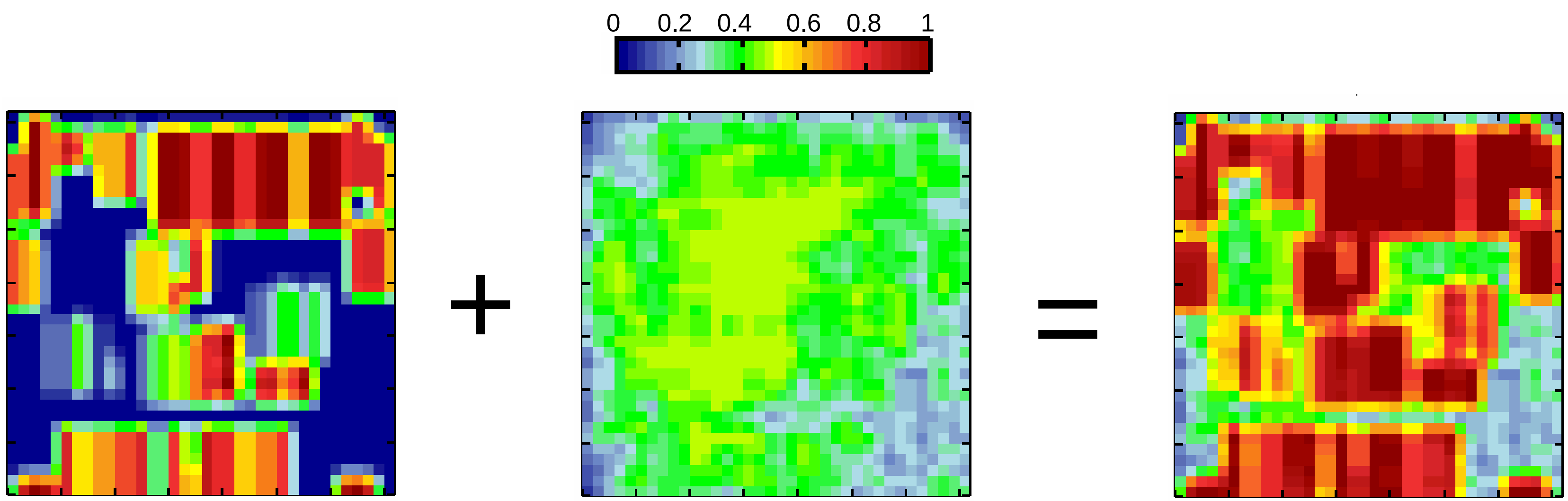
D'^{max}_b maximum combined density (preplaced density + metal density)

Computing Maximum Combined Density

$$D'^{\,max}_{b} = \text{target\_utilization}(1.0 - \text{combined\_density})$$

$$\text{combined\_density} = \text{preplaced\_density} + \text{scaled\_metal\_density}$$

$$\text{scaled\_metal\_density} = s_1(M_b^v - \min M_b^v) + s_2(M_b^h - \min M_b^h)$$



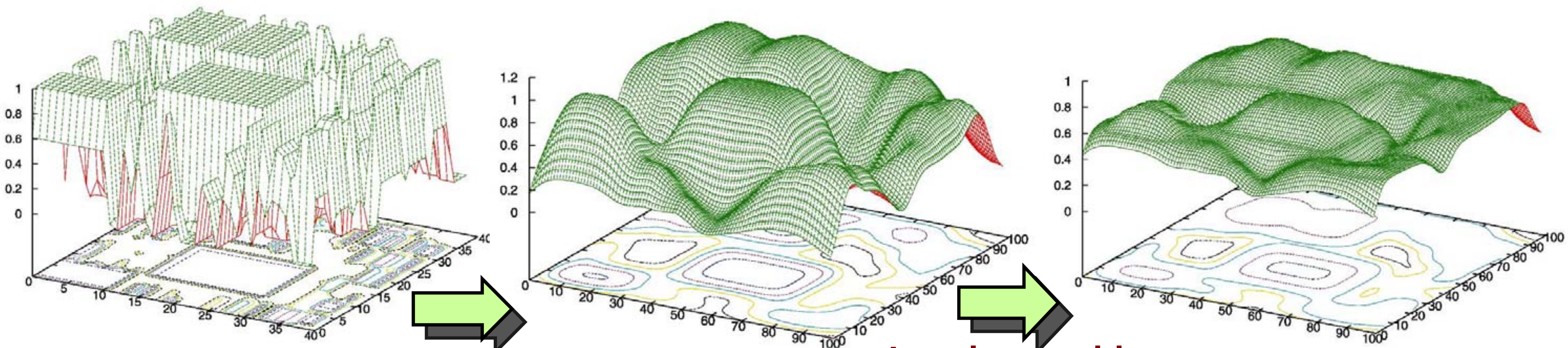
Preplaced block density

Scaled metal density

Combined density

Density Smoothing

- A smooth objective function helps the gradient method to find a desired solution.



Gaussian smoothing

$$G(x,y) = \frac{1}{2\pi\sigma^2} e^{-\frac{x^2+y^2}{2\sigma^2}}$$

Level smoothing

$$p'(x,y) = \begin{cases} \overline{p} + (p(x,y) - \overline{p})^{\delta} & if\ \ p(x,y) \geq \overline{p} \\ \overline{p} - (\overline{p} - p(x,y))^{\delta} & if\ \ p(x,y) \leq \overline{p} \end{cases}$$

- Three smoothing parameters
  - k gradually increases to the user-specified whitespace ratio
  - σ controls the range of the Gaussian smoothing (15% to 1%)
  - δ controls the degree of level smoothing (5 to 1)

Flow

- Loop 1 (L1)
  - Multilevel
- Loop 2 (L2)
  - Objective function
- Loop 3 (L3)
  - Solver

- The metal density is updated inside the L3, and the base potential is updated accordingly.
- The smoothing parameters are updated in L2.

Multilevel Metal-Density Driven Placement

Input: a circuit hypergraph
Output: desired block positions

```
create the clustering hierarchy;
initialize block positions;
do
    initialize the bin structure and λ;
    do
        Update smoothing parameters;
        // find min W(x, y) + λ∑(D_b − a_b^{u'})^2;
        do
            compute the conjugate gradient direction;
            update current block positions;
            Estimate wire and metal density;
            Update combined density;
        until (the minimal value is found);
        increase λ by 2;
    until (spreading enough);
    decluster blocks;
until (all clusters are declustered);
legalize the placement;
return block positions;
```

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Experiment Setup

- CPU: AMD Opteron 2.2GHz
- Benchmarks: adaptec from ISPD'06
- Placement: NTUplace3 (ICCAD'06)
- Routing: BoxRouter (DAC'06,ICCAD'07)
- Routing configurations (from ISPD'07)
  - Six metal layers; 20% tracks available in metal 1 and metal 2
  - Block porosity: the reaming routing resource above the macros
- Predictive CMP model for computing Cu thickness

Circuit	Placement				Routing	
	Mov #	Fixed #	Net #	Util. (%)	Track #	B.P.† (%)
adaptec1	211k	543	221k	57	35	50
adaptec2	254k	566	266k	44	35	20
adaptec3	451k	723	467k	33	30	50
adaptec4	495k	1329	516k	27	30	50
adaptec5	842k	646	868k	49	50	20

B.P.: macro block porosity

Placement Techniques Compared

① Wirelength-driven placement (WLD)

- Minimize wirelength
- Target utilization = 1.0

② Cell-density driven placement (CDD)

- Evenly distribute cells over the chip
- Target utilization = design density

③ Metal-density driven placement (MDD)

- Spread cells to minimize metal density variation
- Set max k = 90% to use 90% whitespace for metal density optimization

Results

① Circuit	Wirelength-Driven (WLD)											
	Placement		Routing				CMP (Hori. Layer)			CMP (Vert. Layer)		
	HPWL (× e7)	CPU (min)	WL (× e7)	WL/ HPWL	Over-flow	CPU (min)	Dummy	Cu-Avg	Cu-Std	Dummy	Cu-Avg	Cu-Std
adaptec1	8.15	14	11.87	1.46	0	711	5984	0.95	3.16	6034	0.95	3.09
adaptec2	9.02	15	12.38	1.37	2758	2279	13567	0.96	3.84	13644	0.96	4.03
adaptec3	22.35	32	26.27	1.18	938	140	45432	0.96	7.48	43843	0.96	7.78
adaptec4	20.02	29	22.38	1.12	31	1839	51258	0.96	7.81	50322	0.96	7.73
adaptec5	36.09	76	47.36	1.33	26672	2386	16766	0.96	5.73	16462	0.96	5.70
Comp.	0.81	0.76	0.89	1.29	—	33.42	1.06	1.00	1.12	1.06	1.00	1.11

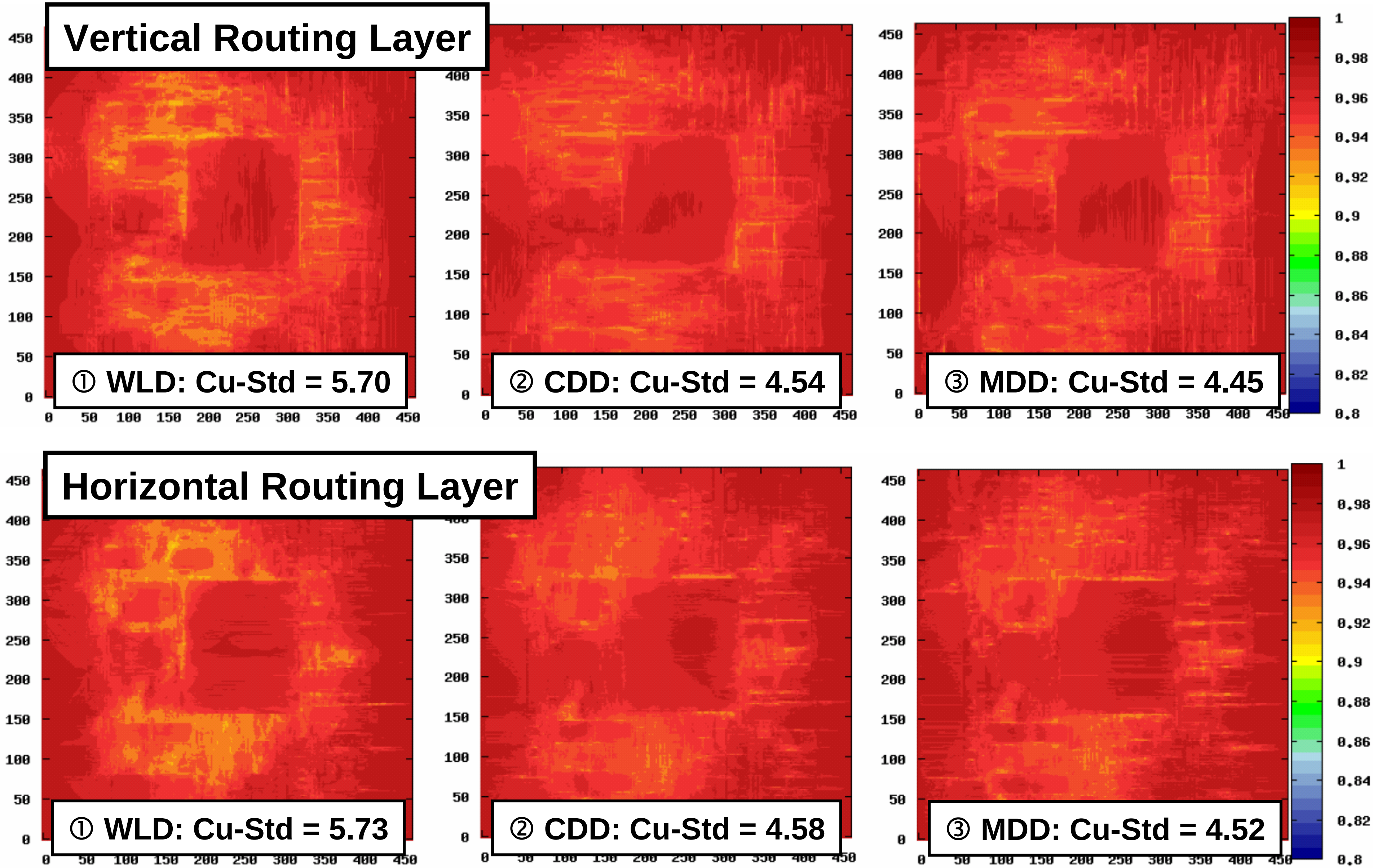
② Circuit	Cell-Density Driven (CDD)											
	Placement		Routing				CMP (Hori. Layer)			CMP (Vert. Layer)		
	HPWL (× e7)	CPU (min)	WL (× e7)	WL/ HPWL	Over-flow	CPU (min)	Dummy	Cu-Avg	Cu-Std	Dummy	Cu-Avg	Cu-Std
adaptec1	9.20	15	12.12	1.32	0	130	5929	0.95	3.09	5986	0.95	3.14
adaptec2	10.32	17	13.08	1.27	0	208	13166	0.96	3.50	13248	0.96	3.83
adaptec3	27.42	28	31.19	1.14	28	1119	43575	0.96	7.24	42096	0.96	7.44
adaptec4	22.61	52	24.67	1.09	0	30	49078	0.96	7.36	48174	0.96	7.18
adaptec5	38.90	67	49.62	1.29	875	1788	15972	0.96	4.58	15560	0.96	4.54
Comp.	0.92	0.90	0.96	1.22	—	4.67	1.02	1.00	1.03	1.02	1.00	1.03

③ Circuit	Metal-Density Driven (MDD)											
	Placement		Routing				CMP (Hori. Layer)			CMP (Vert. Layer)		
	HPWL (× e7)	CPU (min)	WL (× e7)	WL/ HPWL	Over-flow	CPU (min)	Dummy	Cu-Avg	Cu-Std	Dummy	Cu-Avg	Cu-Std
adaptec1	9.41	17	11.54	1.23	0	42	5914	0.95	3.02	5927	0.95	3.03
adaptec2	11.63	23	13.63	1.17	0	28	12913	0.96	3.36	12952	0.96	3.69
adaptec3	30.35	38	34.10	1.12	0	121	42253	0.96	7.06	40525	0.96	7.24
adaptec4	26.40	35	28.69	1.09	0	28	46481	0.96	7.05	45741	0.96	7.03
adaptec5	39.82	110	48.73	1.22	0	707	16198	0.96	4.52	15687	0.96	4.45
Comp.	1.00	1.00	1.00	1.17	—	1.00	1.00	1.00	1.00	1.00	1.00	1.00

Result Summary

	CMP		Routability		Place
	Thickness variation	Dummy fills	Total Overflow	Routing CPU time	CPU
WLD	1.12	1.06	30,399	33.42	0.81
CDD	1.03	1.02	903	4.67	0.92
MDD	1.00	1.00	0	1.00	1.00

Metal-Density Map for adaptec5



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Conclusion

- Presented the first metal-density driven placement
  - Predictive CMP model
  - Metal-density-aware cell spreading
  - Density smoothing
- Compared with the wirelength-driven placement, we
  - Reduced the copper thickness variation by 12%
  - Reduced the dummy fills by 6%
- Results also led to higher routability
  - Less overflow
  - Less routing time

Thank You!

Questions?