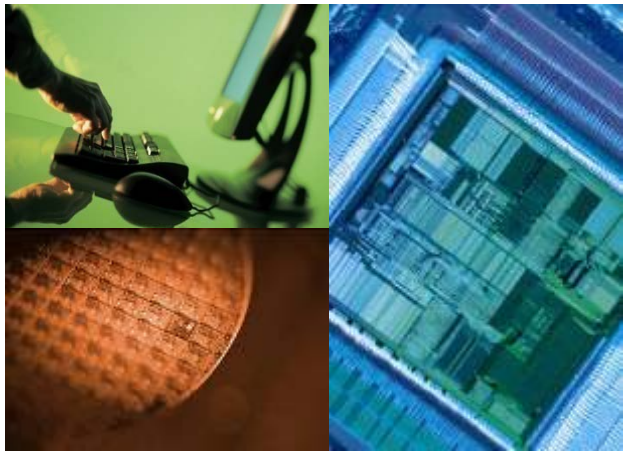
Design or Manufacturing?

Which Is the Best Driver for Physical Design?

ISPD 2008

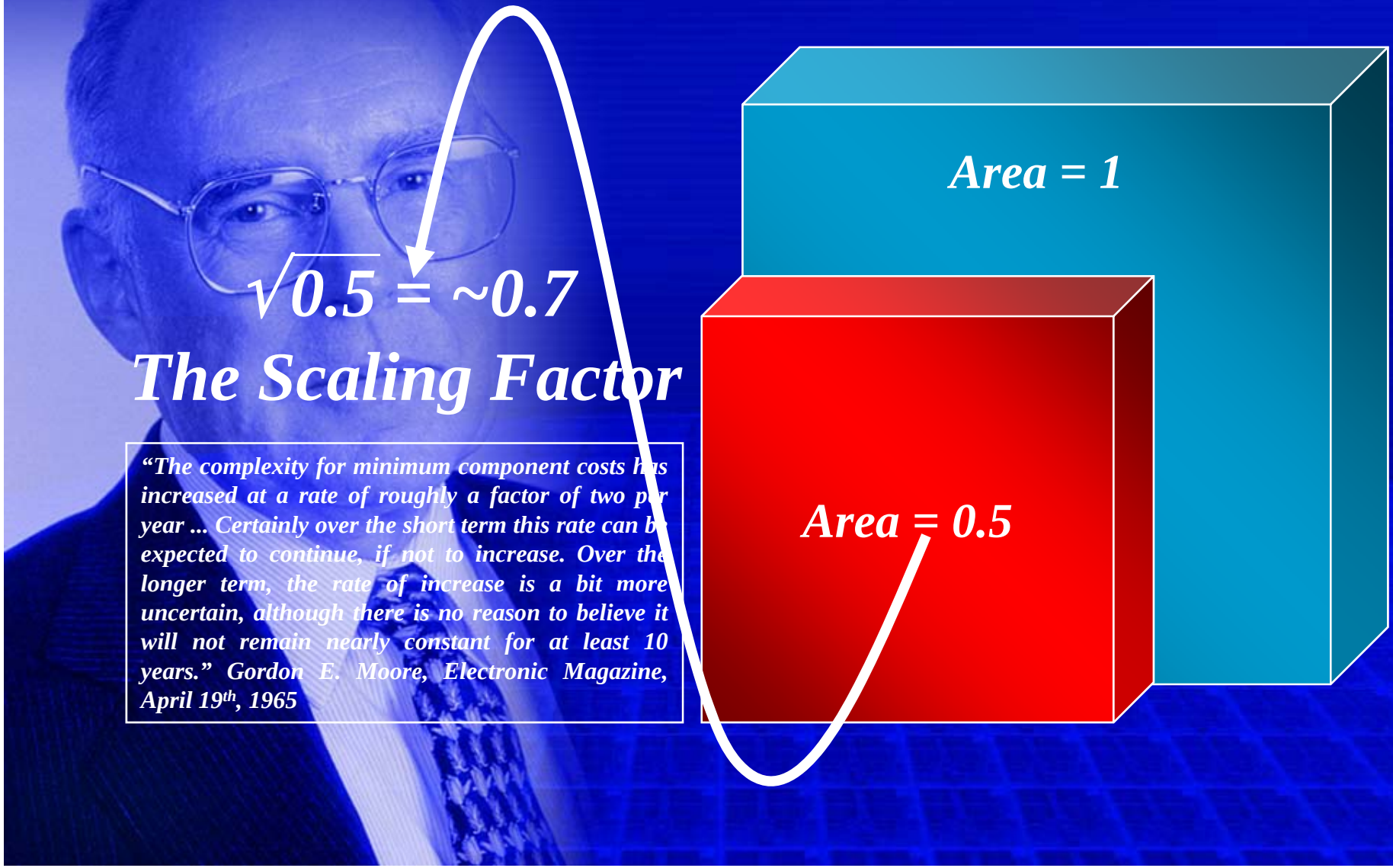


Antun Domic
GM, Implementation Group
Synopsys, Inc

SYNOPSYS®
Predictable Success

Dr. Gordon E. Moore's Law

Twice the Number of Transistors, for the Same Price, Approximately Every Two Years



$\sqrt{0.5} = \sim 0.7$

The Scaling Factor

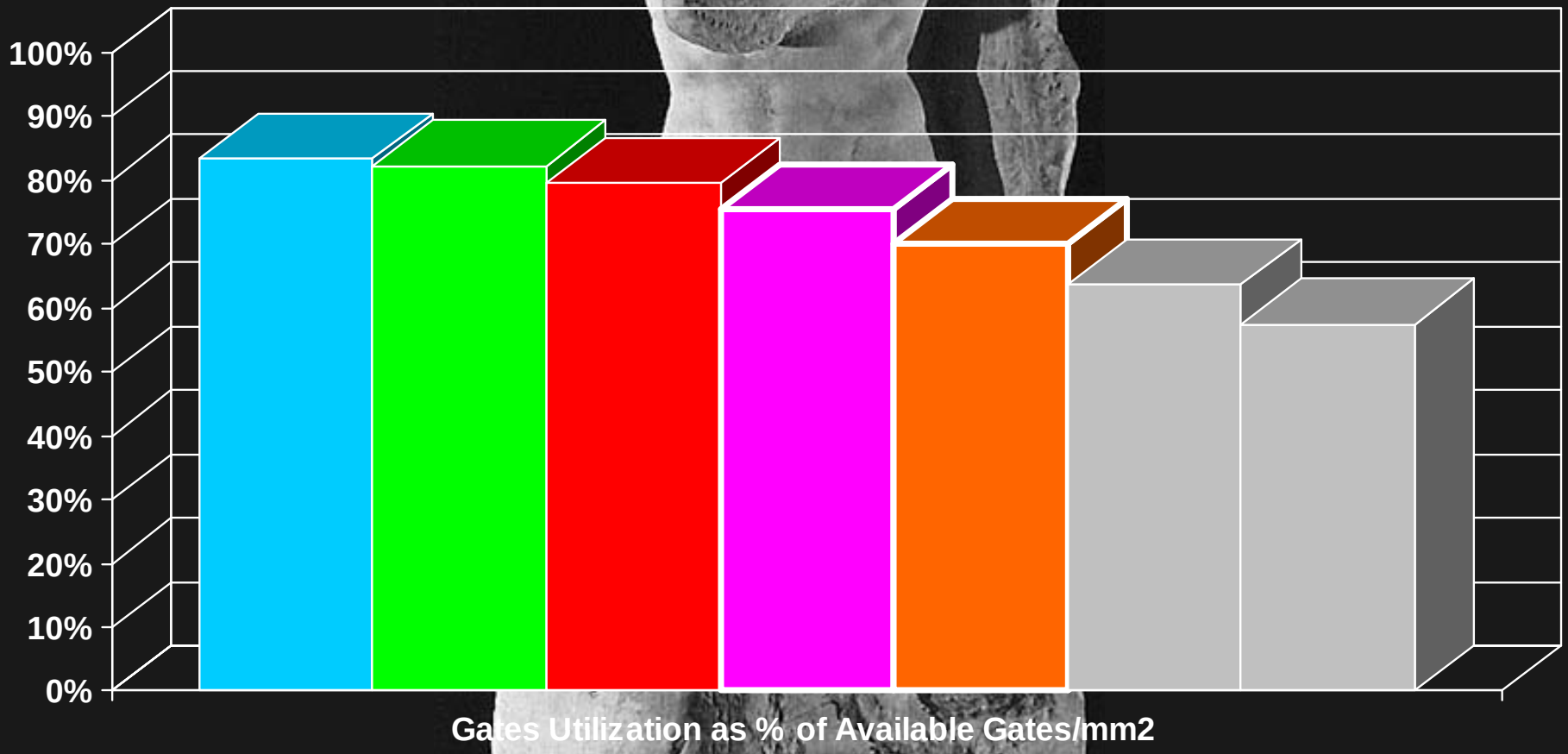
Area = 1

Area = 0.5

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years." Gordon E. Moore, Electronic Magazine, April 19th, 1965

But there is some Inefficiency

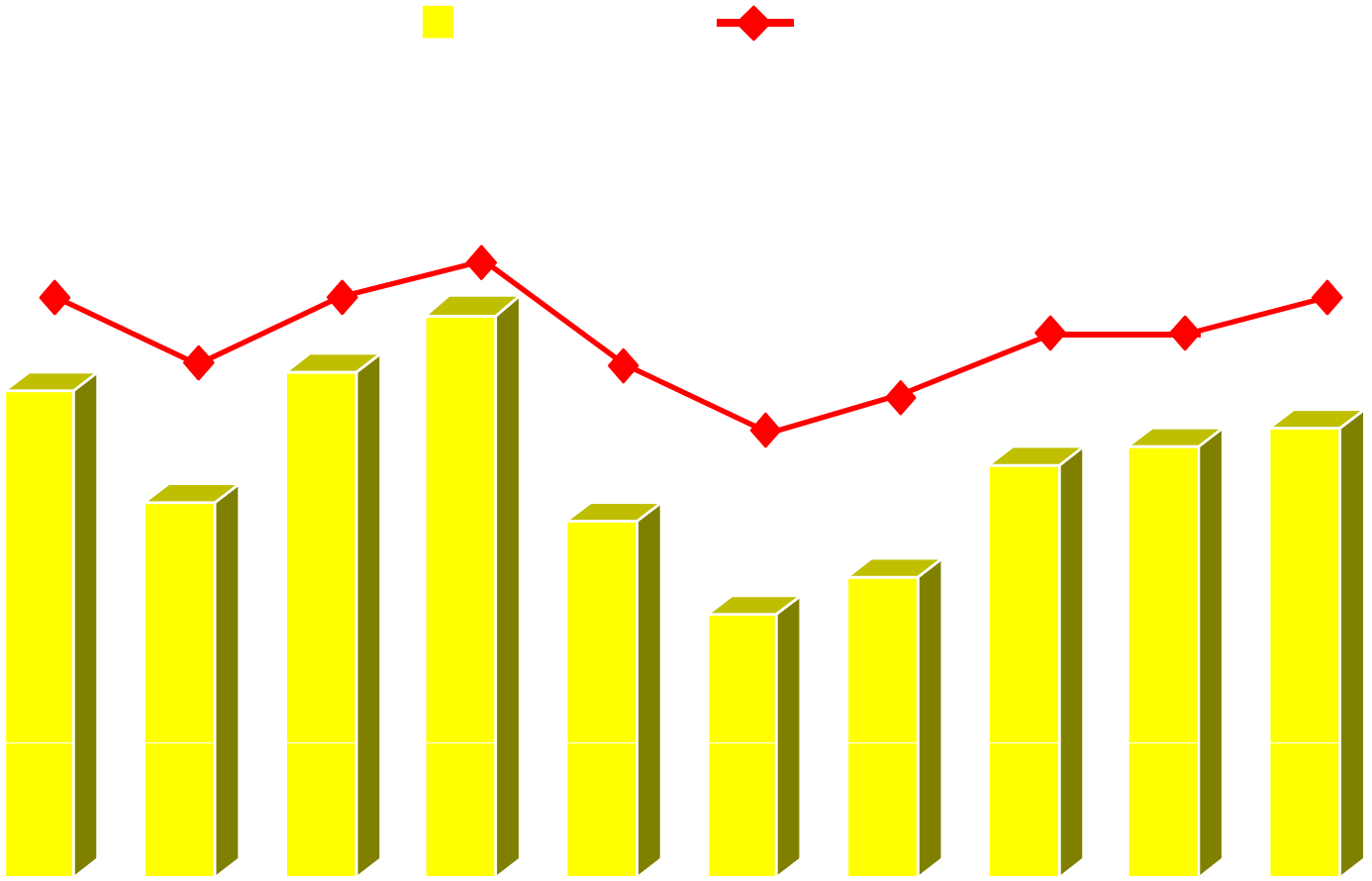
Gate Utilization as % of Available Gates/mm² Declines



Source: IBS 2007

Dr. Gordon E. Moore's Corollary

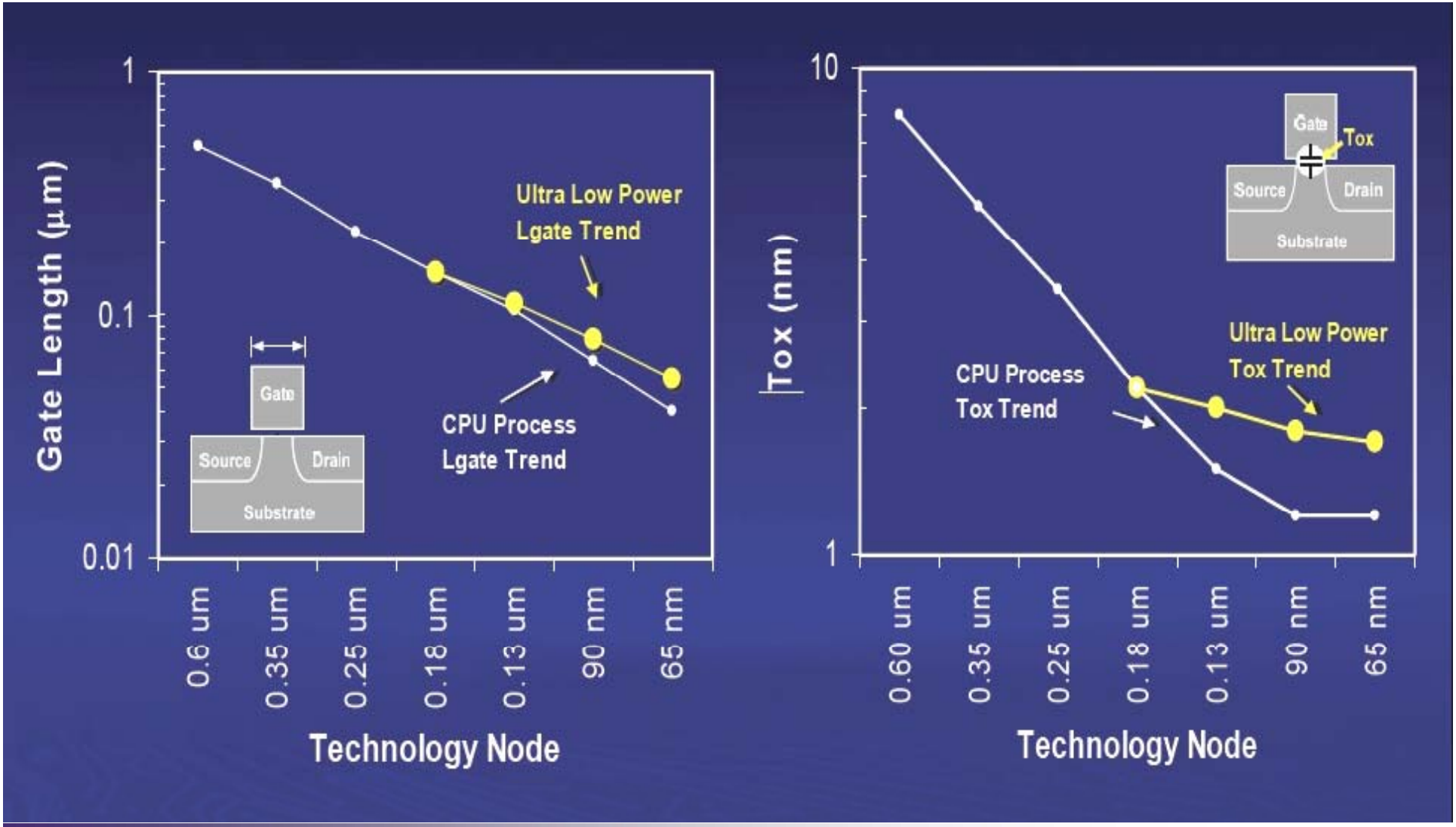
"We've Sold Area on the Silicon Wafer for about $1B an Acre, as Long as I've Been in the Industry."



Source: G. Moore, Intel, IDF 1997; Future Horizons 2007

Technology Fork From 180 Nanometers

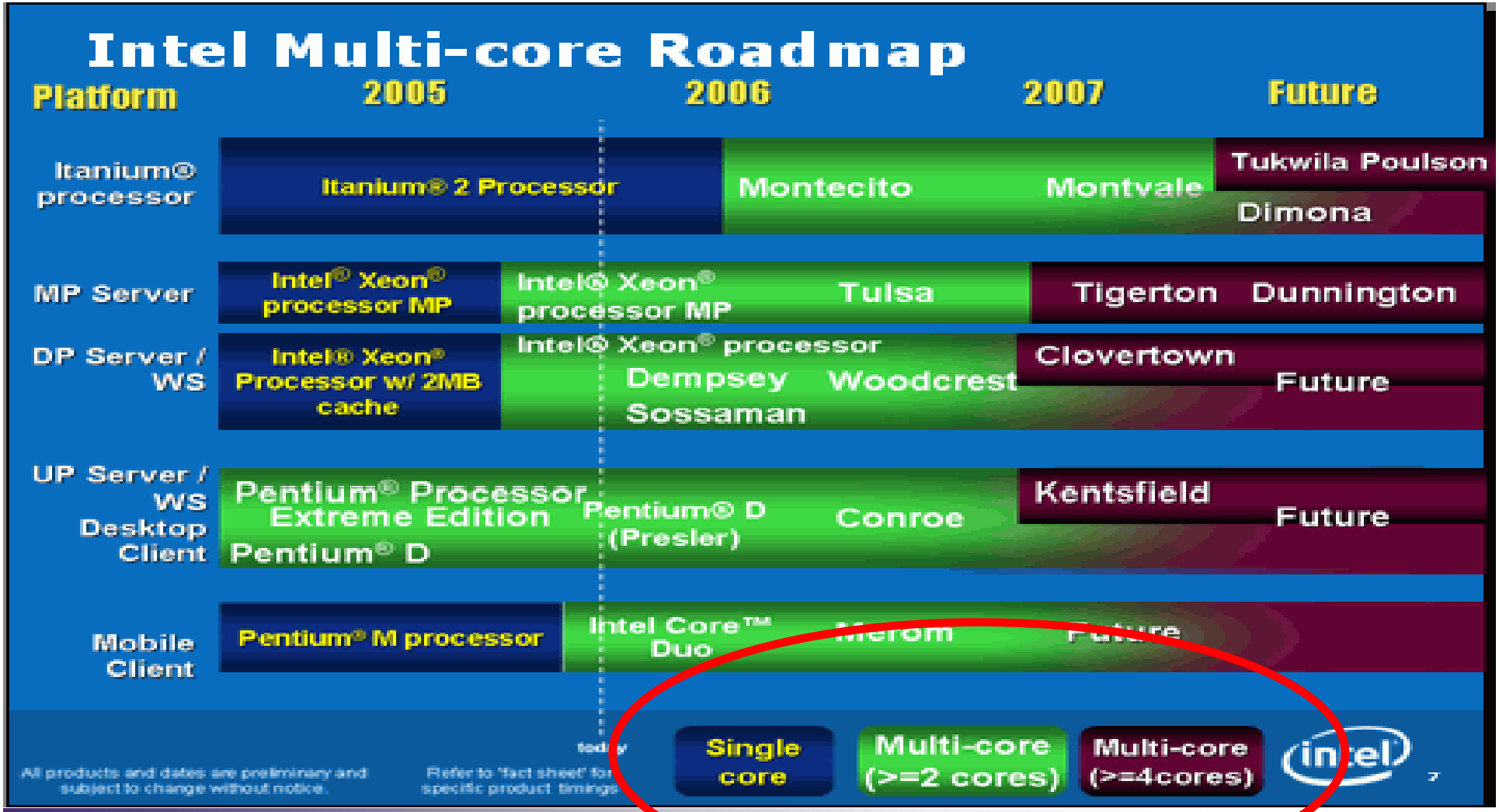
Manufacture for Ultra-Low Power OR High Performance



Source: P. Bai, Intel, IEDM 2004; C.H. Jan, Intel, IEDM 2005

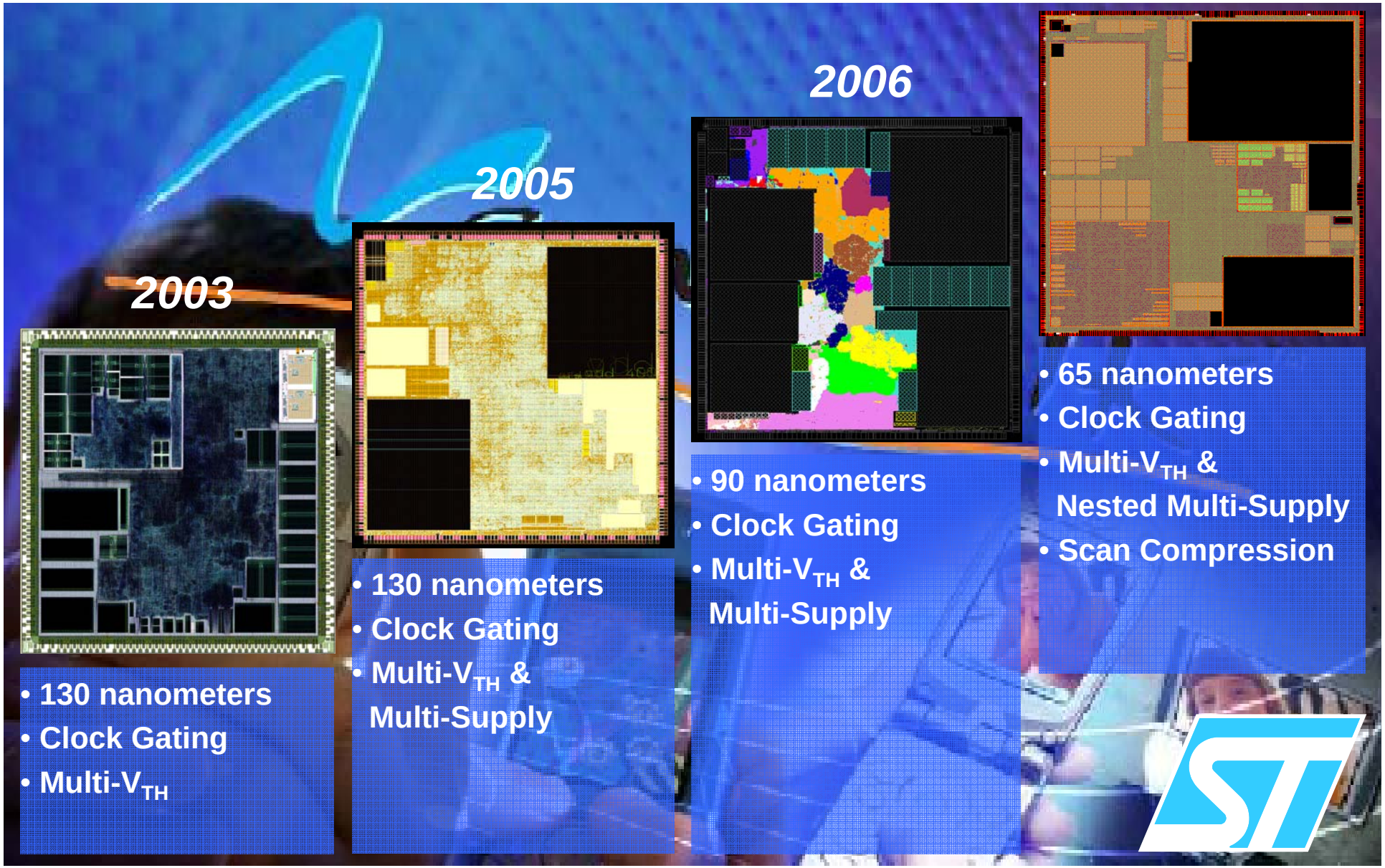
Processor Roadmap Trends

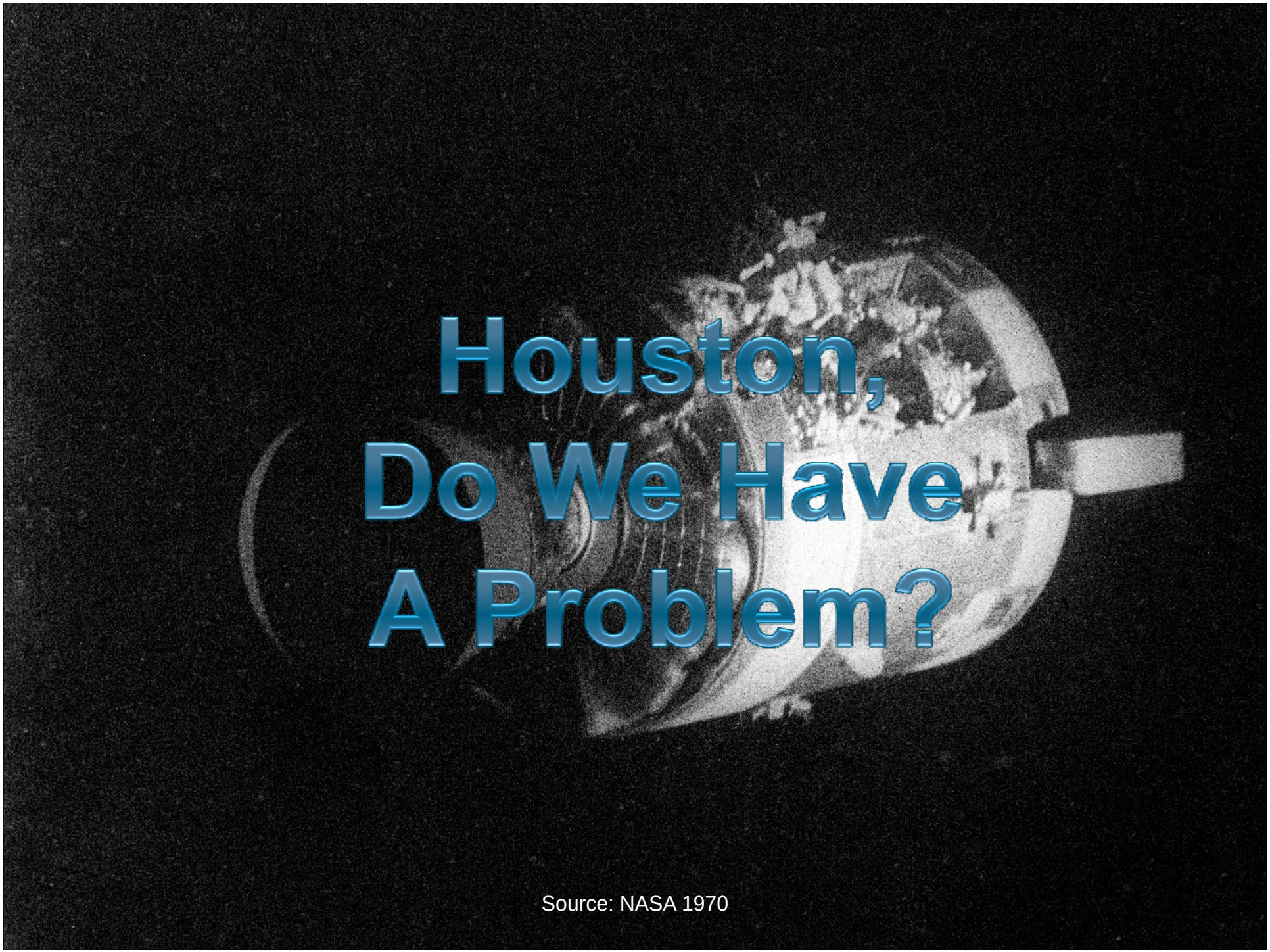
Hi-Performance, Multi-Core



Mobile Roadmap Trends

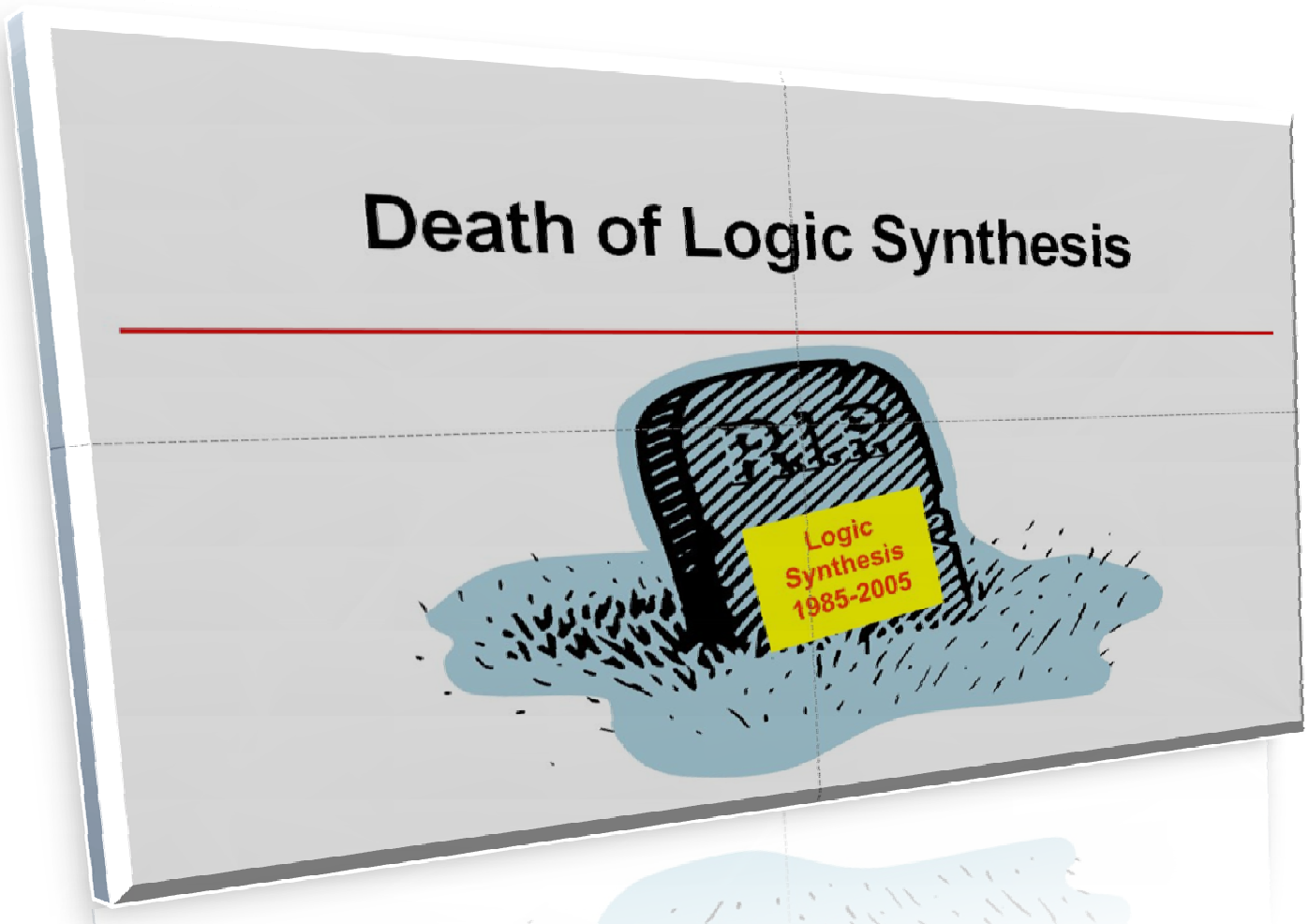
Ultra Low Power





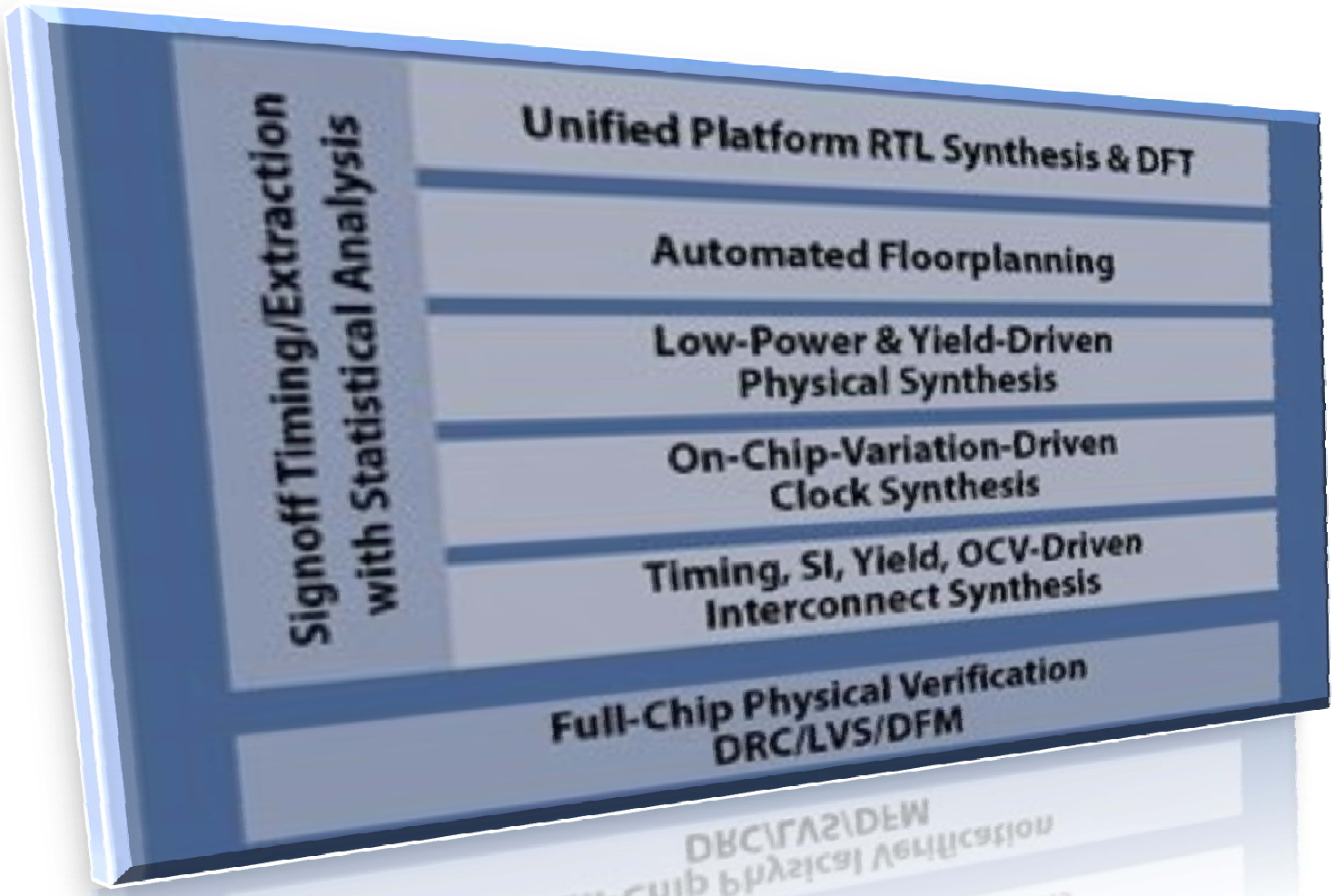
Source: NASA 1970

An Ominous Prediction …



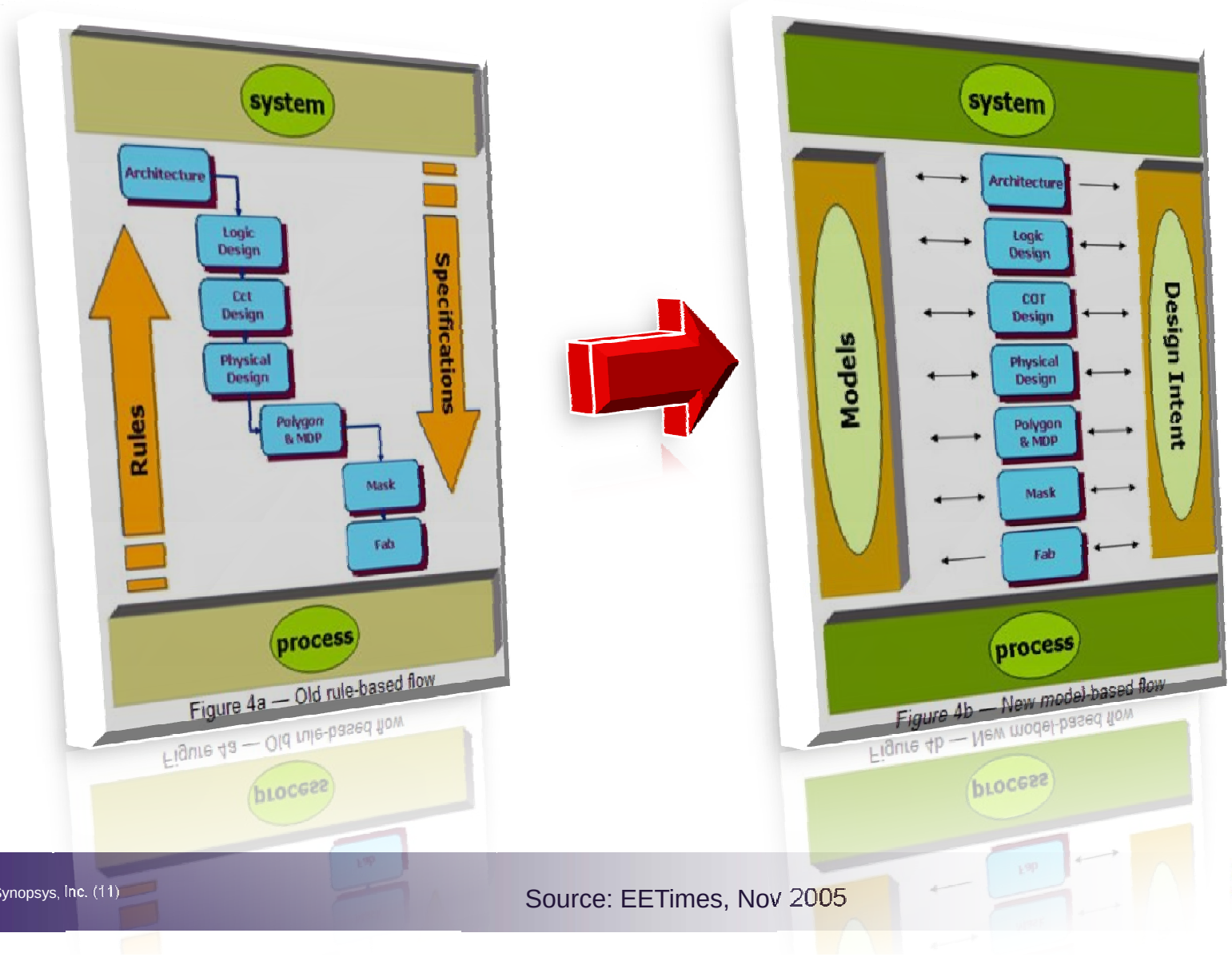
Source: ISPD 2005, R. Madhavan, CEO Magma Design Automation

Statistical Throughout the Flow …



Source: Chip Design, April/May 2005

Followed by Model-Based ...

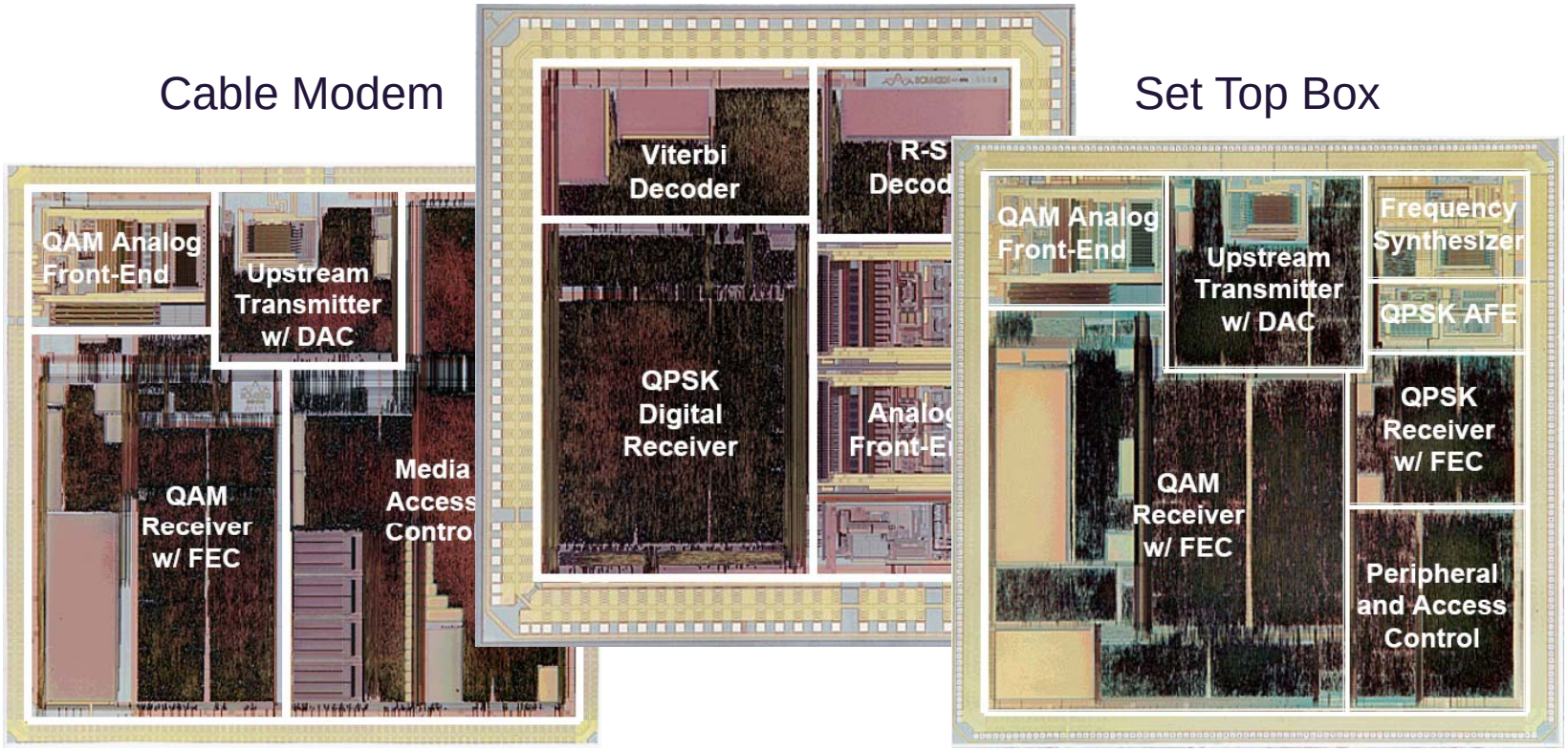


Source: EETimes, Nov 2005

Is the Sky Falling?

Design Complexity Increased Ten Fold

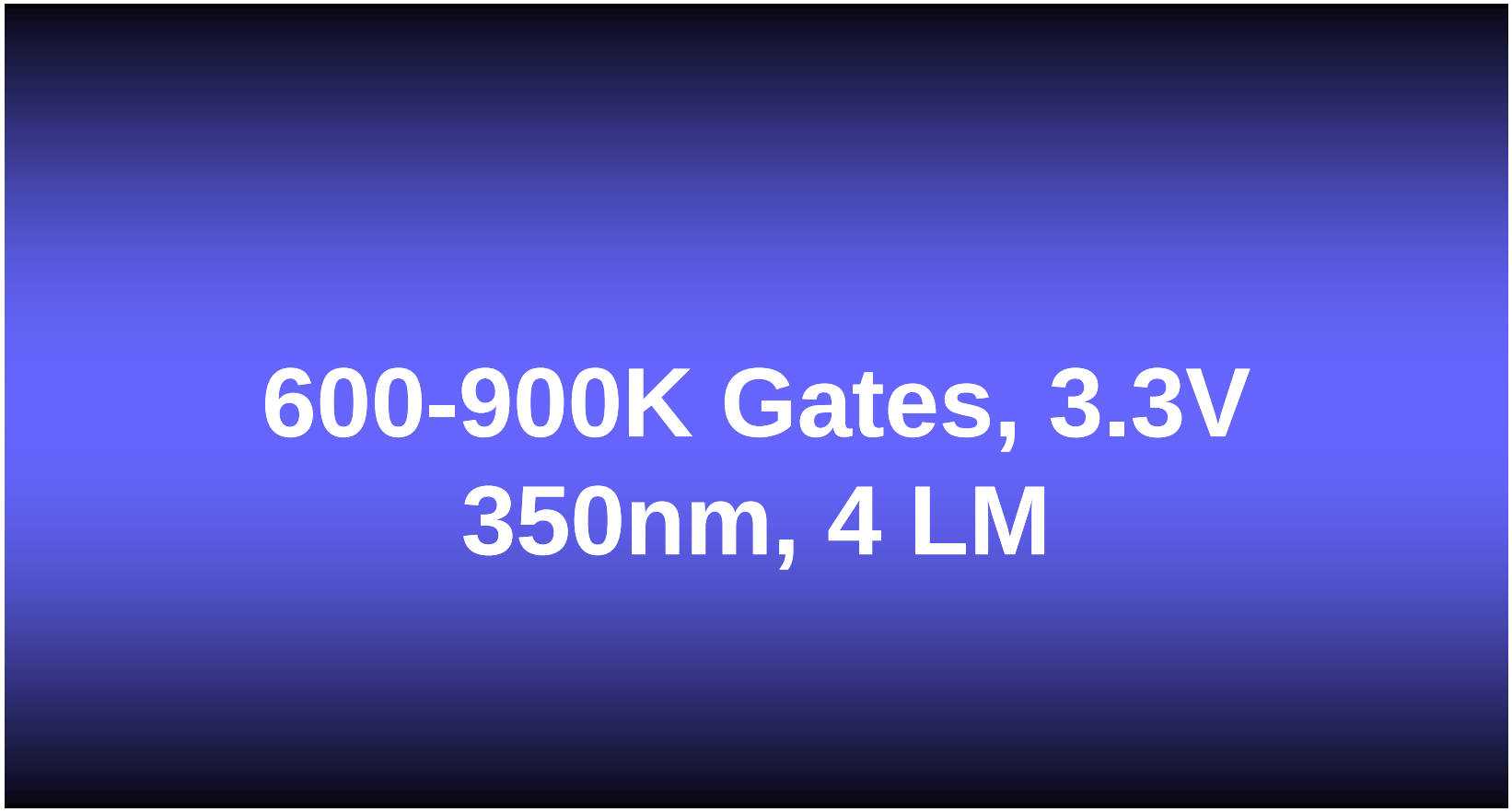
Hot Chips circa 1999



H. Samuelli, Hot Chips Forum Keynote, '99

Design Complexity Increased Ten Fold

Hot Chips circa 1999

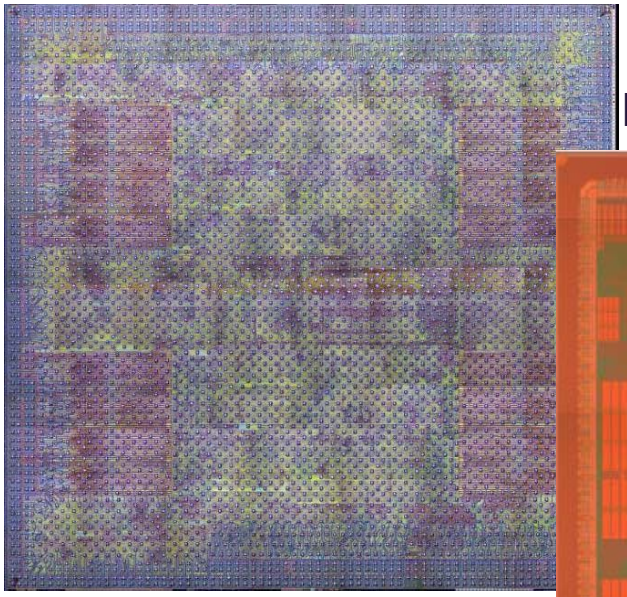


H. Samuelli, Hot Chips Forum Keynote, '99

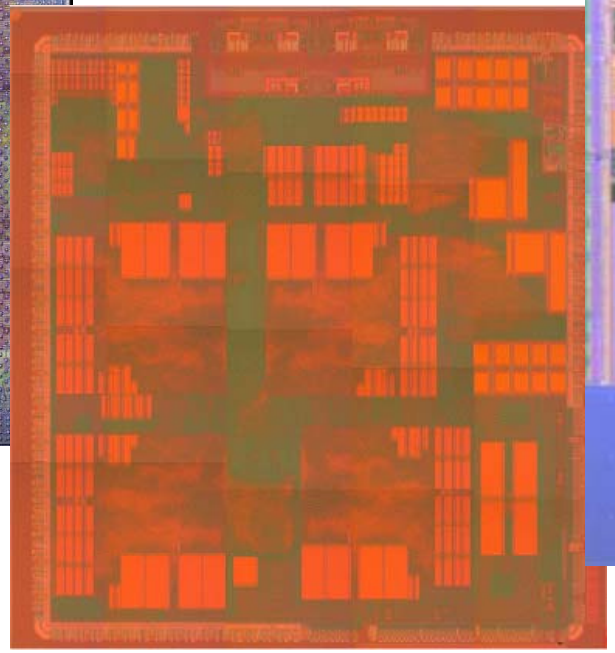
Design Complexity Increased Ten Fold

Hot Chips circa 2007

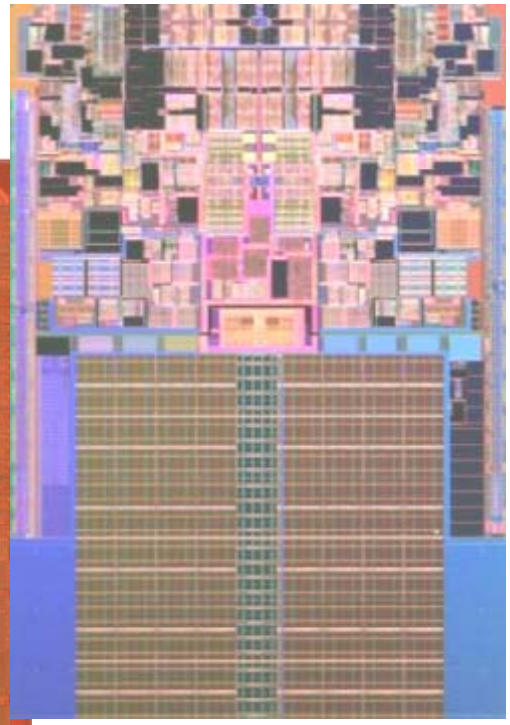
Graphics Processor



Multi-Core
Low Power Processor

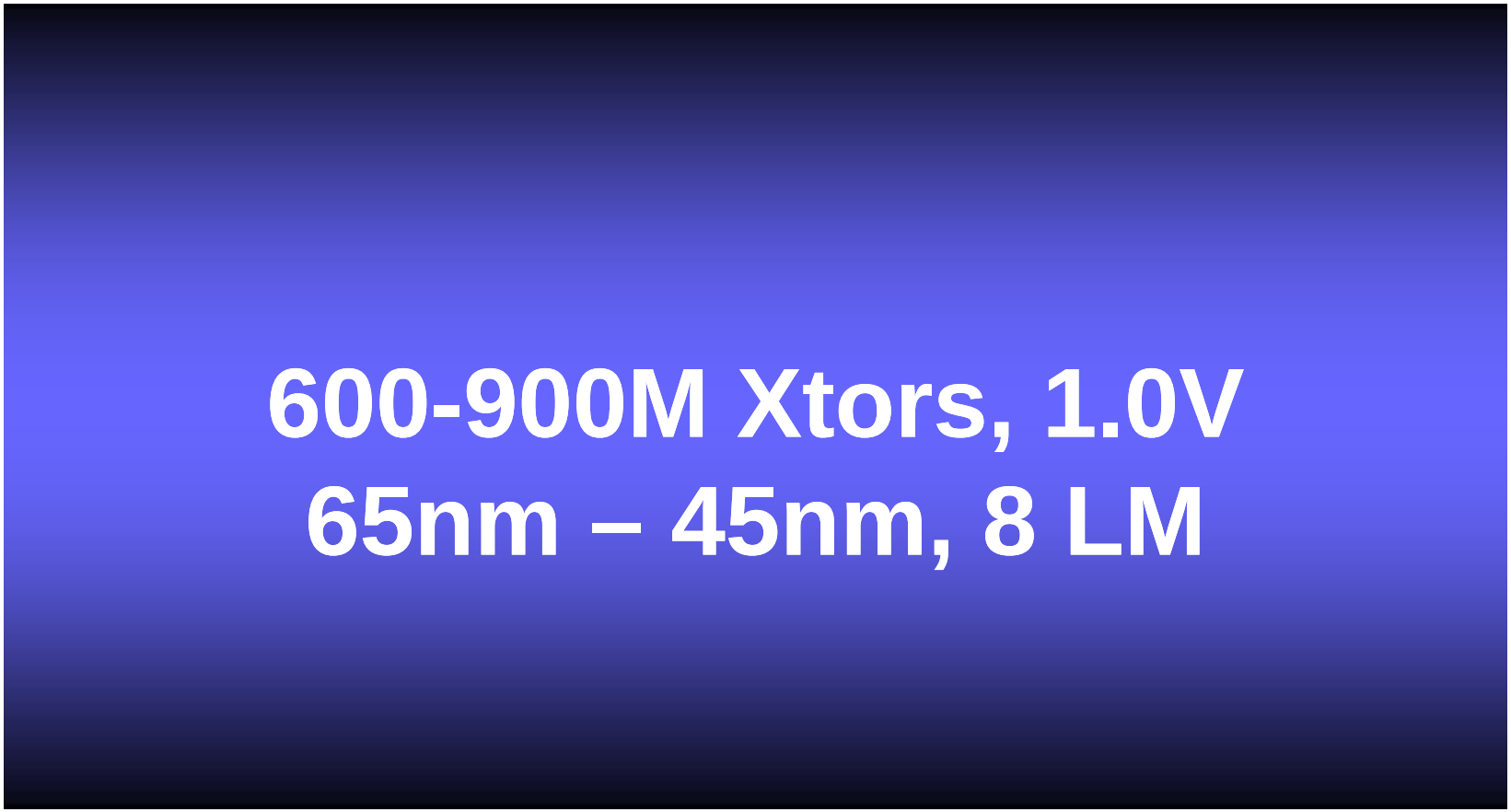


Mobile Processor



Design Complexity Increased Ten Fold

Hot Chips circa 2007



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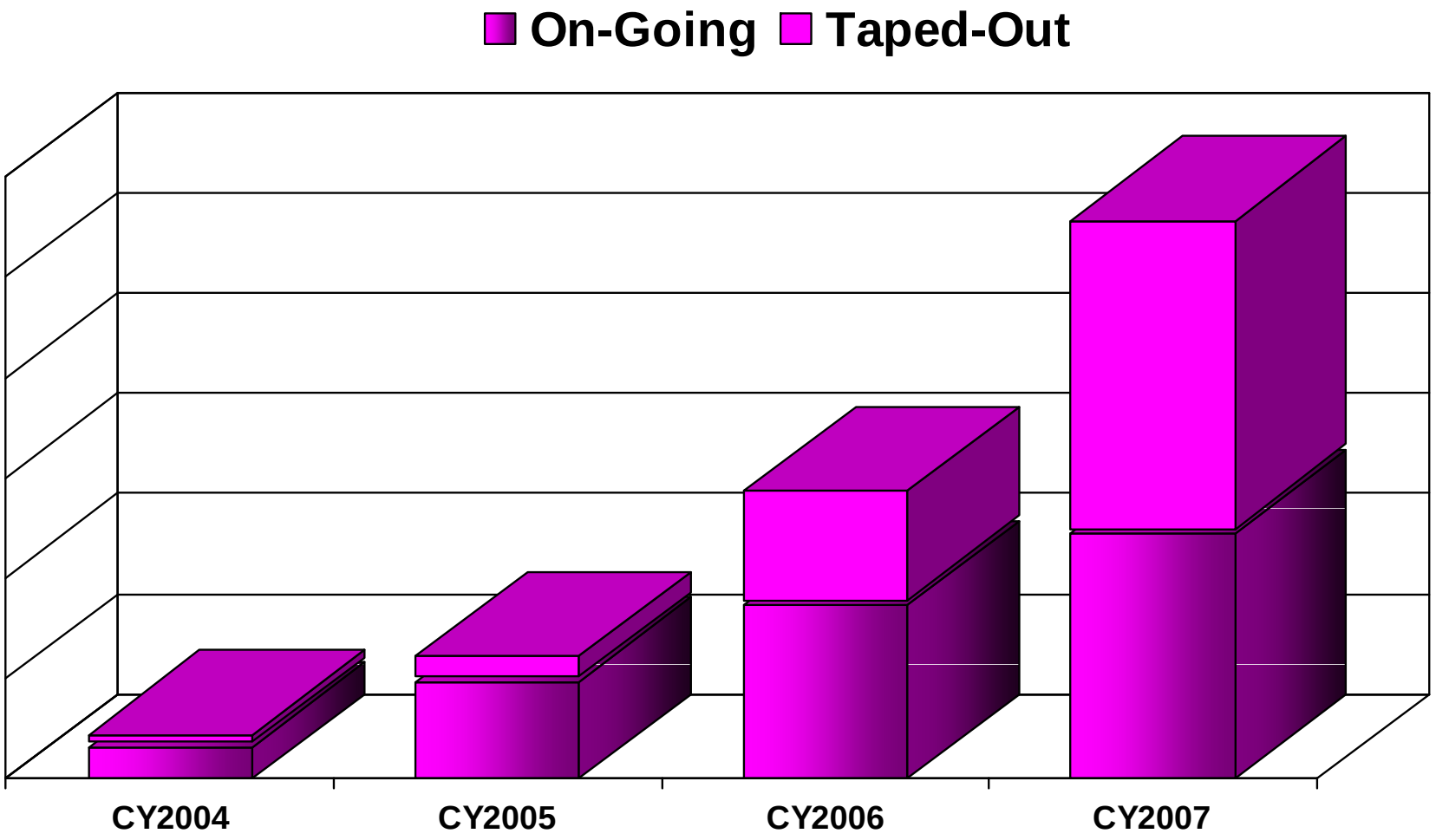
Let the Tapeouts Speak for Themselves

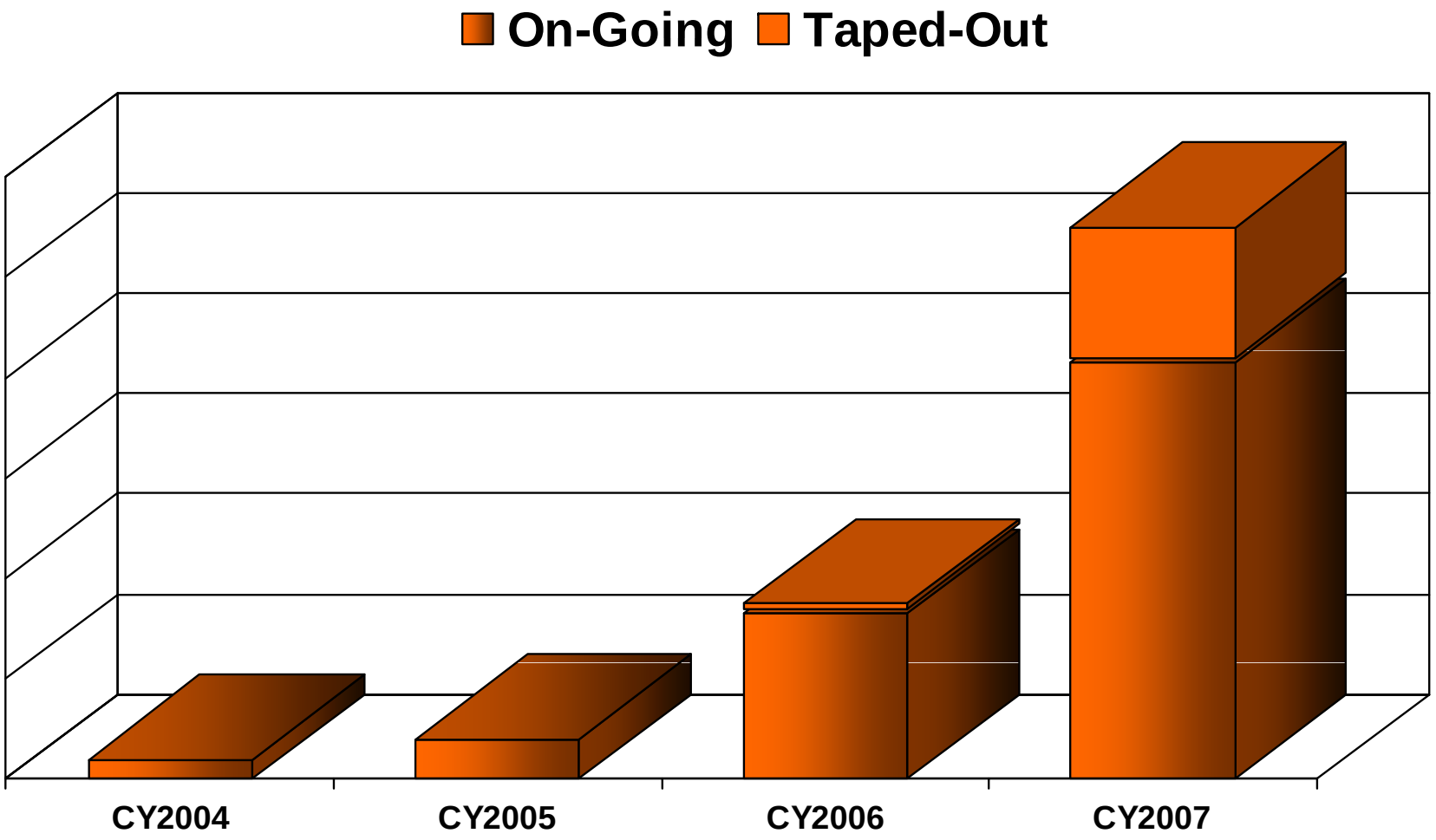
Cumulative Designs & Tape-Outs @ 65 Nanometers



Source: Synopsys 2008

Let the Tapeouts Speak for Themselves

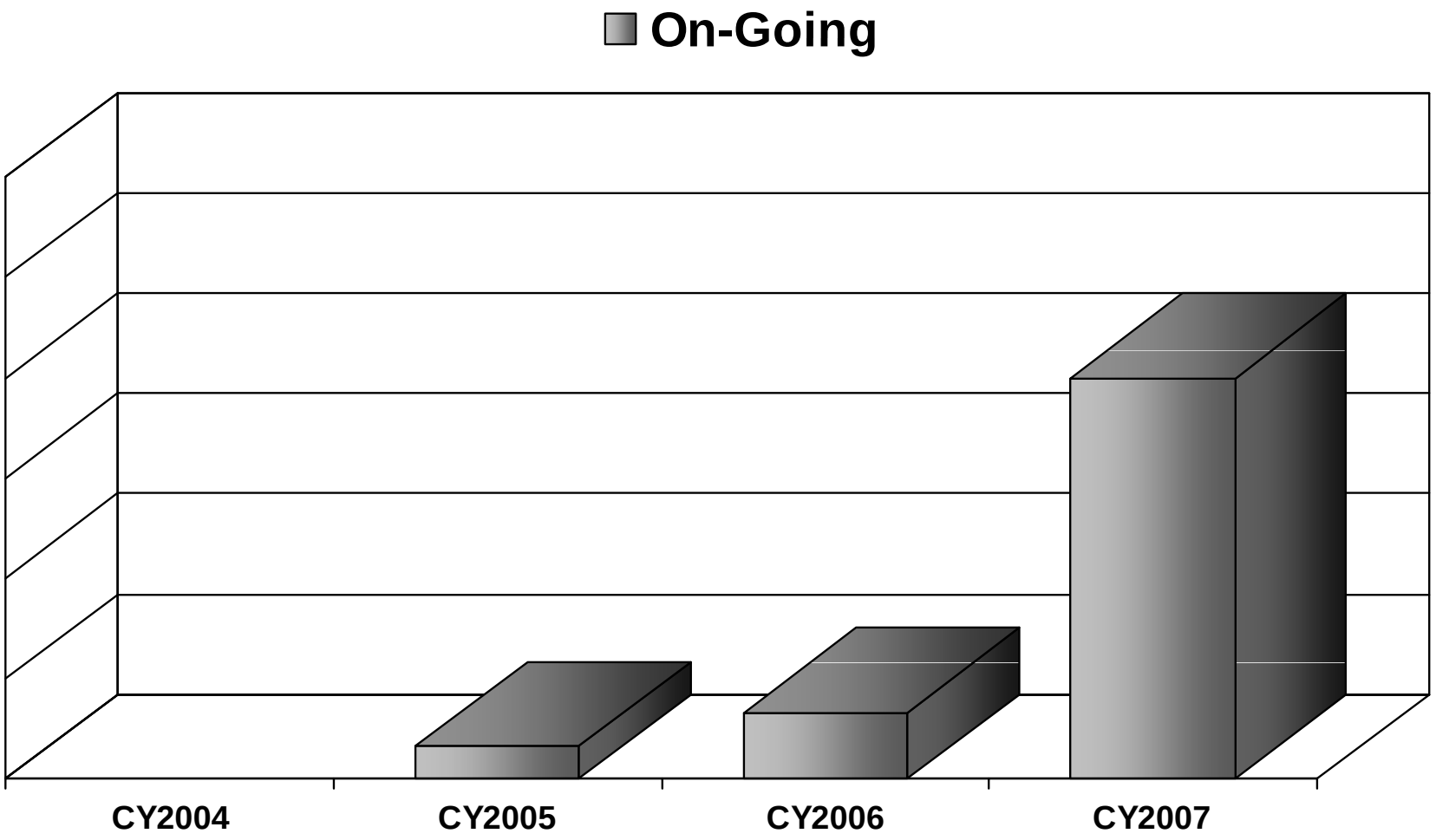
Cumulative Designs & Tape-Outs @ 45 Nanometers



Source: Synopsys 2008

And, We Are Paving The Way, as I Speak

Cumulative Designs @ 32 Nanometers



Source: Synopsys 2008

EDA Supports Industry Trail Blazers in their Challenging Designs

Synopsys IC Compiler Successfully Employed by Matsushita for First 45-nm SoC Design Tapeout

Leading Technologies in Galaxy Design Platform Assisted Matsushita in Achieving Smaller Die Area and Meeting Reduced Power Targets

Intel Selects Synopsys As Its Primary EDA Supplier

Semiconductor and EDA Leaders Sign Multi-Year Commercial, Collaboration Agreement

Synopsys IC Compiler Routing Qualifies for TSMC's 45-Nanometer Process

Enhanced Route Rule Support Immediately Available to All Customers

Source: J.M. William Turner, The Battle of Trafalgar, 1824

What did we all do? The Fabs …

- Manufacturing reduced risk by slowing down introduction of new materials – improved yield by continuing to fine tune existing process materials

- In the “real back end”, OPC/PSM folks stepped up their efforts to reduce distortion between layout – mask – wafer

What did we all do? The Designers …

- Adopted techniques to manage Power:
  - Multi Vth libraries
  - Design with multiple voltages, up to adaptive voltages
  - Aggresive “clock gating”
  - “Power down” full chip blocks
- Re-Use of “standard” blocks, increased
  - processors such as ARMs, MIPS, etc
  - connectivity IP, such as USBs
- Embraced test volume reduction approaches, such as scan compression
- …

The Bottom Line: R&D as a Percentage of Revenue

	250nm		180nm		130nm		90nm		65nm		45nm
	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007
MSFT	17%	17%	15%	16%	17%	15%	21%	21%	16%	14%	14%
NOK	n.a.	n.a.	9%	8%	10%	10%	13%	10%	9%	9%	11%
INTC	9%	10%	11%	11%	14%	15%	14%	14%	13%	17%	15%
STM	15%	16%	16%	13%	15%	16%	17%	17%	18%	17%	18%
QCOM	11%	10%	10%	11%	15%	16%	14%	15%	18%	20%	21%
CDNS	20%	16%	20%	20%	21%	25%	31%	29%	28%	31%	31%
SNPS	22%	22%	20%	26%	27%	24%	24%	26%	32%	34%	31%
MENT	25%	24%	23%	22%	23%	27%	28%	28%	30%	29%	32%

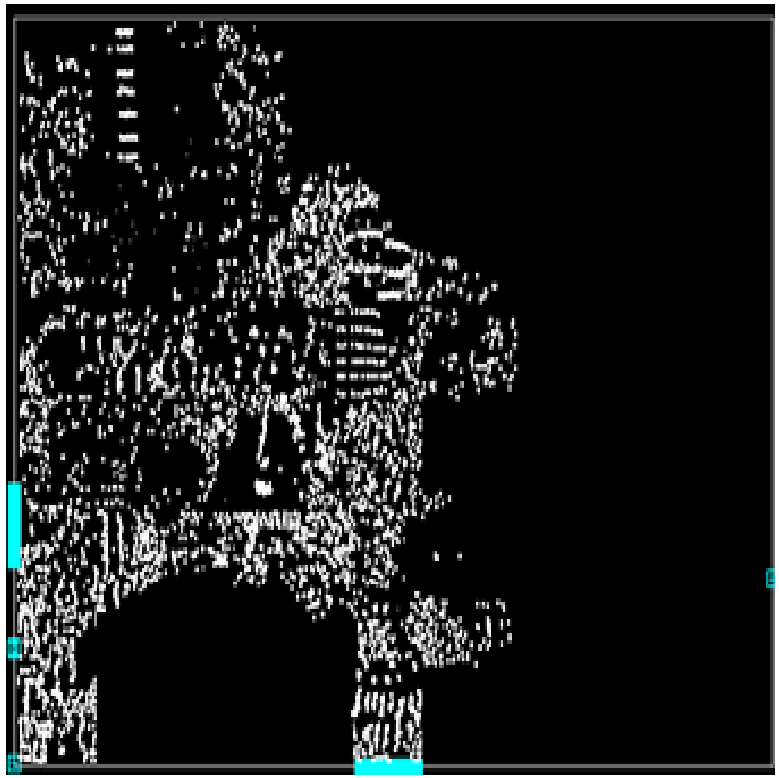
Source: SEC EDGAR 10-Q, 10-K, 20-F 1997-2008

What did we all do? EDA …

- Managed to support the new design techniques
- Kept up with complexity, preserving a “cell based” methodology for digital design
- So what is today “standard” in Physical Design?

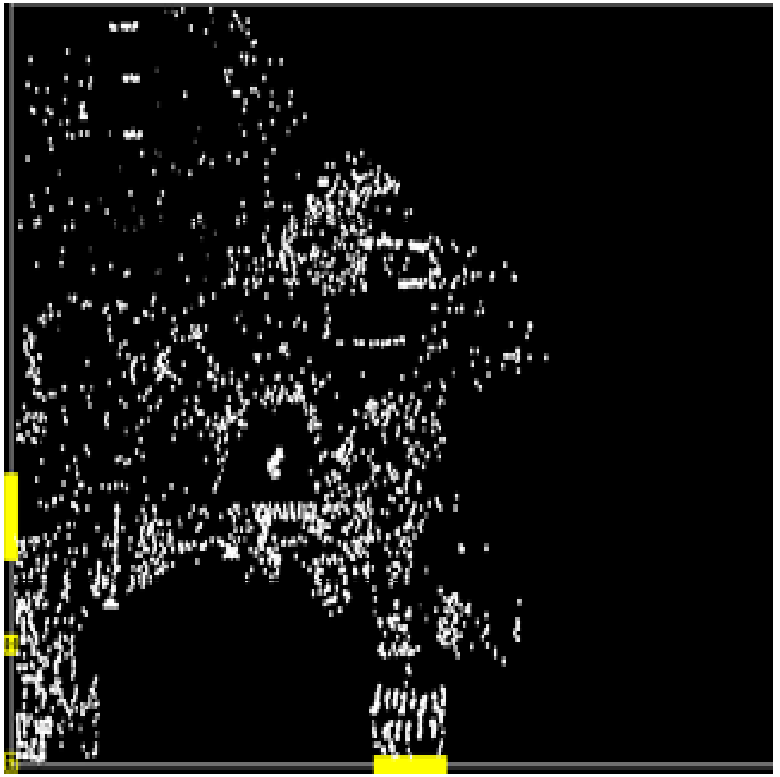
New Technologies for Low Power

Power-Aware Placement & ICG Merging Delivers ~ 20% Dynamic Power Savings



Non-merged Integrated Clock Gating cells with power aware placement

137mW

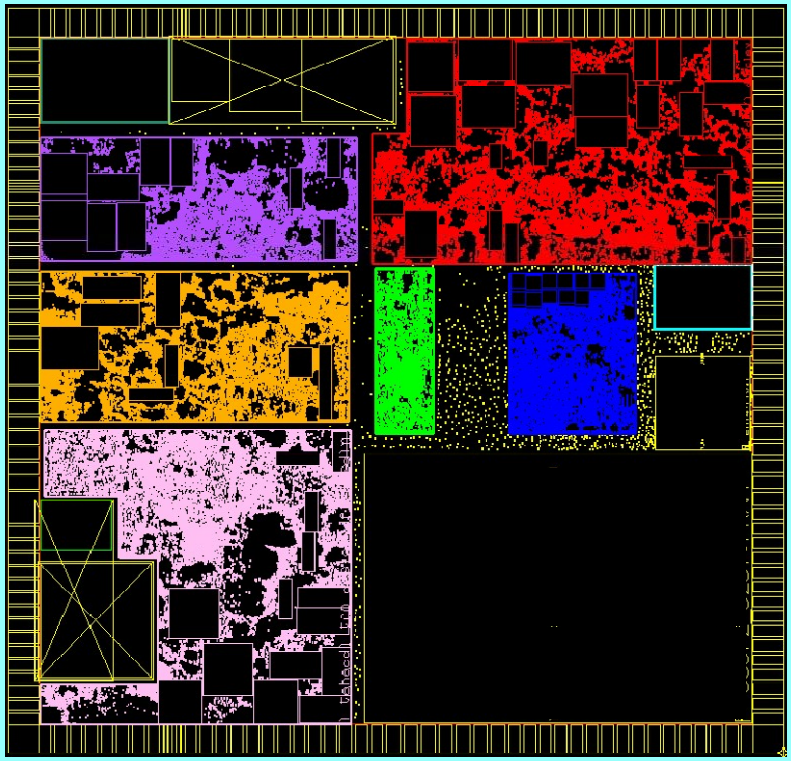


Merged Integrated Clock Gating cells with power aware placement

106mW

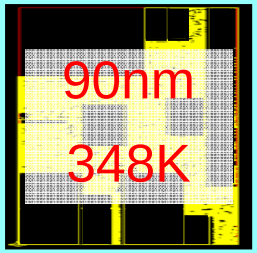
Block Placement and Compaction

Hierarchical Design Planning

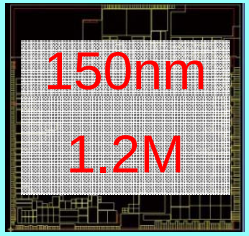


Automatic Die Size Reduction

- Preserves User Intent
- Macros, Blockages, Pin Placement
- Delivers Smallest Routable Area



6% Smaller



14% Smaller

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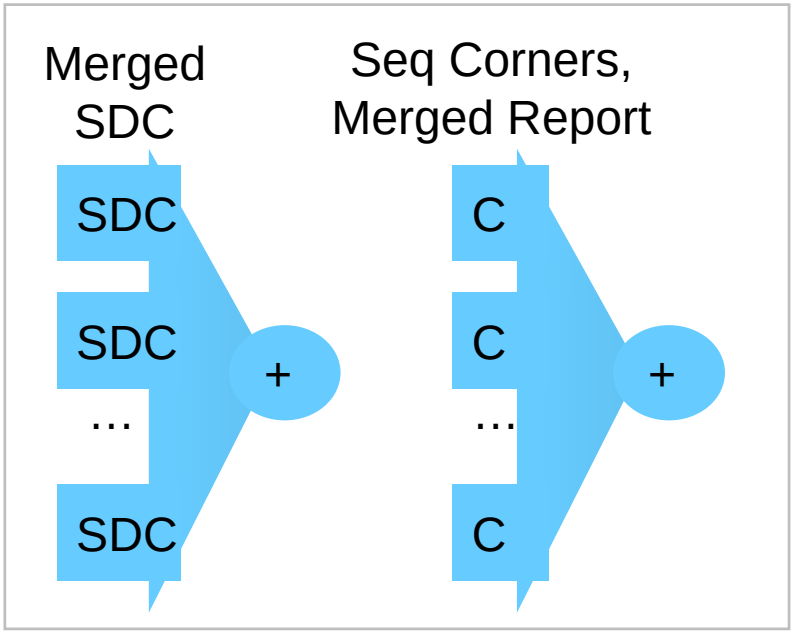
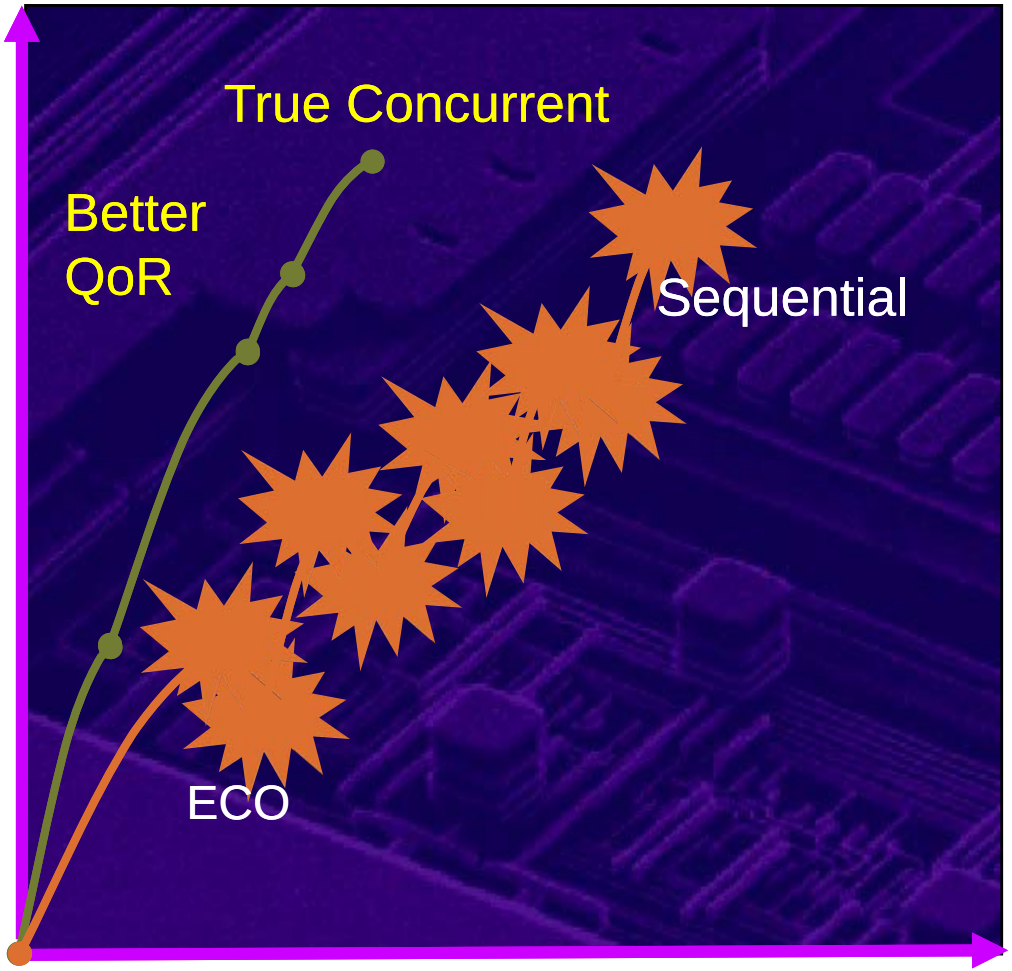
Concurrency in Multi-Mode/Multi-Corner Optimization

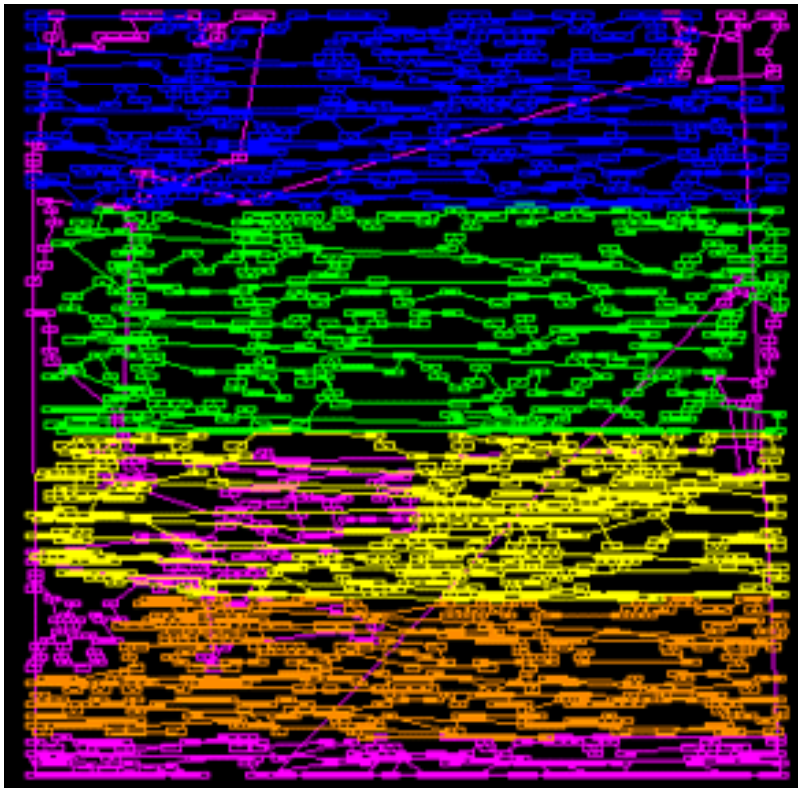




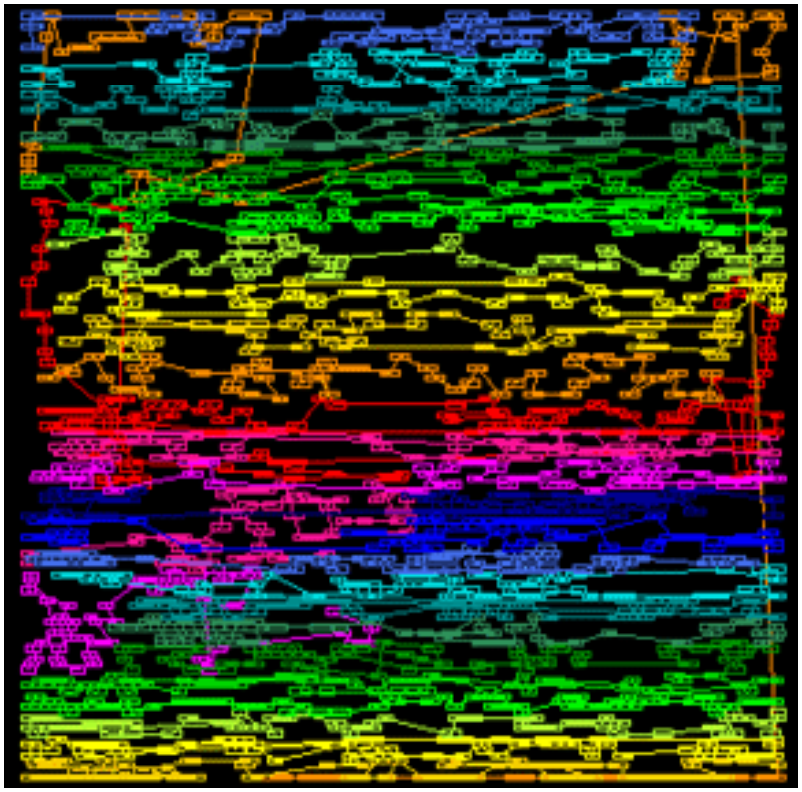
Adaptive Scan Increased Data Complexity

Placement, Timing, Routability All Impacted!

Traditional scan synthesis
generated 5 scan chains



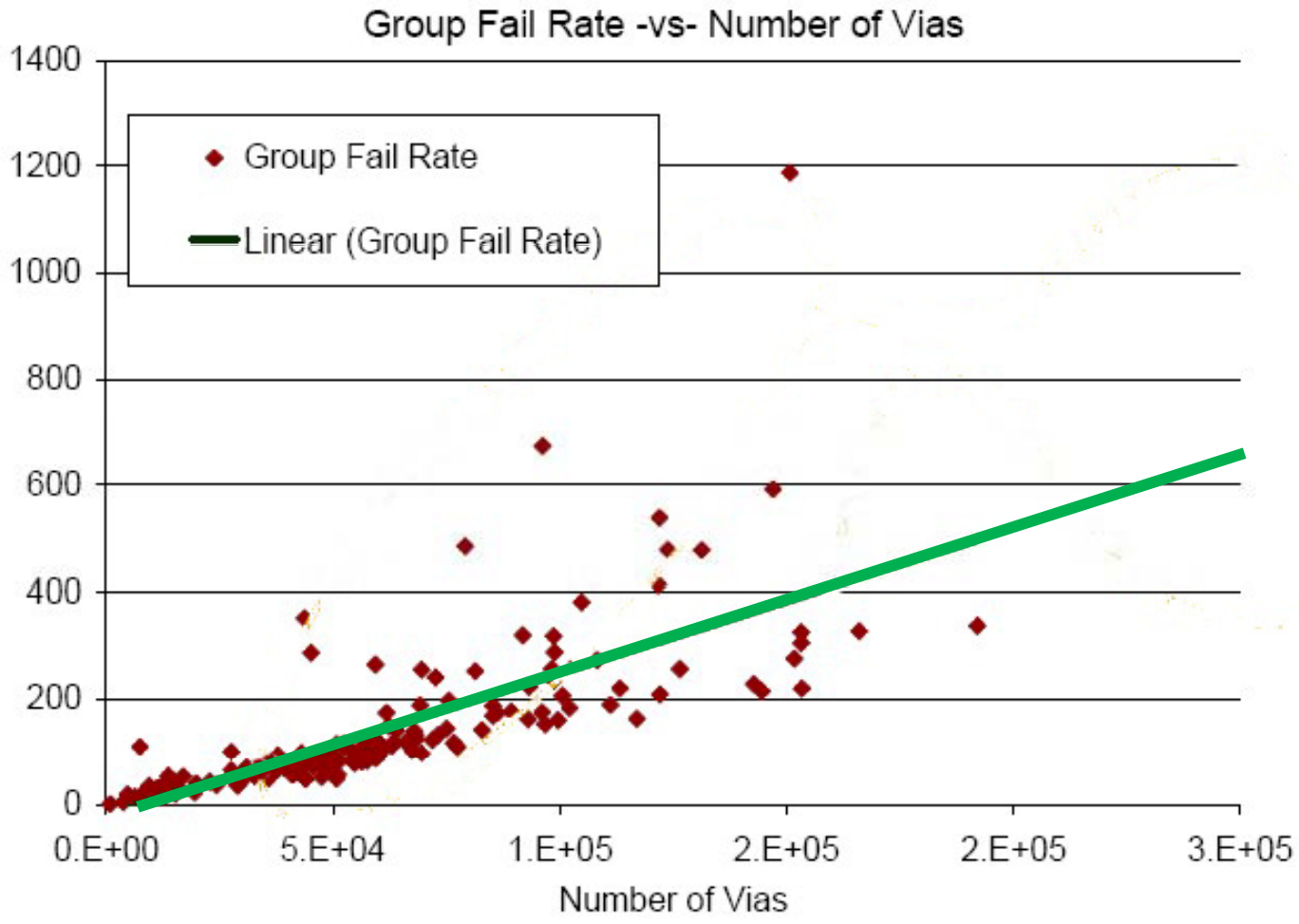
Adaptive scan compression
generated 30 scan chains



Source: Synopsys Compiler Magazine – Rohit Kapur & Kirk Brisacher

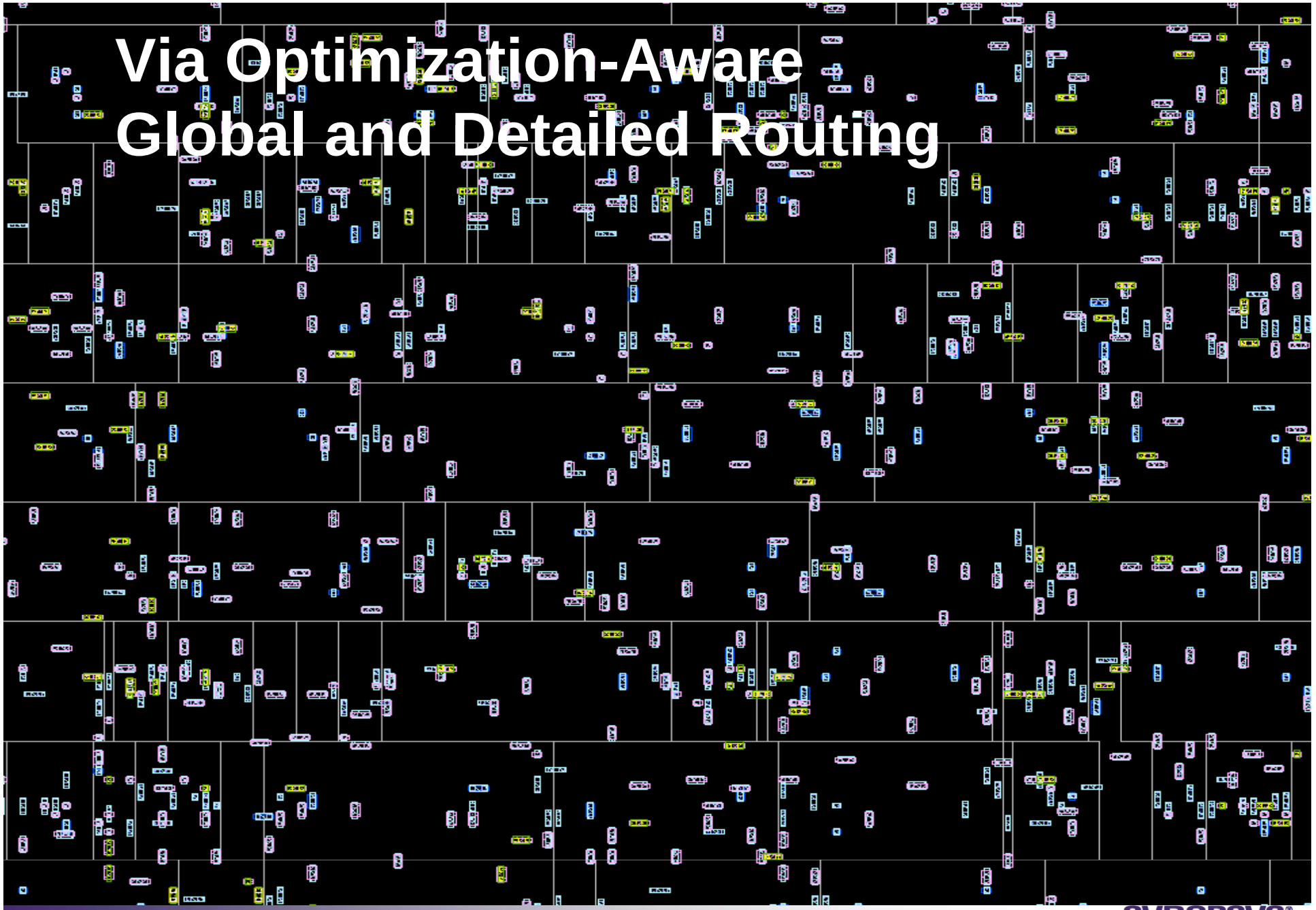
Via Optimization in Routing

Single-Via Fail Rate is 10-100X larger than Double-Via

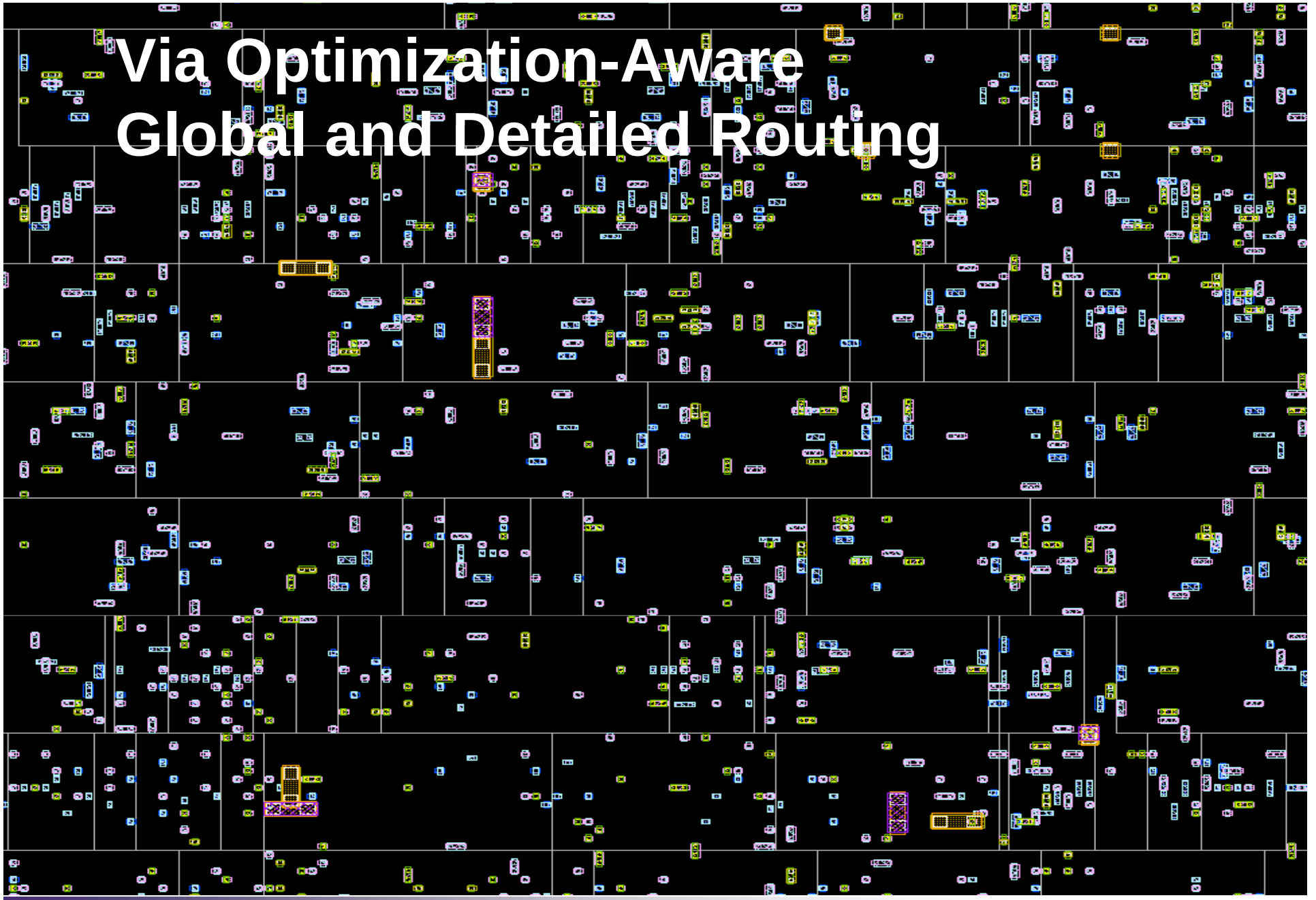


Source: T.Y. Lin, DATE 2007; W.C. Rhines, 2007

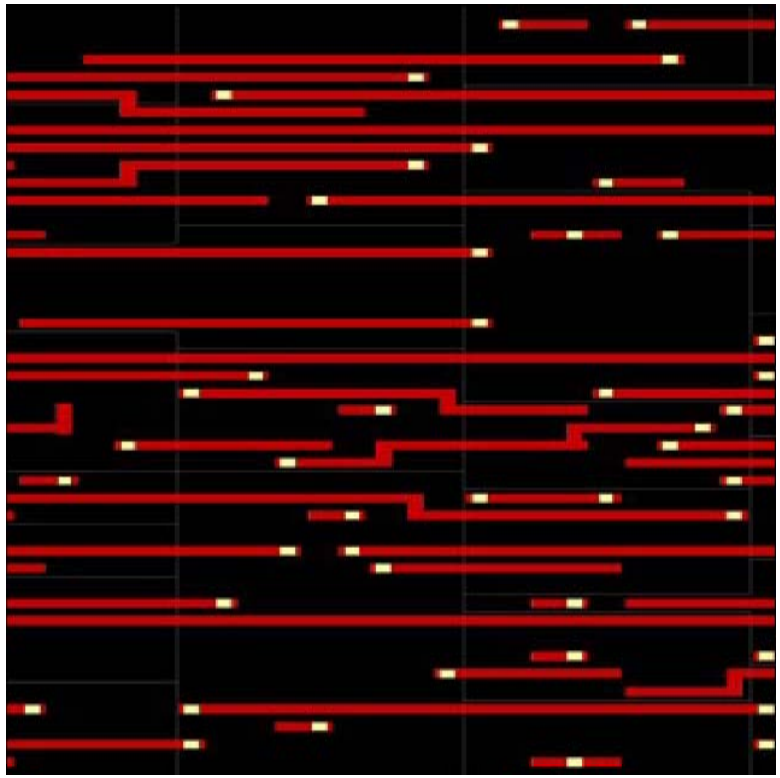
Via Optimization-Aware Global and Detailed Routing



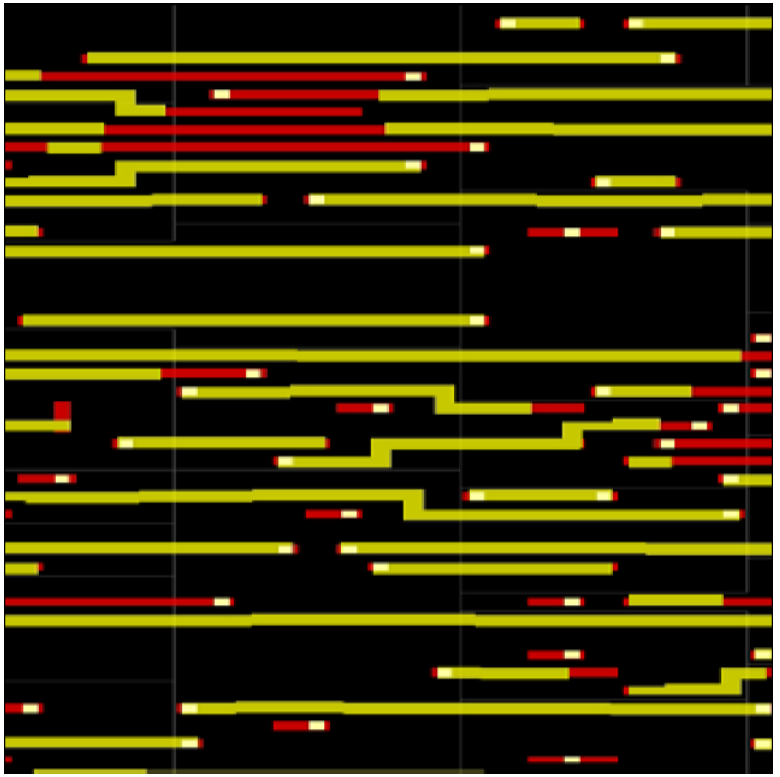
Via Optimization-Aware Global and Detailed Routing



Timing-Driven Wire Spreading/Widening



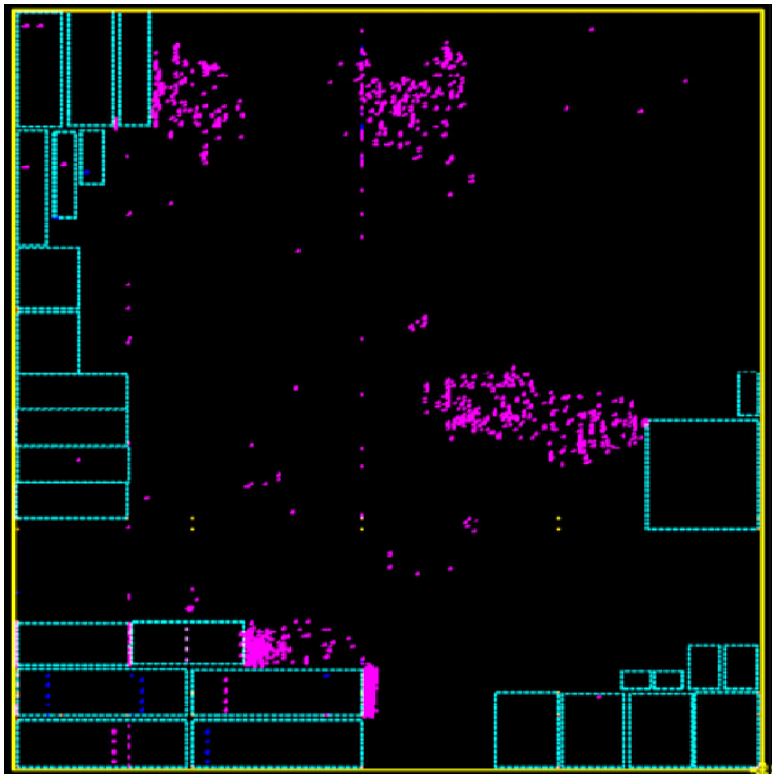
Before Wire Widening



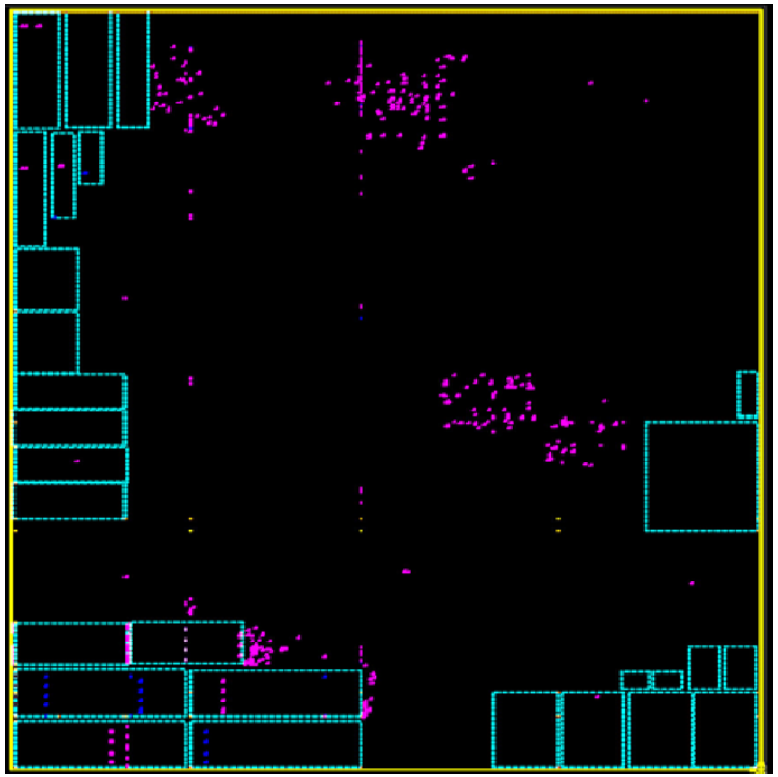
After Wire Widening

Critical Area Optimization (Shorts/Opens)

Timing-Driven Wire Spreading/Widening



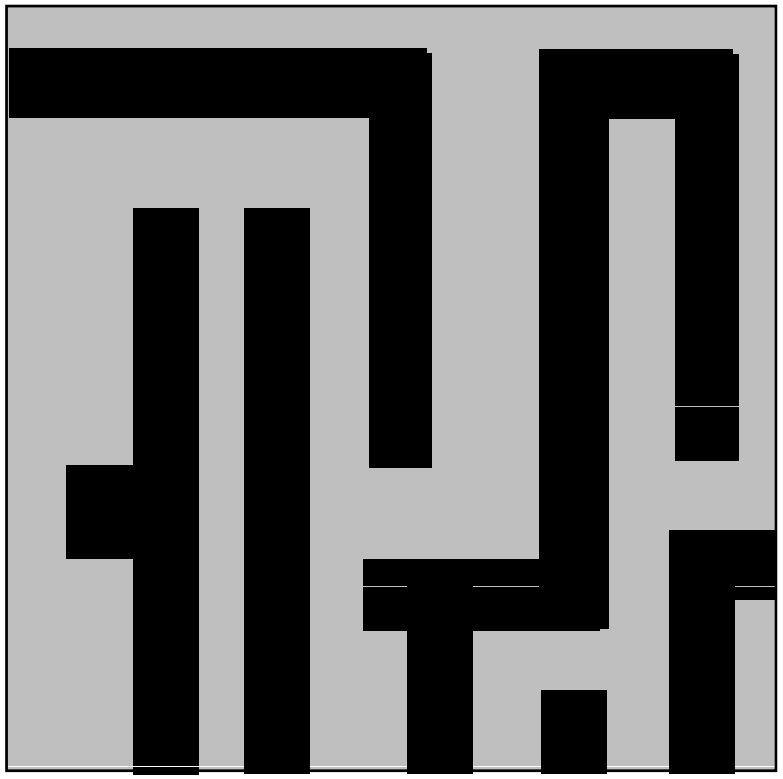
CA Hotspots
Before Wire Spreading/Widening



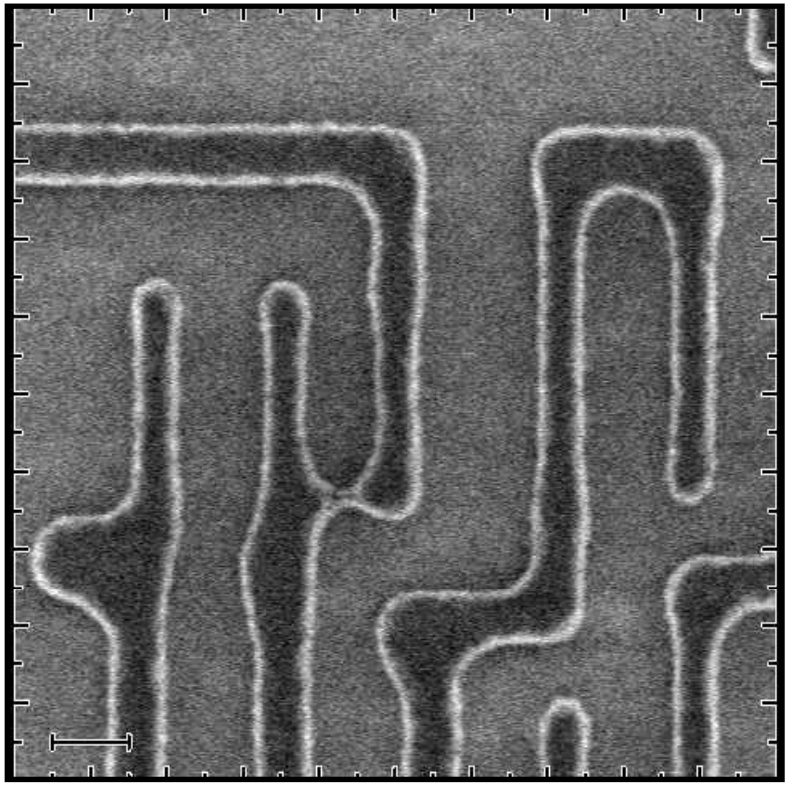
CA Hotspots
After Wire Spreading/Widening

Correctness & Accuracy

100% DRC Correctness May no Longer Be Enough

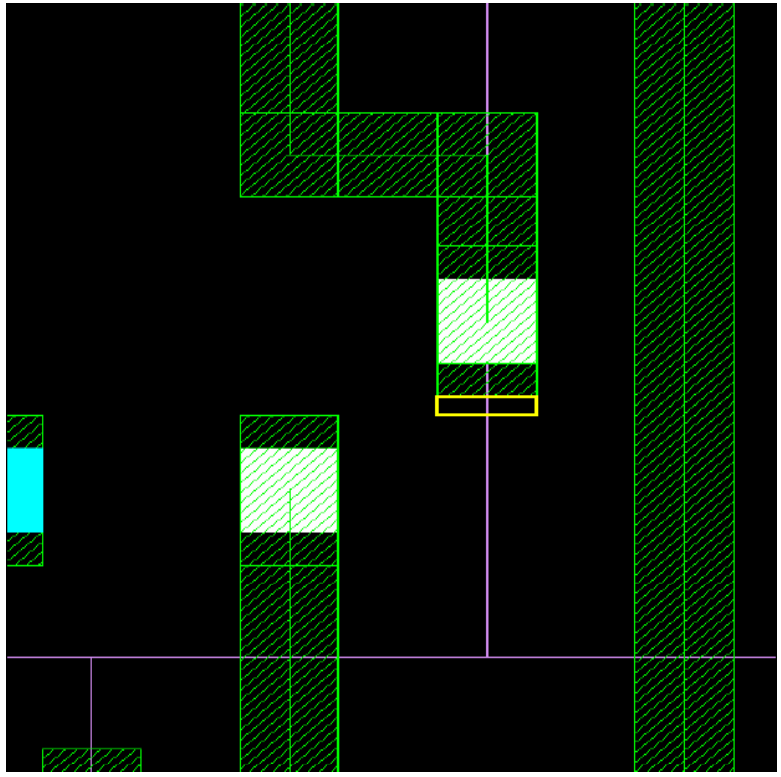


100% DRC Correct

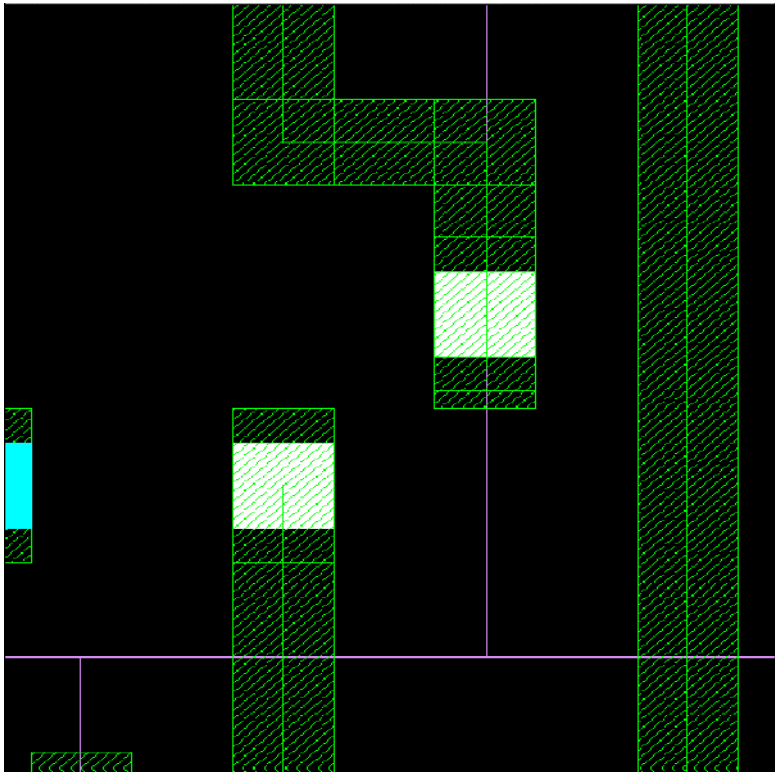


Lithography Hotspot

Litho Hotspots Detection & Correction



Lithography Hotspot Detection



Lithography Hotspot Correction

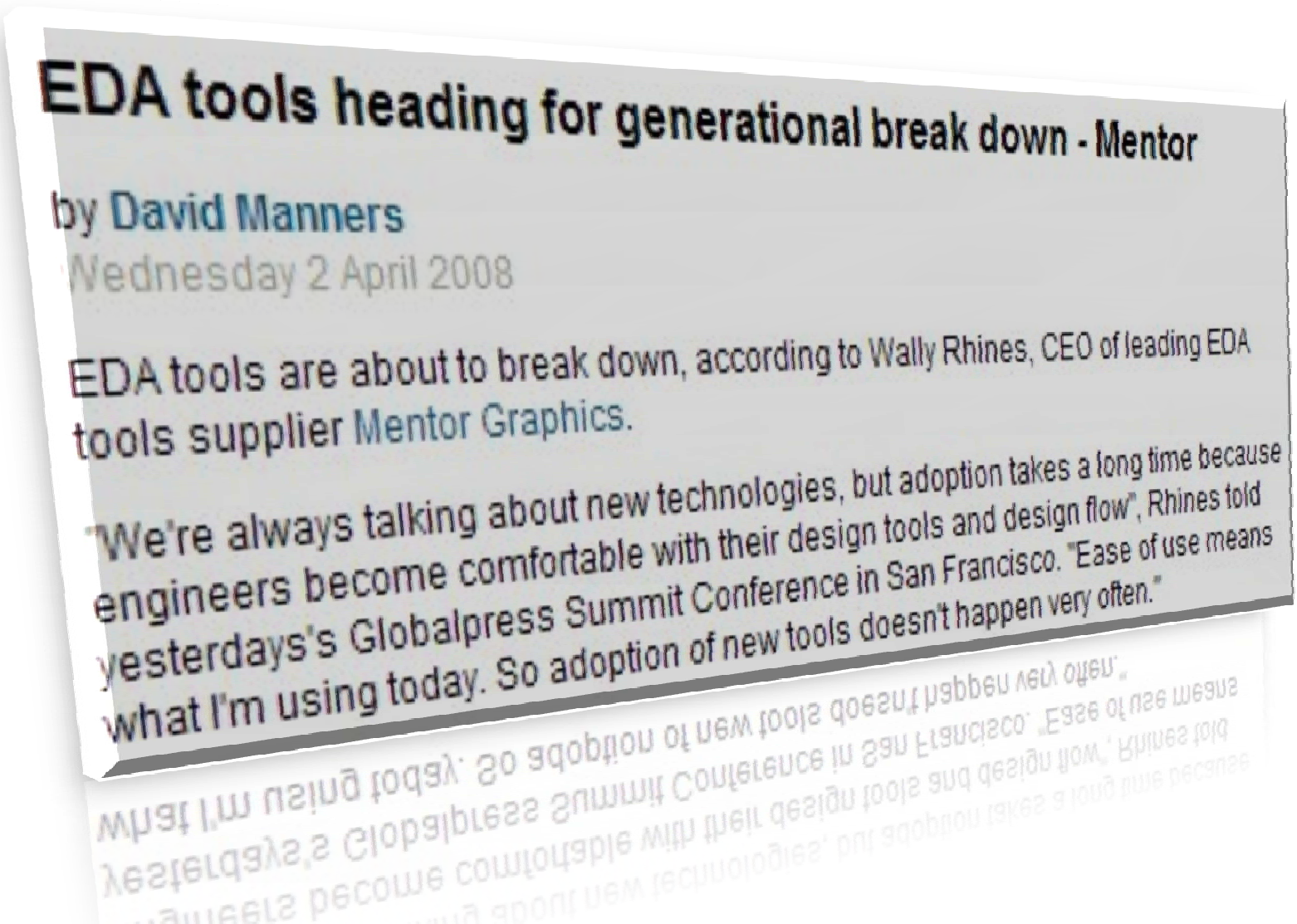
Source: NASA 1970

Disclaimers

Sir Arthur C. Clarke's 1st & 3rd Law

1. "When a distinguished but elderly scientist states that something is possible he is almost certainly right. When he states that something is impossible, he is very probably wrong."
2. "Any sufficiently advanced technology is indistinguishable from magic" and, conversely, "Any technology distinguishable from magic is insufficiently advanced."
3. Having said so…

Recent Comments …



EDA tools heading for generational break down - Mentor

by David Manners

Wednesday 2 April 2008

EDA tools are about to break down, according to Wally Rhines, CEO of leading EDA tools supplier Mentor Graphics.

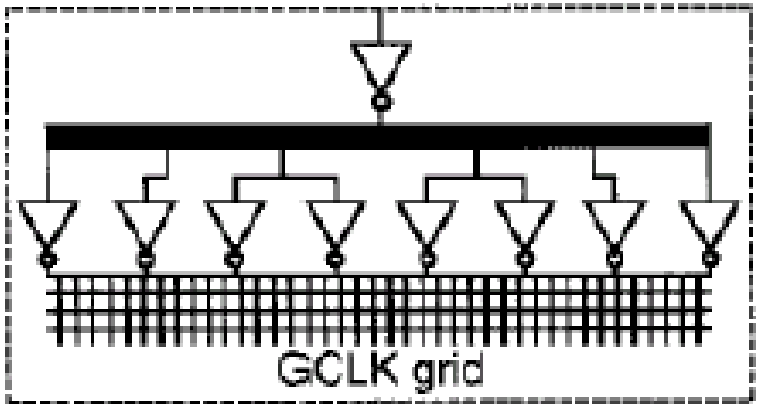
"We're always talking about new technologies, but adoption takes a long time because engineers become comfortable with their design tools and design flow", Rhines told yesterdays's Globalpress Summit Conference in San Francisco. "Ease of use means what I'm using today. So adoption of new tools doesn't happen very often."

Source: Globalpress Summit Conference 2008, W.C. Rhines, CEO Mentor Graphics

Incredibly Complex Clocking Schemes

- Hundreds of clock domains
- Tight skew/latency requirements
- Useful skew time borrowing
- Multi-corner variability management
- Latch based design
- Overlapping/Cascaded clocks
- Gridless clock distribution
- Low power
- Asynchronous clocking schemes

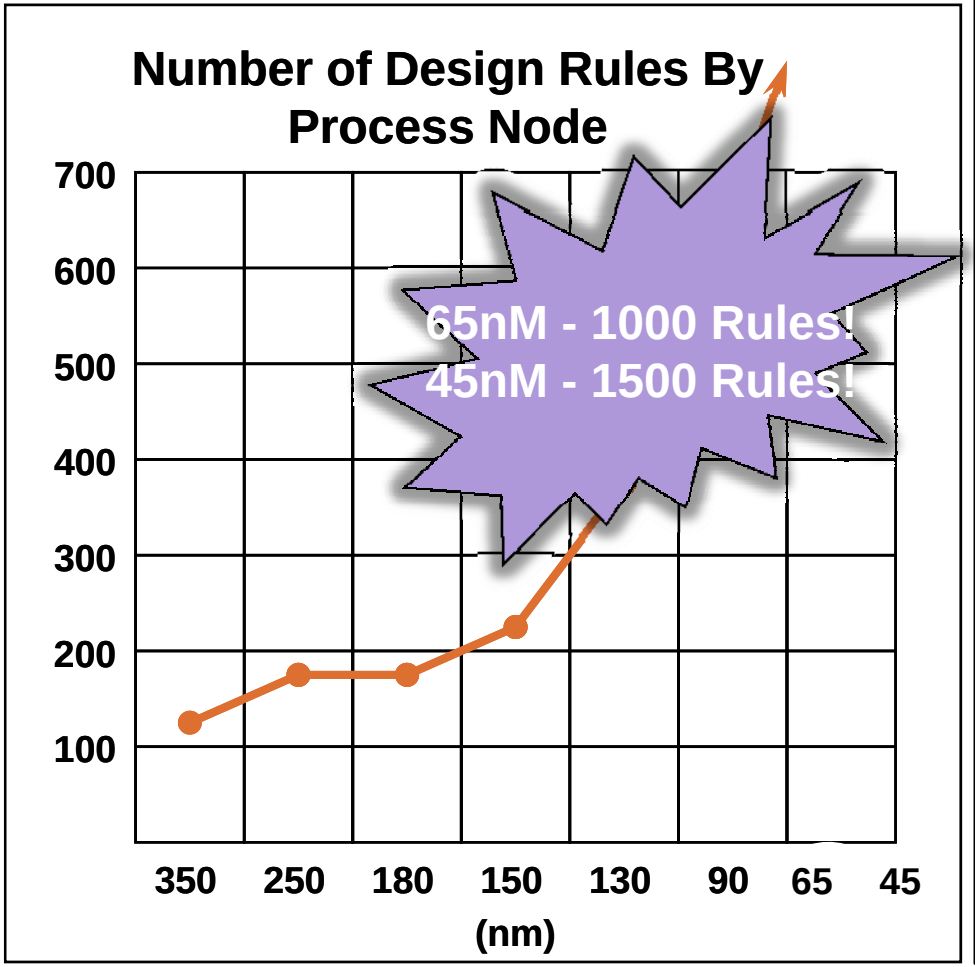
Dec Alpha Clock Distribution

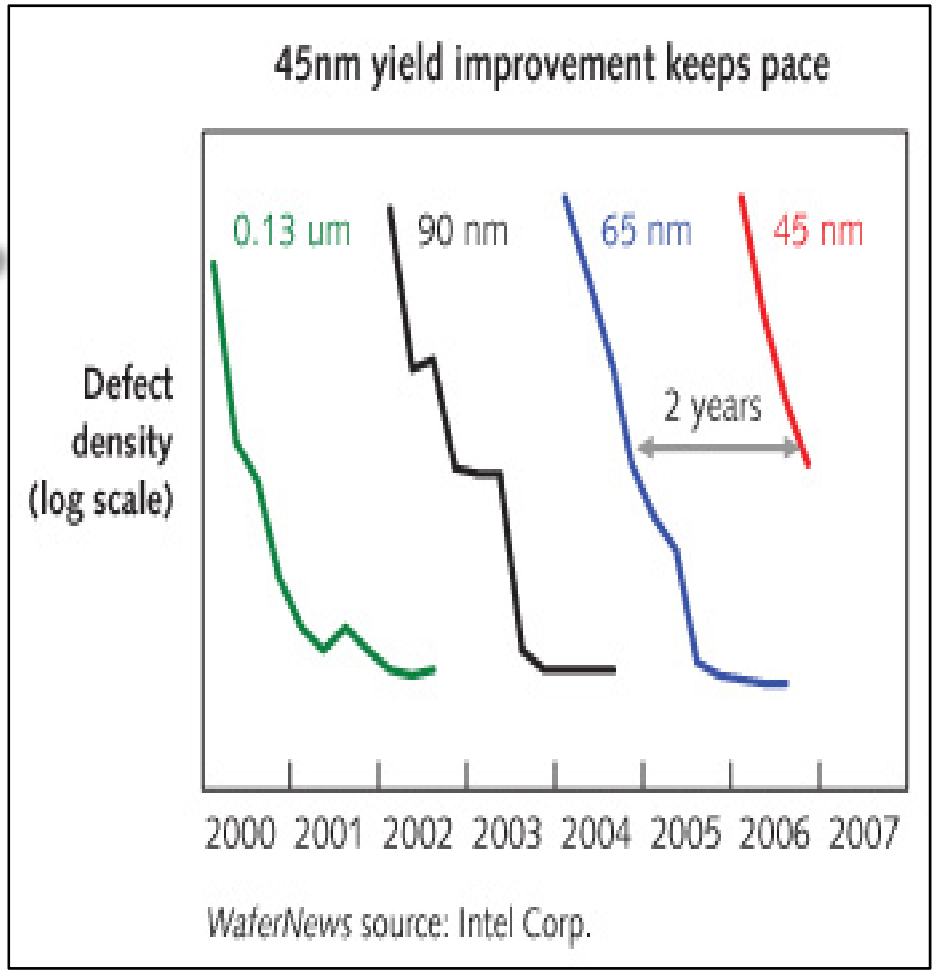


Source: Based on Dennis Sylvester, University of Michigan

Exploding # of Complex Layout Rules

Needed to Extend Use of Litho Techniques





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...

Resulting in

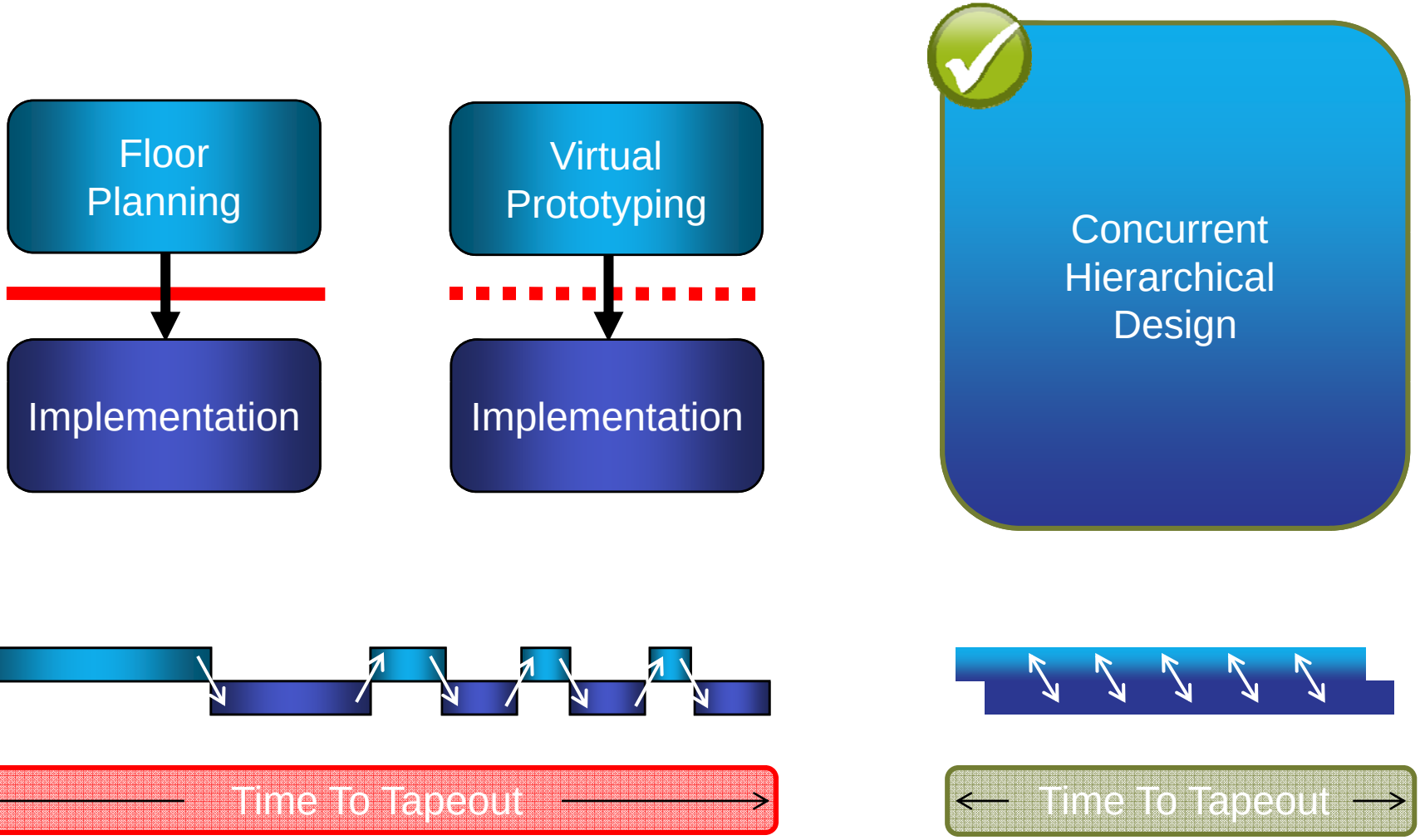
Overloaded

P&R Tools

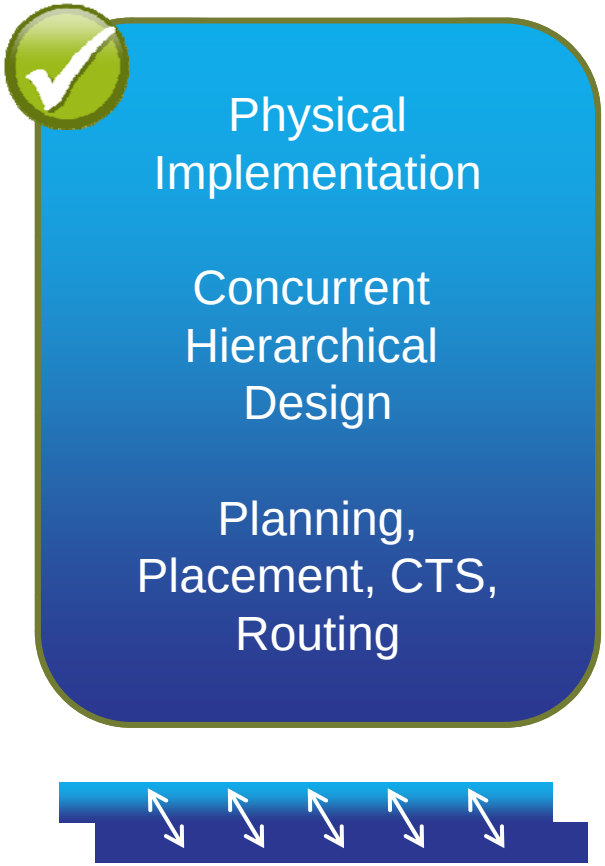
...

Evolution of Physical Design

Concurrent Design Planning & Implementation



Concurrent Design Requires Strong Technology Foundation

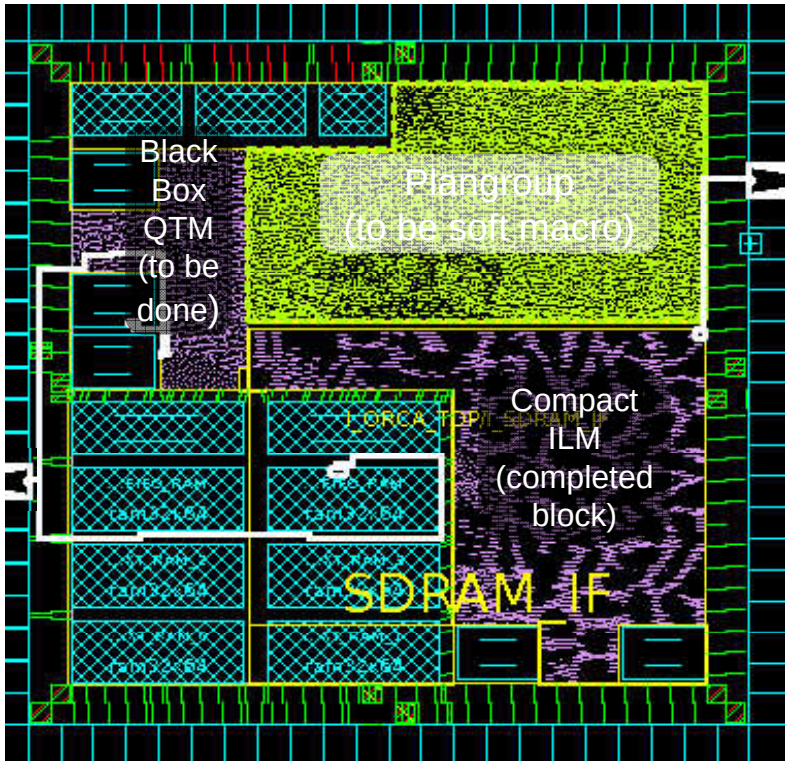


- High predictability and reliability
  - Common engines throughout
  - Single timer throughout
  - Excellent correlation with sign-off
- High degree of automation and productivity
  - Hand-craft quality macro placement
  - Intelligent power network support
  - Technology to get the smallest die
  - Seamlessly integrated environment
- High QoR
  - Sophisticated, scalable optimizations
  - Advanced modeling
  - Best timing, area, power

Concurrent Hierarchical Design

Multi-million Instance Design Implementation

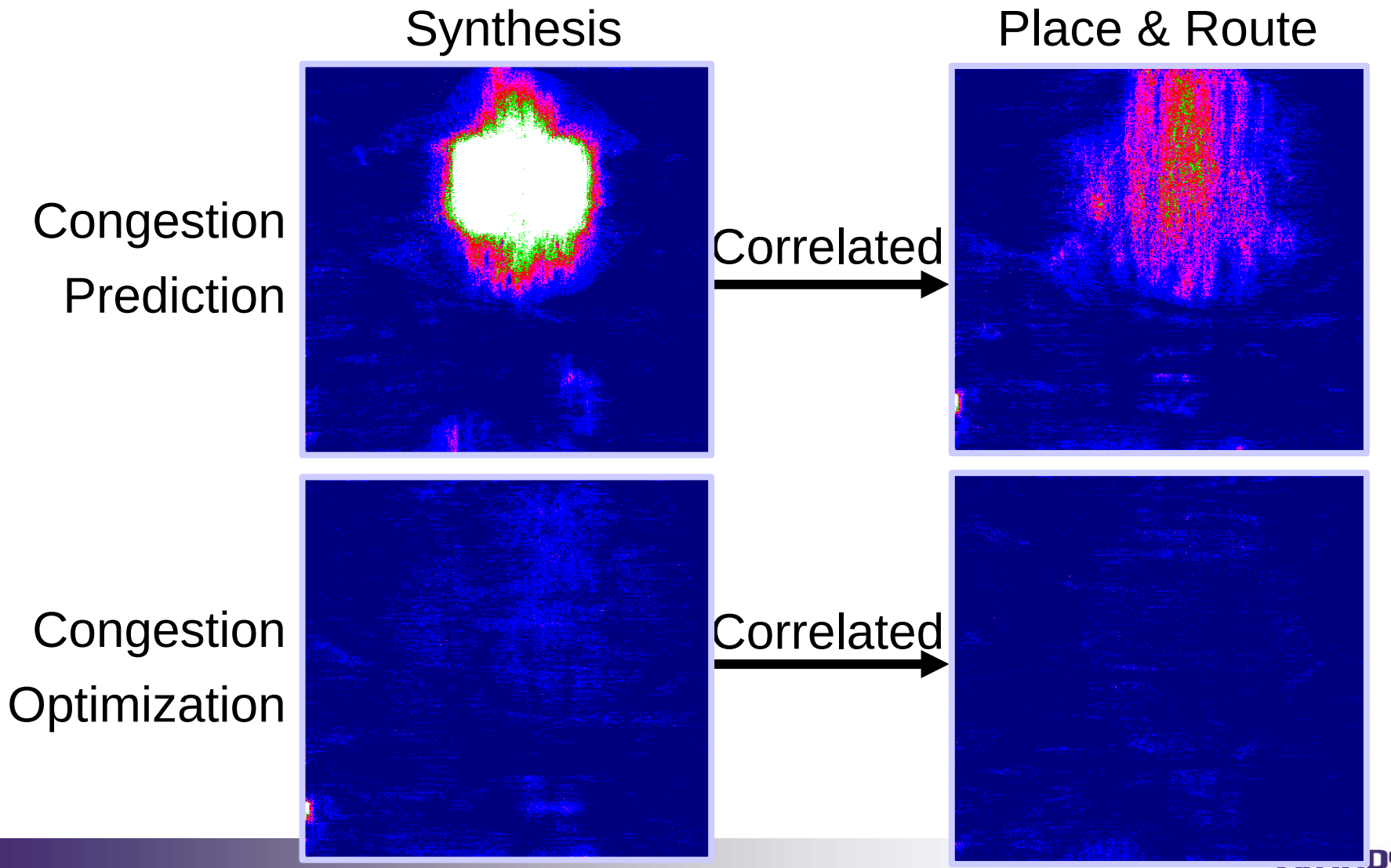
Use All Data Available For Accuracy



- Abstractions to manage runtime & memory
  - Continuous top-level refinement throughout design development
- Physical – shape, macro placement, pin layers and locations
  - Develop in context of full chip
- Timing – clocks, in/out delays, exceptions
  - Accurate topology of external environment inputs produces accurate constraint outputs

Early Relief for P & R Tools

Identify /Fix Congestion Before Hand-off to P&R

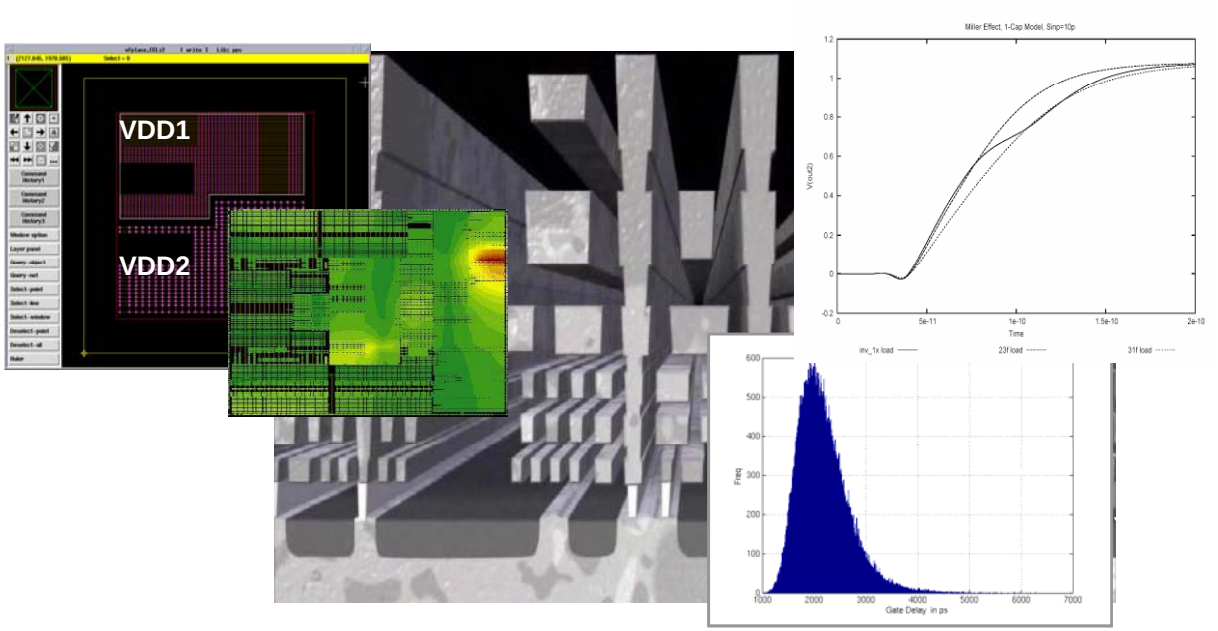


Source: Synopsys Design Compiler Graphical + IC Compiler

Accurate Modeling of Physical Effects

For 65-nm and Below

- Current Source timing/noise/power models
  - Accuracy needed for VDSM technology nodes
  - V/T scaling support to reduce data capacity



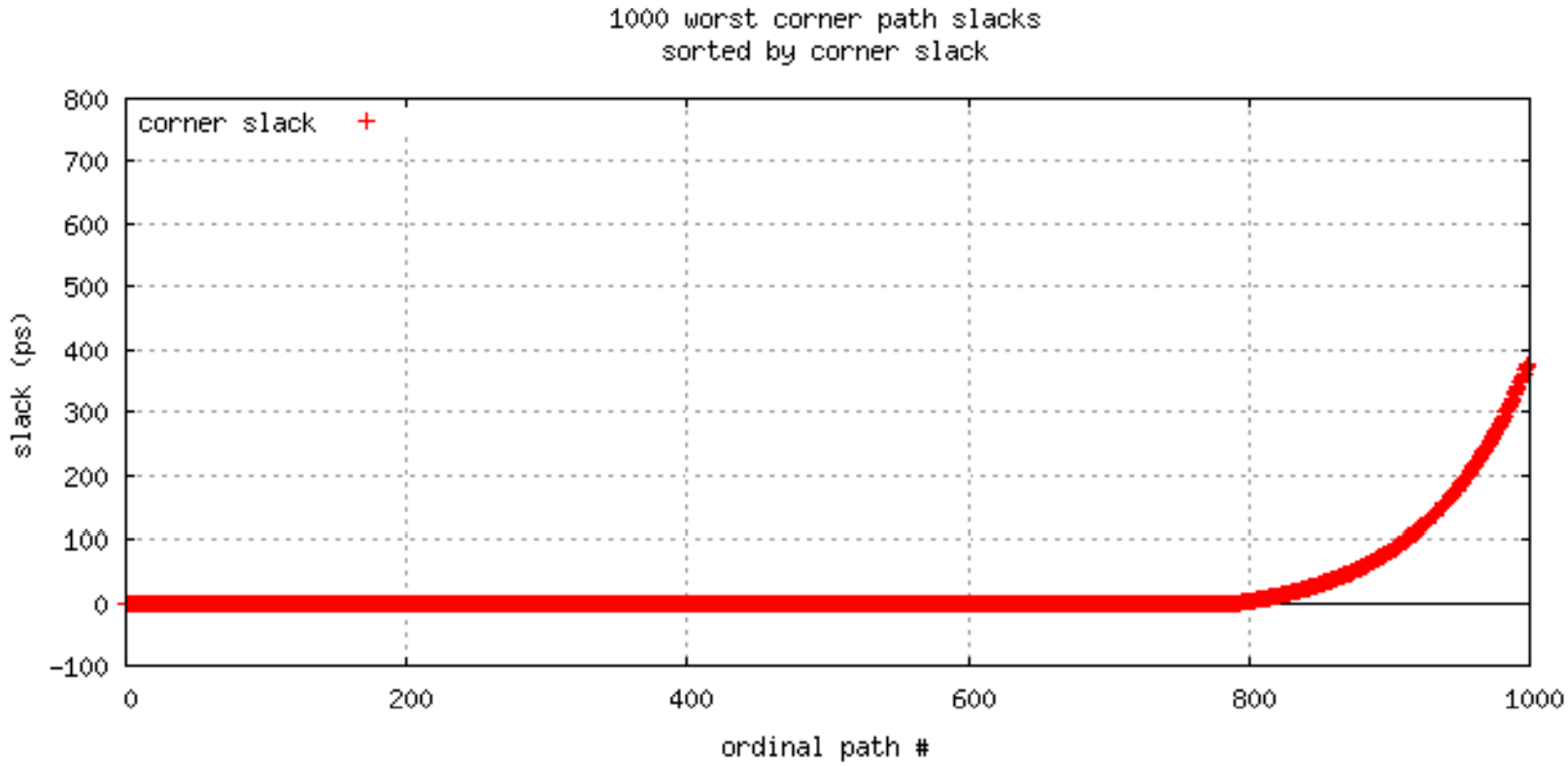
Non-linear Waveforms:

- ***High Impedance nets***
- ***Miller Effect***
- ***Signal Integrity***
- ***Double Switching***

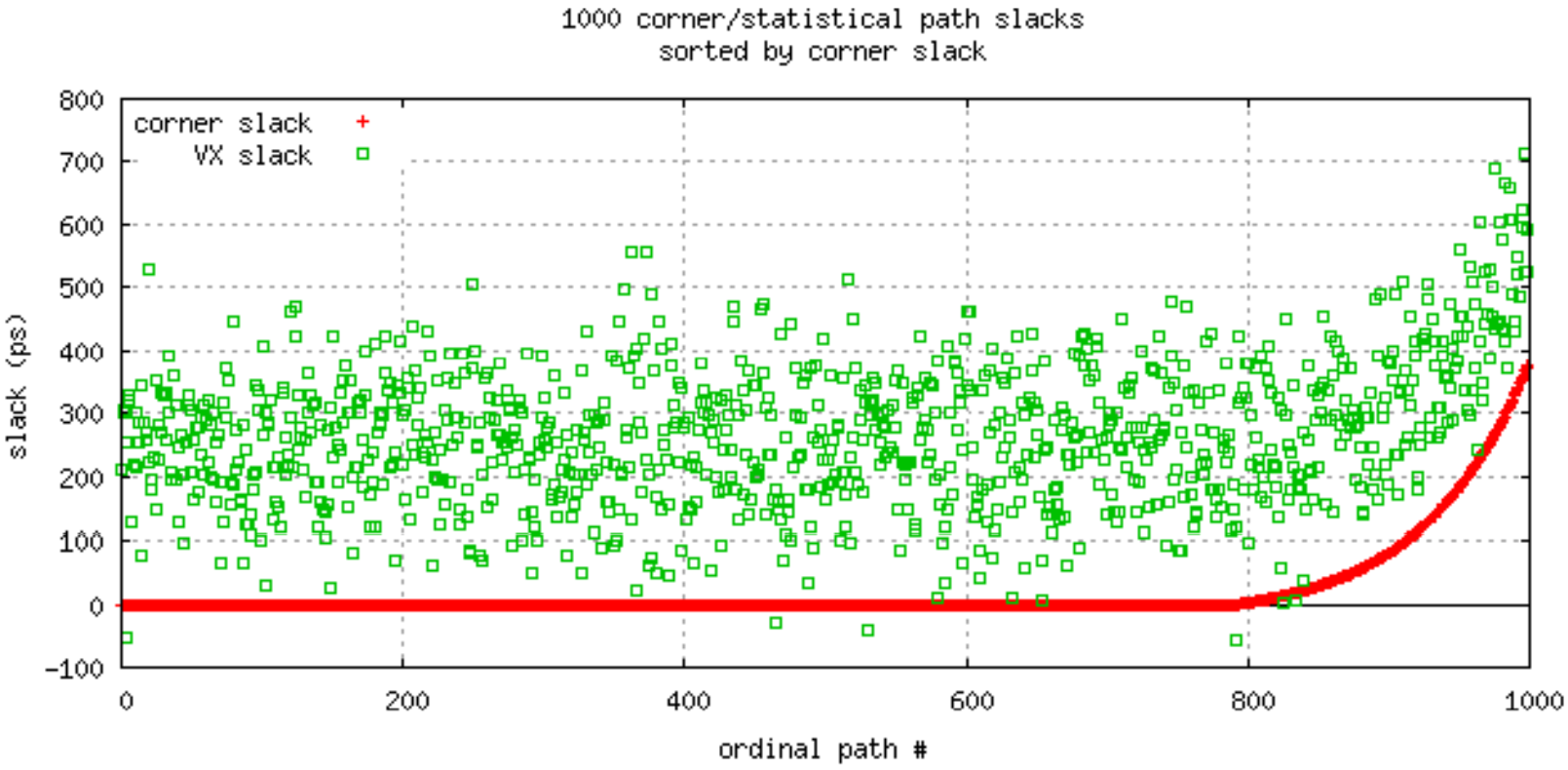
Source: R. Chau, Intel 2003

Corner-Based STA is Pessimistic

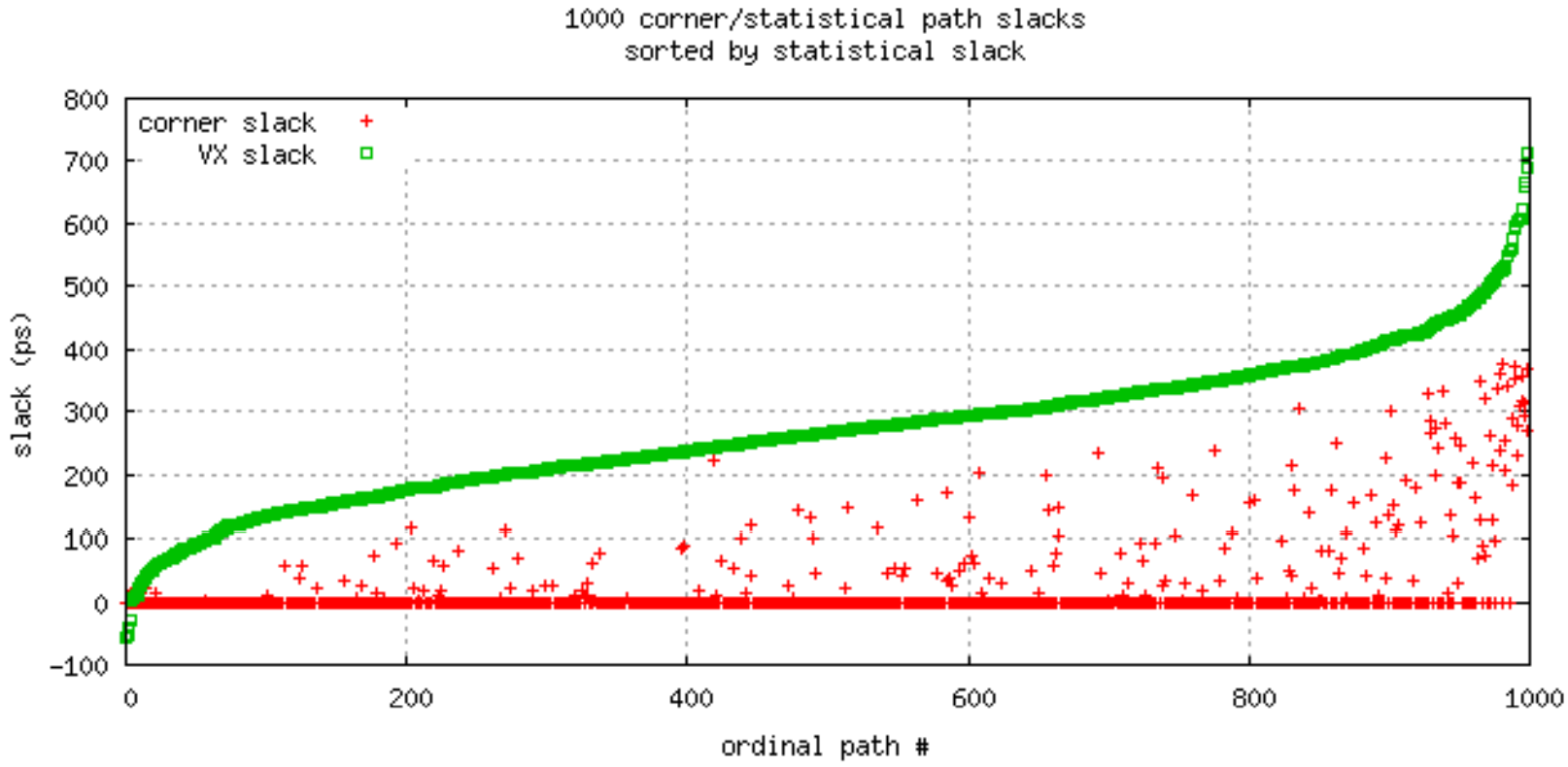
Emphasis on Worst Case Bounds



Statistical STA to Reduce Margins 1

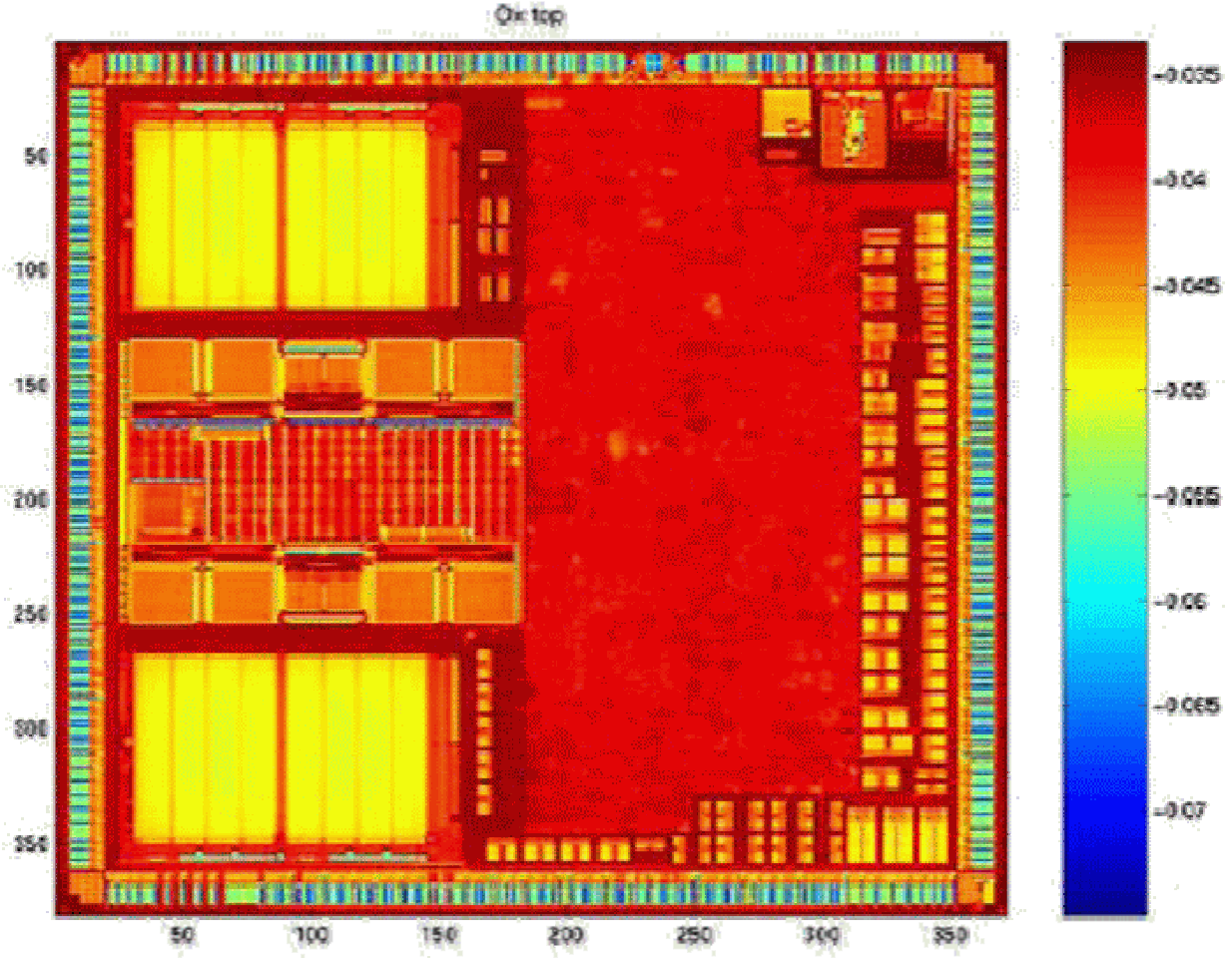


Statistical STA to Reduce Margins 2



Metal Fill

CMP Uniformity Reduces Variability

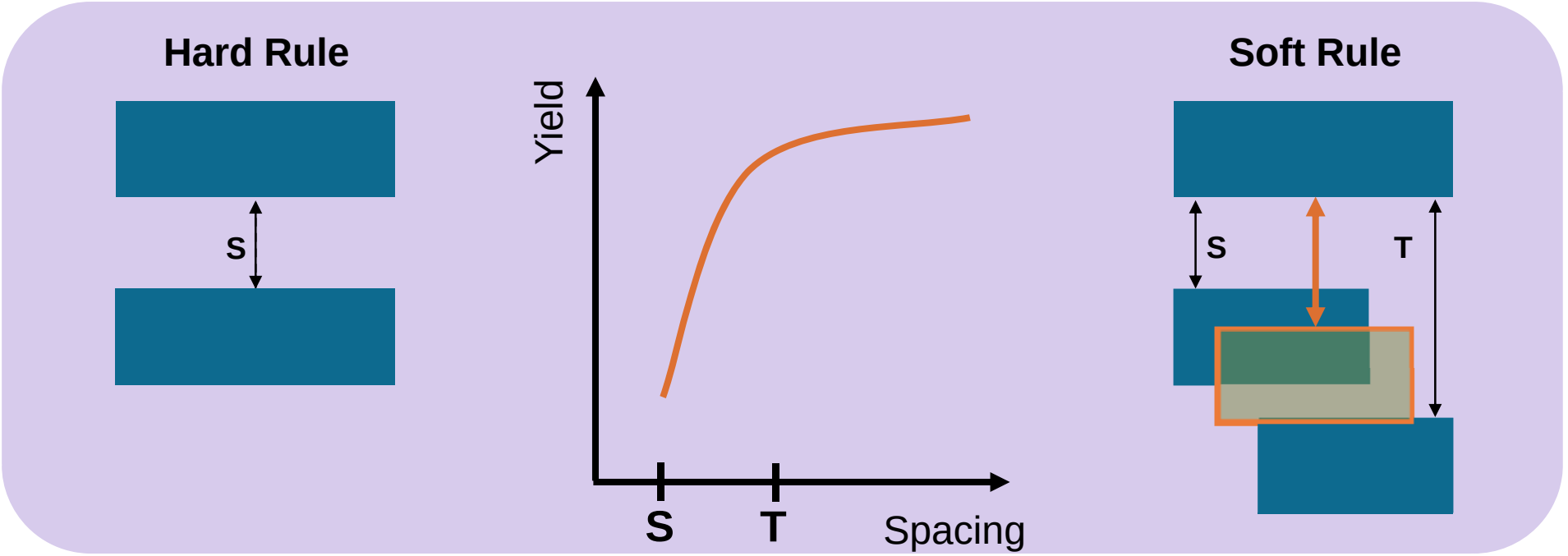


Cu Dishing < 40Å

Source: L. Pileggi, CMU 2005

Native Soft Rule Support for Flexibility

- Yield generally improves when designs are relaxed from the minimums
- Soft rules allow for flexibility based on available space



Source: Michelangelo Buonarroti, La Creazione di Adamo, 1511; Farchild 1958; Intel 2008

Design will be the Driver

Sustainable Differentiation and Innovation

EE Times:

TI to make fabless switch at 45 nm

Mark LaPedus
(01/29/2007 9:00 AM EST)

Texas Instruments Inc. has decided to halt internal process technology development at the 45-nanometer node and use foundry-supplied processes at 32 nm, 22 nm and thereafter. The move would save a great deal of money in both process development and fab building, allowing it to focus on adding value in design.

On the digital front, TI plans to develop closer ties to foundries. Instead of separately creating its own core technology, TI will work collaboratively with foundry partners to specify and drive the next generations of digital process technology, and will continue to make products within its fabs.

The chip maker has clearly been clobbered by what could be termed the perfect storm. Amid a slowdown in its wireless business, TI has seen its rivals--such as Broadcom, Qualcomm and others--close the process technology gap by using foundries.

The handwriting was on the wall for TI last month when it disclosed it was still struggling to ramp up its 193-nm immersion scanners from ASML Holding NV within its leading-edge fabs at the 45-nm node. TI is also moving in a new direction for low-k dielectrics, said TI senior vice president and chief technology officer Hans Stork.

Design will be the Driver

Sustainable Differentiation and Innovation

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Some Conclusions

- P&R must continue to have deep algorithmic enhancements
- There will be some relief for P&R tools
  - better netlists, improved constraints, good timing models, less emphasis on corners and margins
- Improved use of Hierarchy is needed
  - ease of use is the main requirement
- Manufacturing will increase influence, but through rules
  - will be closer, but still a clear distance

Predictable Success