sierra
DESIGN AUTOMATION

Variation and Litho-driven Physical Design

ISPD 2007

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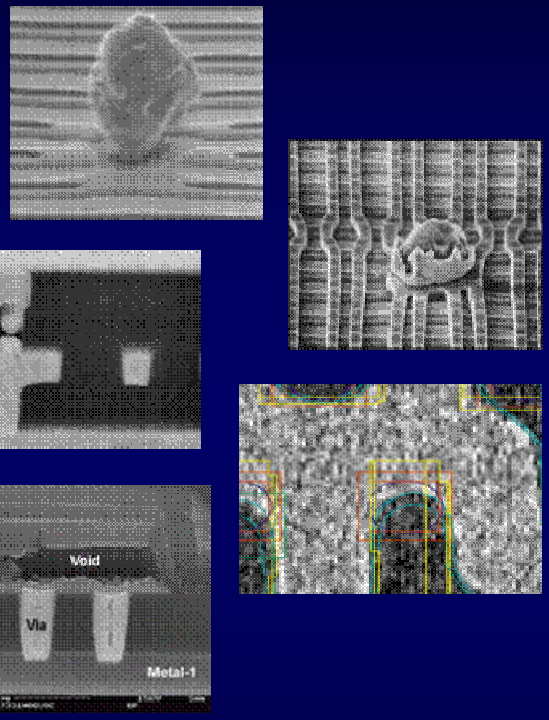
Agenda

- Physical Design at 65nm/45nm
- Variation challenges and solutions
- Routing challenges and solutions
- Summary

Three Major PD Challenges

- Lithography Variations
  - Complexity in Routing Rules
  - Need for DFM-driven routing
- Process & Operational Variations
  - Variation-driven STA
  - Need for Variation-driven implementation
- Large Design Sizes
  - Scalability of Physical Design Algorithms



- *WYSNWYG – 193nm light used to create 65nm/45nm patterns*
- *Due to light dosage, light focus, mask alignment*
- *OPC simulation – exploding data volume*

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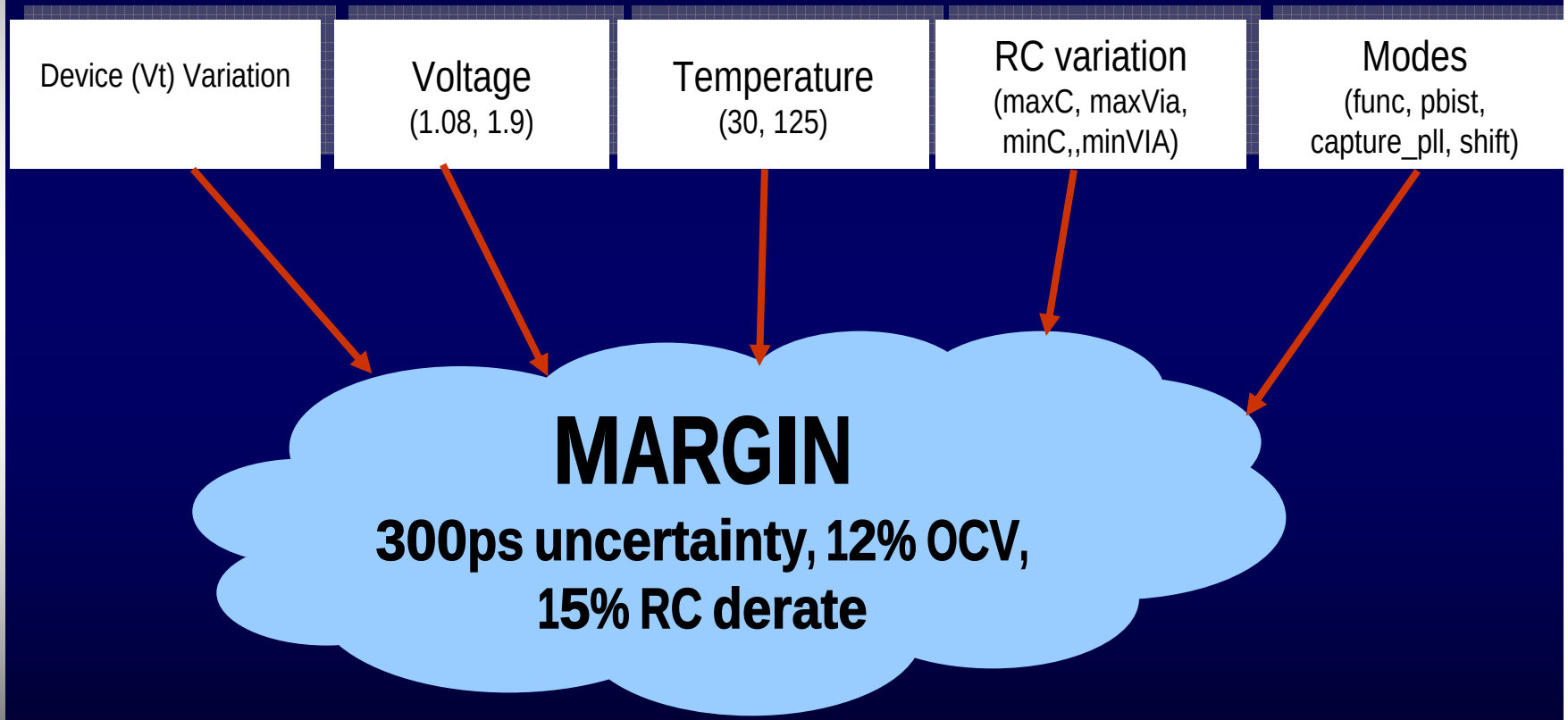
Variability Leads to Design Margins

DSP, 65nm, 9M Gates, 12 modes/corners



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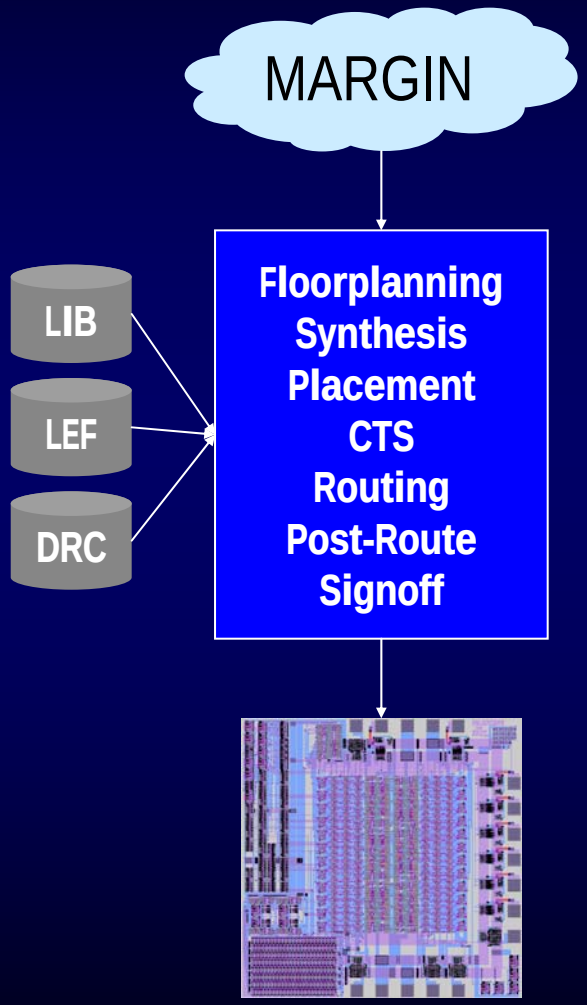
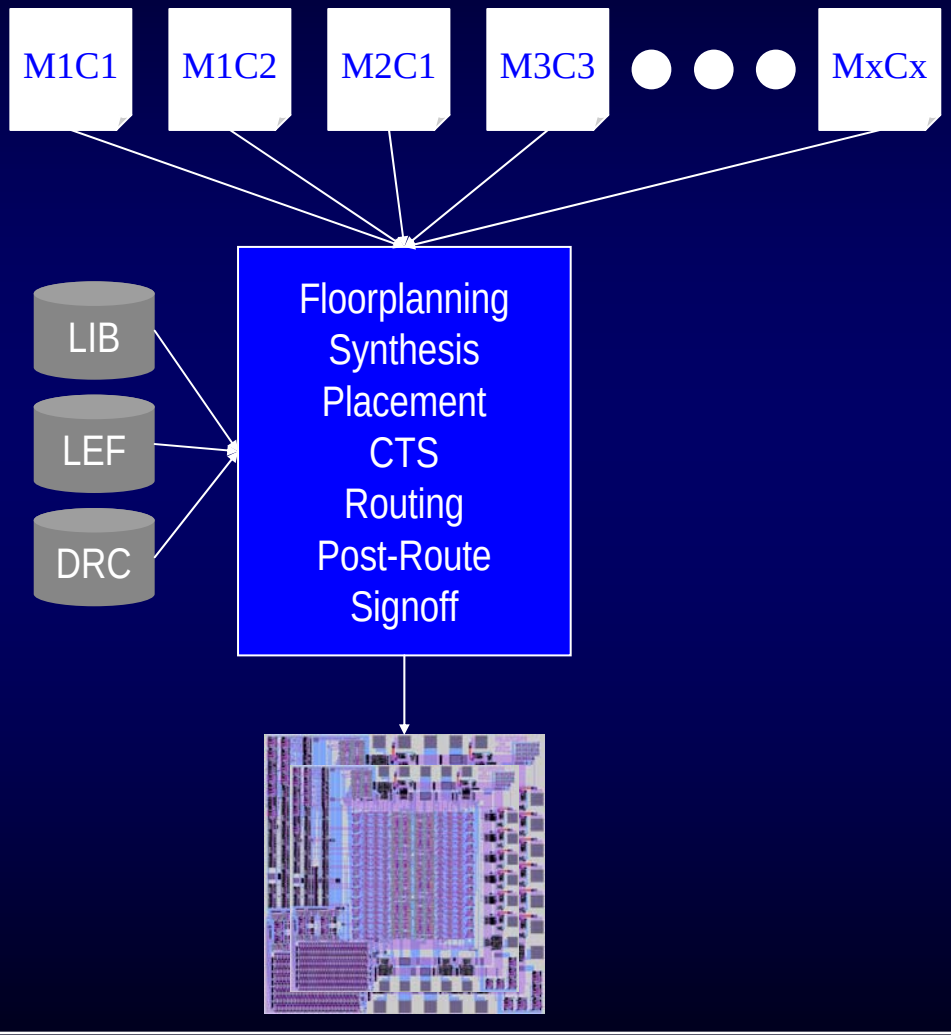
Design Flow with Margins



- Sample Margins
  - 20% faster clock
  - 250-300ps uncertainty
  - 10% RC derating
  - 10% OCV
  - 25% max slew derate
- Resulting Chips
  - 20-100% more time to closure
  - 5-15% bigger die
  - 5-15% more power

Design Flow Without Margins



- Instead of margins, define mode/corner variation scenarios upfront
  - Variation Timer back-bone ensures closure over each step of flow
- Results
  - Up to 2X faster TAT
  - Up to 15% smaller die
  - Up to 15% lesser power

Case Study : Server Chip

- Design Details:
  - 12M gates flat (3M instances)
  - 4 Corners + 6 Modes (24 Combinations)

XAUI	(slow_ocv, Cworst)	setup, hold	BIST	(slow_ocv, Cworst)	setup, hold
XAUI	(fast_ocv RCbest)	hold, leakage	BIST	(fast_ocv RCbest)	hold, leakage
XAUI	(fast_lv, Cbest)	hold, leakage	BIST	(fast_lv, Cbest)	hold, leakage
XAUI	(fast_ht, RCworst)	hold, leakage	BIST	(fast_ht, RCworst)	hold, leakage
RGMII	(slow_ocv, Cworst)	setup, hold	SHFT	(slow_ocv, Cworst)	setup, hold
RGMII	(fast_ocv, RCbest)	hold, leakage	SHFT	(fast_ocv, RCbest)	hold, leakage
RGMII	(fast_lv, Cbest)	hold, leakage	SHFT	(fast_lv, Cbest)	hold, leakage
RGMII	(fast_ht, RCworst)	hold, leakage	SHFT	(fast_ht, RCworst)	hold, leakage
LB	(slow_ocv, Cworst)	setup, hold	CAP	(slow_ocv, Cworst)	setup, hold
LB	(fast_ocv, RCbest)	hold, leakage	CAP	(fast_ocv, RCbest)	hold, leakage
LB	(fast_lv, Cbest)	hold, leakage	CAP	(fast_lv, Cbest)	hold, leakage
LB	(fast_ht, RCworst)	hold, leakage	CAP	(fast_ht, RCworst)	hold, leakage

- Target:
  - Fix Setup, Hold for All 24 modes/corners
  - Leakage opt on selected combinations
  - 14hrs CPU

Key Technologies Needed for Variation aware tools

- Concurrent Multi-mode analysis (operational variability)
- Concurrent Multi-corner analysis (global variability)
- Concurrent local variability analysis (OCV, NBTI, Statistical Models)
- Concurrent Multi-mode Multi-corner Implementation
  - Placement, CTS, Optimization, Routing, DFM Steps
- Scalability
  - Sub-linear increase in runtime and memory with number of scenarios
- Hierarchical Methodology
  - Budgeting, chip-level timing closure are affected by modes and corners

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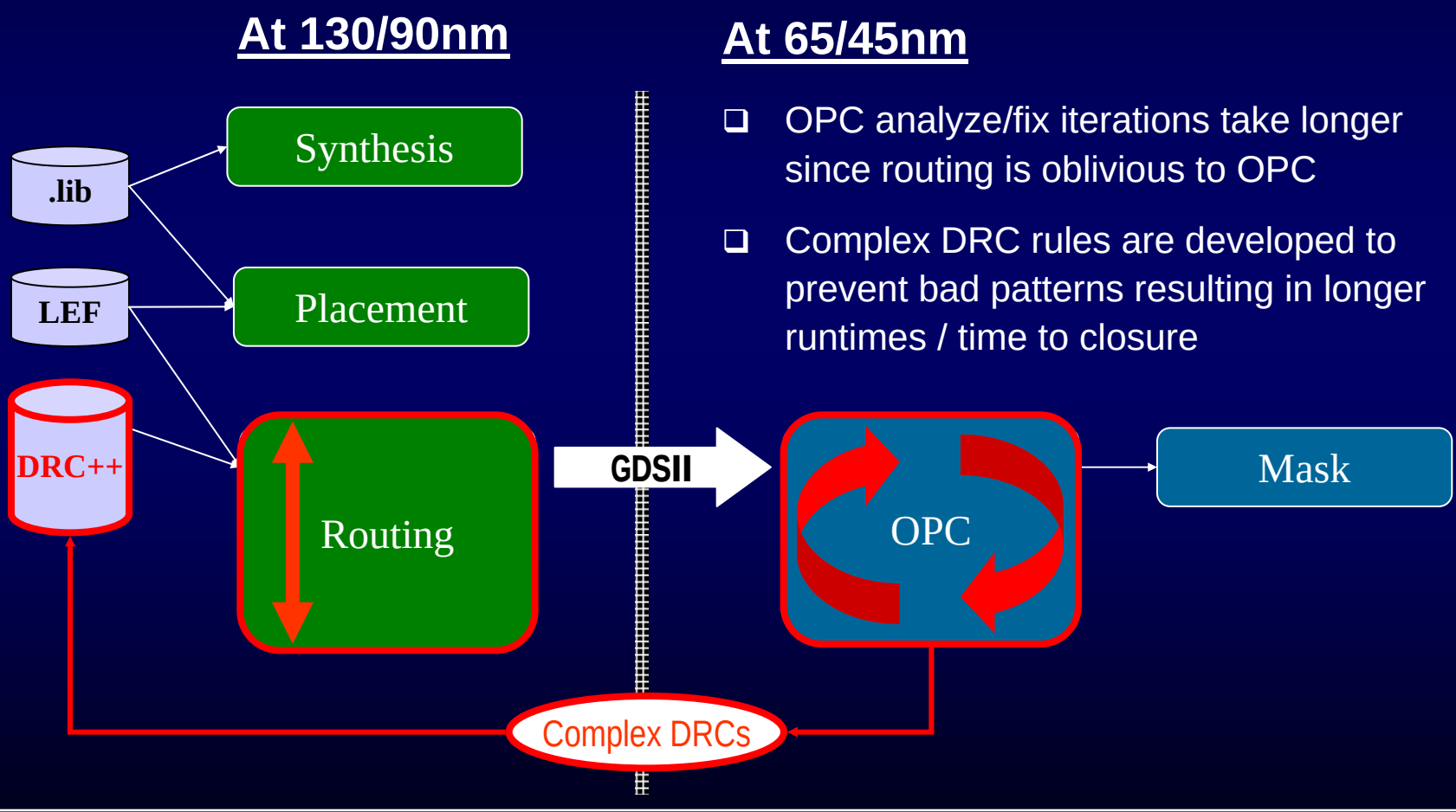
Routing / OPC interaction



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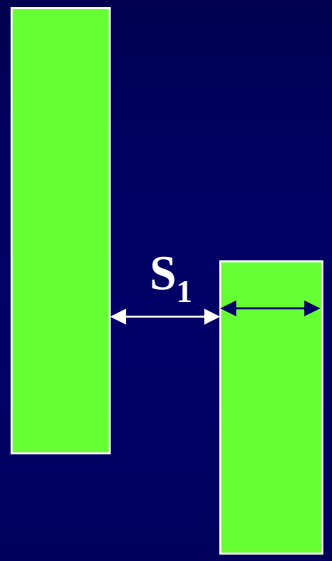
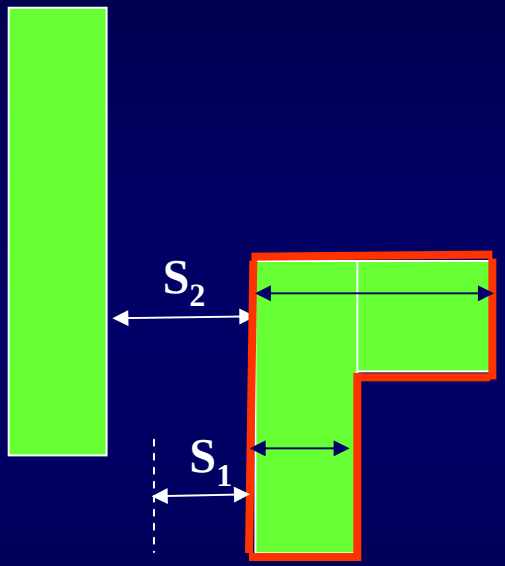
Impact on Routing Rules

- Complexity of Routing DRC Rules Increasing
  - Number of rules increasing from node to node
  - More rules are becoming dependent on ranges of variables like width, halo, parallel length
  - Increasing number of objects involved in a rule
  - Stringent requirements with each node
- Recommended or “Soft” Routing Rules increasing in number from node to node, usually for DFM
- Routing has to consider Timing and SI constraints
- Flexible routing flow and algorithms needed

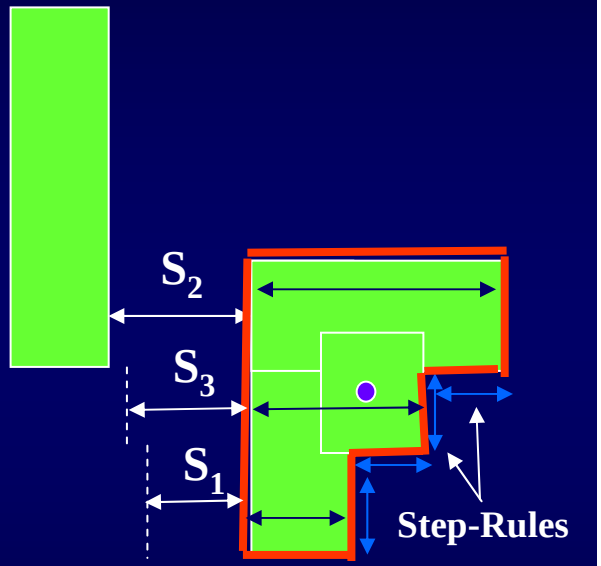
Migration to shape-based checks



Edge-to-Edge spacing check



Composite shape causes different spacing requirements



Adding a via causes more complicated DRCs to be triggered

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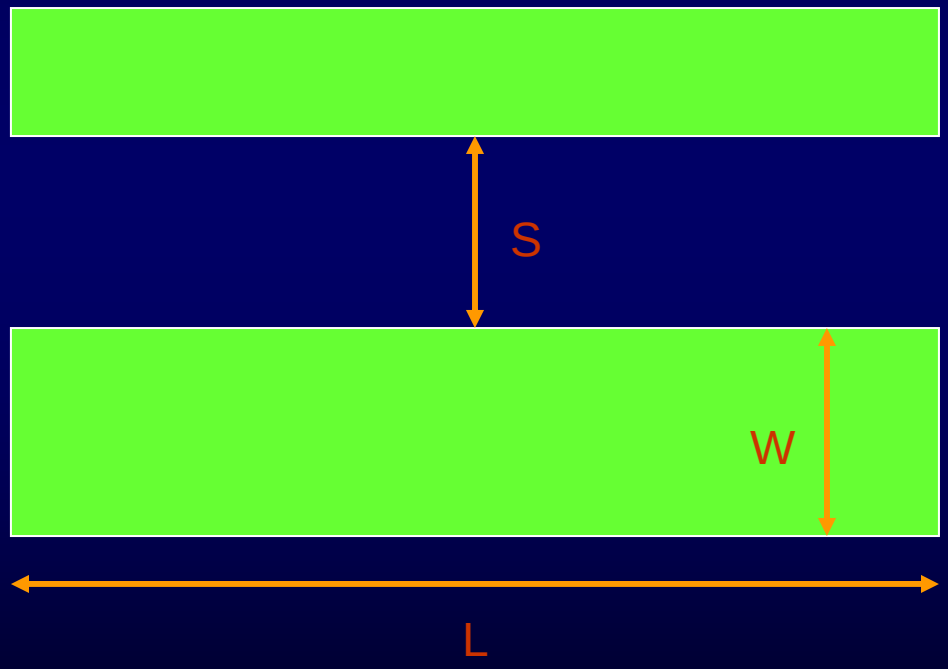
Spacing Rules

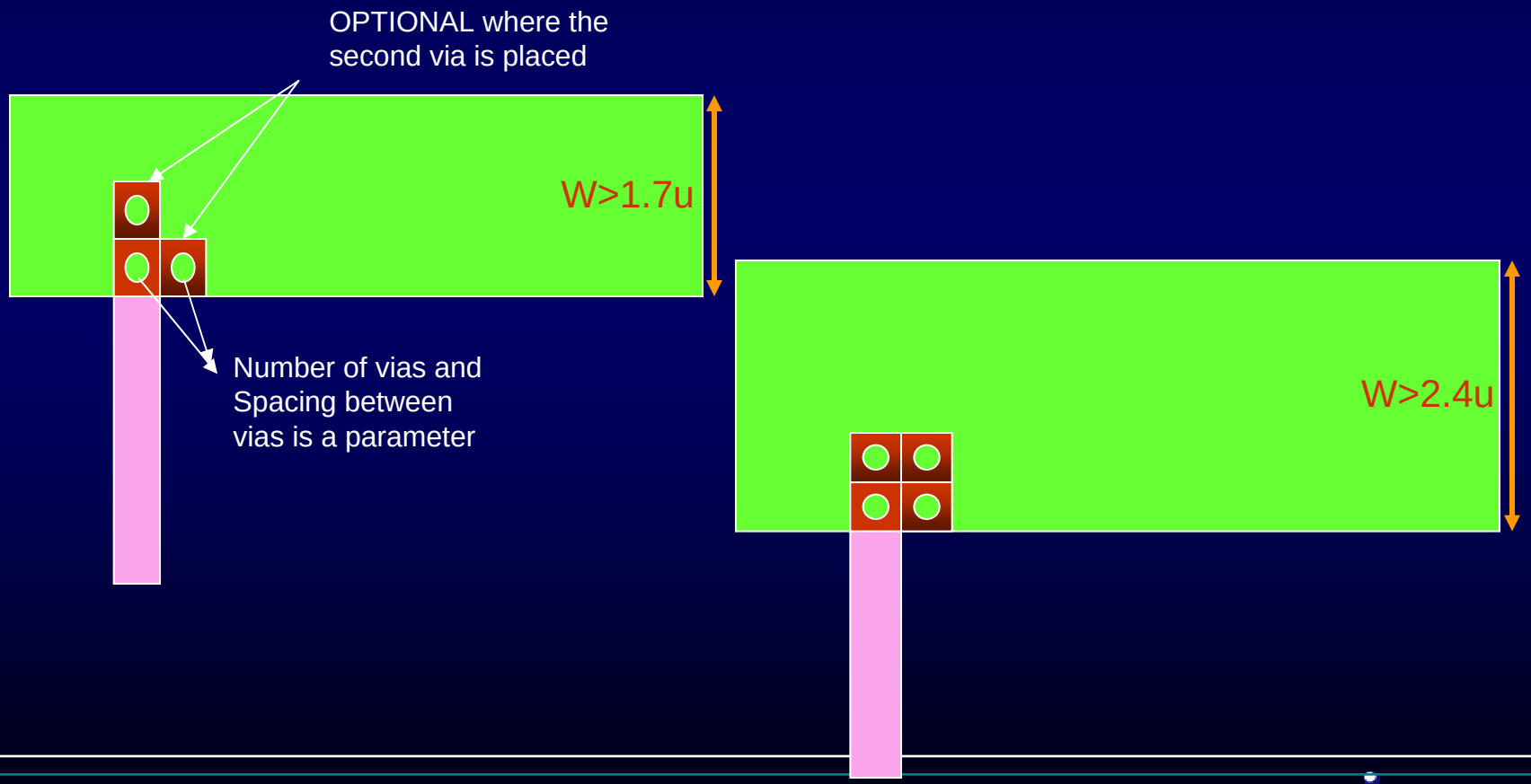
- Between different-nets and same-net objects.
- Objects can be port-shapes, wire segments, via metal, pre-routes



Parallel Length Overlap	Metal Width Range	Spacing
> L_1	> W_1	S_1
> L_2	> W_2	S_2
> L_3	> W_3	S_3

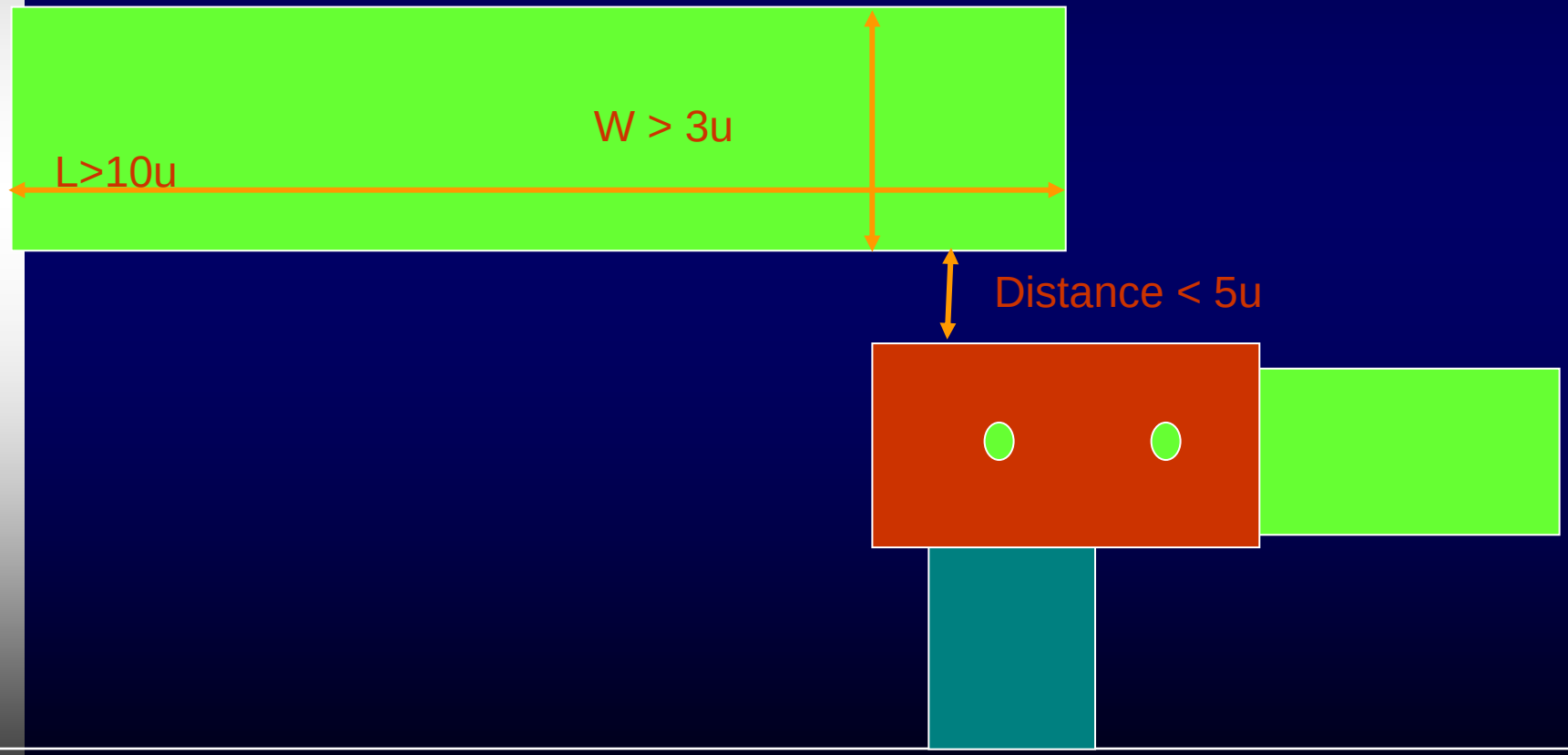
Cut Number Rule

- Number of vias and spacing between vias when used on “fat” metal

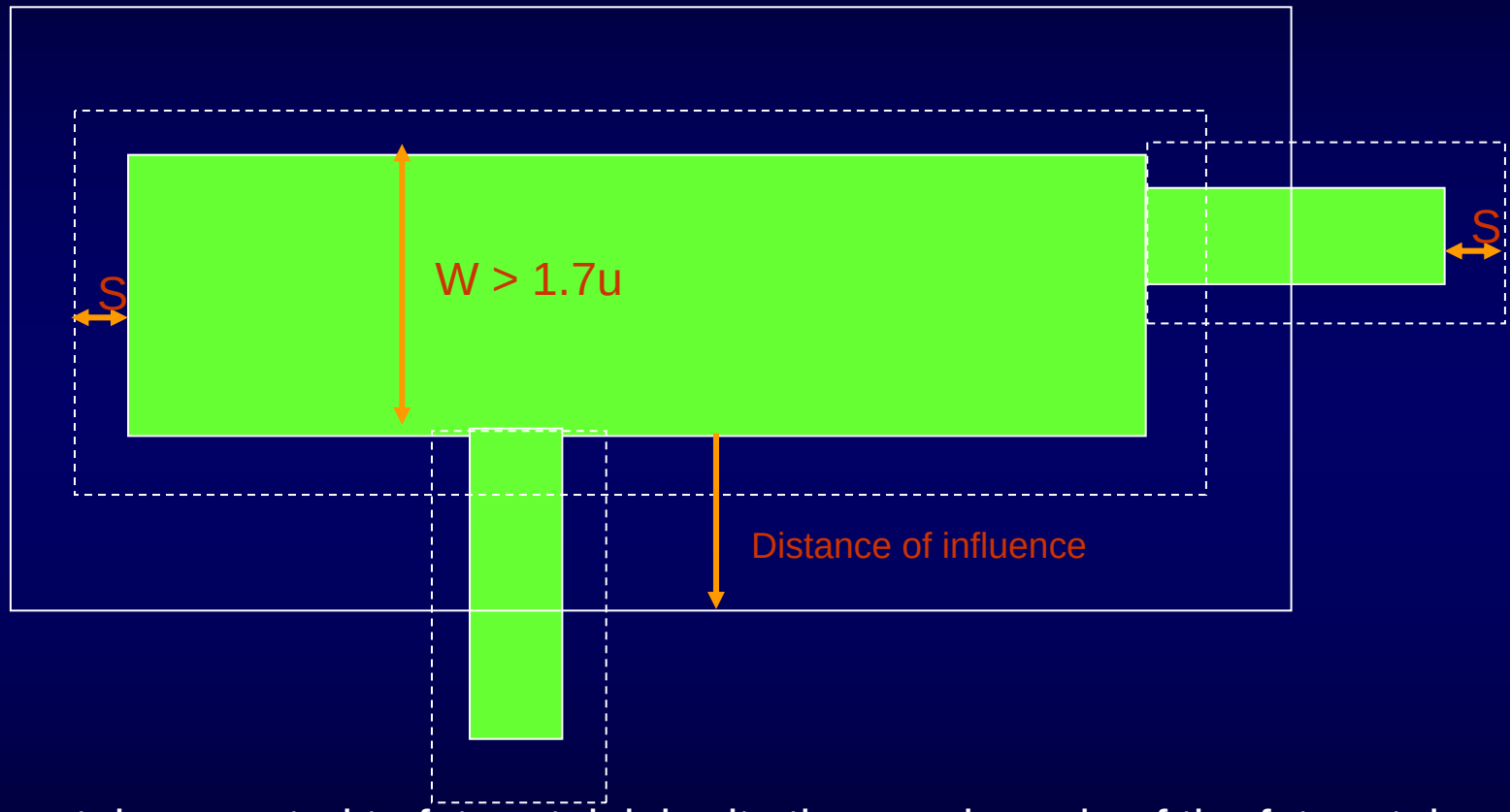


Complex Via Rules

- Use double via when turn is less than 5u away from a wide metal
- Parameters are length, width and distance from neighbor. Value is number of vias needed

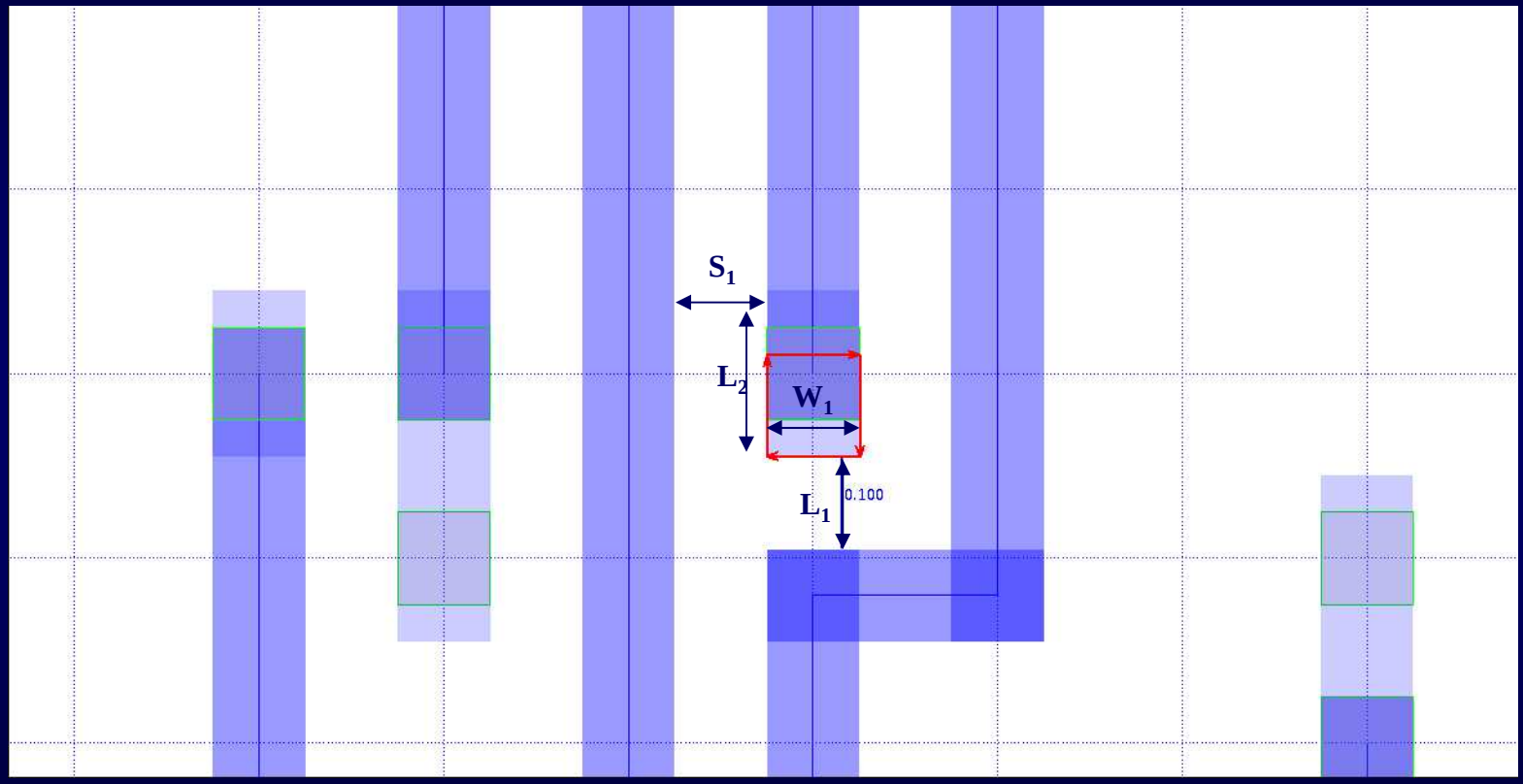


INFLUENCE Rule



All metal connected to fat-metal, inherits the spacing rule of the fat-metal. Also depends upon “distance of influence”. Beyond this distance use standard spacing rules

“Dense” End-of-line Rule for OPC Prevention



- Litho error prevention rule appears in 65nm/45nm nodes

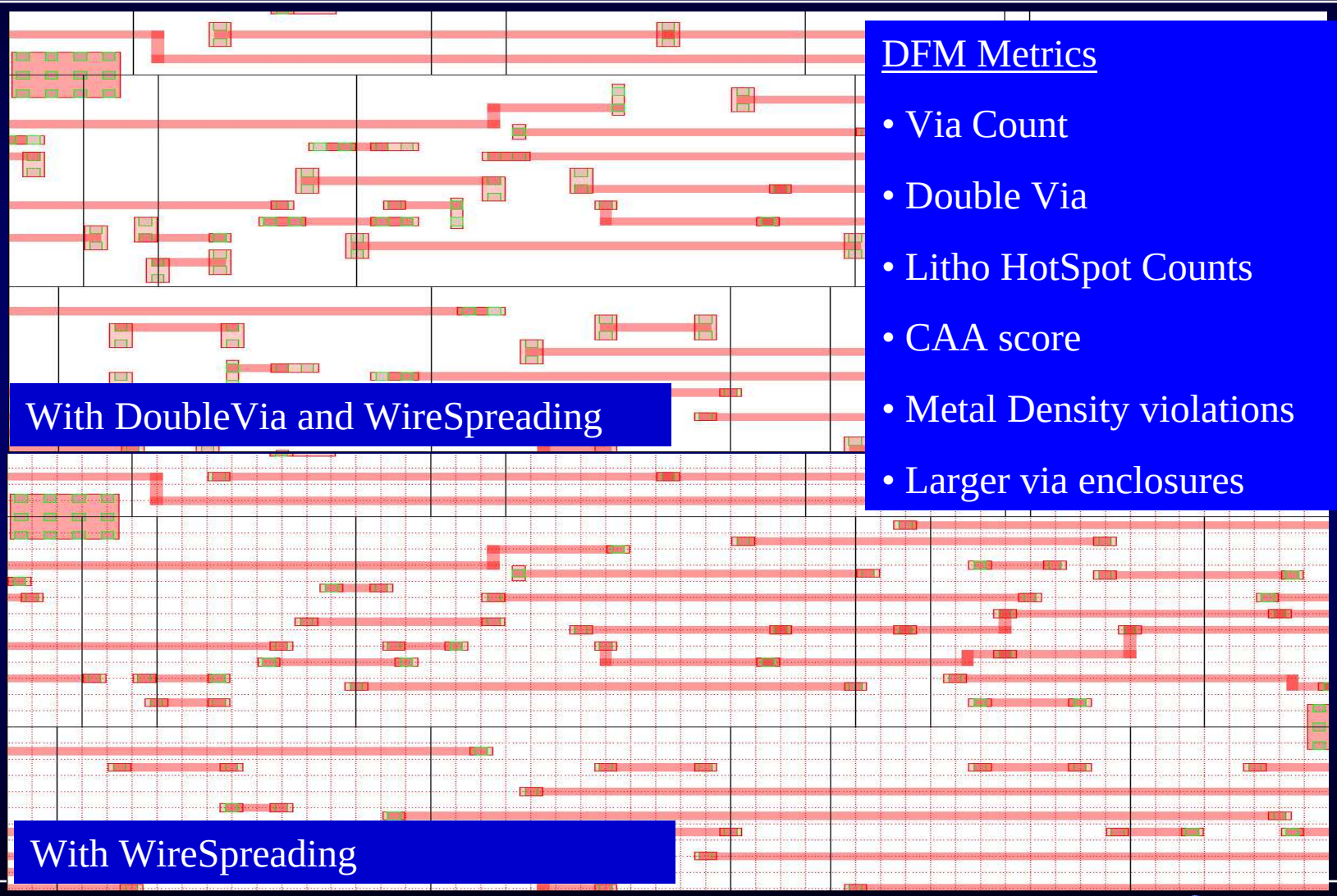
Growing DRC Complexity

DRC Rule	130nm	90nm	65nm	45nm
Width-based Spacing	1-2	2-3	3-5	7
Min-Area	1pitch	2pitch	3pitch	5pitch
Cut Number	n.a	1-2	4-5	5-6
Dense End-of-Line (OPC)	n.a	n.a	M1/M2	All layers
Min-step (OPC)	n.a	1	5	5

DFM Requirements

- Recommended Rules
  - Via Minimization
  - Double-via replacement levels
  - Metal Density Rules
  - Increase via enclosure where possible
- Litho Hot-spot avoidance, detection and repair
- Critical Area Analysis (CAA) and CAA-driven wire-spreading for random defect prevention

DFM Metrics



DFM Metrics

- Via Count
- Double Via
- Litho HotSpot Counts
- CAA score
- Metal Density violations
- Larger via enclosures

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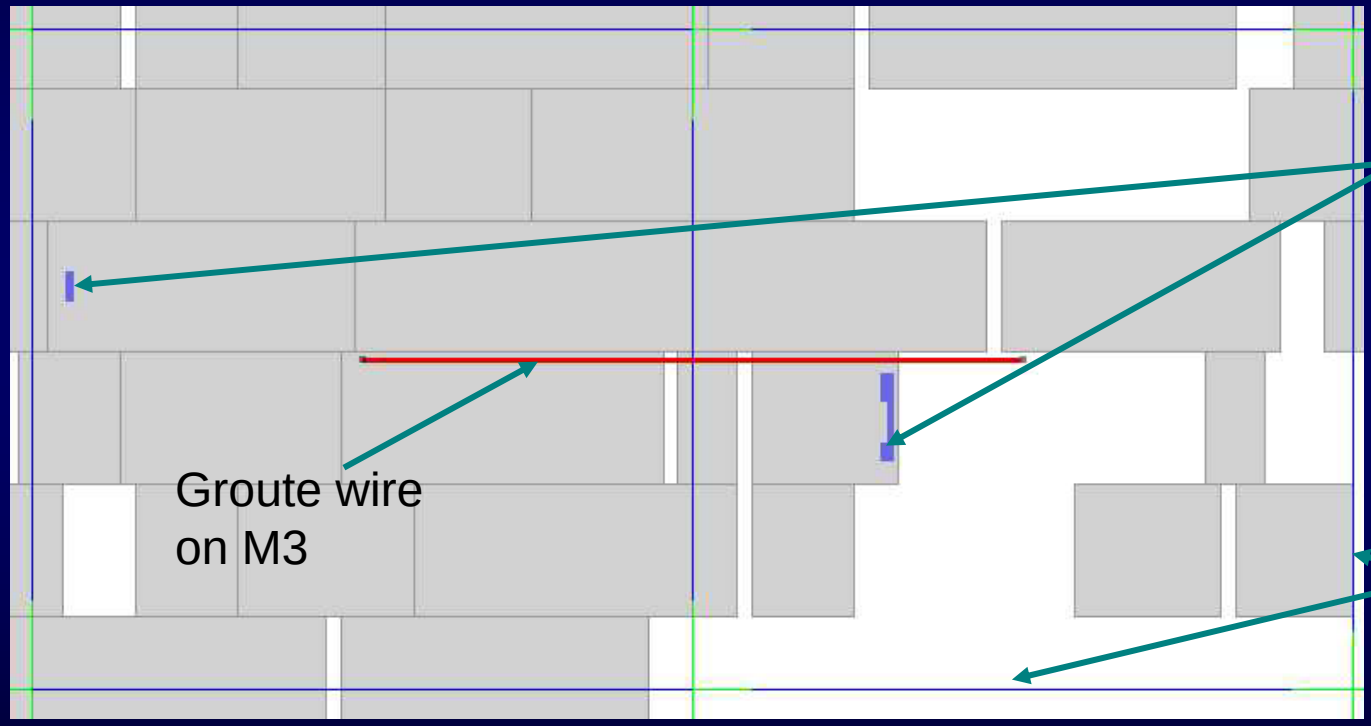
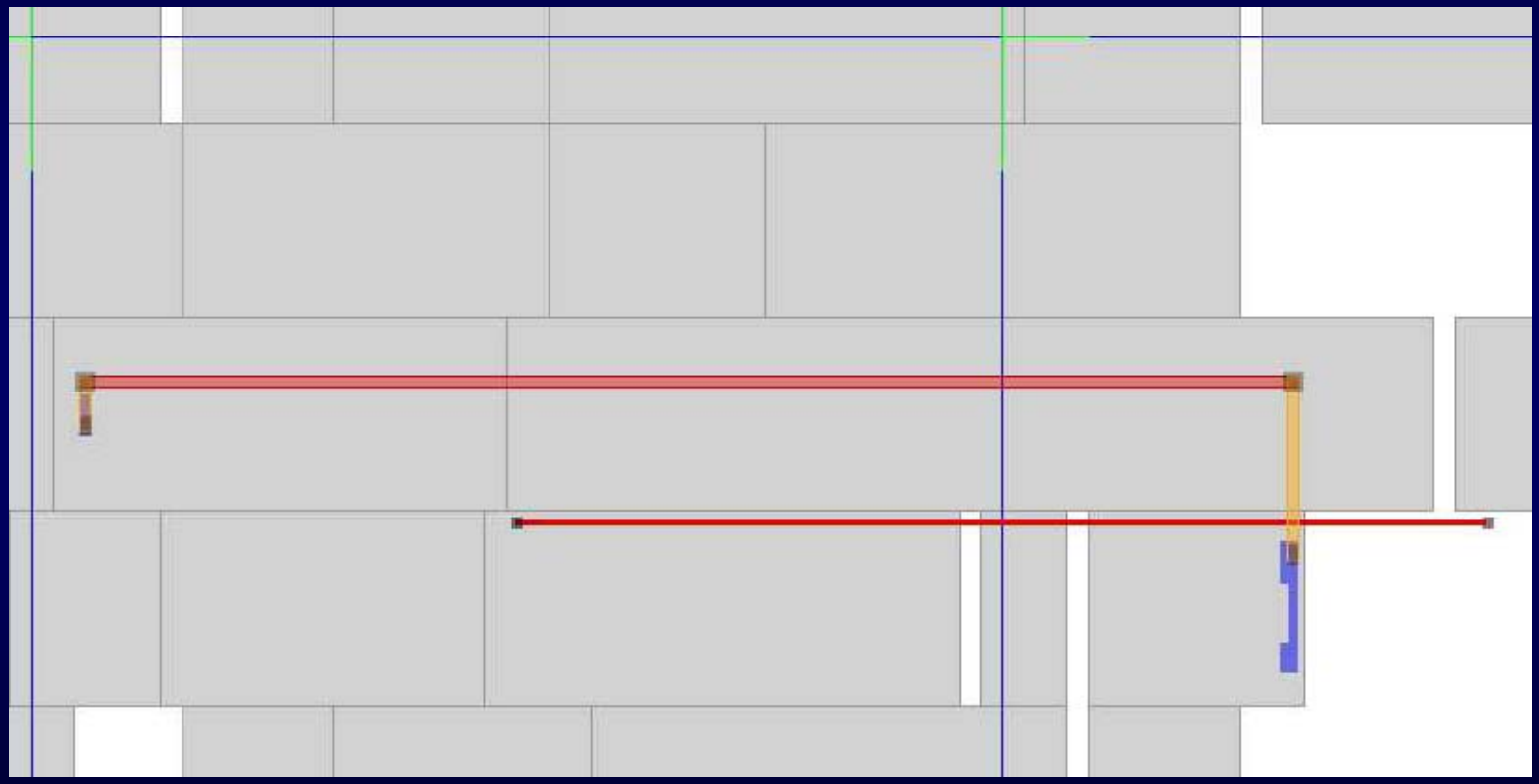
Introduction to Routing Flow

- 4 major steps
  - Global Routing
    - Computes total resource availability over the chip
    - Assigns initial topologies to nets
  - Track Routing
    - Takes Global Routes as “guides”
    - Assigns detailed wires on different layers to nets
  - Detail Routing
    - Starts with track routing and cleans up DRCs using local routing within small windows
    - Uses simplified model of complex DRCs for speed
  - Post-Processing
    - Cleans up remaining DRC errors with local re-routing in conjunction with DRC checker

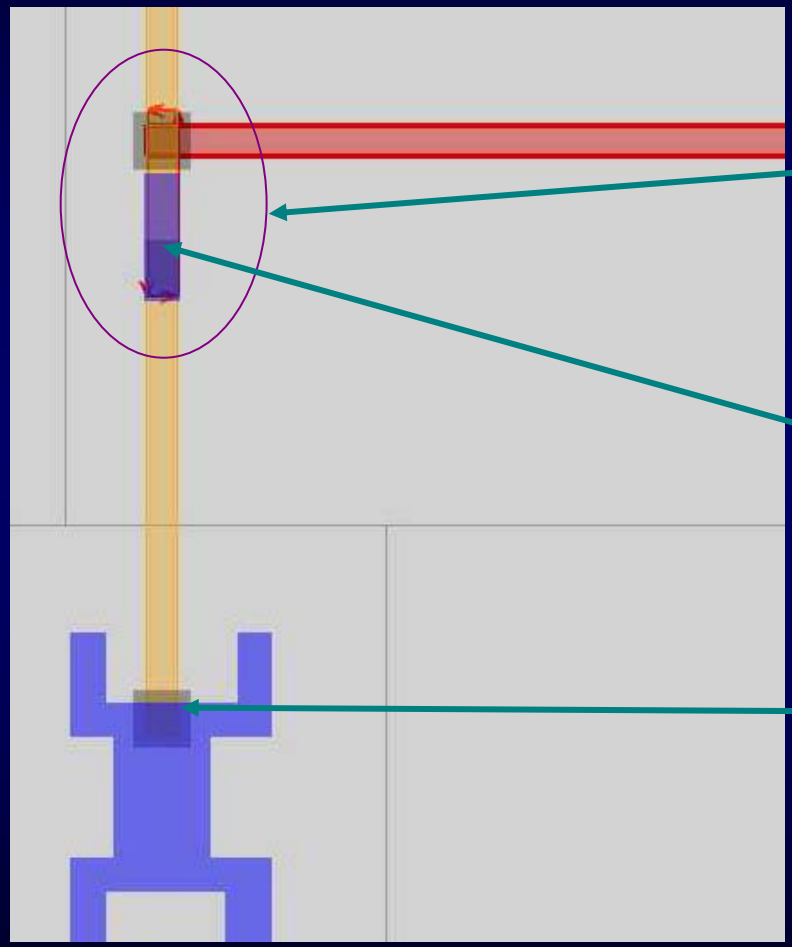
Routing Flow : Global Routing

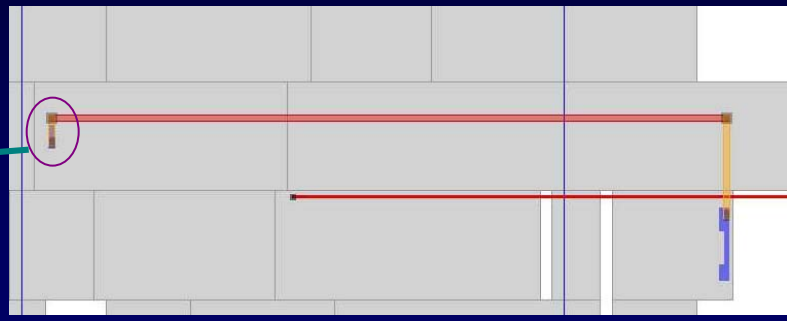


Routing Flow : Track Routing



Routing Flow : Track Routing

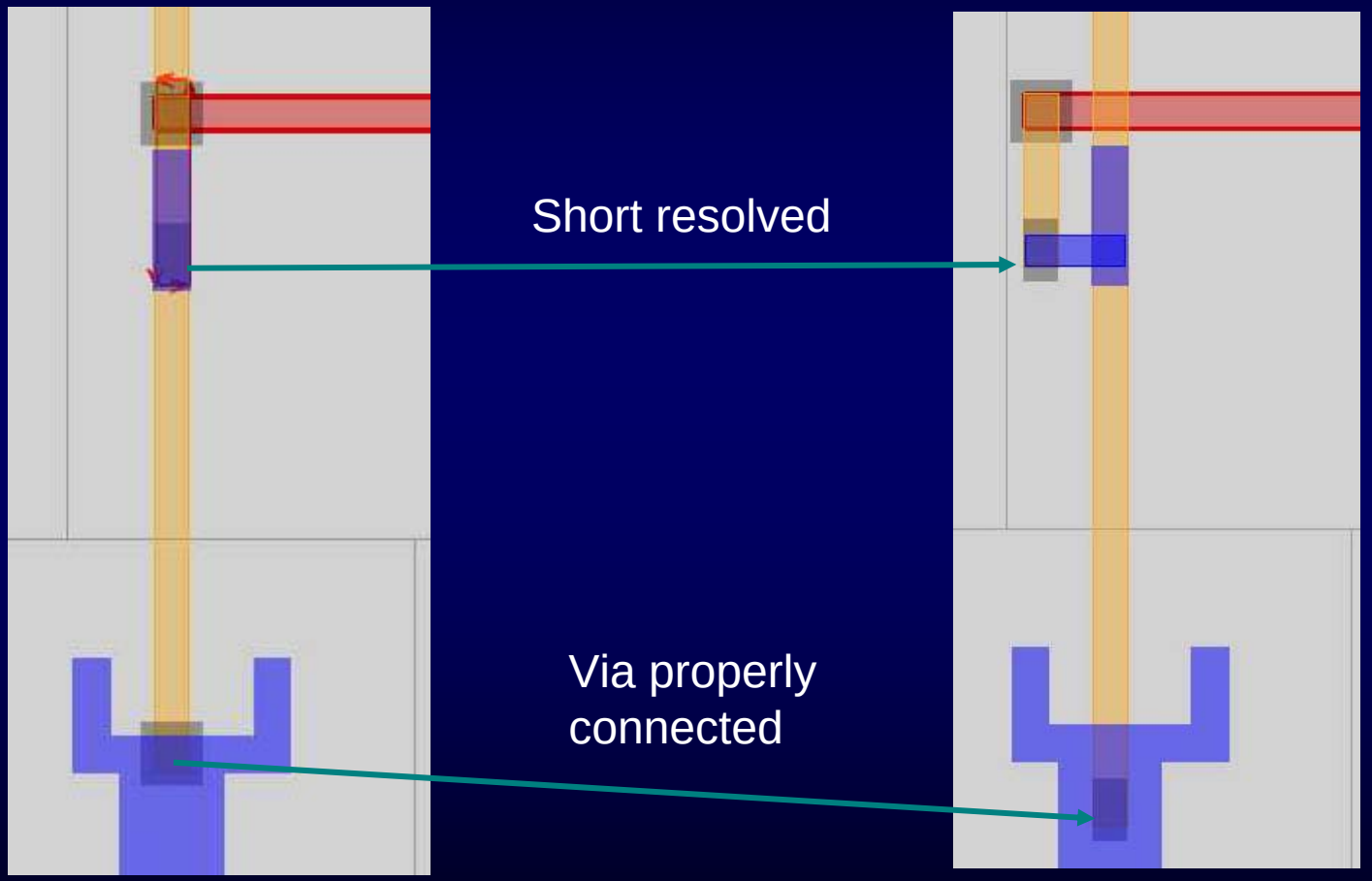




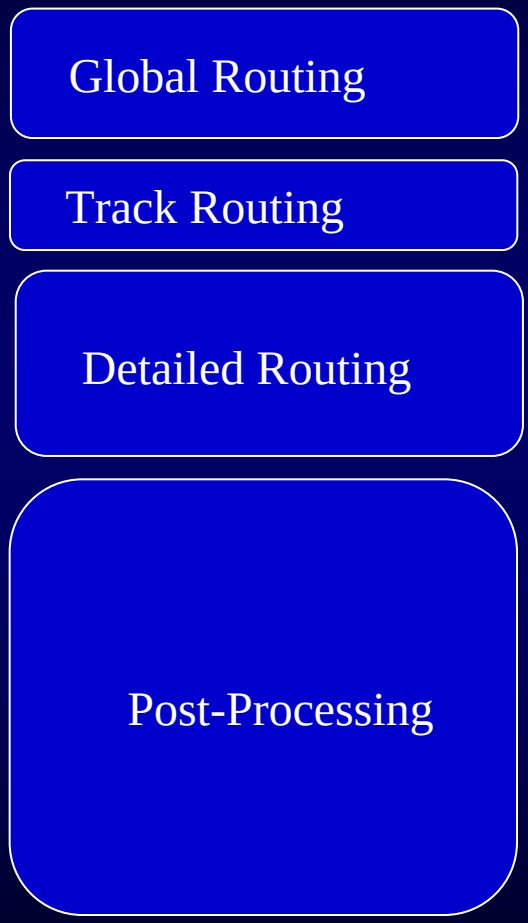
Target M1 pin is blocked by another net on M2 ➔ short …

Via is not clean

Routing Flow : Detail Routing

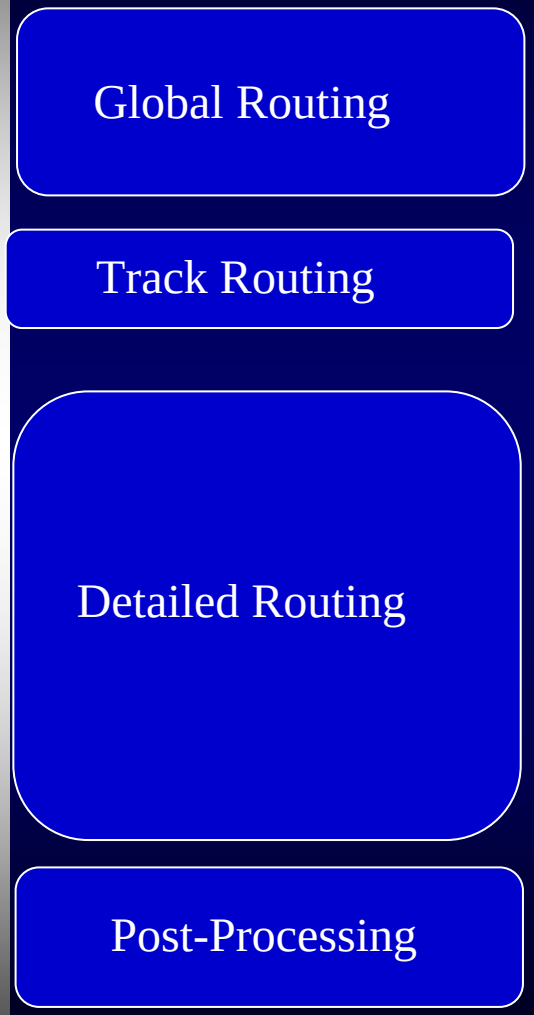


Routing Flows : Traditional Flow



- Simplified DRC models used for all stages except Post-processing
- Pros
  - Complex DRCs/DFM fixed only when all details are complete
  - Global/Track/Detailed steps are very fast due to simpler DRC model
- Cons
  - Final clean-up is unpredictable in runtime
  - Complex DRCs in congested areas may lead to extensive re-routing without success at the very end
  - DFM metrics may be poor for congested designs where routing density is high

Routing Flows : Proposed Flow



- Full DRC/DFM models used for all stages
- Pros
  - Complex DRCs/DFM is modeled throughout the flow rendering final step less critical
  - Shorter total routing runtime especially for congested designs
  - Complex DRCs in congested areas are handled much better since it is considered throughout the flow
  - DFM metrics are considered throughout the flow
- Cons
  - Routing algorithms becomes more complex because of introduction of complex DRCs in maze search
  - Need strategies to gracefully scale-back on Recommended DFM Rules in case of congested designs

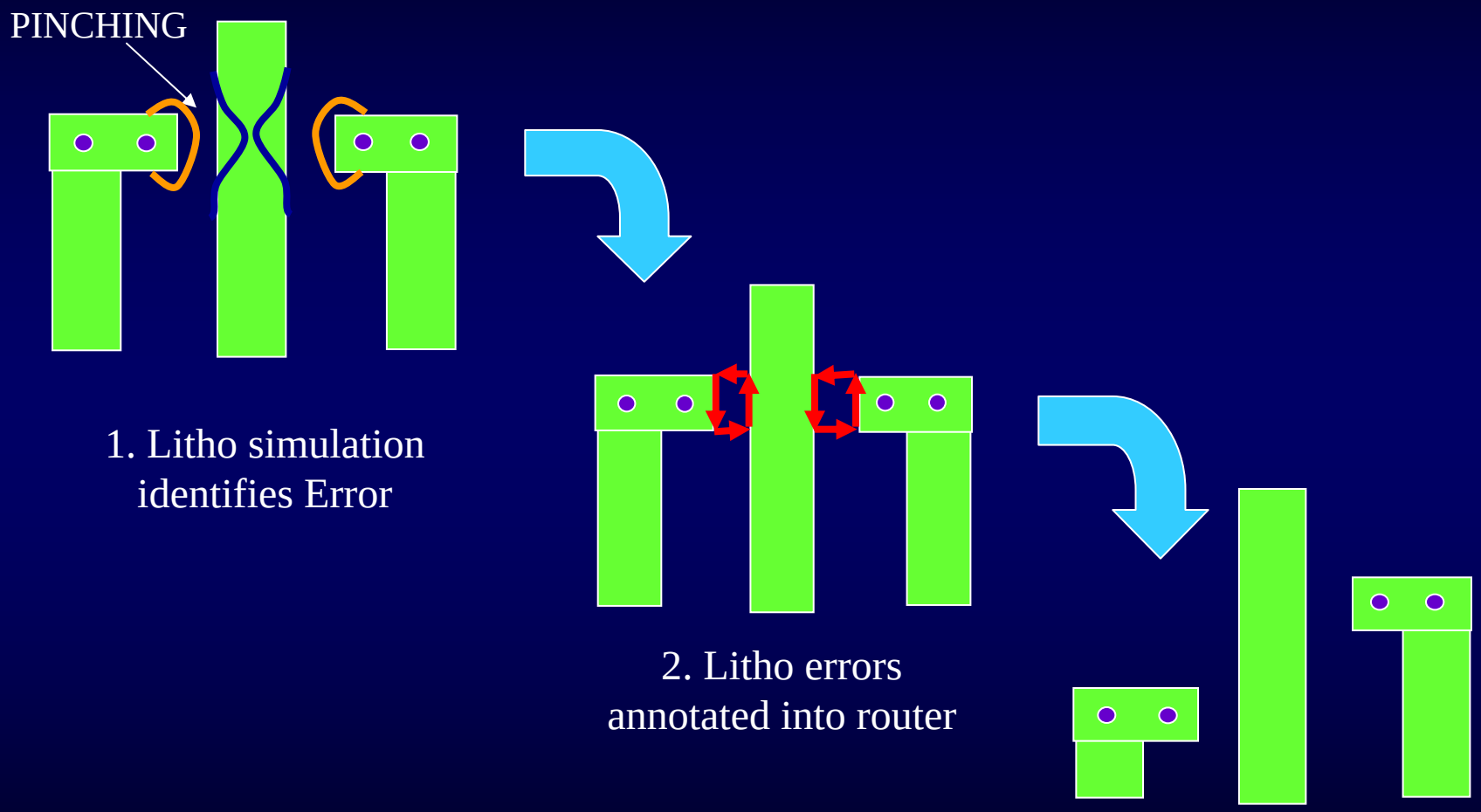
Impact of complex DRCs on routing

- Testcase : High performance core, 65nm, 260K nets

Traditional | Proposed

Metric	Simple	+MinStep	+Cut Number	+ Fat Space	+ Cut Space	+End Of Line
Runtime	66	66	76	81	82	84
WL	10.45	10.45	10.49	10.51	10.48	10.48
Via	2.35M	2.35M	2.38M	2.41M	2.42M	2.42M
Incoming DRCs	73K	73K	41K	5.7K	4K	0
Final Cleanup	105	105	96	24	19	0
Total time	171	171	172	105	101	84

Litho Hot-spot Fixing



Summary

- Timing Variation, Litho Variation and Capacity have to be addressed at 65nm/45nm
- Modeling timing variation with concurrent multi-mode/multi-corner analysis reduces the need for design margins in physical design
- At 65nm/45nm, there is a significant increase in routing complexity due to complex DRCs and DFM rules
- A flexible routing flow and new routing algorithms are needed to produce good results