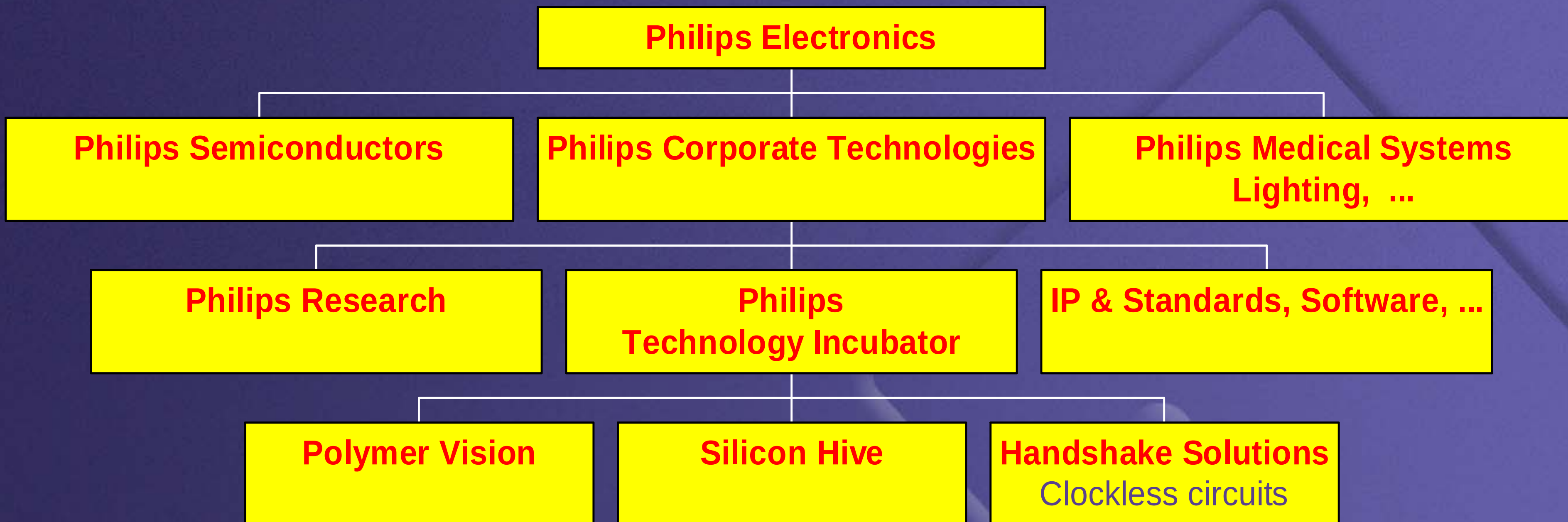
Clockless IC Design using Handshake Technology

Ad Peeters

Handshake Solutions



Handshake Solutions is a line of business of Philips Electronics that License Handshake Technology to the semiconductor and electronics industry in the form of design tools, design support and services, and IP blocks

Handshake Technology

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A rigorous design methodology and associated toolset for clockless, self-timed circuits

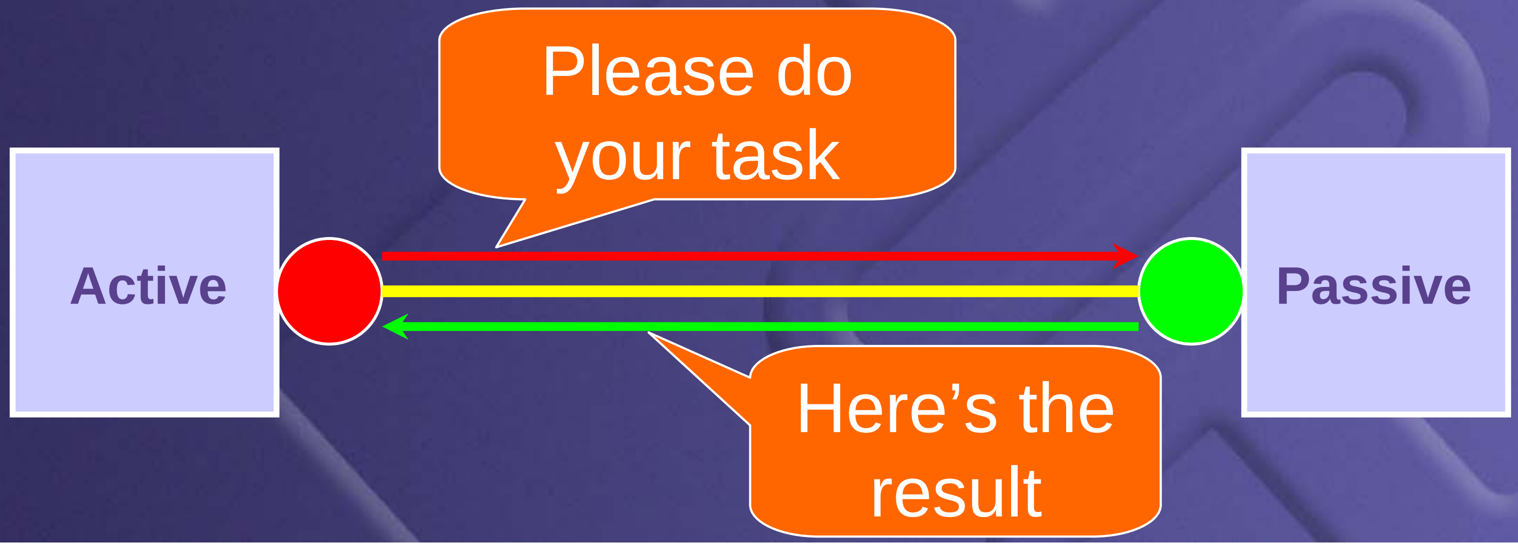
The familiar global clock used in traditional chips is replaced with handshake signaling

HT Customer:

“Handshake Technology isn’t really asynchronous design – it’s much more structured, robust and easy to use.”

Handshake Technology

- Handshakes are between active and passive partner
- Communication is by means of alternating request (from active to passive) and acknowledge (from passive to active) signals
- Request and acknowledge may contain (encode) data
- Handshakes provide distributed control and activation



Handshake Technology
Some implementation choices

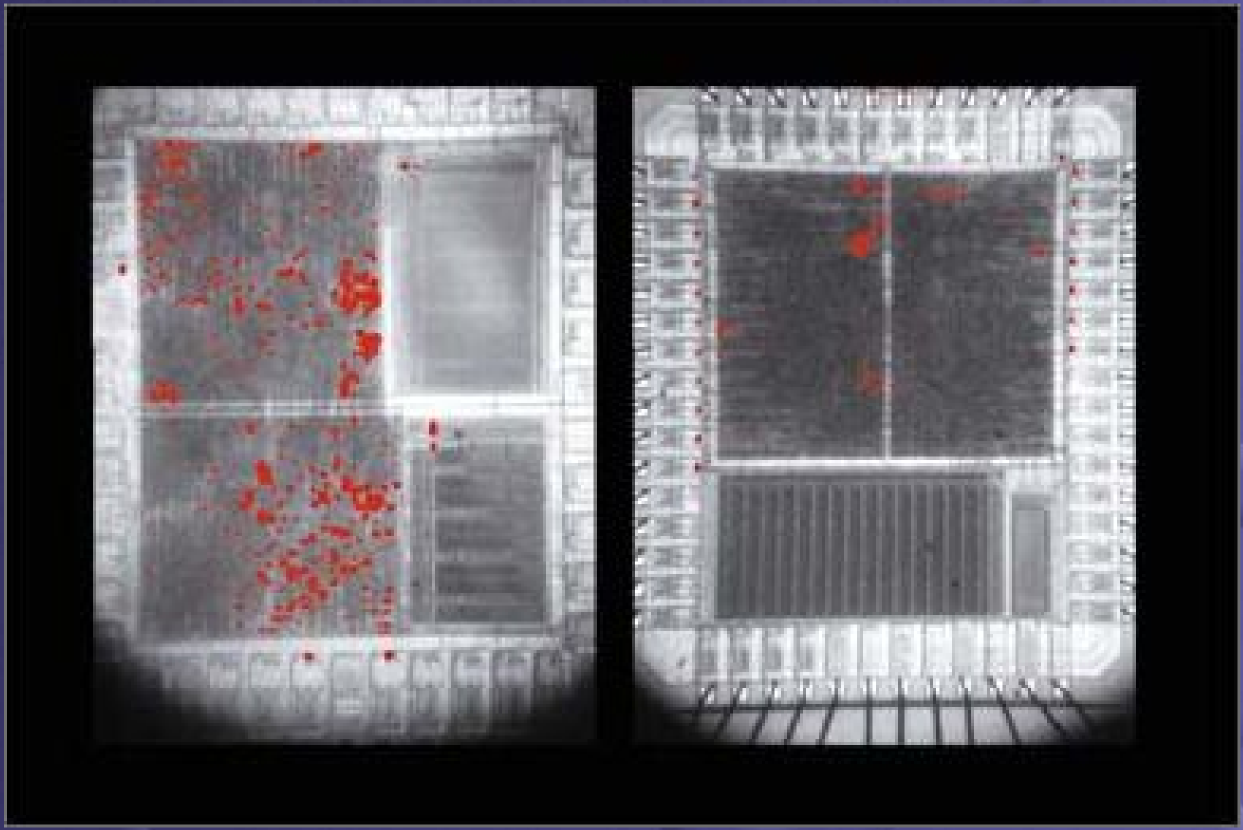
- Number of wires for control
  - 1ω (req and ack on single wire, a.k.a. single-track, tristate)
  - 2ω (separate wire for req and ack)
- Number of phases in handshake protocol
  - 2φ (non return-to-zero, NRZ)
  - 4φ (return-to-zero, RTZ)
  - τ (synchronous, sampling of req and ack wire)
- Encoding of data
  - double rail (2 wires per bit)
  - single rail (1 wire per bit plus data-valid)
  - M-out-of-N (1-out-of-4 is interesting)

Handshake Technology
Key features

- Ultra low energy consumption
- Zero standby power
- Immediate response to exceptions
- Low electromagnetic emissions
- Low current peaks
- Robustness against variations in environmental conditions
- Increased design productivity through behavioral design entry

Handshake Technology
Low power

‘Circuit is only active *when* and *where* needed’

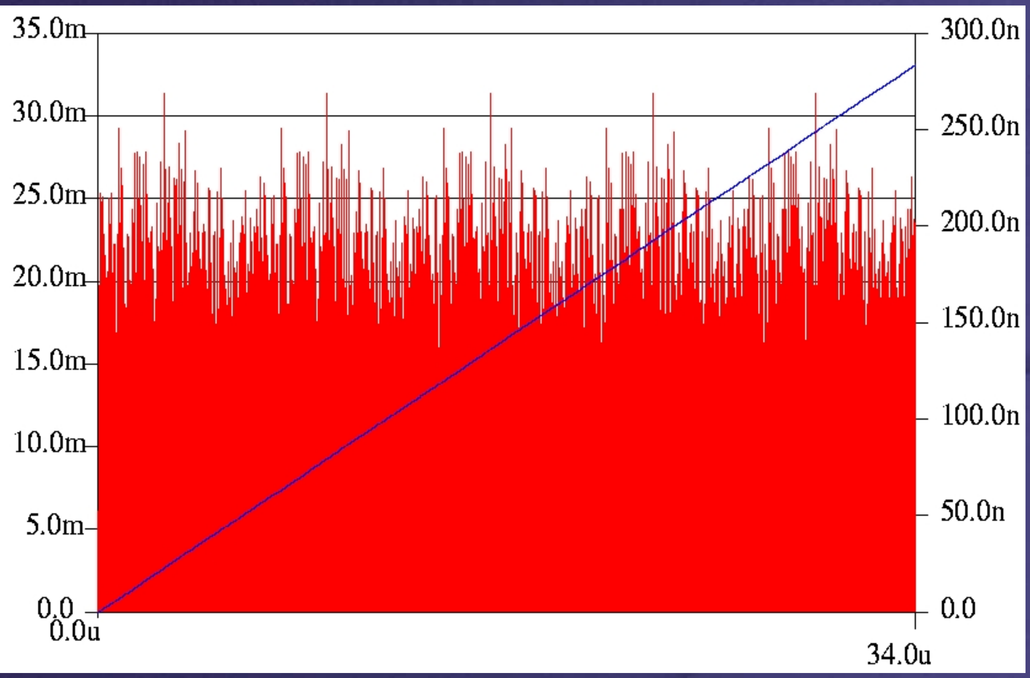


Clocked 80c51 Handshake 80c51

Handshake Technology
Low current peaks (and power)

Current (A)

Cumulative Energy (J)

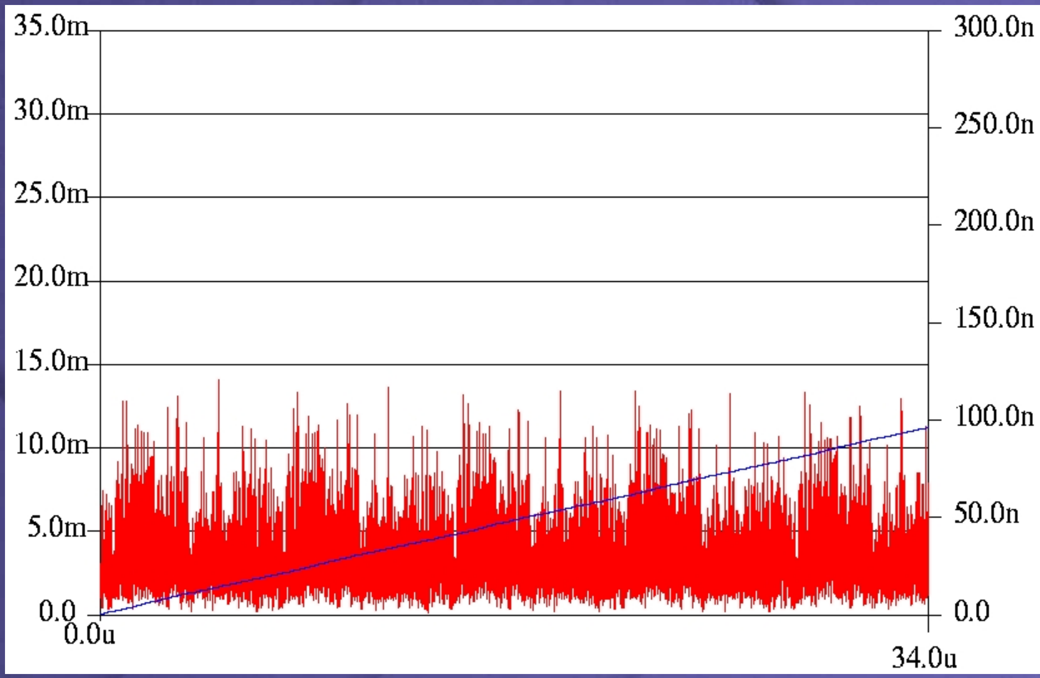


Time (s)

Clock-gated ARM968E-S processor

Current (A)

Cumulative Energy (J)

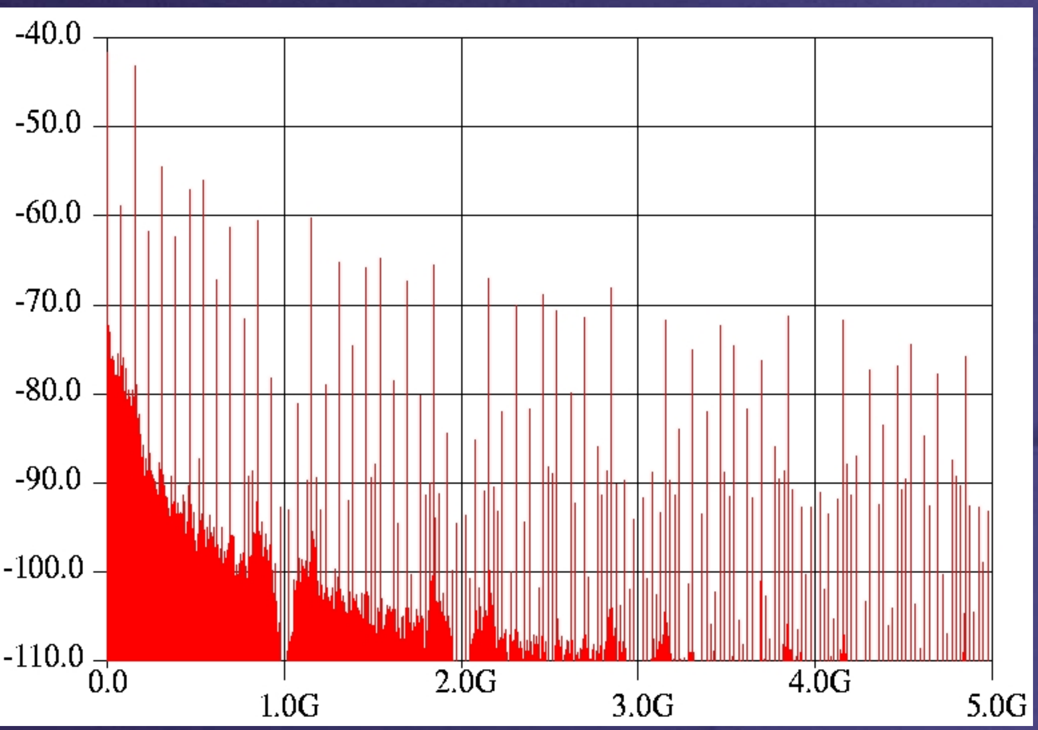


Time (s)

Handshake ARM996HS processor

Handshake Technology
Low electromagnetic emissions

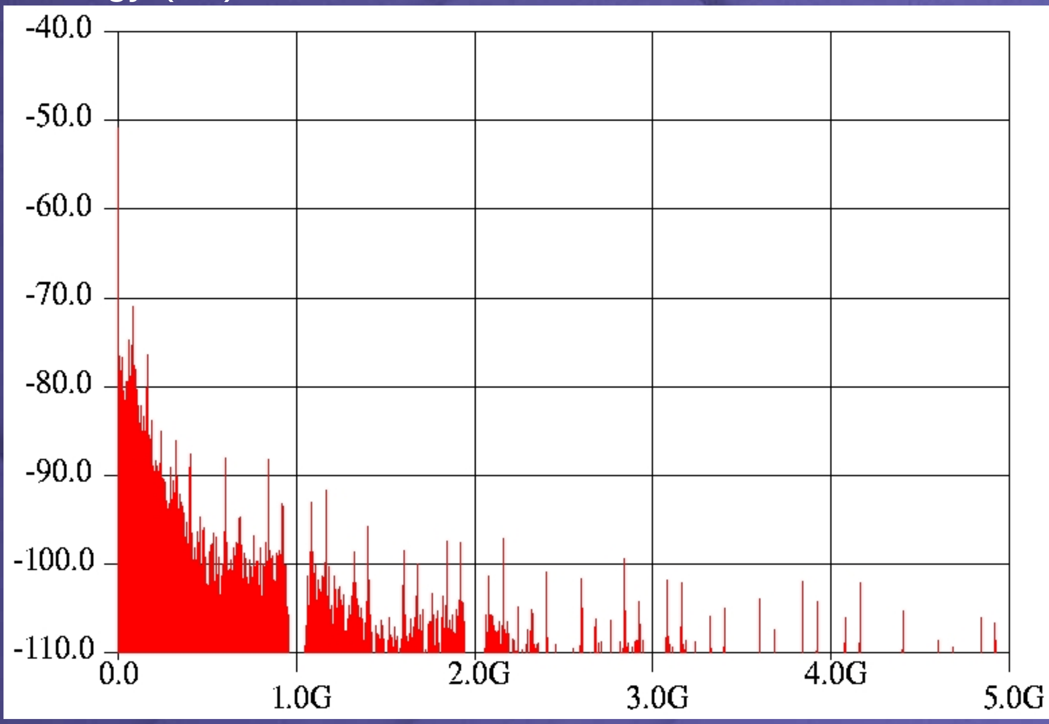
Energy (dB)



Frequency (Hz)

Clock-gated ARM968E-S processor

Energy (dB)



Frequency (Hz)

Handshake ARM996HS processor

Handshake Technology
In the market

100M+ Handshake Technology based ICs sold

25+ market-tested products

Proven by many years of use in design projects

Applications in:
• Smartcards
• Automotive
• Wireless connectivity

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Handshake Technology
In the market

HANDSHAKE SOLUTIONS

Handshake Technology

In the market

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Handshake Technology
Design flow

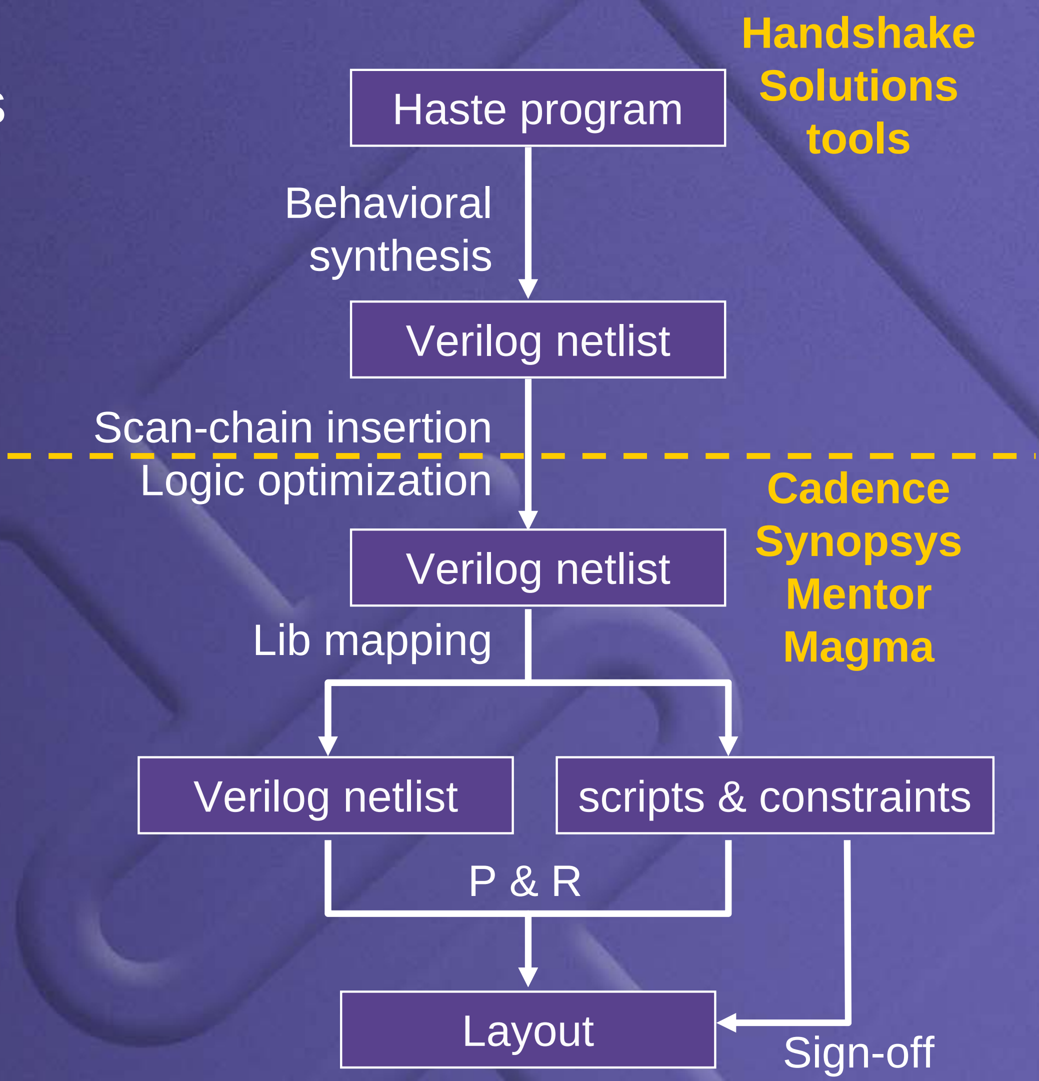
- HT flow is *complementary to* and *compatible with* standard design flows
- Frontend to standard third-party EDA flow
- High-level design entry (Haste)
- Standard-cell hand-over

Handshake Technology Design Flow → Standard EDA flow

Cadence
Magma
Mentor
Synopsys
Synplicity

Design Flow
Key features

- Based on standard-cell libraries
- No dedicated cells needed
- Supports FPGA prototyping
- Supports scan-test-based DfT
- Interfaces to third-party EDA tools for:
  - Logic optimization
  - Timing verification
  - Test-pattern generation
  - Placement and routing
- Supports integration with synchronous blocks and systems



Design Flow
Challenge nr 1: Correctness

- Most tools are not designed with asynchronous circuits in mind
- Correct operation of an asynchronous circuit may depend on
  - Relative timing assumption (control not faster than datapath)
  - Completion detection
  - Analog properties (logic threshold in arbiters)
- Many of these properties cannot be expressed in standard constraints
- Correct handling of asynchronous circuits requires a combination of constraints and scripting

Design Flow
Challenge nr 2: Optimization

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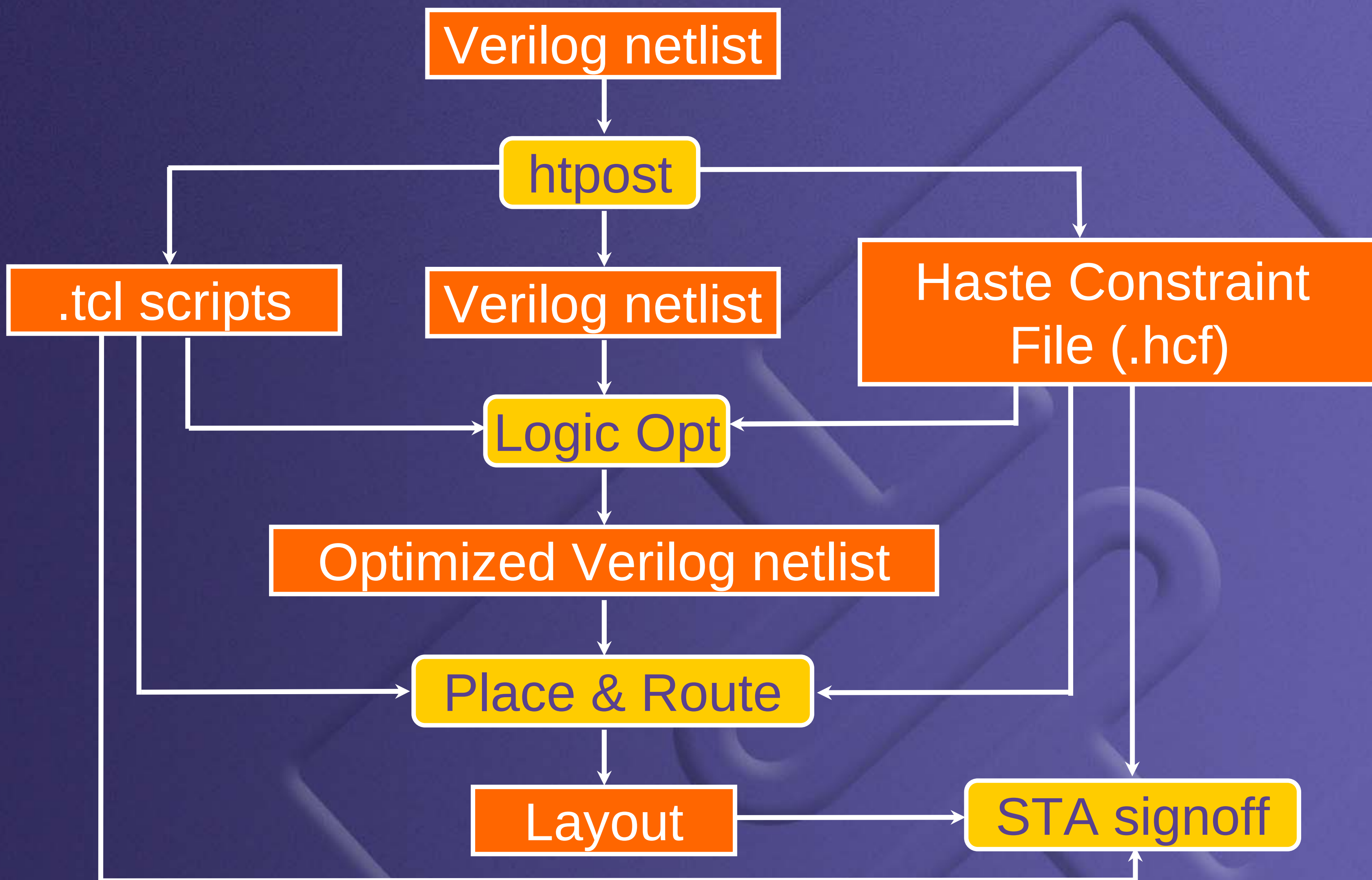
- ‘Synchronous’ tools are very good in optimizing circuits e.g. for speed or power
- However, they will do only what you ask for
- No goal, no glory
- Specification of an asynchronous circuit partly timeless
- Realistic and fast targets for datapath blocks need to be ‘invented’ or supplied by designer
- Optimal handling of asynchronous circuits requires a combination of constraints and scripting

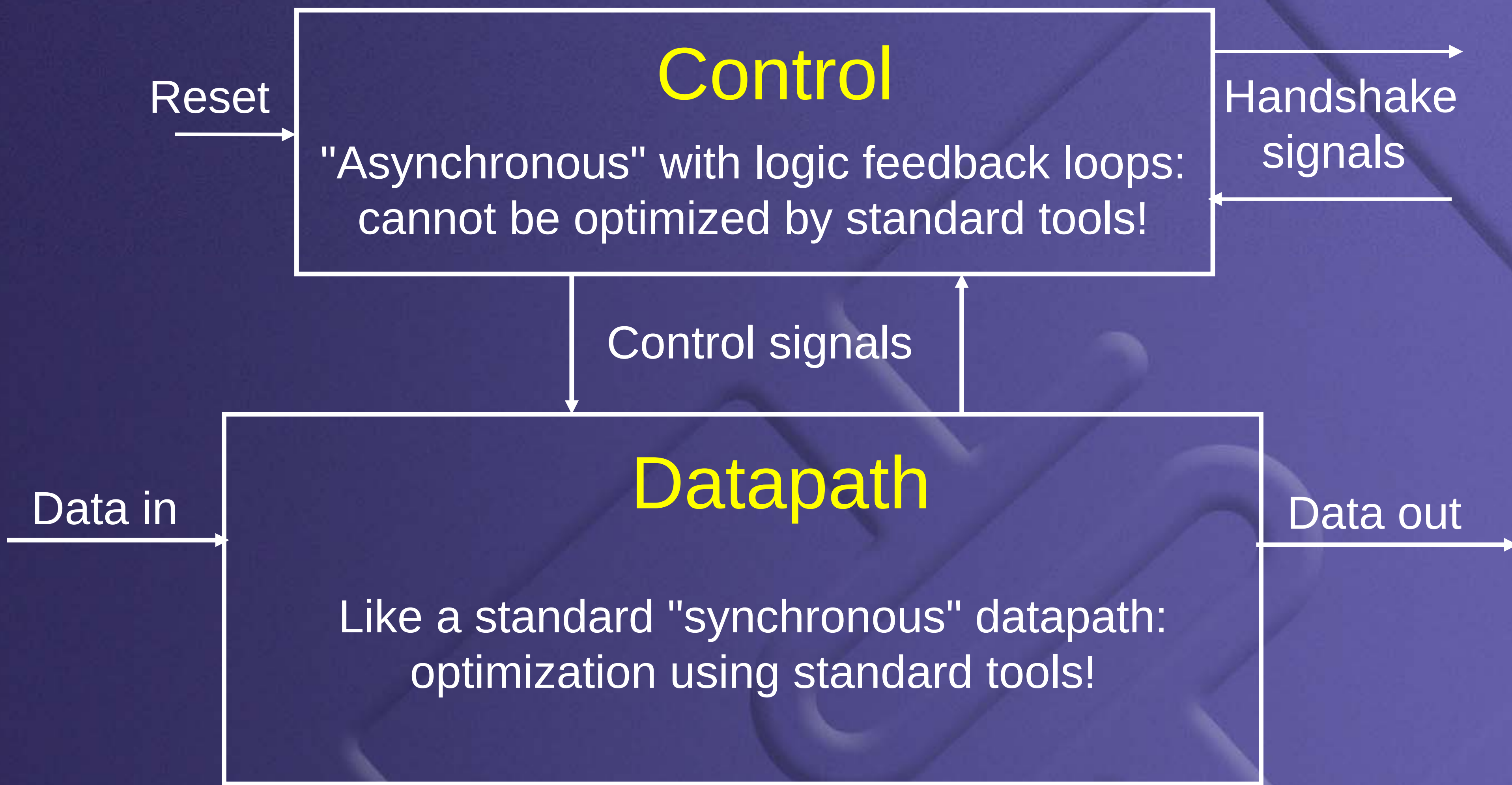
Design Flow
Haste Constraint File

- Unfortunately, SDC format not suited for our constraints
  - Especially relative timing cannot be expressed in SDC
- Solution: Haste Constraint File
  - Generic enough to denote all constraints
  - Easy (computer) readable
  - Future proof (upward compatible)
- We address both correctness and optimization constraints
  - Control-datapath matching for relative timing constraints
  - Breaking of combinational loops for timing analysis
  - Local clock domains for clock-tree synthesis
  - High-fanout nets (reset, test, small clock domains)
- We provide .tcl parsers and procedures for several third-party EDA tools

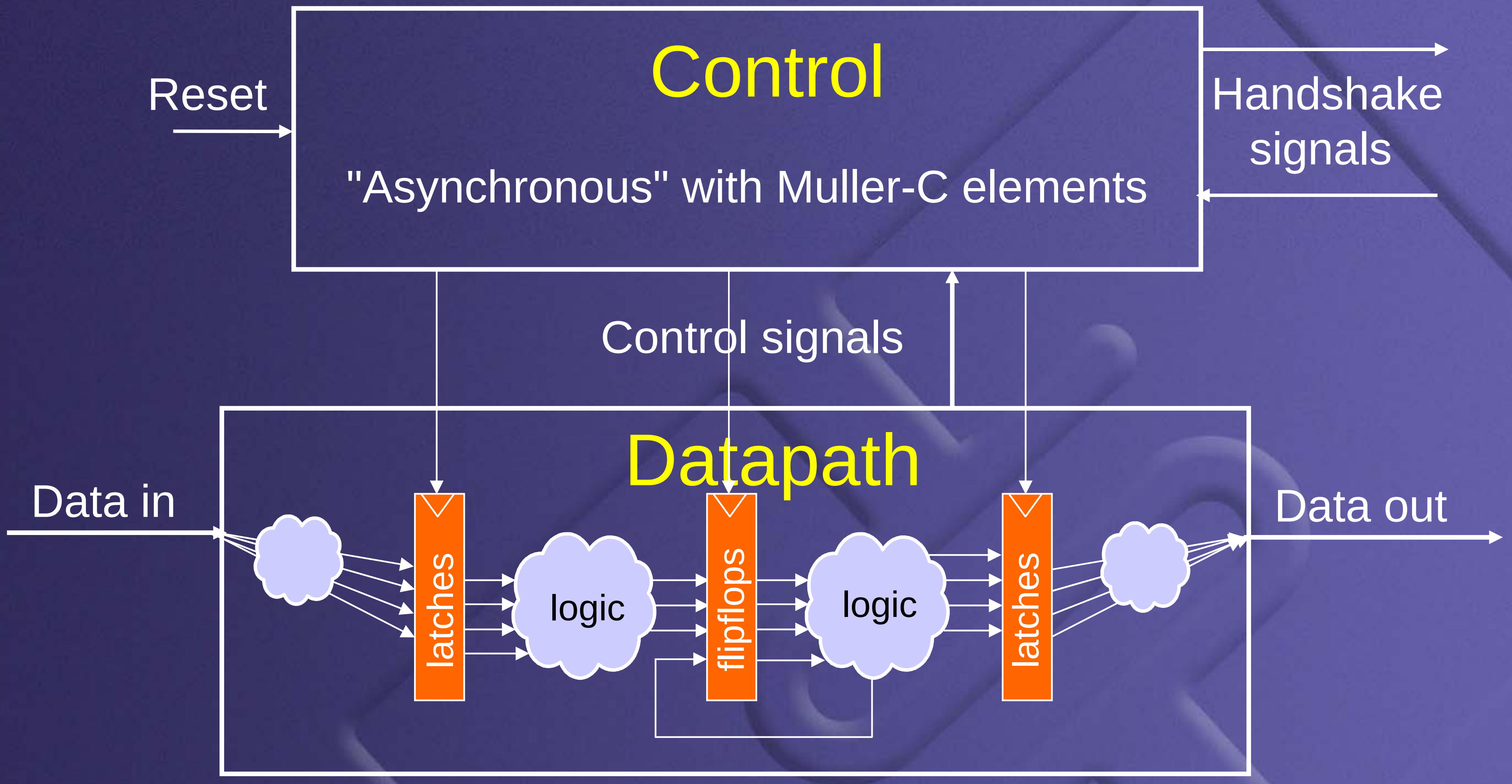
Design Flow
Correctness and Optimization



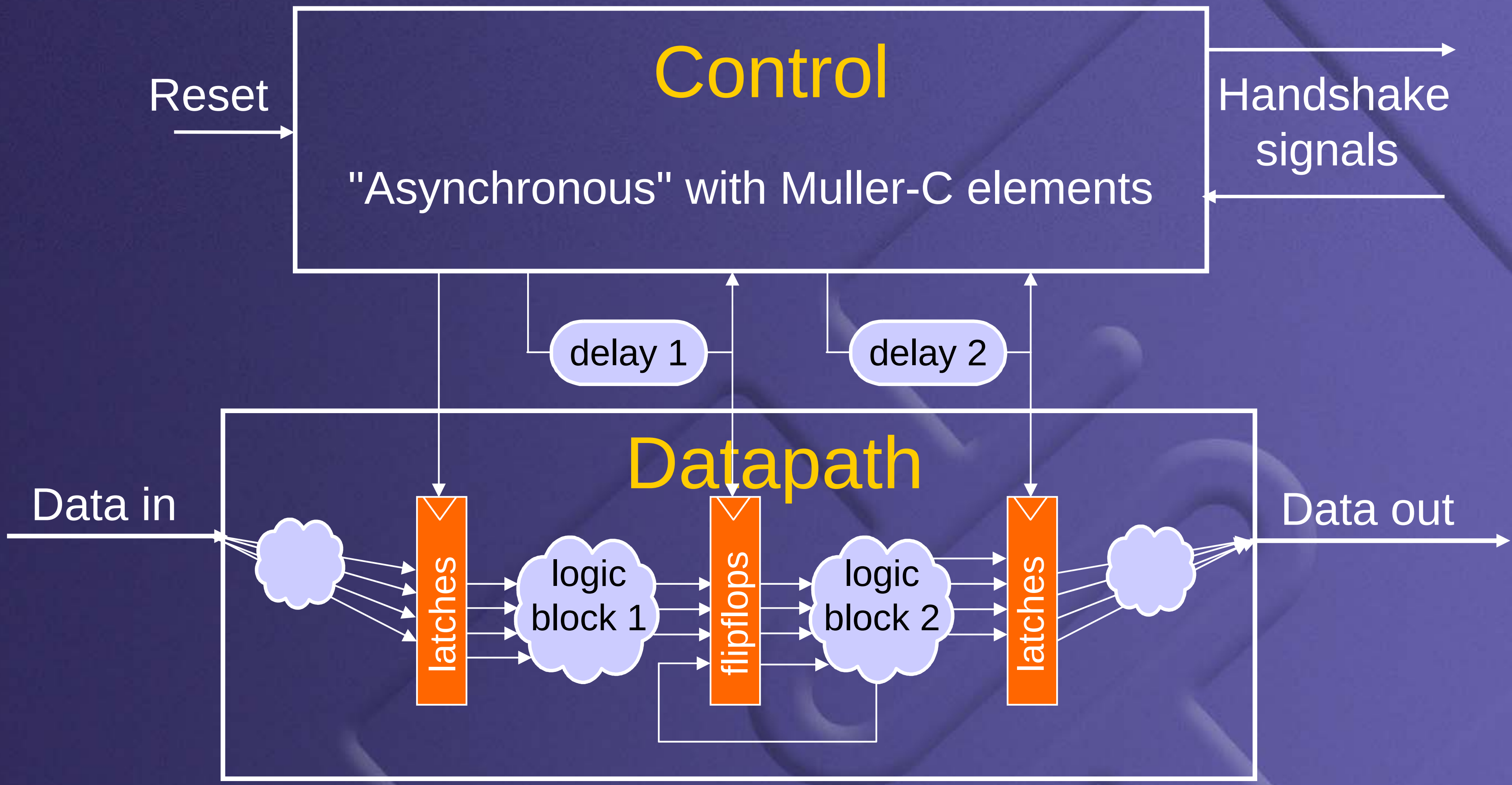
Design Flow
Correctness and Optimization



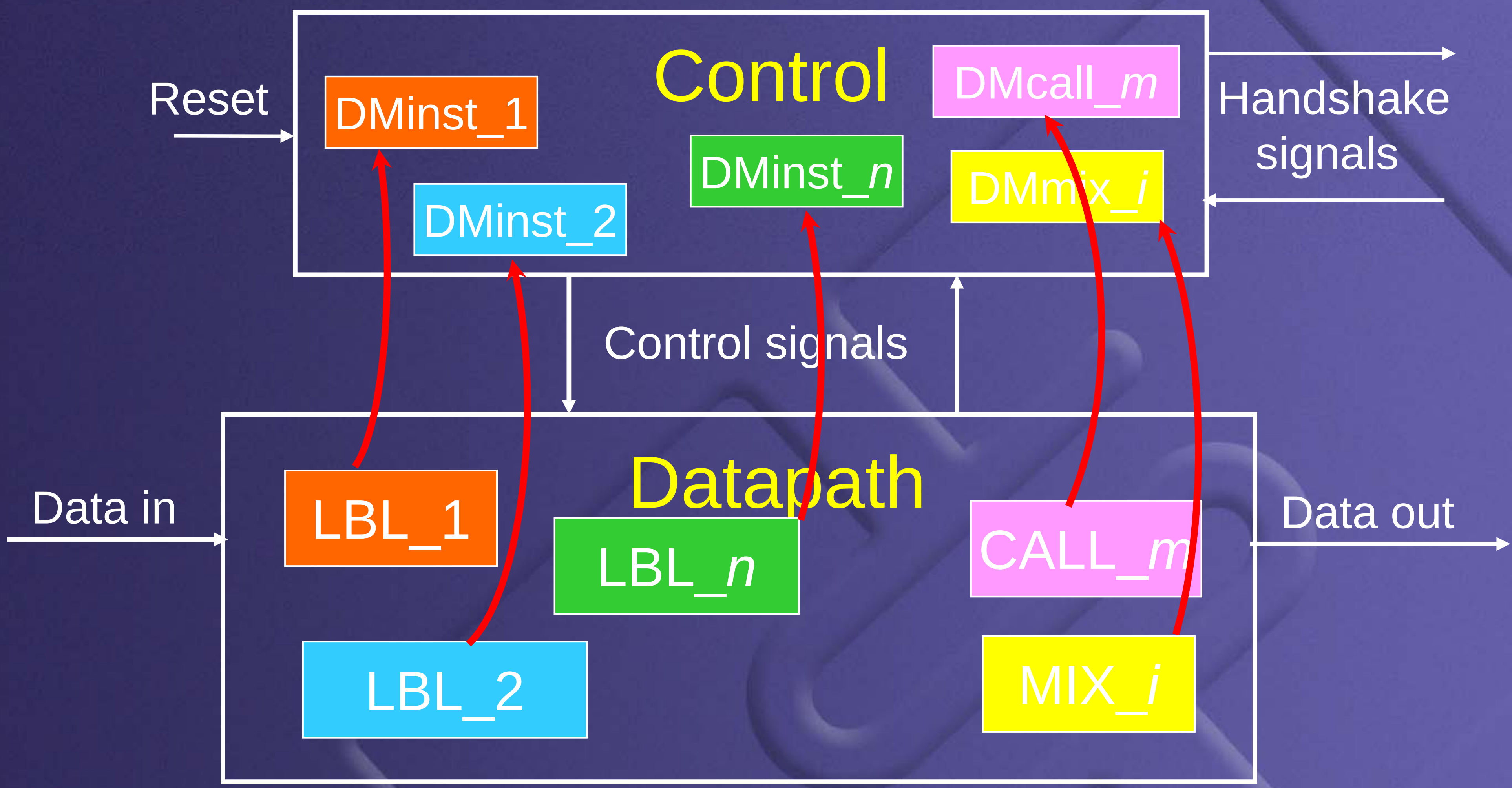
Design Flow
Correctness and Optimization



Design Flow
Correctness and Optimization



Design Flow
Correctness and Optimization



Design Flow

Haste Constraint File

Name of delay chain

Start of total delay path

Start of section

End of total delay path

```
DELAY DMINST_1
DELAYBEGIN PIN CTRinst/DMinst_1/A
DELAYEND PIN CTRinst/DMinst_1/Z
INPUT PIN LBinst/VAR_ab_0_m0/Q
INPUT PIN LBinst/VAR_ab_1_m0/Q
INPUT PIN LBinst/VAR_ab_2_m0/Q
INPUT PIN LBinst/VAR_ab_3_m0/Q
OUTPUT PIN LBinst/do1_e_0
ENDDELAY
```

Input of logic block

Output of logic block

End of section

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Design Flow

Haste Constraint File

Name of delay chain

Start of section

Start of total delay path

```
HOLD DMPULSE_1
DELAYBEGIN PIN CTRinst/VAR_ab_0_en_A
DELAYEND PIN CTRinst/DMpulse_1/Z
INPUT PIN LBinst/VAR_ab_0_m0/CP
OUTPUT PIN LBinst/C_0_
INPUT PIN LBinst/VAR_ab_1_m0/CP
OUTPUT PIN LBinst/C_1_
INPUT PIN LBinst/VAR_ab_2_m0/CP
OUTPUT PIN LBinst/C_2_
INPUT PIN LBinst/VAR_ab_3_m0/CP
OUTPUT PIN LBinst/C_3_
ENDHOLD
```

End of total delay path

Clock input of register

End of section

Output of register
(or a pin connected to it)

Handshake Technology
Physical design status

- Fortunately, we can reuse existing design flows
  - Unfortunately, all ‘synchronous’ tools are subtly different
  - Fortunately, from a distance they are alike
  - We get good support from the EDA community
- Correctness has been addressed
  - Constraints, procedures, and verification
- Optimization just started
  - Haste Constraint Format for upward compatibility
  - ‘double optimization runs’ to identify realistic targets for speed
  - Timing evaluation for control paths a challenge
  - Many constraints can only be specified in relation to a clock

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Thank you

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