The ISPD 2006 Placement Contest and Benchmark Suite

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Summary of ISPD 2005 Placement Contest

- 9 academic placement tools participated
  - Good coverage of placement tools
- 8 new placement benchmarks were released.
  - All were derived from real industrial ASIC designs
  - Extensively being used in placement research
- HPWL was used as sole quality metric
  - No routability estimation
  - No timing analysis
  - No runtime measurement
- Analytic placement tools dominated

A bit of Criticism

- “The contest, however, evaluated legality and wire length, not routability, which is a key concern for commercial placement tools”… EETimes 04/06/2005

- Rather high free space in benchmarks (i.e., low utilization)
  - Sort of favors analytic placement algorithm

ISPD 2006 Placement Contest

- 9 teams again
  - APlace3, Capo, DPlace, Dragon, FastPlace, Kraftwerk, mFAR, mPL6, Ntuplace
- Provide another suite of real placement benchmarks
- More advanced form of quality of metric
  - Legality
  - HPWL
  - Routability estimation via density target
  - Runtime
- Contestants submit executables and administrator runs them on new benchmarks

Placement Solution Scoring Function

$$HPWL*(1 + Scaled\_overflow\_factor + CPU\_factor)$$

Placement Solution Scoring Function

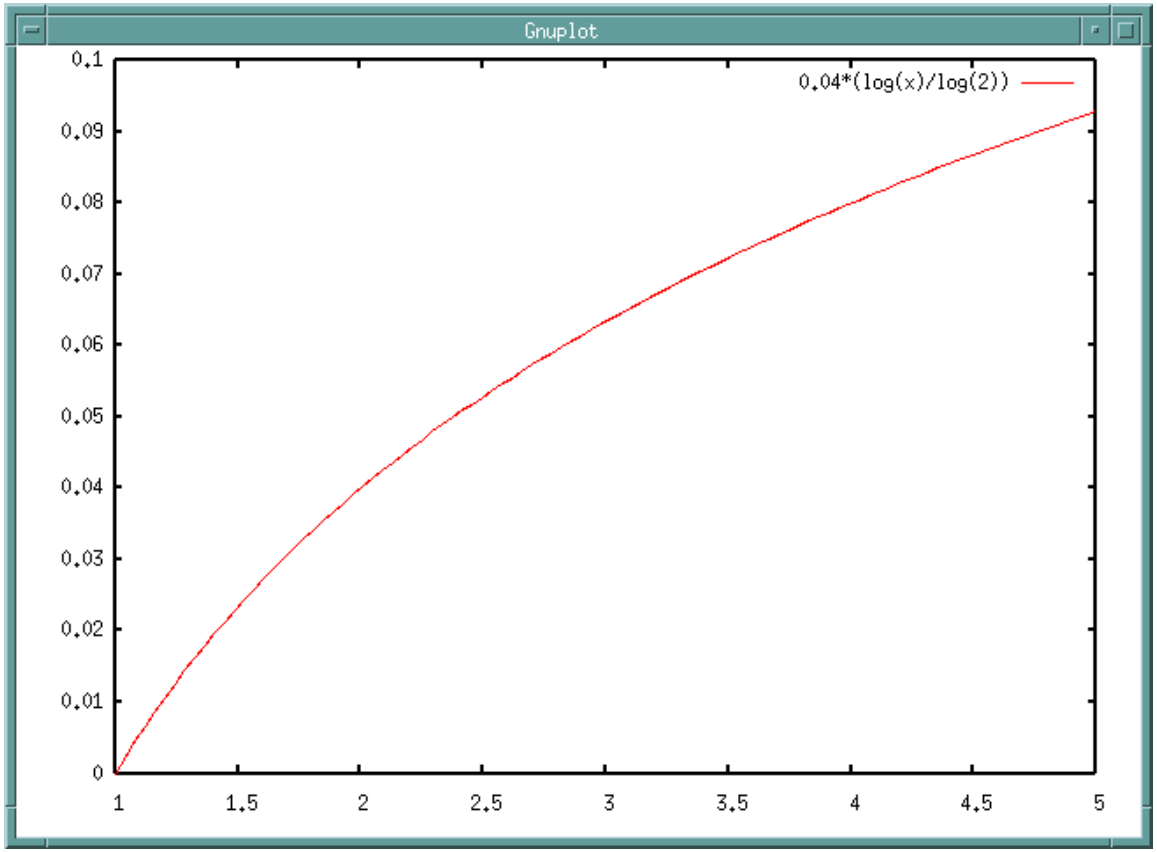
$$HPWL*(1 + Scaled\_overflow\_factor + CPU\_factor)$$

- Impose a bin grid (10 circuit row height, width)
- Measure the overflow
  - BOF = Σmovable_area_bin – bin_free_space*density_target
  - TOF = ΣBOF
- Scale the total overflow TOF
  - Scaled_overflow_factor = TOF * bin_area * density_target / Σmovable_objects_area
  - Scaled_overflow_factor^2 is used

Placement Solution Scoring Function

HPWL*(1 + Scaled_overflow_factor + CPU_factor)

- CPU_factor = 0.04*LOG2(your_CPU / median_CPU)
- 2x slower ~ 4% penalty
- 4x slower ~ 8% penalty
- max 10% penalty

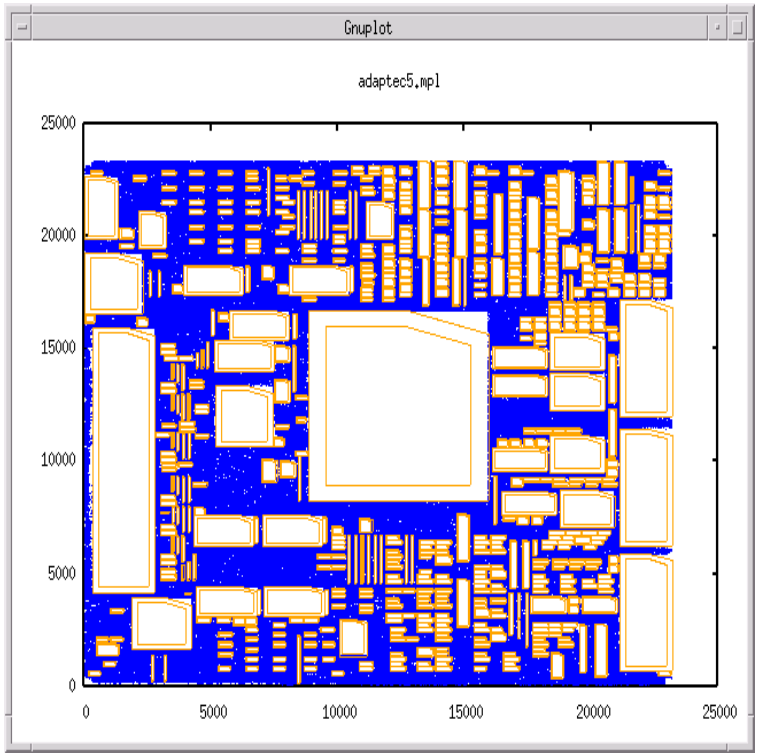


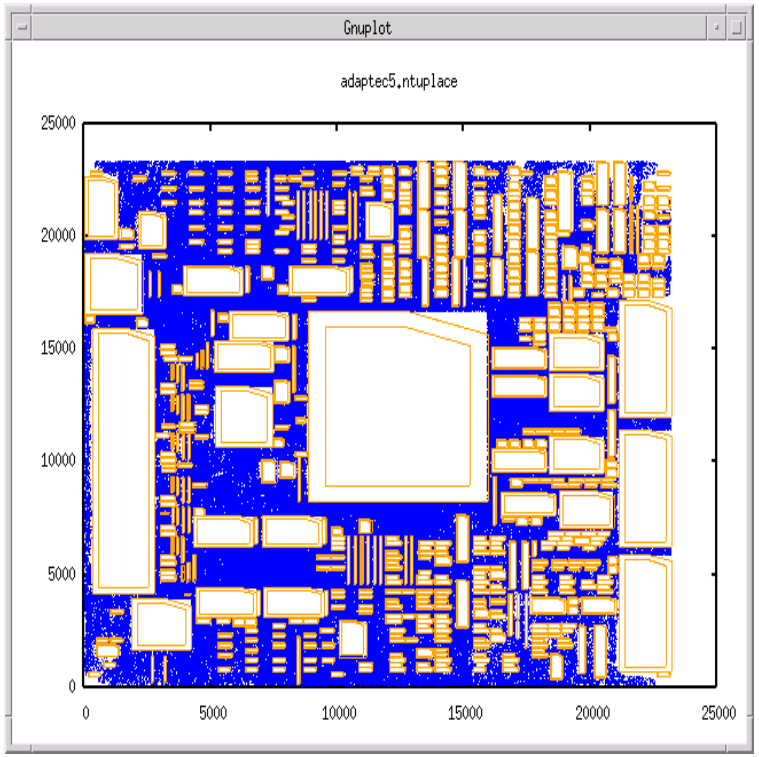
ISPD 2006 Benchmark Suite

Name	#Objs	#Movs	#Fixed	#Nets	Density %	Utilization %	Density Target%
adaptec5	843128	842482	646	867798	78.64	49.98	50
newblue1	330474	330137	337	338901	85.73	83.20	80
newblue2	441516	330239	1277	465219	86.14	61.66	90
newblue3	494011	482833	11178	552199	84.70	26.31	80
newblue4	646139	642717	3422	637051	65.72	46.45	50
newblue5	1233058	1228177	4881	1284251	74.54	49.56	50
newblue6	1255039	1248150	6889	1288443	59.27	38.78	80
newblue7	2507954	2481372	26582	2636820	76.46	49.31	80

adaptec5

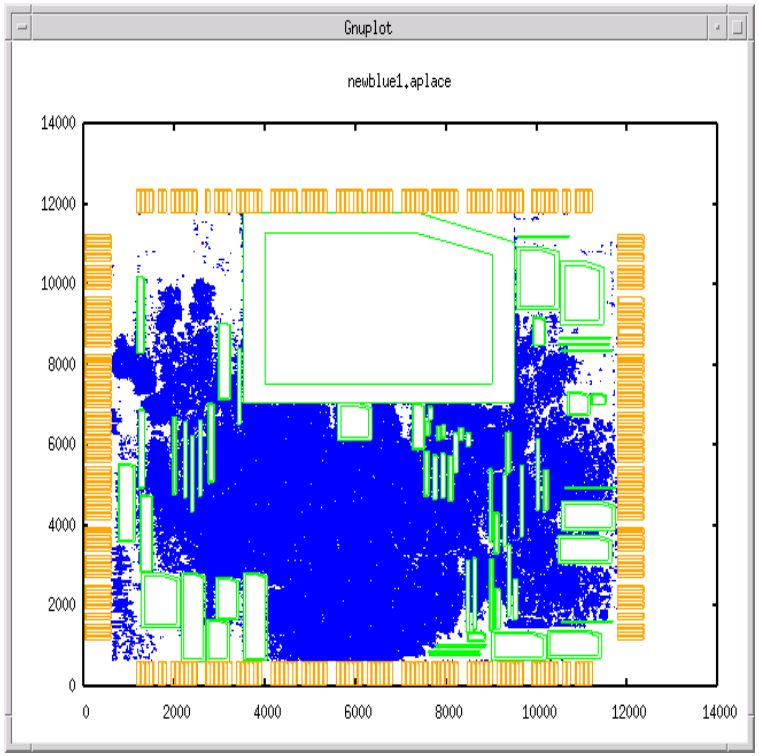
- 843K objects
- Density 79%, Utilization 50%
- Density target 50%

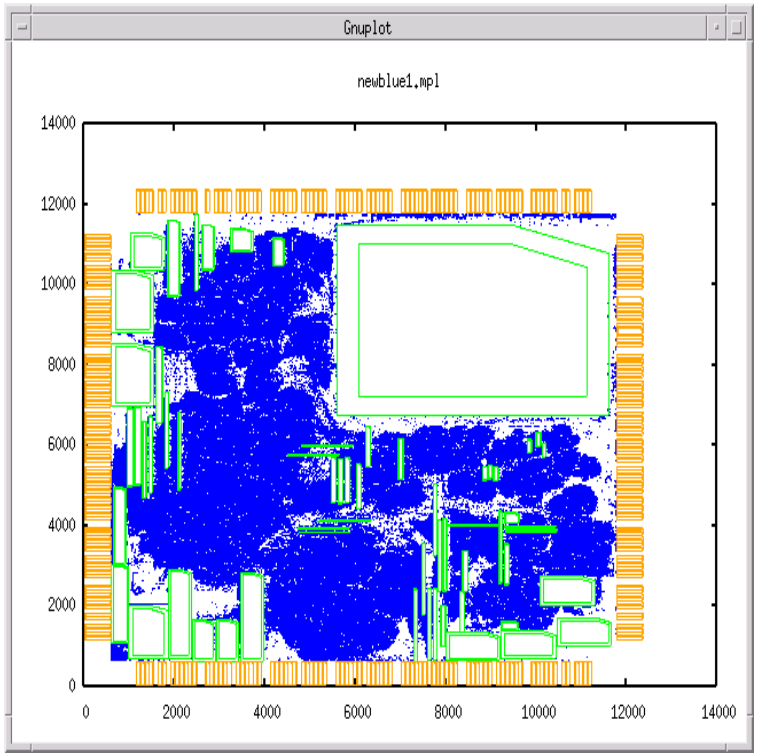




newblue1

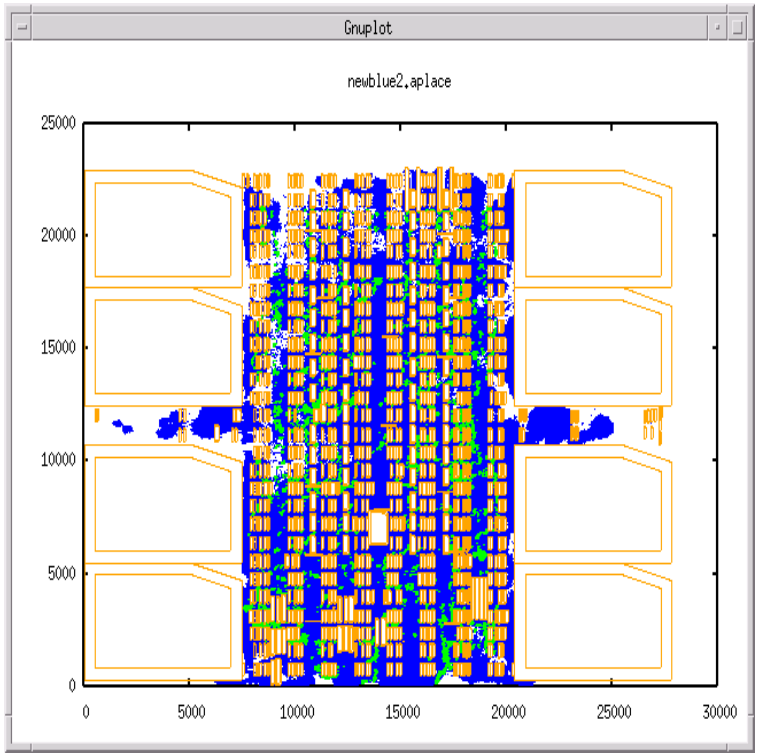
- 330K objects
- Lots of large movable macros
- Density 86%, Utilization 83%
- Density target 80%

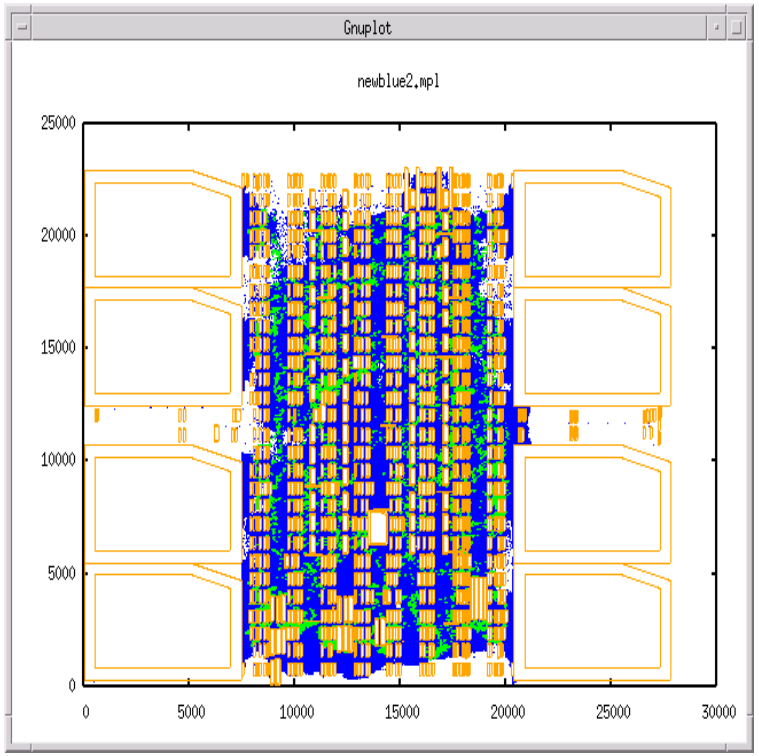




newblue2

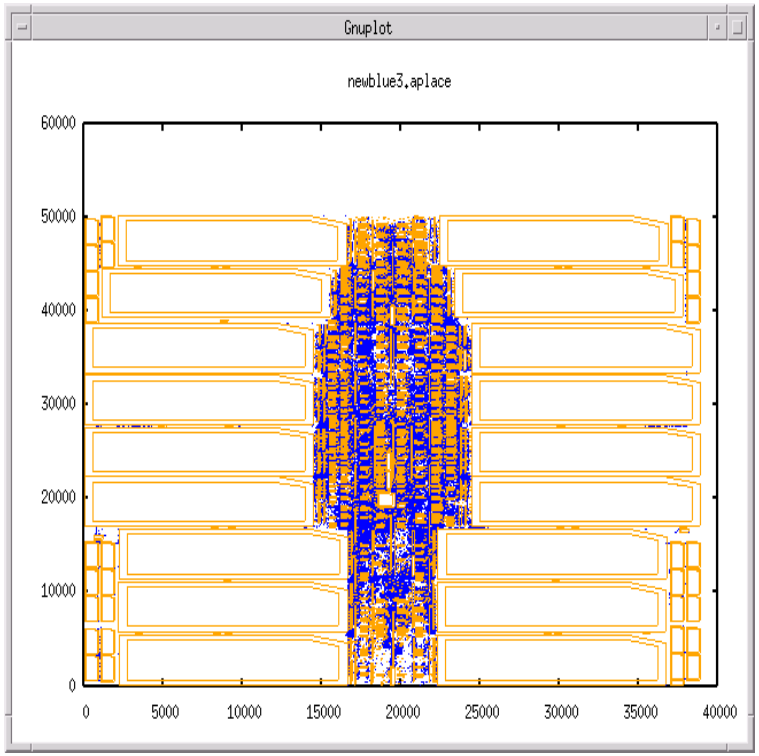
- 442K objects
- All standard cells were inflated by 2x
- 3.7K small movable macros (a few circuit row height)
- Density 86%, Utilization 62%
- Density target 90%

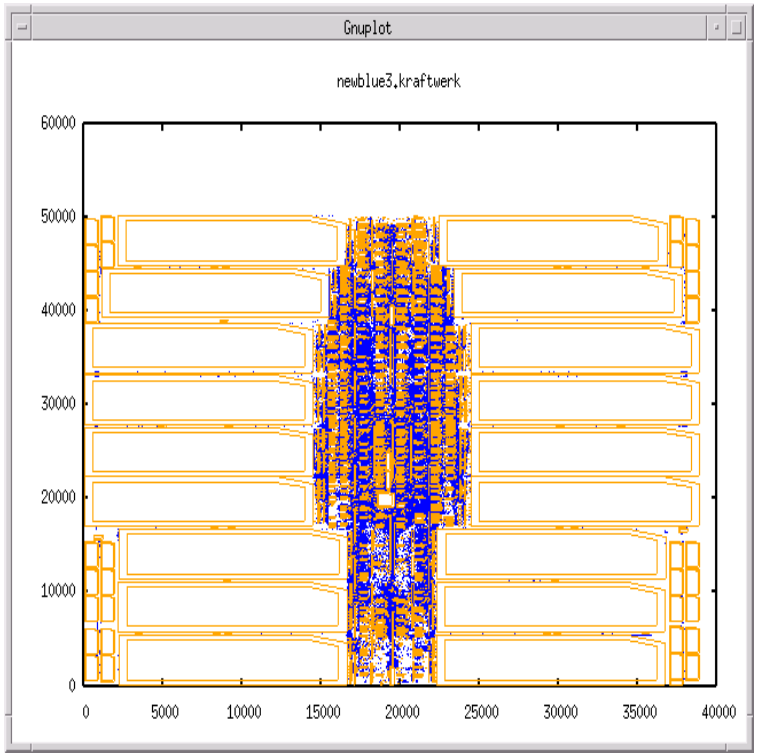




newblue3

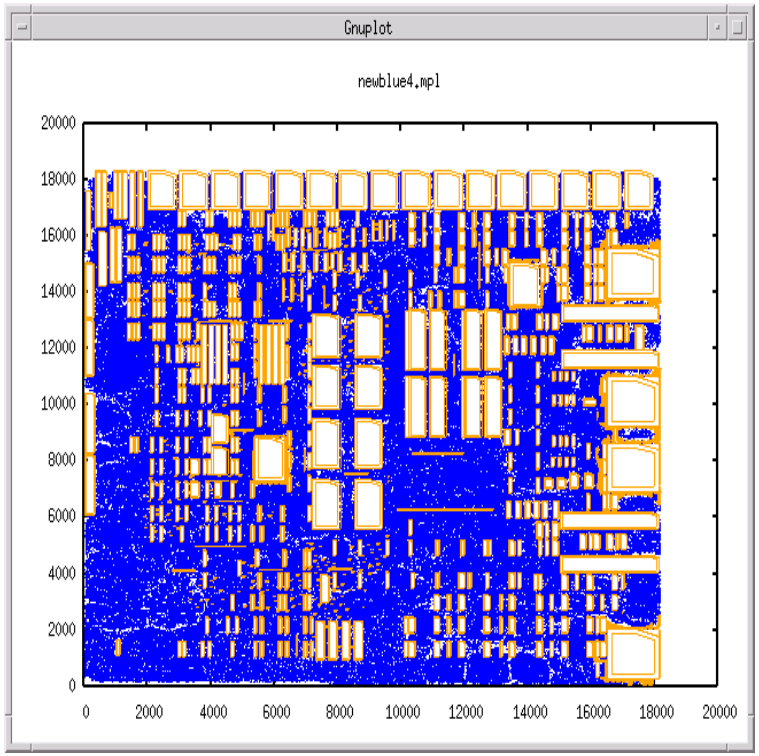
- 494K objects
- Interesting floorplan
- Density 85%, Utilization 26%
- Density target 80%

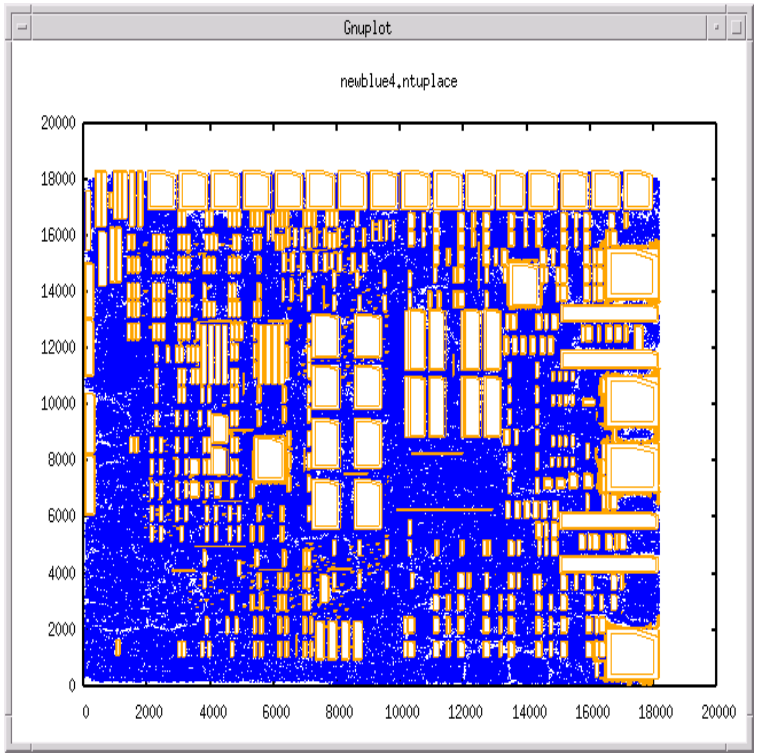




newblue4

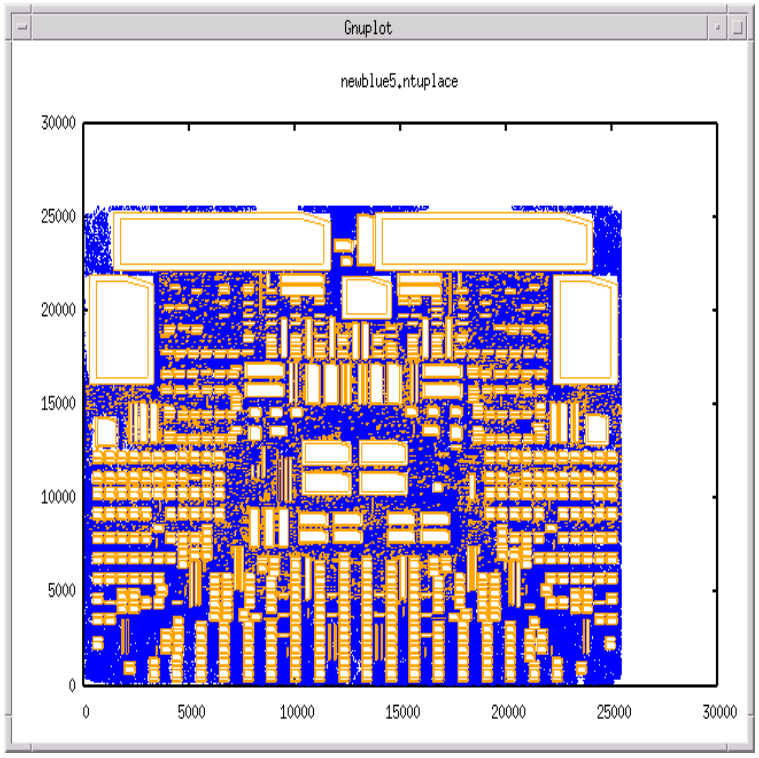
- 646K objects
- Density 66%, Utilization 46%
- Density target 50%

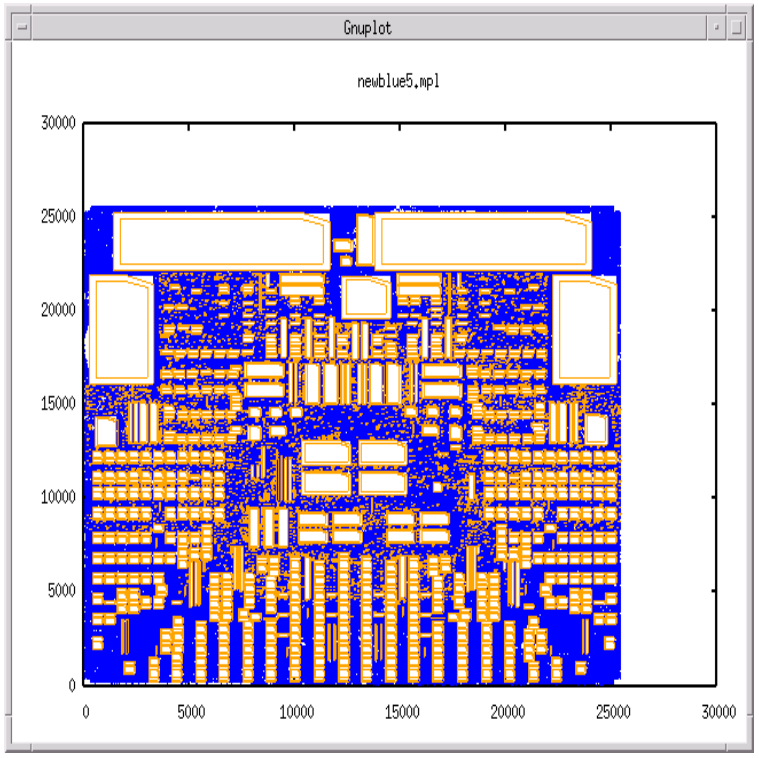




newblue5

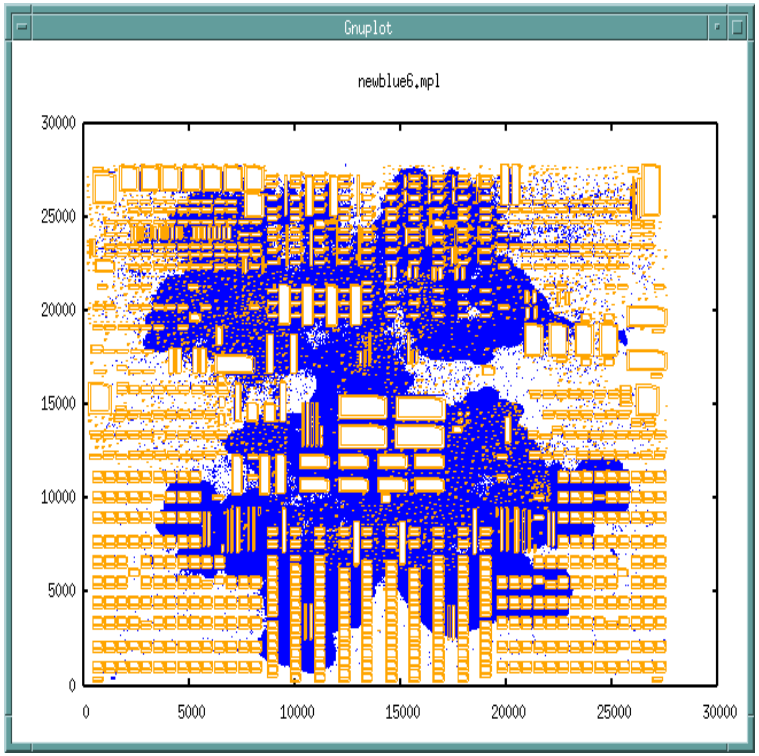
- 1233K objects
- Density 75%, Utilization 50%
- Density target 50%

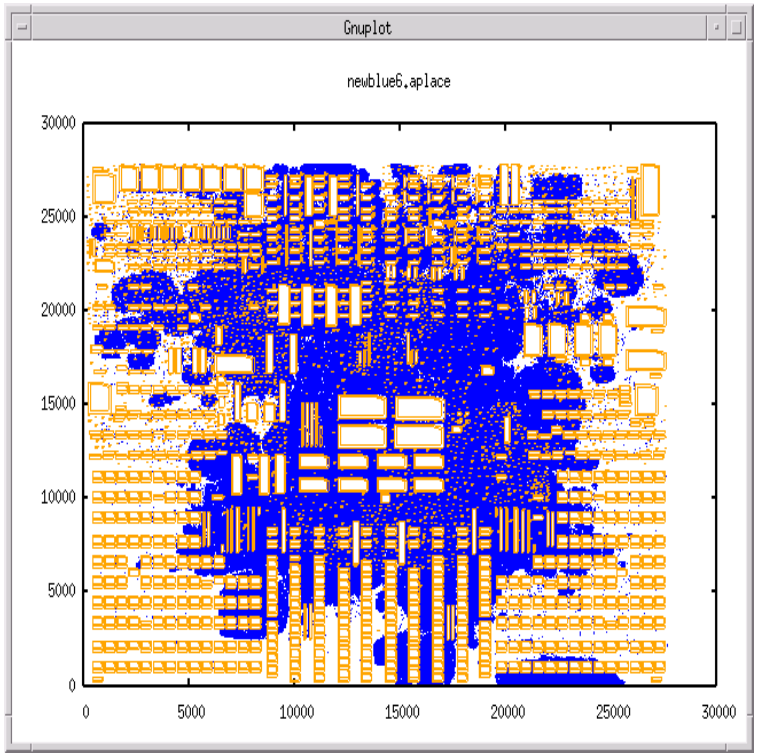




newblue6

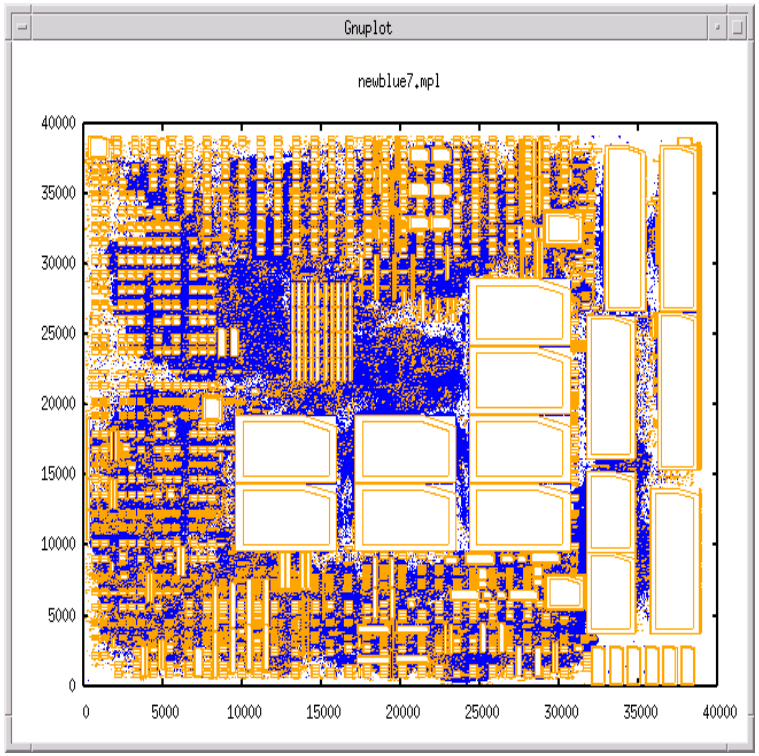
- 1255K objects
- Density 60%, Utilization 39%
- Density target 80%

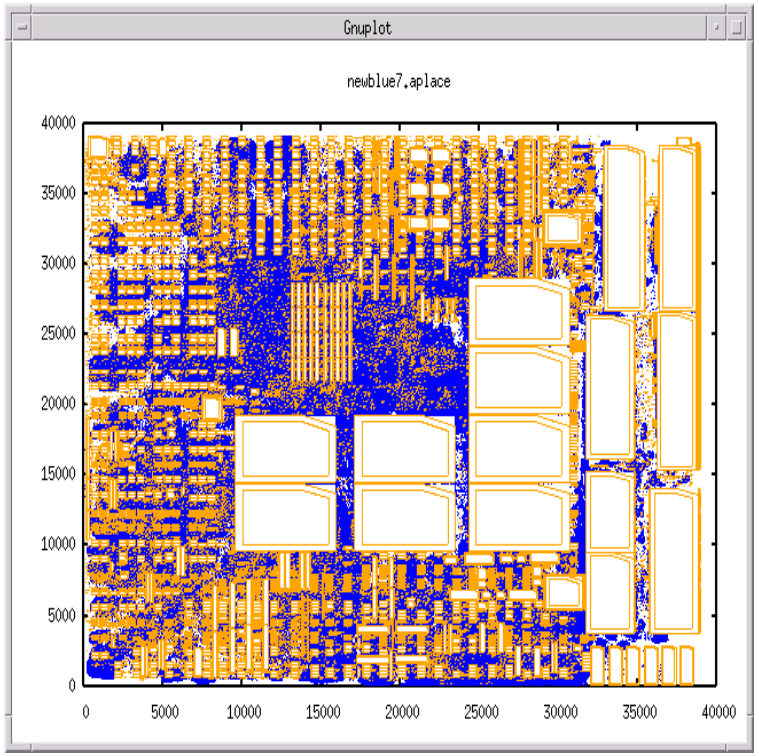




newblue7

- 2508K objects
- Density 76%, Utilization 49%
- Density target 80%





Contest Results

	ad5	nb1	nb2	nb3	nb4	nb5	nb6	nb7	Avg.
place1	1.01	1.19	1.00	1.00	1.01	1.04	1.00	1.00	1.03
place2	1.00	1.06	1.07	1.17	1.00	1.02	1.00	1.00	1.04
place3	1.02	1.00	1.07	1.16	1.03	1.00	1.04	1.07	1.05
place4	1.09	1.23	1.09	1.16	1.09	1.13	1.03	1.04	1.11
place5	1.26	1.20	1.05	1.13	1.35	1.21	1.06	1.05	1.16
place6	1.08	1.21	1.29	1.90	1.05	1.13	1.03	1.23	1.24
place7	1.82	1.22	1.02	1.37	1.35	1.76	1.04	1.05	1.33
place8	1.26	1.55	1.77*	1.36	1.14	1.35	1.23	1.25	1.36
place9	1.16	1.57	1.64	1.44	1.22	1.28	1.32	1.46	1.39

Contest Results

	ad5	nb1	nb2	nb3	nb4	nb5	nb6	nb7	Avg.
place1	1.01	1.19	1.00	1.00	1.01	1.04	1.00	1.00	1.03
place2	1.00	1.06	1.07	1.17	1.00	1.02	1.00	1.00	1.04
ntuplace	1.02	1.00	1.07	1.16	1.03	1.00	1.04	1.07	1.05
place4	1.09	1.23	1.09	1.16	1.09	1.13	1.03	1.04	1.11
place5	1.26	1.20	1.05	1.13	1.35	1.21	1.06	1.05	1.16
place6	1.08	1.21	1.29	1.90	1.05	1.13	1.03	1.23	1.24
place7	1.82	1.22	1.02	1.37	1.35	1.76	1.04	1.05	1.33
place8	1.26	1.55	1.77*	1.36	1.14	1.35	1.23	1.25	1.36
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place1	1.01	1.19	1.00	1.00	1.01	1.04	1.00	1.00	1.03
mPL6	1.00	1.06	1.07	1.17	1.00	1.02	1.00	1.00	1.04
ntuplace	1.02	1.00	1.07	1.16	1.03	1.00	1.04	1.07	1.05
place4	1.09	1.23	1.09	1.16	1.09	1.13	1.03	1.04	1.11
place5	1.26	1.20	1.05	1.13	1.35	1.21	1.06	1.05	1.16
place6	1.08	1.21	1.29	1.90	1.05	1.13	1.03	1.23	1.24
place7	1.82	1.22	1.02	1.37	1.35	1.76	1.04	1.05	1.33
place8	1.26	1.55	1.77*	1.36	1.14	1.35	1.23	1.25	1.36
place9	1.16	1.57	1.64	1.44	1.22	1.28	1.32	1.46	1.39

Contest Results

	ad5	nb1	nb2	nb3	nb4	nb5	nb6	nb7	Avg.
kraftwerk	1.01	1.19	1.00	1.00	1.01	1.04	1.00	1.00	1.03
mPL6	1.00	1.06	1.07	1.17	1.00	1.02	1.00	1.00	1.04
ntuplace	1.02	1.00	1.07	1.16	1.03	1.00	1.04	1.07	1.05
mFAR	1.09	1.23	1.09	1.16	1.09	1.13	1.03	1.04	1.11
APlace3	1.26	1.20	1.05	1.13	1.35	1.21	1.06	1.05	1.16
Dragon	1.08	1.21	1.29	1.90	1.05	1.13	1.03	1.23	1.24
FastPlace	1.82	1.22	1.02	1.37	1.35	1.76	1.04	1.05	1.33
DPlace	1.26	1.55	1.77*	1.36	1.14	1.35	1.23	1.25	1.36
Capo	1.16	1.57	1.64	1.44	1.22	1.28	1.32	1.46	1.39

*Illegal solution with few overlaps on AMD platform, Legal solution on Intel platform

Contest Results

	Avg. WL	Avg. Overflow Penalty%	Avg. CPU Factor%
kraftwerk	1.09	1.68	-5.04
mPL6	1.03	1.36	1.58
ntuplace	1.02	4.10	1.66
mFAR	1.11	2.71	-0.12
APlace3	1.10	3.82	5.31
Dragon	1.33	0.12	-5.90
FastPlace	1.18	22.09	-5.62
DPlace	1.34	9.32	-4.54
Capo	1.38	0.32	2.69

Results: What if CPU_factor is not included….

	ad5	nb1	nb2	nb3	nb4	nb5	nb6	nb7	Avg.
mPL6	1.00	1.06	1.01	1.05	1.00	1.04	1.00	1.00	1.02
ntuplace	1.00	1.00	1.03	1.06	1.02	1.00	1.03	1.09	1.03
kraftwerk	1.06	1.24	1.05	1.03	1.05	1.10	1.05	1.08	1.08
APlace3	1.21	1.15	1.00	1.00	1.28	1.19	1.01	1.01	1.11
mFAR	1.10	1.22	1.07	1.11	1.08	1.16	1.03	1.07	1.11
Dragon	1.16	1.27	1.32	1.92	1.14	1.26	1.10	1.30	1.31
Capo	1.15	1.55	1.56	1.32	1.21	1.27	1.29	1.40	1.34
FastPlace	1.87	1.33	1.07	1.33	1.43	1.86	1.11	1.14	1.39
DPlace	1.33	1.62	1.66	1.39	1.22	1.45	1.32	1.33	1.42

Conclusion

- Total 16 new placement benchmarks
  - All derived from real ASIC designs
  - Variety of floorplans
  - 5 benchmarks with more than million objects
- ISPD 2006 Contest
  - Indirectly address routability issue
  - Turn-around time
  - Improvements from ISPD 2005 results
- Can we include timing analysis into this flow?