Noise Driven In Package Decoupling Capacitor Optimization for Power Integrity

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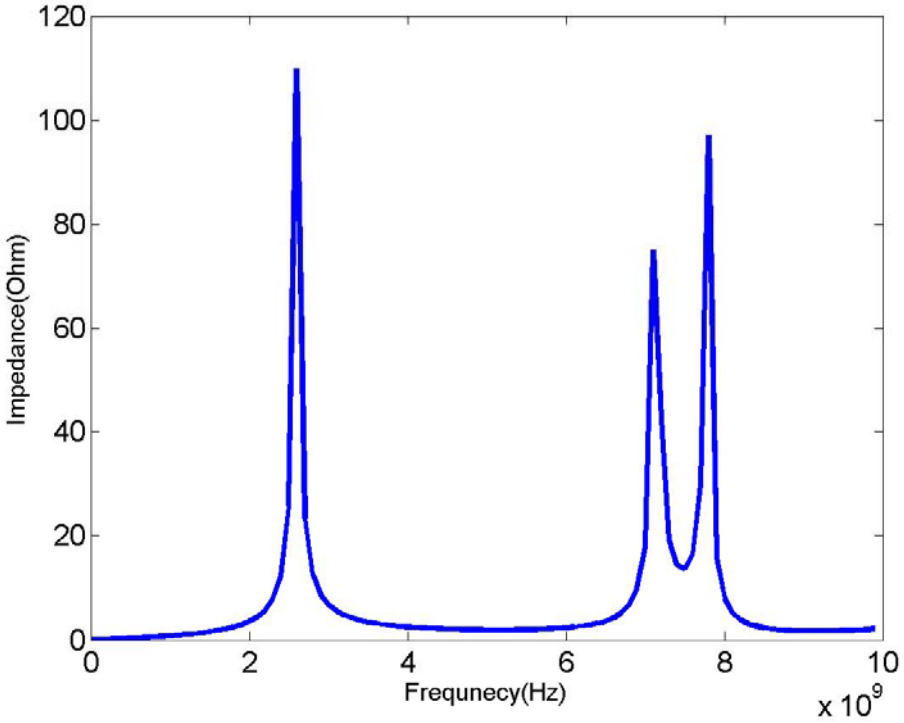
Outline

- Introduction
- Electrical models
- Incremental impedance computation and noise computation
- Optimization results
- Conclusion

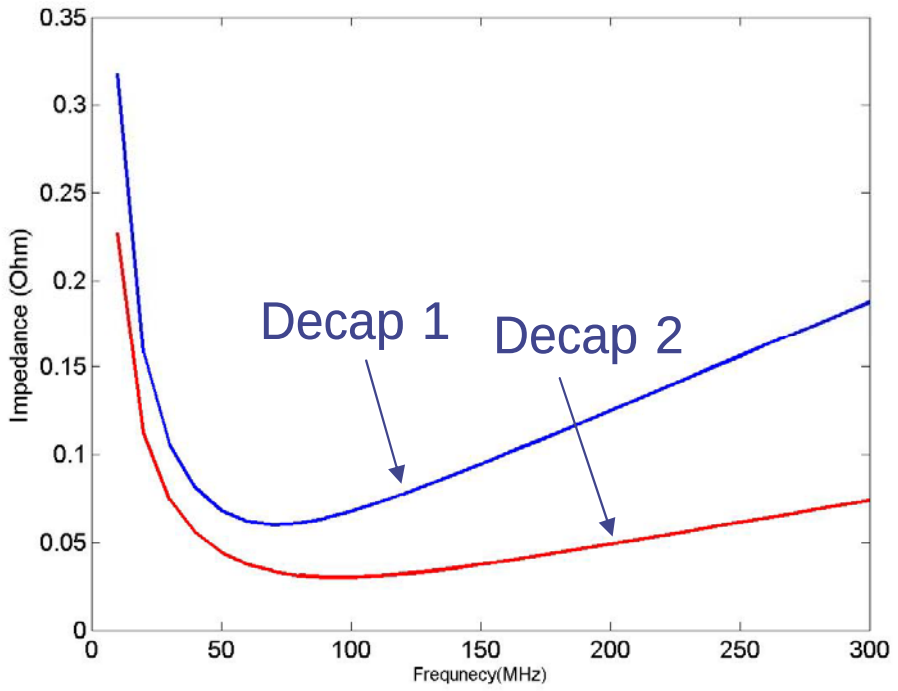
Power Integrity

- Noise in power delivery system (PDS)
  - IR drop
  - dI/dt drop
  - Resonance
- Challenges in advanced high-performance package
  - Hugh power consumption
    - Large current
  - High clock frequency
    - Large inductive effects and resonance
  - Large number of I/O's
    - SSN



Decoupling capacitors

- Improve power integrity with decoupling capacitors
  - Low impedance path
  - Temporary current source
- In-Package decoupling capacitors for package
  - Discrete elements
  - Discrete ESC, ESL, ESR
  - Different effective frequencies
  - Different in costs



In-Package decoupling capacitor optimization problem

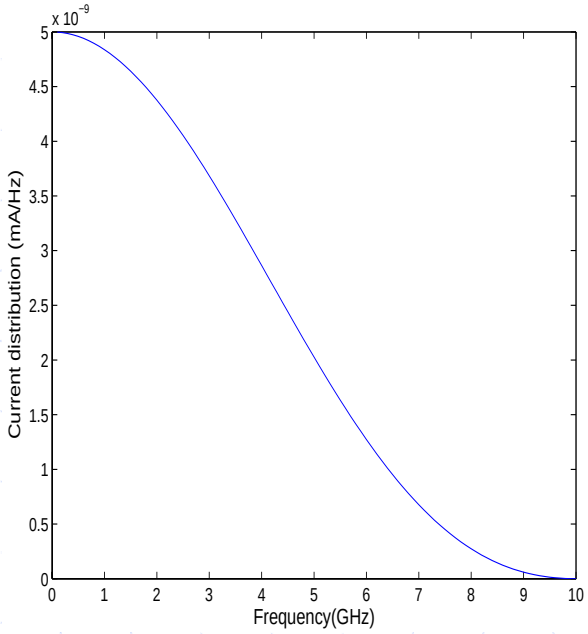
- Optimization problem for in-package decoupling capacitors
  - Given a package and chip I/Os
  - Find the best types and locations of decoupling capacitors
  - Such that the cost is minimized
  - Subject to SSN noise bound
- Challenges
  - Large number of I/O's and possible locations and types for decoupling capacitors
  - Complex model with inductance
  - Non-monotonic solution space
    - More decoupling capacitors do not always lead to better integrity
    - Locations closer to I/O does not always lead to better solutions
    - Hard to use mathematic programming for optimization

Existing Work

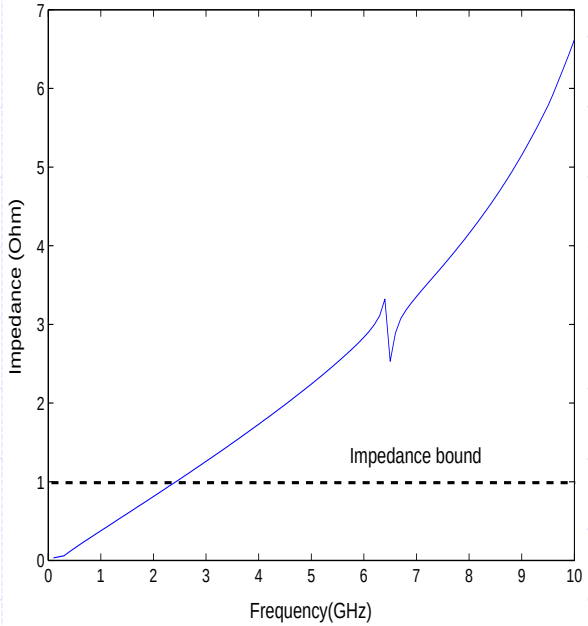
- Manual trial-and-error approaches
  - [Chen et al., ECTC ’96]
  - [Yang et al., EPEP 2002]
- Automatic optimization
  - [Kamo et al., EPEP 2000], [Hattori et al., EPEP 2002]
    - Ignore ESL and ESR.
  - [Zheng et al., CICC 2003]
    - Use impedance as noise metric

Limitation of Impedance Metric

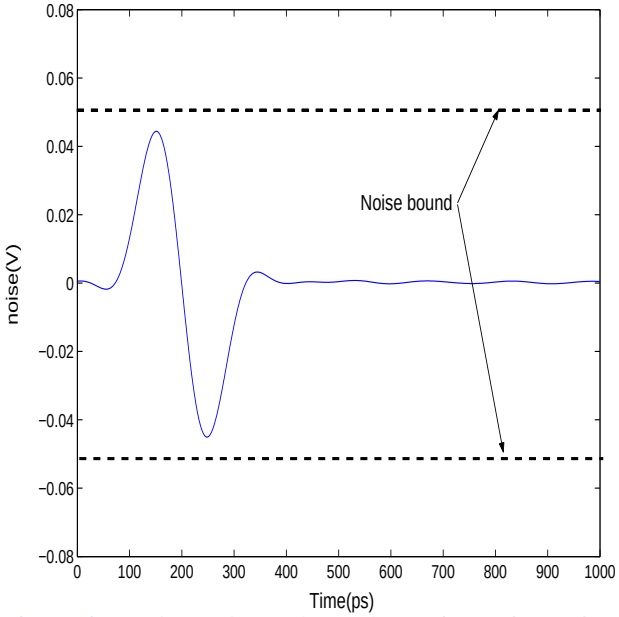
- Traditional noise bound can not capture noise accurately
- Will Lead to large over-design
- Difficult to consider coupling noise between ports



I(f)



Z(f)



$V_n(t)$

Our contributions

- Efficient noise model
  - Efficient incremental impedance computation
    - Time complexity: $O(n^2)$ vs $O(n^3)$
  - Explicit time-domain noise metric
    - FFT
- Optimize both types and locations of decoupling capacitors based on explicit noise model
  - 3x smaller cost compared to impedance based approach
  - 10x speedup compared to admittance matrix inversion based method

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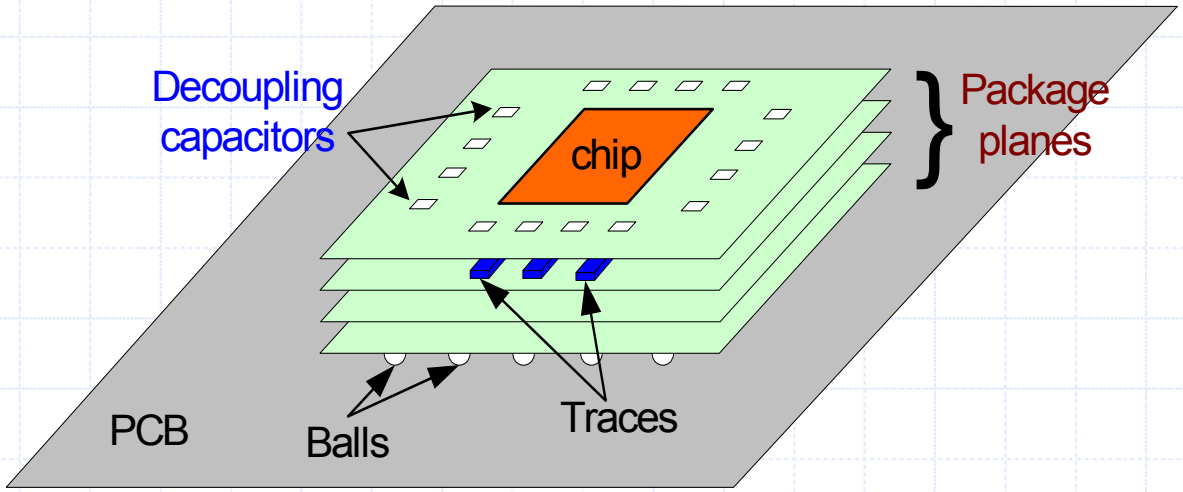
Package model

- IC package
  - Multiple signal layers, power planes and ground planes
  - Planes stapled with Vias

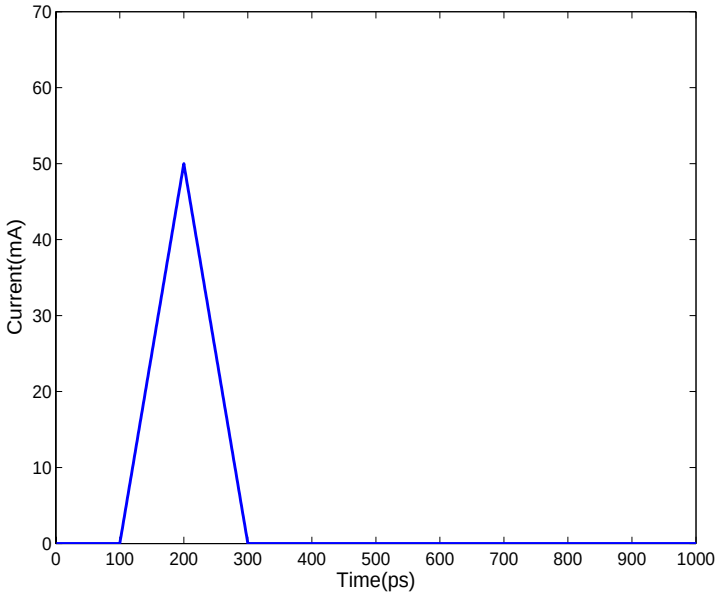


Macromodel of PDS

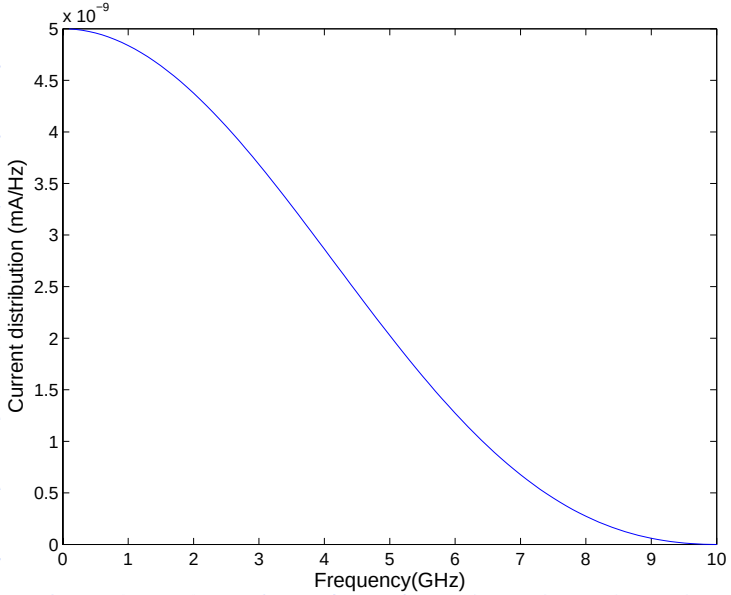
- Given ports
  - Known I/O locations
  - Possible decoupling capacitor locations
- Pre-compute macromodel of PDS before optimization at sampling frequency f_k
  - Impedance matrix $Z(f_k)$
    - Detailed PEEC model+model order reduction
  - Field solver, measurement, …
  - Not limited to package
    - May include VRM, PCB and on-chip P/G grid.

Model of Switching Current

- I/O cells
  - Pre-characterize time dependent switching current
  - Transform waveform into frequency domain



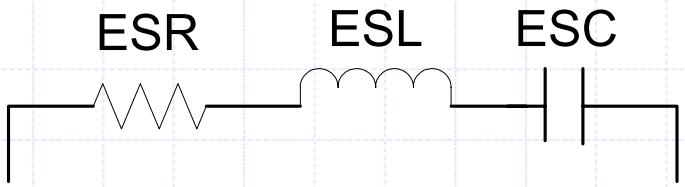
Time domain



Frequency domain

Decoupling capacitor model

- Decoupling capacitor
  - ESC, ESR and ESL



  - Pre-compute frequency dependent impedance

$$Z_d(\omega) = \mathrm{ESR} + \frac{1}{j\omega \mathrm{ESC}} + j\omega \mathrm{ESL}$$

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Existing Approach for Impedance Updating

- To compute the noise accurately, impedance at a large number of frequencies needs to be computed
- With pre-computed macromodel, [Zhao and Mandhana, EPEP2004]

$$\mathbf{Z} = (\mathbf{Y} + \mathbf{Y}_d)^{-1}$$

Admittance w/o decaps Admittance of decaps

- Disadvantages:
  - Involving inversion of large matrix at each frequency
    - $O(n^3)$ complexity
  - Compute all the Z_{ij} each iteration.
    - Better solution: update Z_{ij} when necessary

Incremental impedance updating with decoupling capacitor

- Update each Z_{ij} individually.
- Consider one decoupling capacitor each time.
- When adding one decoupling capacitor Z_d at port k

$$\hat{Z}_{ij} = Z_{ij} - \frac{Z_{ik} Z_{kj}}{Z_{kk} + Z_d}$$

- When removing one decoupling capacitor Z_d at port k

$$\hat{Z}_{ij} = Z_{ij} - \frac{Z_{ik} Z_{kj}}{Z_{kk} - Z_d}$$

- Complexity is O(1) for one port.

Time complexity

- For entire system, with one or a few decoupling capacitors changed
  - $O(n_p^2)$: n_p is the number of ports
  - Existing work: $O(n_p^3)$
- Suitable for trial-and-error or iterative methods
  - Only a few decoupling capacitors changed in each iteration
  - Able to compute only impedance of I/O ports before updating rest ports

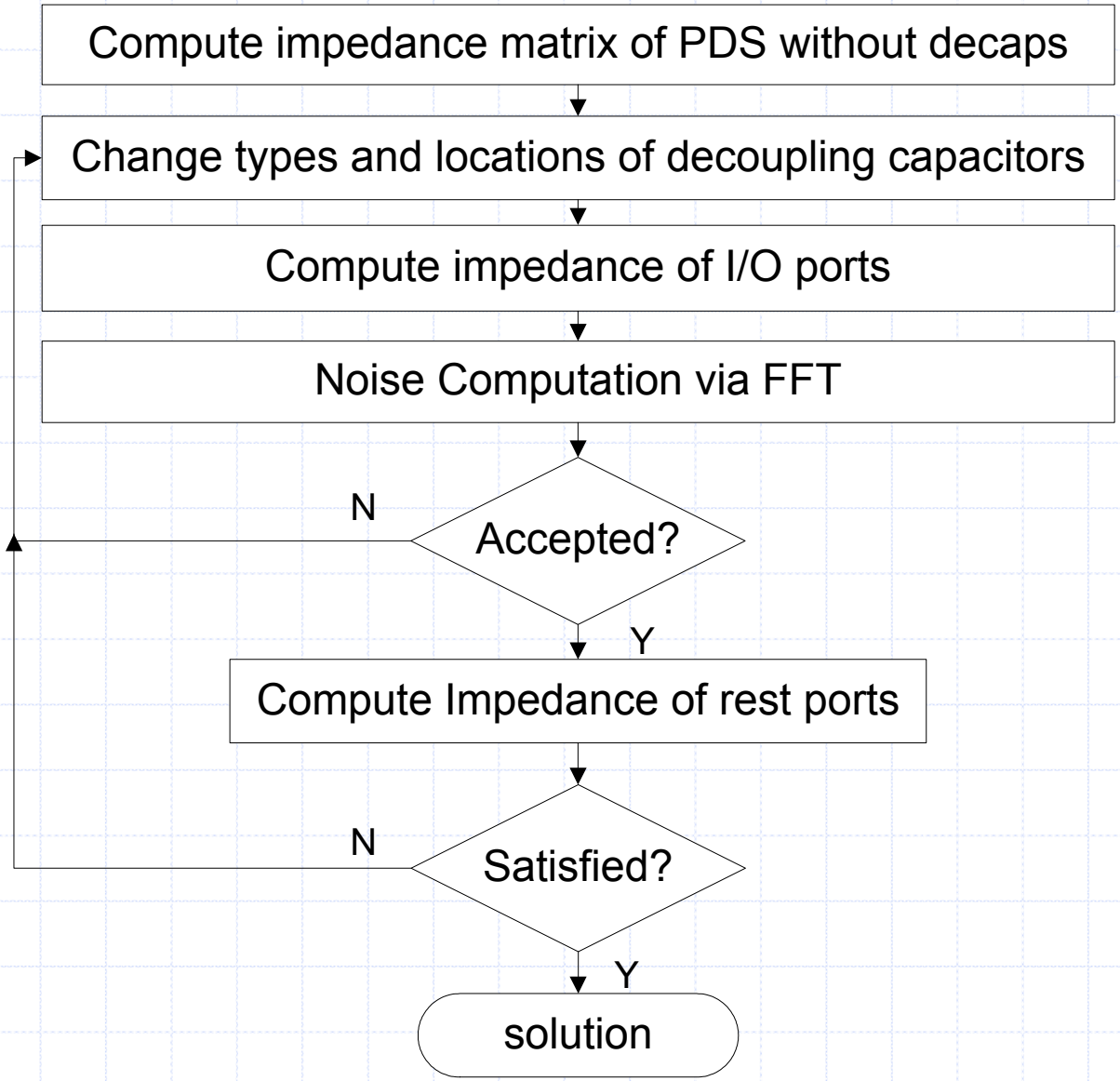
Noise Calculation

- FFT methods
  - Impedance is computed at a large number of frequencies
  - Frequency components of noise from port *j* to port *i*

$$V_{ij}(f_k) = Z_{ij}(f_k) \bullet I_j(f_k)$$

- Worst case noise
  - Consider coupling noise from other ports
  - Superposition

Efficient General Iterative Optimization Flow



$O(n_{I/O}^2)$

$O(n_p^2)$

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Algorithm

- Simulated annealing with objective function

$$F(p_i, c_i) = \alpha \sum_{i \in IO} p_i + \beta \sum_j c_i$$

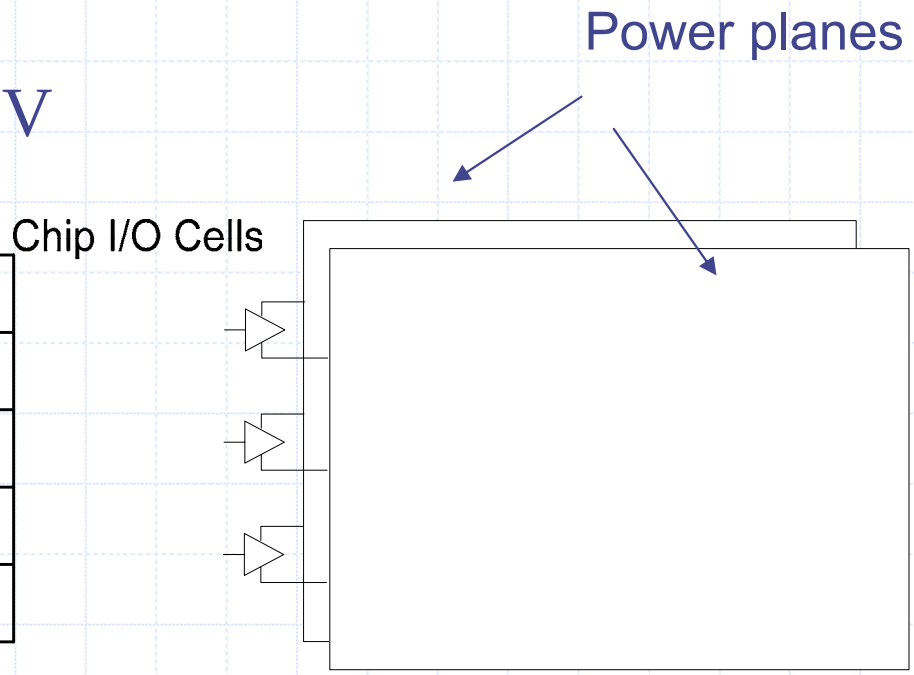
  - p_i: Penalty function for noise violation
  - c_i: cost of decoupling capacitor
  - α, β: weights

Example

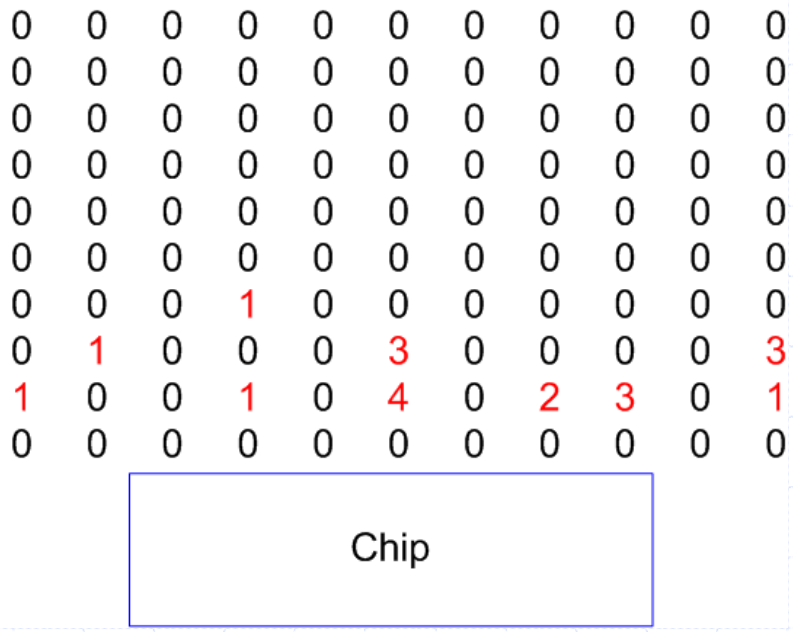
- 4 types of decoupling capacitors
- 3 I/O ports
  - Each connected to 10 I/O cells
- 90 possible locations for decoupling capacitors
- Total 93 ports
- Worst case noise bound: 0.35V

Type	1	2	3	4
ESC(nF)	50	100	50	100
ESR(Ω)	0.06	0.06	0.03	0.03
ESL(pH)	100	100	40	40
Price	1	2	2	4

[Zheng et al., CICC 2003]



Experiment results: noise based



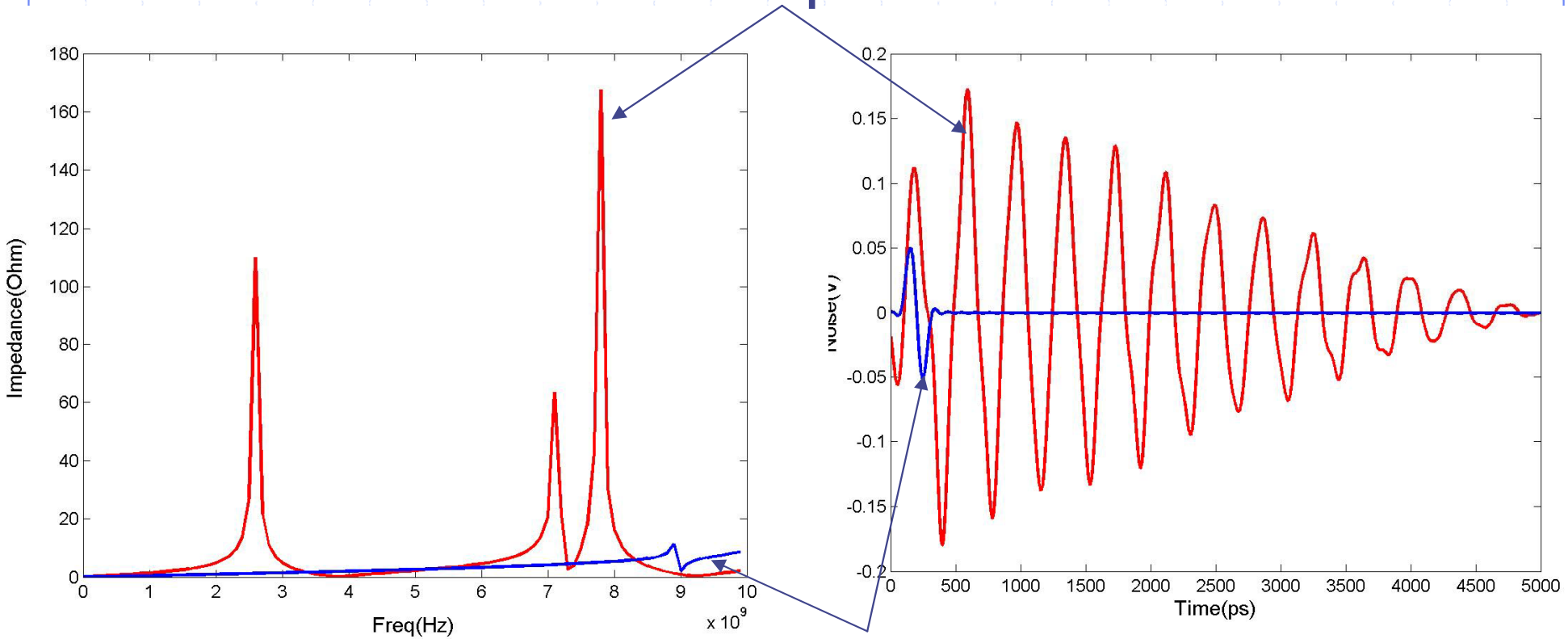
Type	1	2	3	4
ESC(nF)	50	100	50	100
ESR(Ω)	0.06	0.06	0.03	0.03
ESL(pH)	100	100	40	40
Price	1	2	2	4

- Cost=20

port	1	2	3
before optimization	2.52V	2.49V	2.48V
after optimization	0.344V	0.343V	0.344V

Impedance and Noise

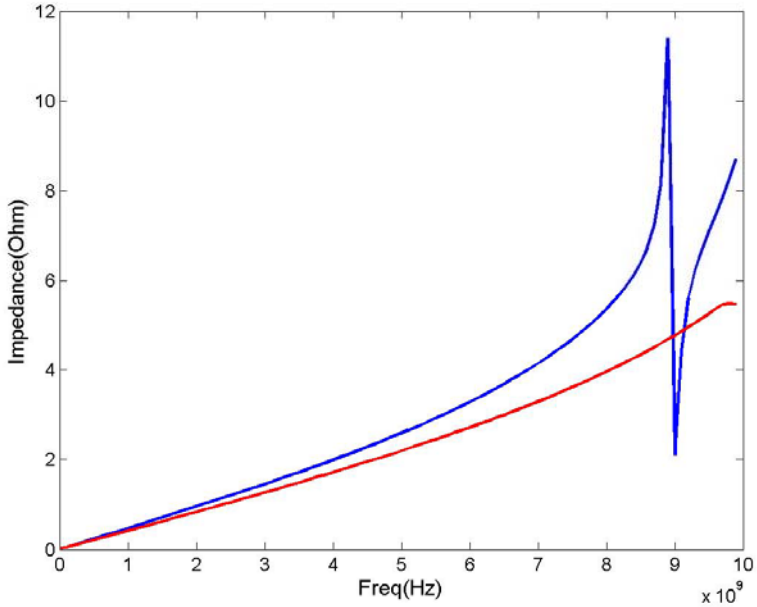
Before optimization



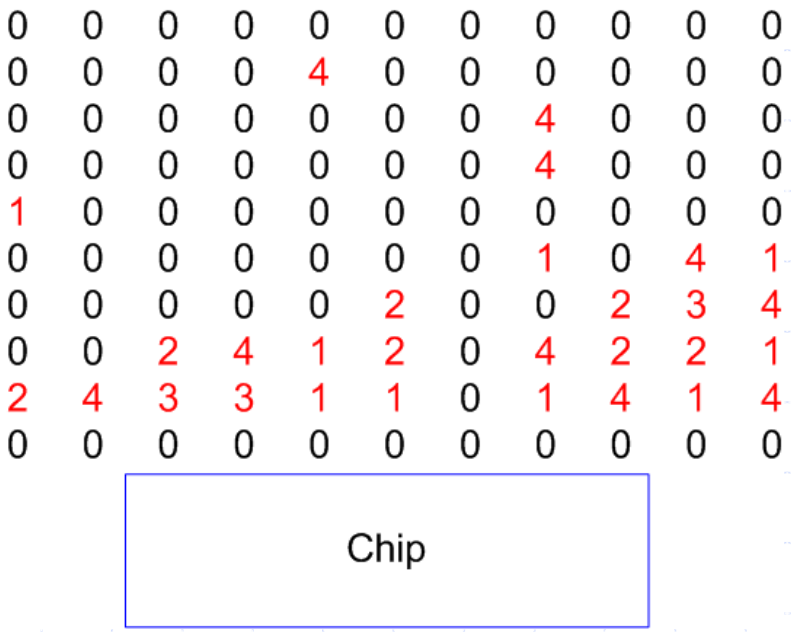
After optimization

Comparison: Impedance based approach

- Cost=72
  - 3X larger than noise based
- Impedance bound is not met but noise bound has already been met.
  - Overdesign



port	1	2	3	bound
Maximum Impedance	5.31Ω	5.59Ω	7.12Ω	0.7Ω
worst-case noise	0.256V	0.302V	0.284V	0.35V



Runtime Comparison

1	Noise based via incremental impedance computation
2	Noise based via admittance matrix inversion [Zhao et al, EPEP 2004]
3	Impedance based [Zheng et al, CICC 2003]

approach	1	2	3
ports	93	93	20
iterations	5881	5403	1920
runtime(s)	389.5	4156.1	2916
avg. runtime(s)	0.0662	0.7692	1.519

10x speedup compared to method based on admittance matrix inversion

Conclusion

- Proposed efficient noise computation model based on incremental impedance updating
- Proposed efficient noise driven decoupling capacitor optimization algorithm
  - 3X smaller cost
  - 10x speedup
- Demonstrated impedance based approach leads to large overdesign.