NEMO: A New Implicit Connection Graph-Based Gridless Router with Multi-Layer Planes and Pseudo-Tile Propagation

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Outline

Introduction

New Implicit Connection Graph-Based Router (NEMO)

General-Purpose Routing

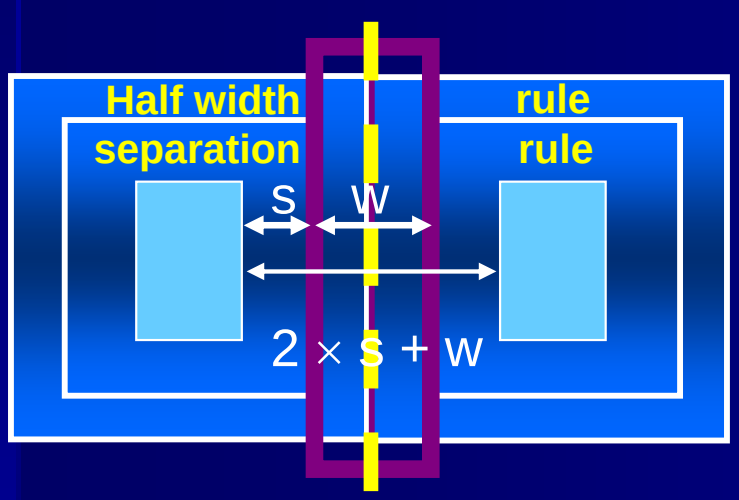
Experimental Results

Conclusion

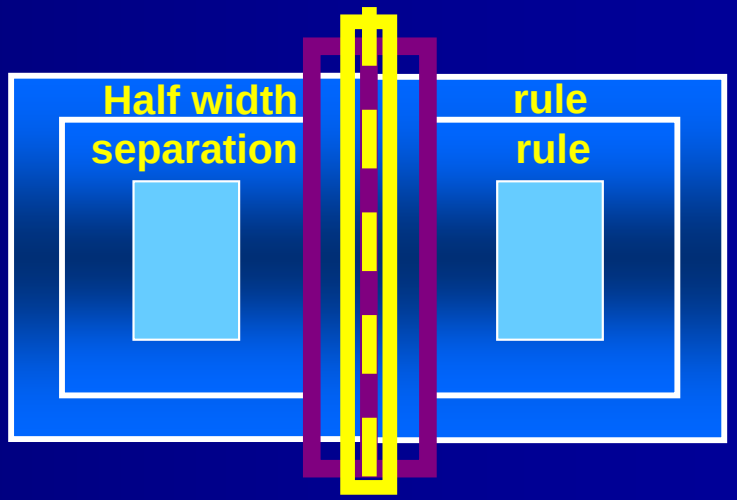
Why Gridless Routing ?

- Variable-width and variable-space routing becomes inevitable for modern designs
  - Wide space and fat wire for crosstalk and delay optimization
- Gridless routers are more flexible for variable-rule routing than grid-based routers

Basic Concept

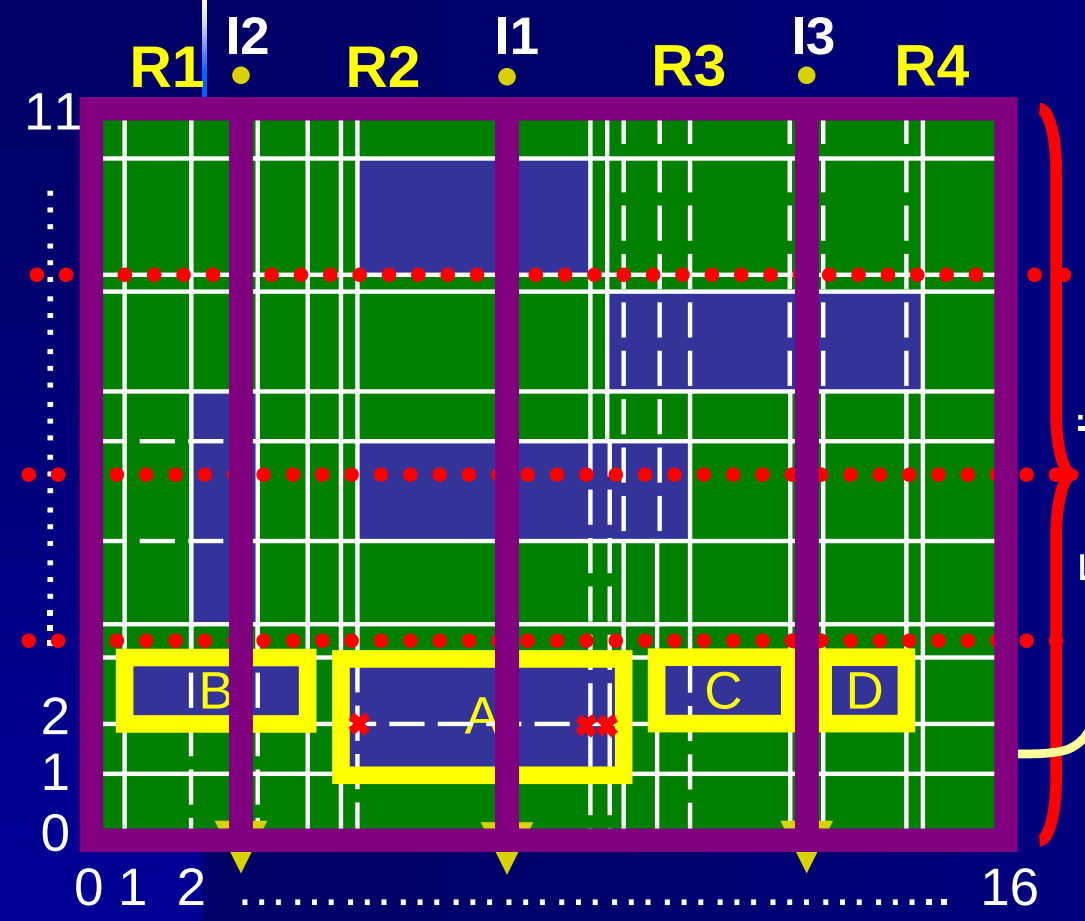


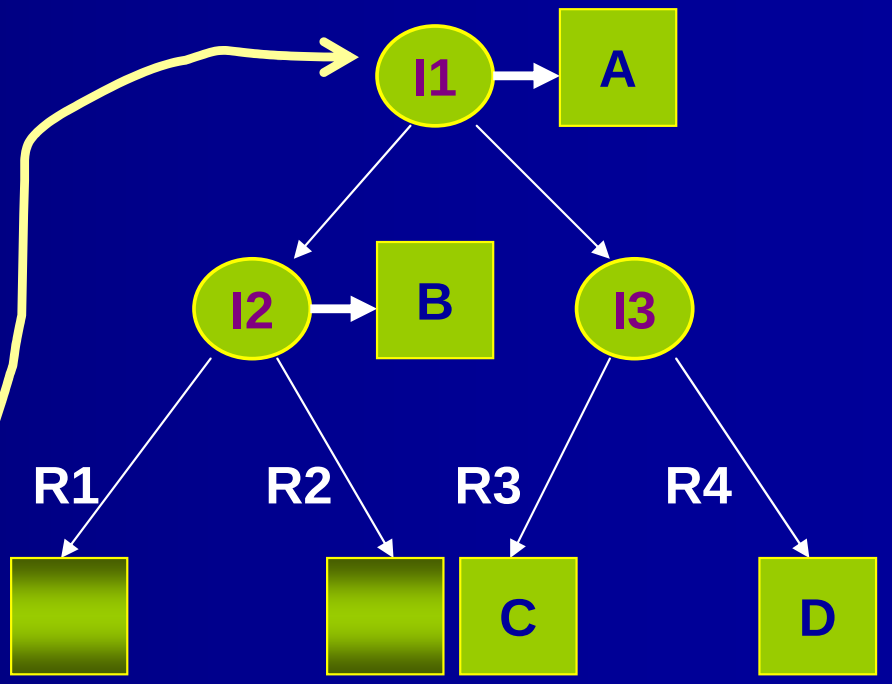
Zero-width Model



Nonzero-width Model

Implicit Connection Graph-Based Router



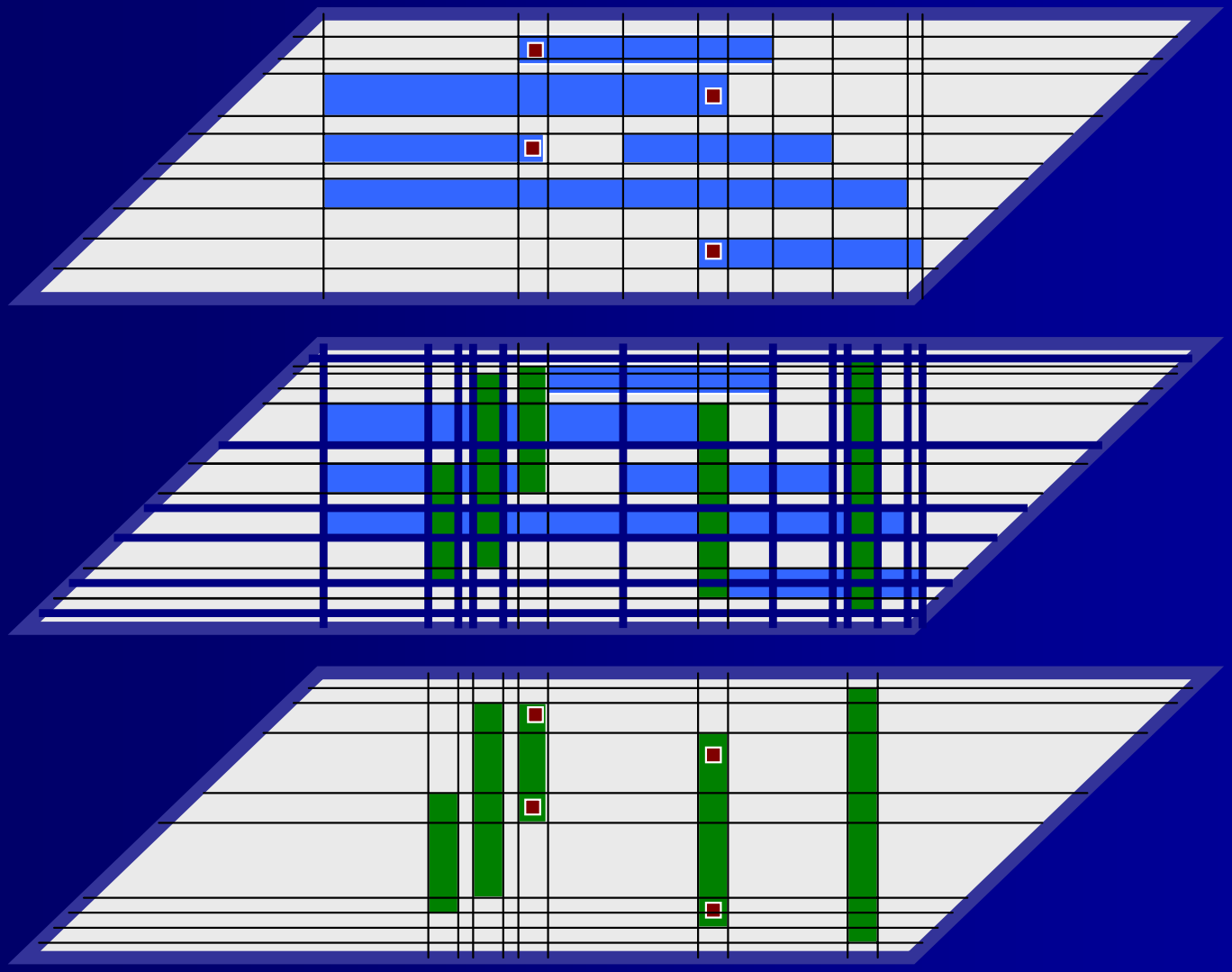


Fast routing graph construction

- J. Cong et al., "An Implicit connection graph maze Routing Algorithm for ECO routing," in ISPD99

Efficient query data structure (Slit tree + Interval Tree)

Implicit Connection Routing Graph



Contribution of This Work

- We propose a new implicit connection graph-based router with pseudo-tile extraction and propagation to
  - reduce the time required for query operations
  - speed up path searching.

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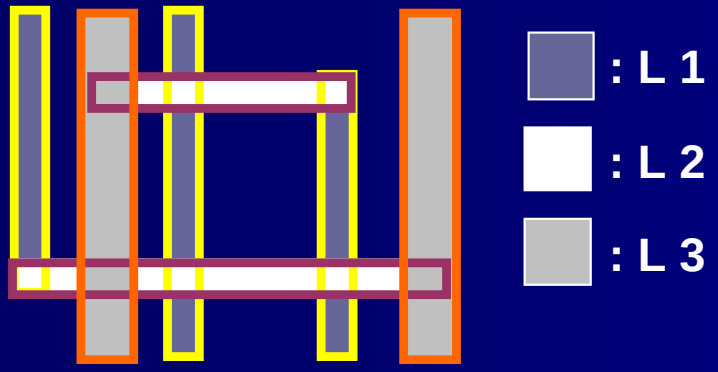
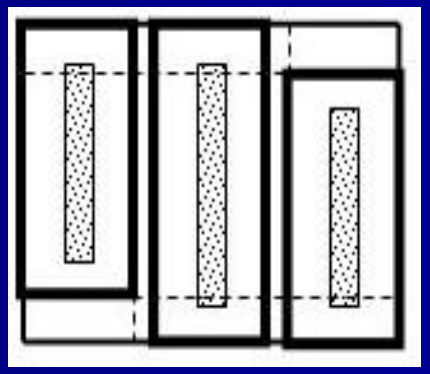
Features of NEMO

- Multi-Plane Routing Graph
- Tile plane but not grid plane
- Non-zero width wire model
- Pseudo Maximum (horizontally or vertically) Stripped Tile (PMT) Extraction and Propagation
- Pseudo Blockage Insertion & Gridline Reduction

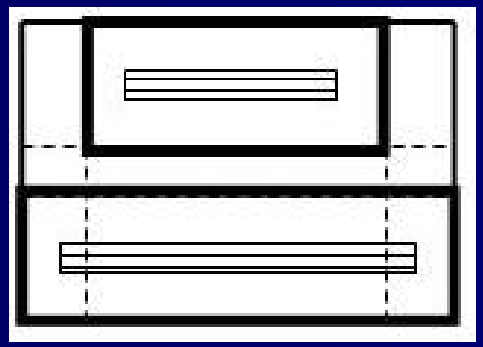
Multi-Plane Routing Graph



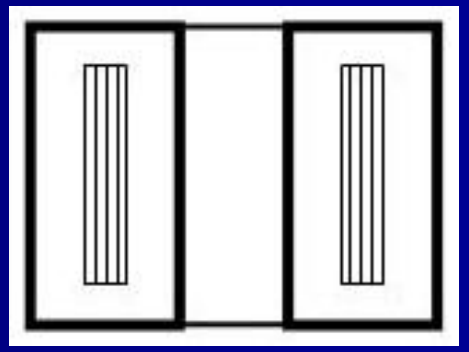
An 3-layer routing example



L 1

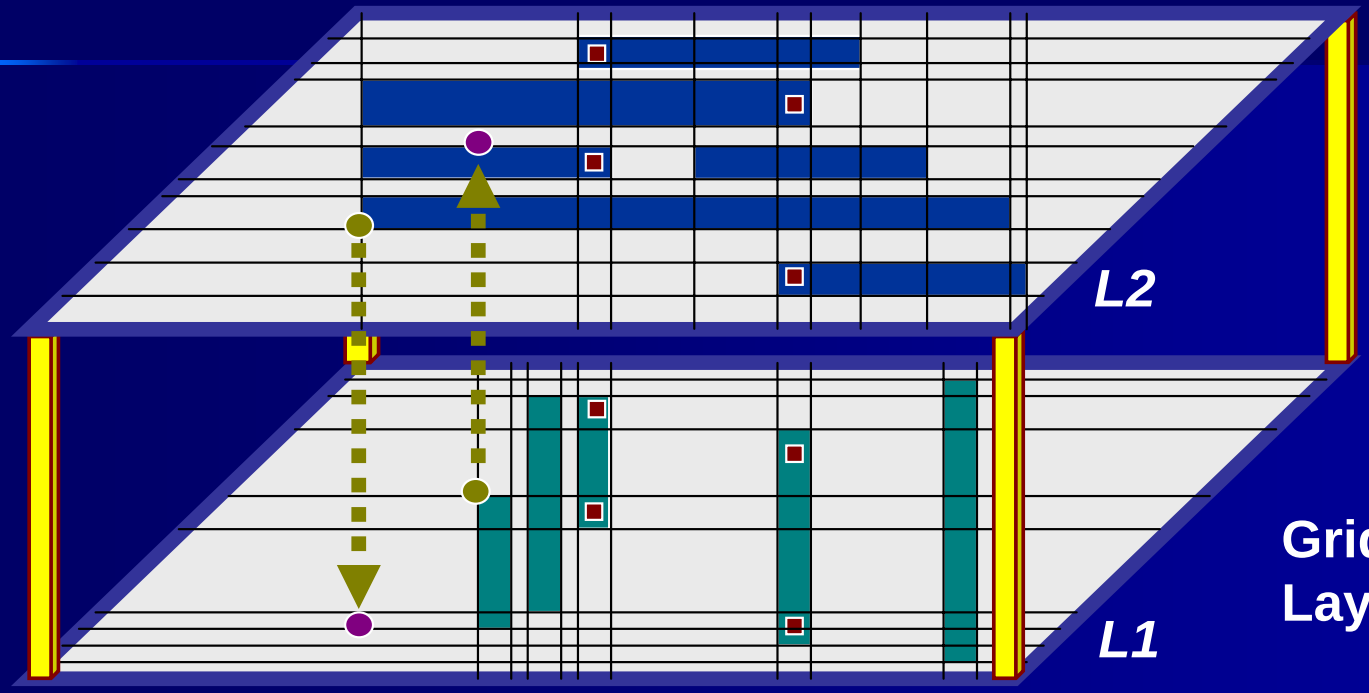


L 2

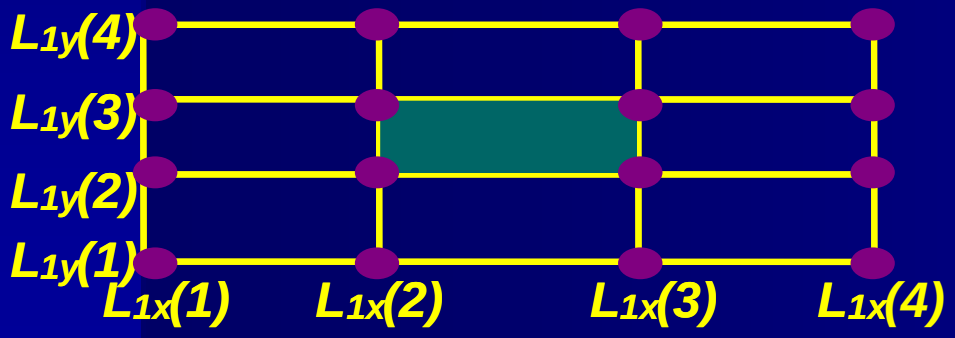


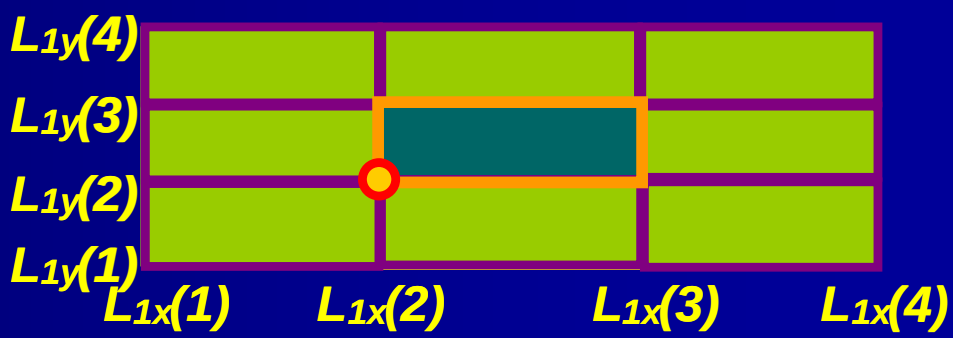
L 3

Why Tile, Not Grid

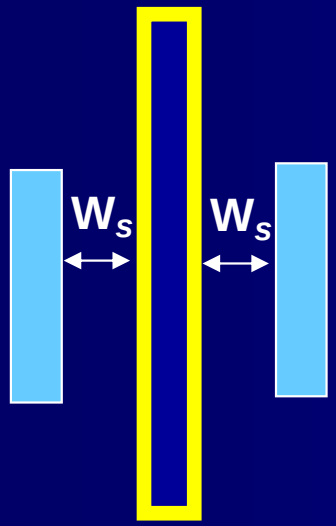


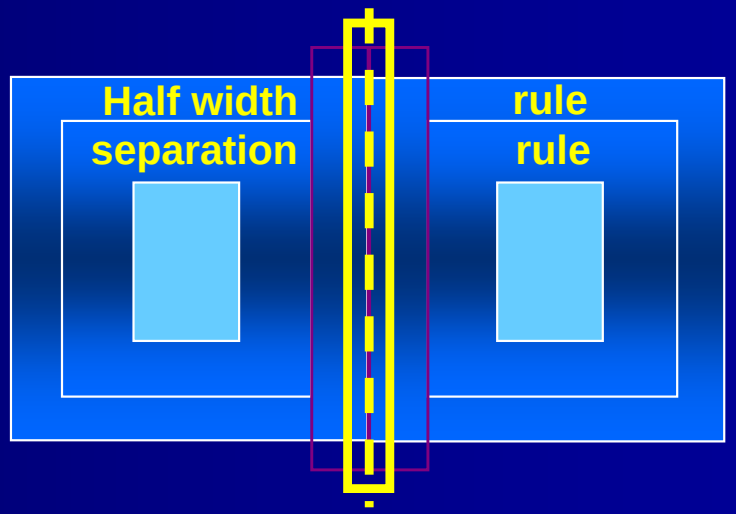
Grids on adjacent Layers don't align



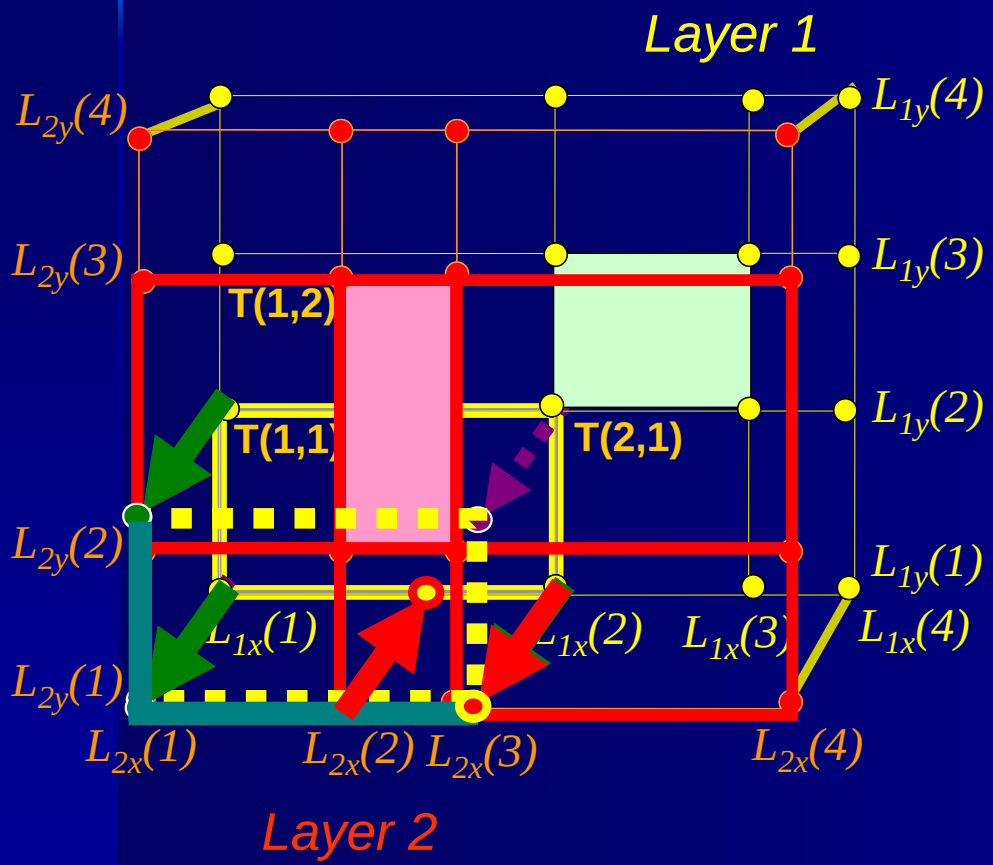


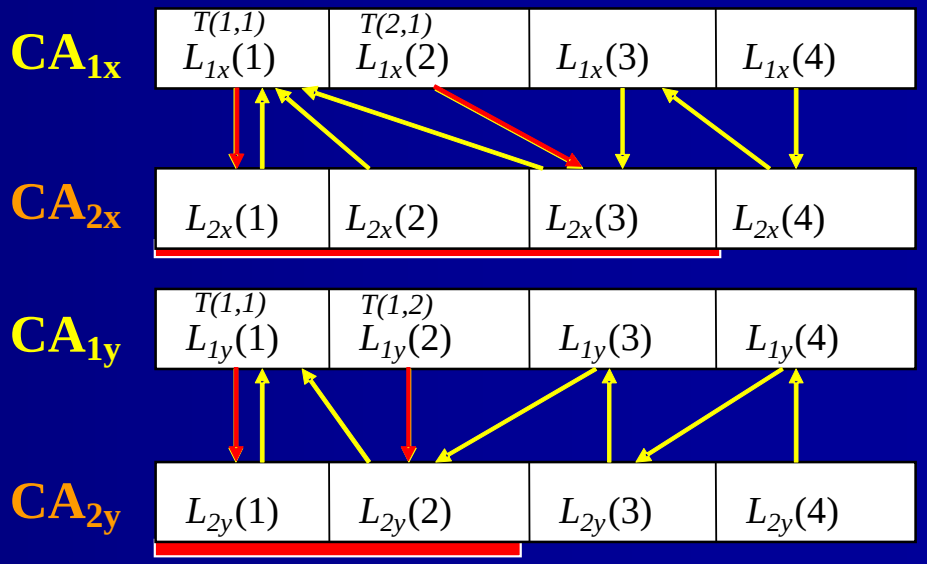
Non-Zero Width Wire Model





Multi-Layer Routing



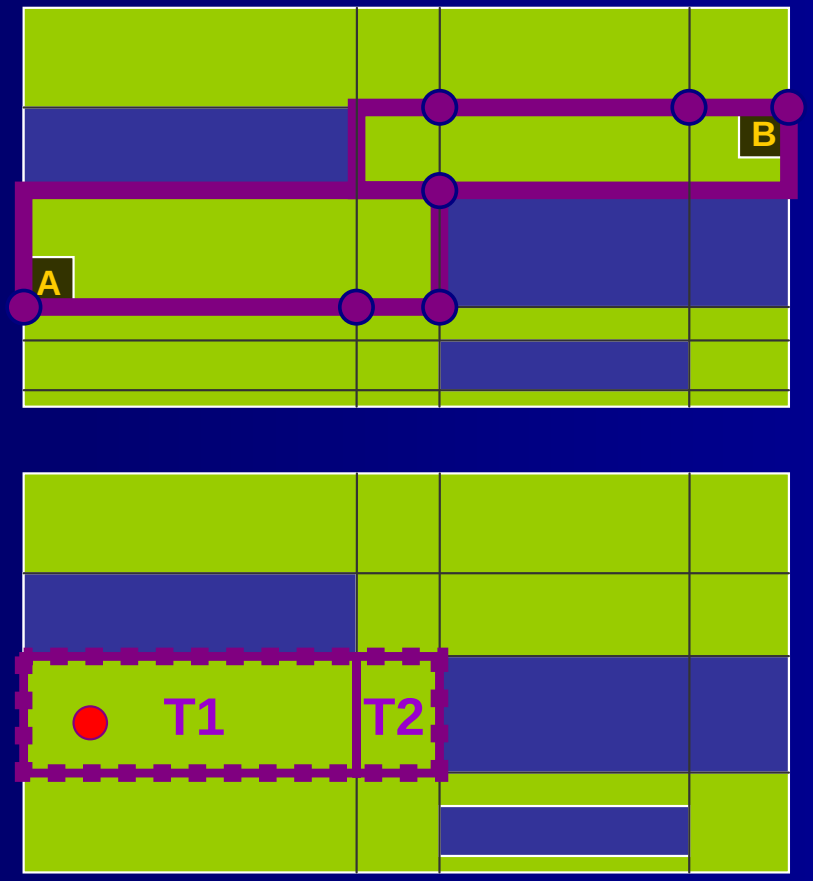


Layer 2: T(1,1), T(2,1), T(3,1)

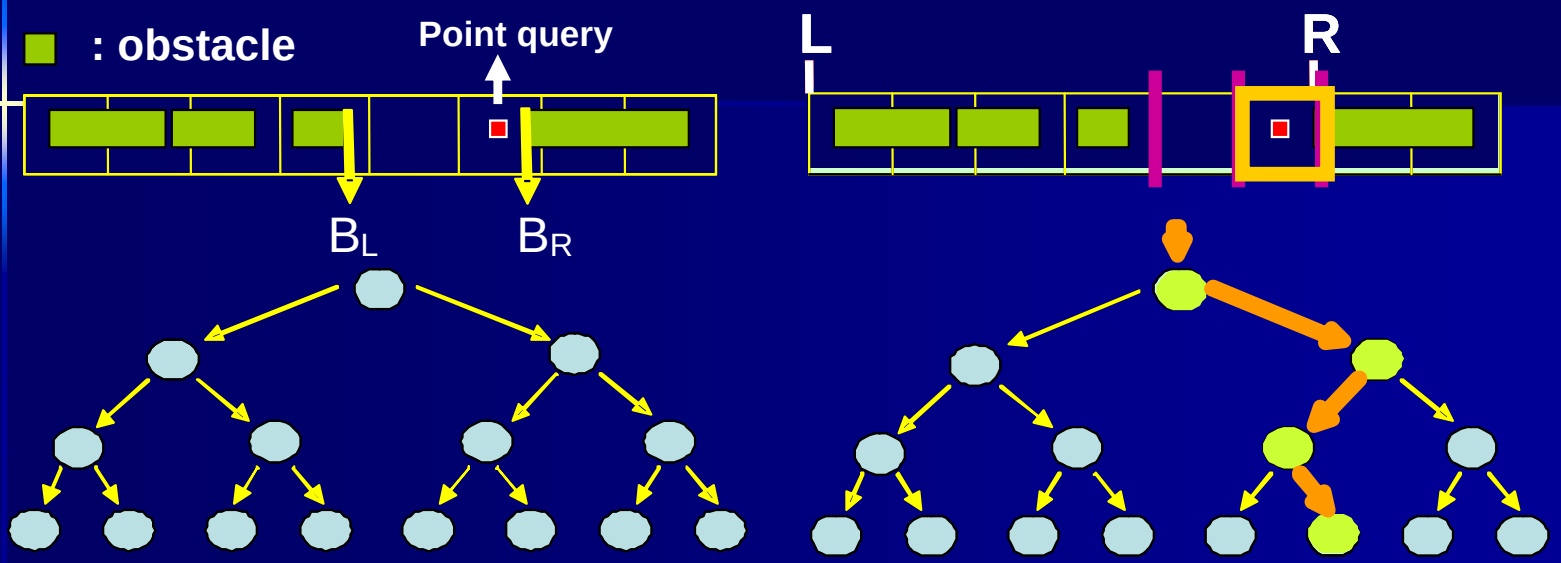
T(1,2), T(2,2), T(3,2)

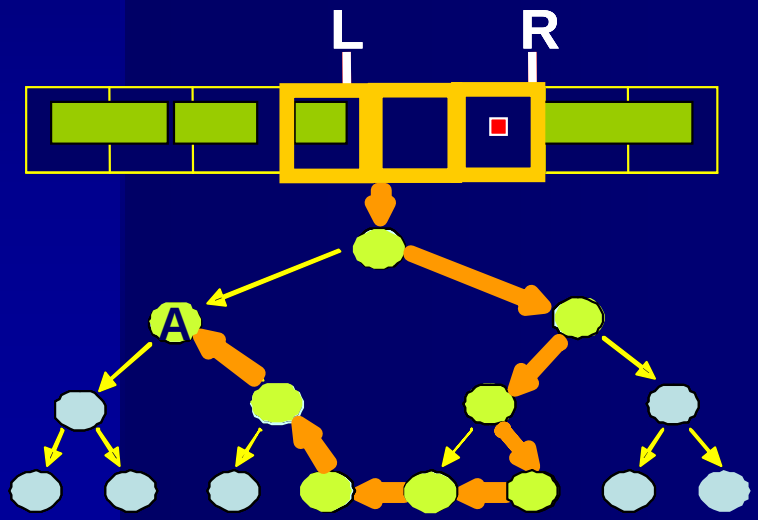
Path Search by PMT

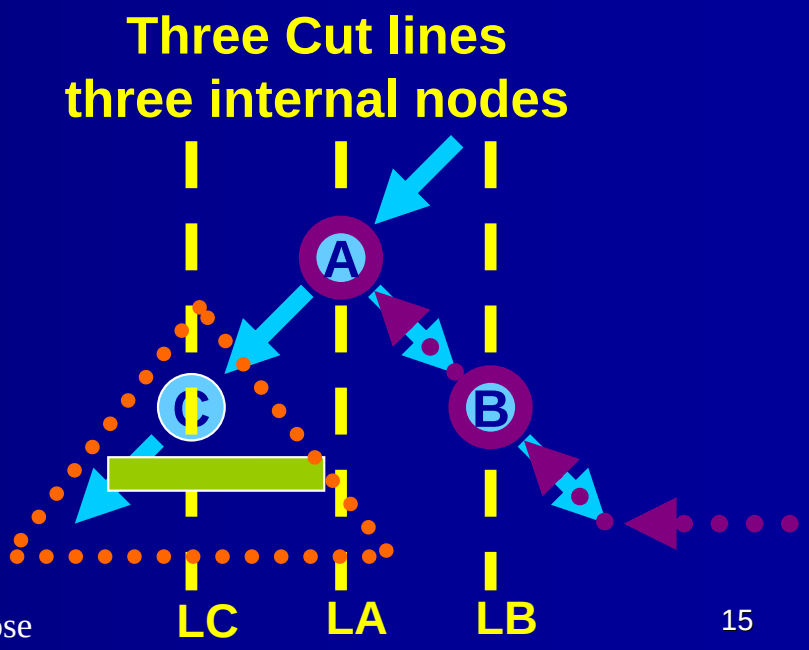
Maximum horizontally stripped



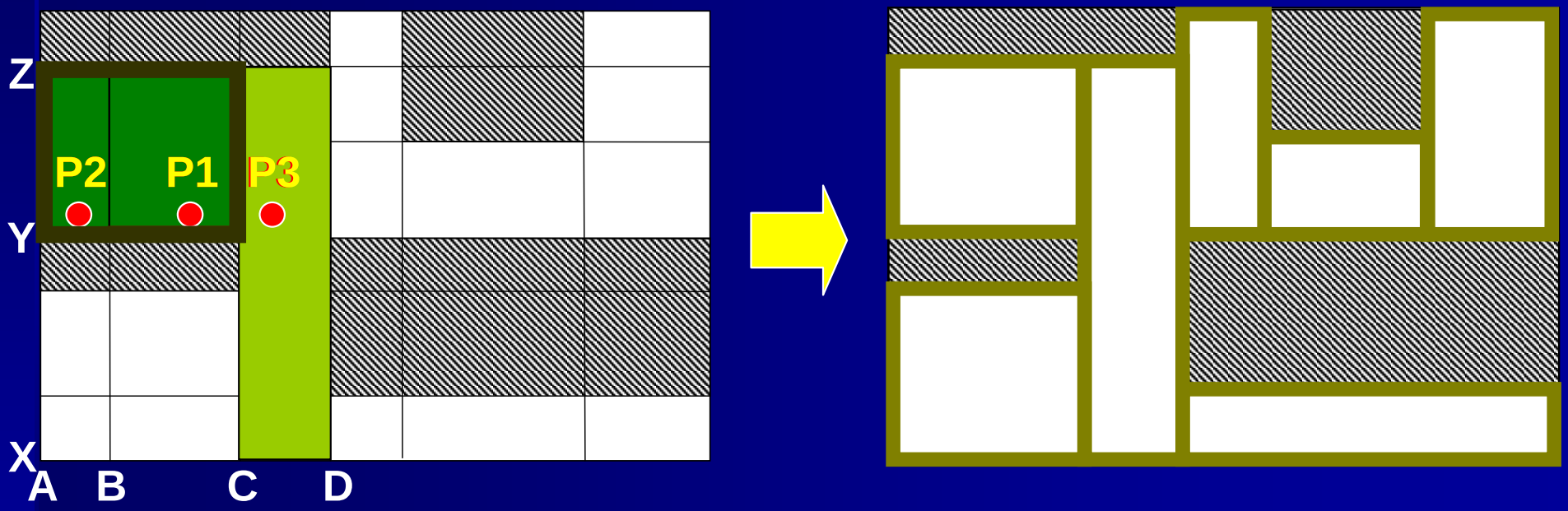
PMT Extraction – Tile Query







PMT Extraction – Merging



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General-purpose Routing

Experimental Results

Conclusion

Routing Flow

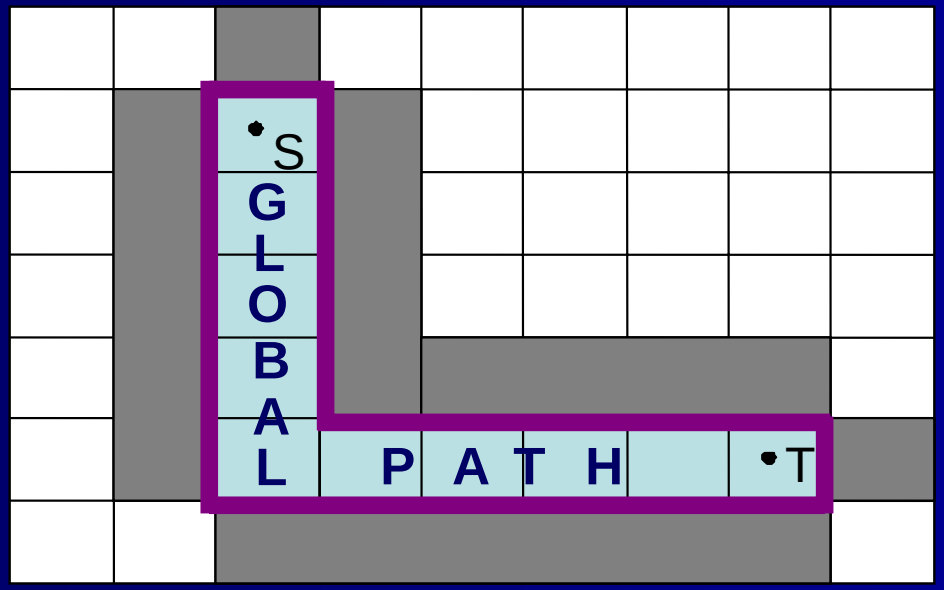
Decompose multi-terminal net routing into multiple 2-pin net routing

Perform congestion-driven global routing

Rip up and Rerouting

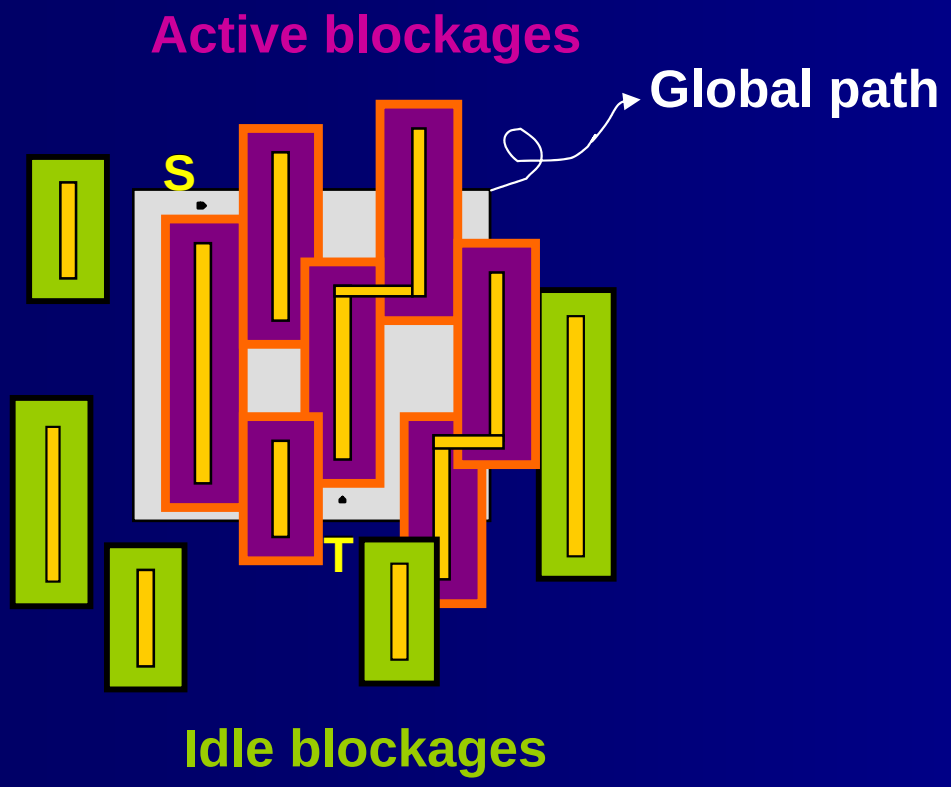
Complete point-to-point detailed routing

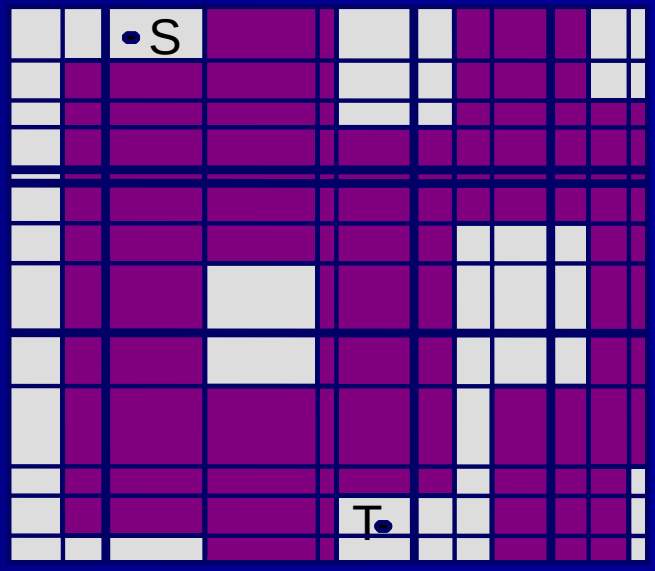
Pseudo Block Insertion



: global path : blockage

Gridline Reduction





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Full-Chip Routing
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Experimental Results – Point-to-point Routing

Table 1. Statistics of the design under the test

Test Case	Rectangles		Chip Dimension x × y (um)
	Met2	Met3	
D1	5,106	3,720	470.00 × 455.00
D2	1,649,866	1,018,221	7320.00 × 7320.00

Table 2. Point-to-point routing results for the circuit D1

	Cong et al. ISPD99			NEMO			
	WL (μm)	#Via	Time (s)	WL (μm)	#Via	Time (s)	SU
TEST1	539.50	10	0.719	539.50	10	0.109	6.6
TEST2	382.20	6	0.515	382.20	6	0.047	10.96
TEST3	419.50	12	0.532	419.50	12	0.063	8.44
TEST4	527.50	8	0.734	527.50	8	0.078	9.41
TEST5	649.00	8	0.922	649.00	8	0.094	9.81

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Experimental Results – Point-to-point Routing

Table 3. Point-to-point routing results for the circuit D2

	Cong et al. ISPD99			NEMO			
	WL (μm)	#Via	Time (s)	WL (μm)	#Via	Time (s)	SU
TEST1	4997.00	238	73	4997.00	238	5	14.6
TEST2	9478.00	366	170	9478.00	366	38	4.47
TEST3	8299.00	246	96	8299.00	246	6	16
TEST4	11794.00	446	127	11794.00	446	11	11.55
TEST5	12391.00	458	166	12375.00	490	25	6.64
TEST6	10212.00	374	109	10212.00	374	8	13.63
TEST7	11538.00	410	134	11538.00	410	11	12.18
TEST8	15413.00	180	329	15413.00	180	72	4.57

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Experimental Results – General-Purpose Routing

Table 4. Statistics of the benchmark circuits for general-purpose routing

Circuit	Size (μm)	#Layers	#Nets	#Pins
S5378	4350 x 2390	3	3124	4818
S9234	4040 x 2250	3	2774	4260
S13207	6600 x 3650	3	6995	10776
S15850	7050 x 3890	3	8321	12793
S38417	11440 x 6190	3	21035	32344
S38584	12950 x 6720	3	28177	42931

Experimental Results – General-Purpose Routing

Table 5. The comparison of routing results among four gridless routers

Circuit	(A) Three-Level Routing Cong et al. TCAD05			(B) Multilevel Routing Cong et al. TCAD05			(C) Multilevel Routing Chen et al. ASP-DAC06			(D) NEMO		
	T/T_n (s)	WL (μm)	# of F.N.	T/T_n (s)	WL (μm)	# of F.N.	T/T_n (s)	WL (μm)	# of F.N.	Time (s)	WL (μm)	# of F.N.
S5378	430/158	-	517	30/11	-	0	5.7/4.8	7.4e4	0	3.7	7.5e4	0
S9234	355/130	-	307	23/8	-	0	4.3/3.6	5.4e4	0	2.7	5.5e4	0
S13207	1099/403	-	877	85/31	-	0	17.9/14.9	1.8e5	0	10.2	1.8e5	0
S15850	1469/539	-	978	107/39	-	0	22.7/18.9	2.2e5	0	15.5	2.2e5	0
S38417	3560/1306	-	1945	251/92	-	0	70.7/58.9	4.7e5	0	55	4.8e5	0
S38584	7086/2599	-	2535	466/171	-	0	209/174.2	6.6e5	0	146.5	6.7e5	0
Comp.	34.4			2.42			1.26	0.989		1	1	

(A) And (B) were run on a 440-MHz Sun Ultra-10 with 384MB memory
(C) was run on a 1 GHz Sun Blade 2000 with 8 GB memory
(D) was run on a 1.2 GHz Sun Blade 2000 with 2 GB memory

Experimental Results – General-Purpose Routing

Table 6. The comparison of routing results between a multi-level grid-based router and NEMO

Circuit	(A) Multilevel Router without antenna avoidance Ho et al. ISPD04				(B) NEMO			
	WL (μm)	#Vias	T/T_n (s)	# of F.N.	WL (μm)	#Vias	Time (s)	# of F.N.
S5378	8.2e4	7163	35/29	0	7.5e4	7045	3.7	0
S9234	6.0e4	6287	26/22	0	5.5e4	5818	2.7	0
S13207	2.2e5	14938	106/88	0	1.8e5	14865	10.2	0
S15850	2.4e5	17334	538/448	0	2.2e5	17260	15.5	0
S38417	5.9e5	43551	899/749	0	4.8e5	43193	55	0
S38584	7.7e5	61053	1953/1628	0	6.7e5	60180	146.5	0

(B) was run on a 1GHz Sun Blade 2000 with 1 GB memory

Conclusions

- We propose a new implicit connection graph-based router with
  - Efficient PMT extraction,
  - PMT propagation, and
  - Simplified connection graph

THANK YOU VERY MUCH