An Introduction to Electromigration-Aware Physical Design

Jens Lienig

Dresden University of Technology

Dresden, Germany

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Electromigration (EM):

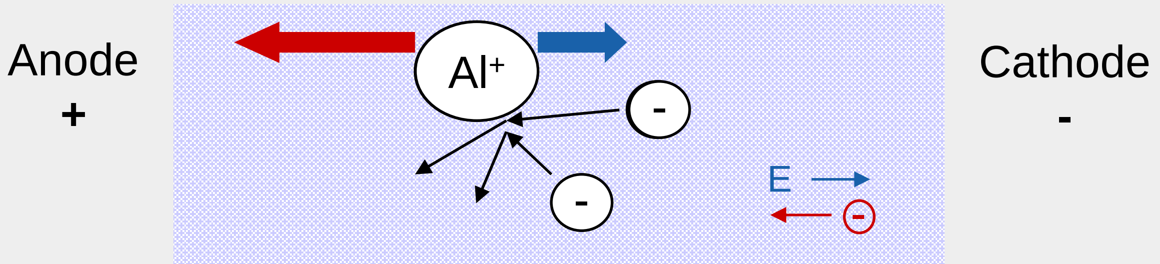
Electromigration is the forced movement of metal ions due to an electric field

$F_{total} = F_{direct} + F_{wind}$

Direct action of electric field on metal ions

<<

Force on metal ions resulting from momentum transfer from the conduction electrons



Note: For simplicity, the term “electron wind force” often refers to the net effect of these two electrical forces

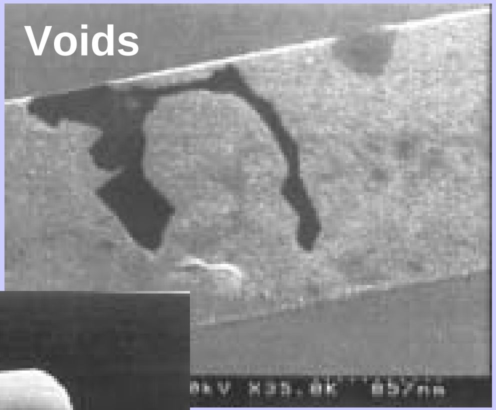
Introduction: Electromigration

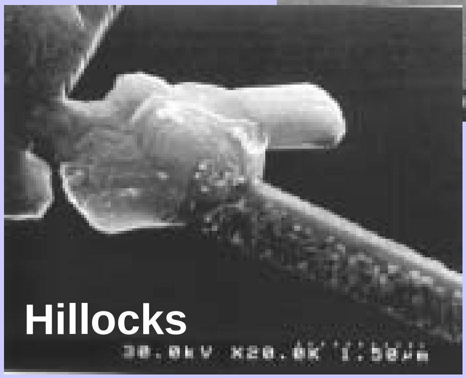
=> Metal atoms (ions) travel toward the positive end of the conductor while vacancies move toward the negative end

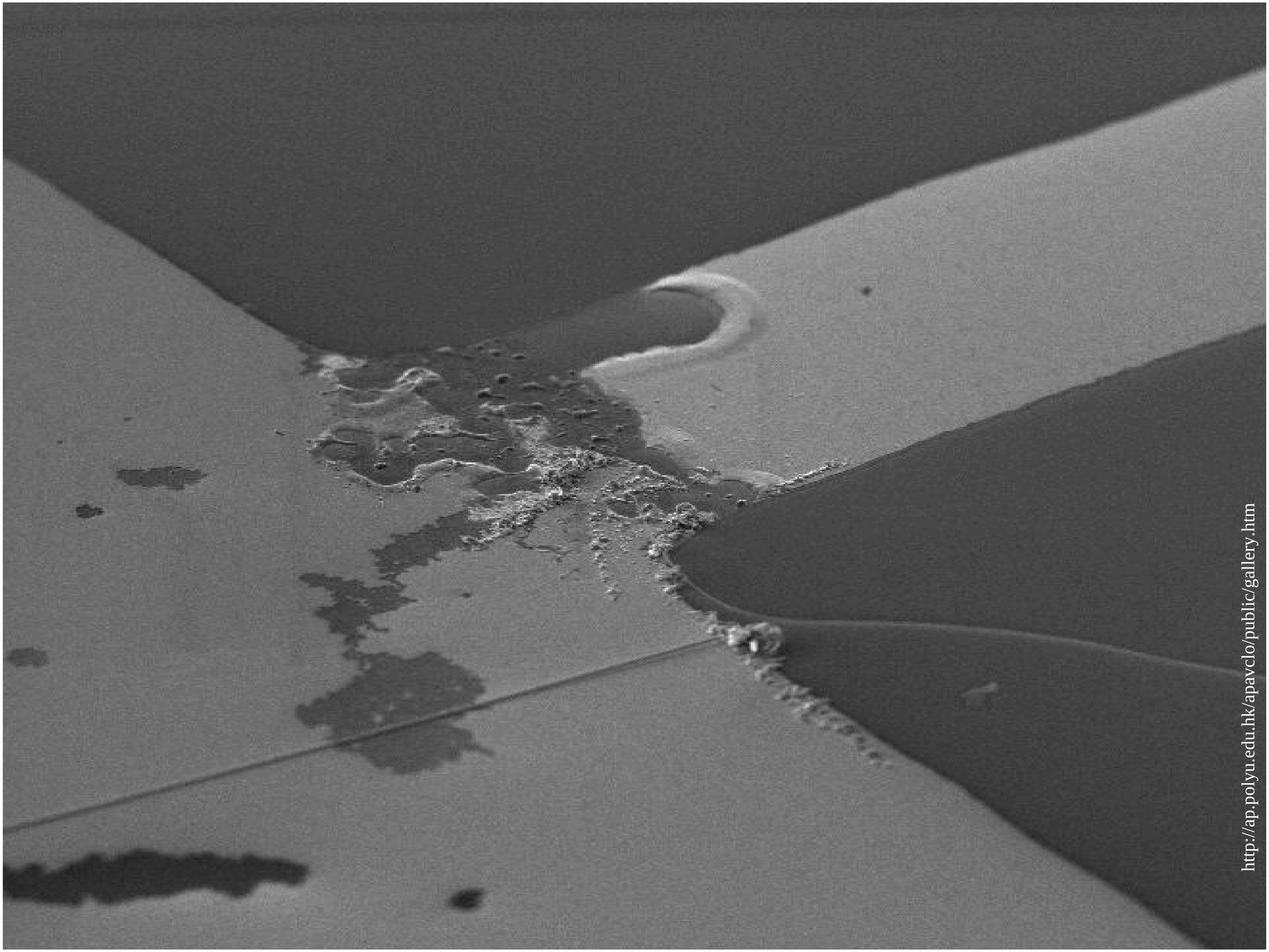
Effects of electromigration in metal interconnects:

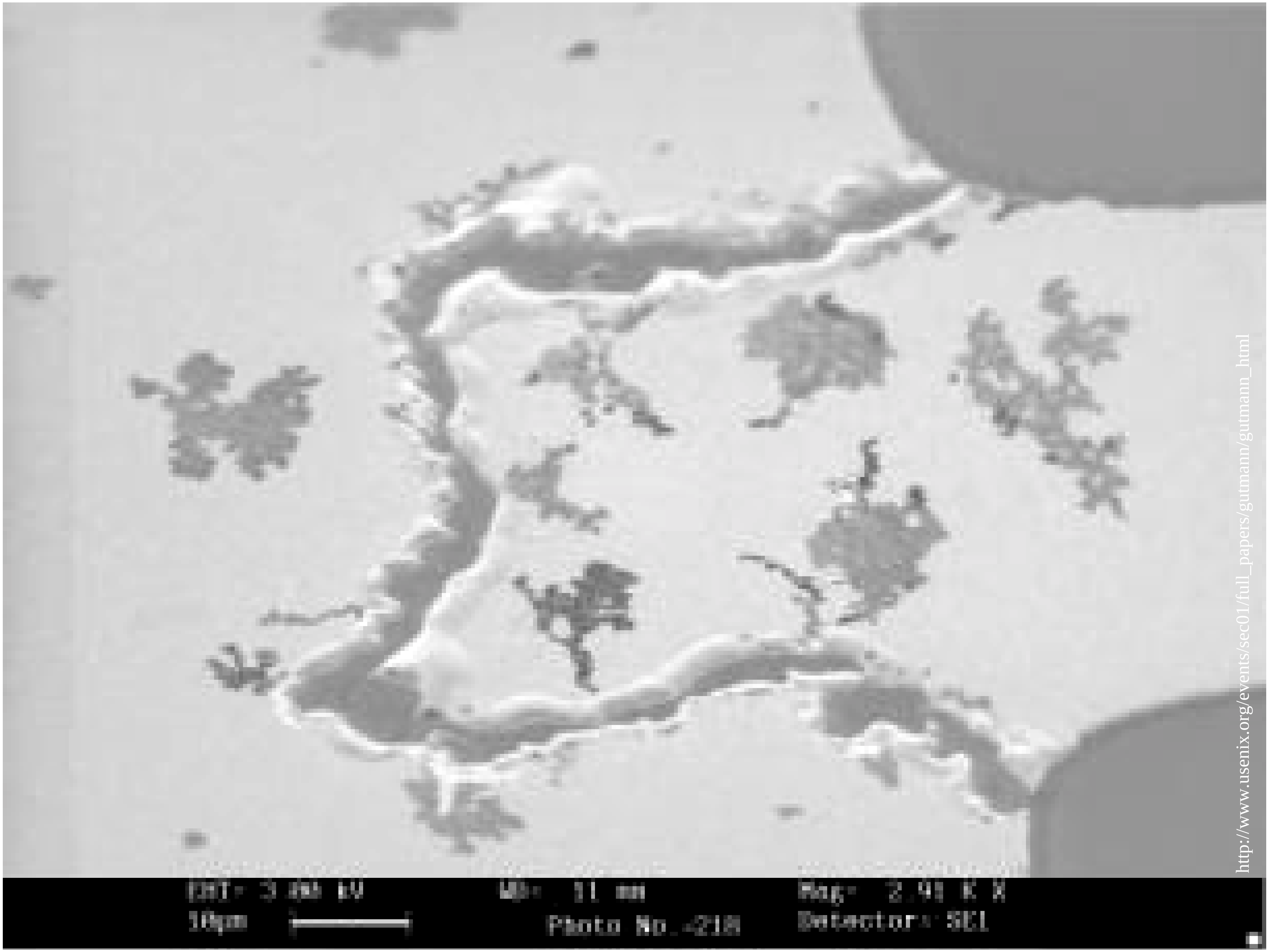
- Depletion of atoms (Voids):
  $\rightarrow$ Slow reduction of connectivity
  $\rightarrow$ Interconnect failure

- Deposition of atoms (Hillocks, Whisker):
  $\rightarrow$ Short cuts






http://ap.polyu.edu.hk/apavclo/public/gallery.htm



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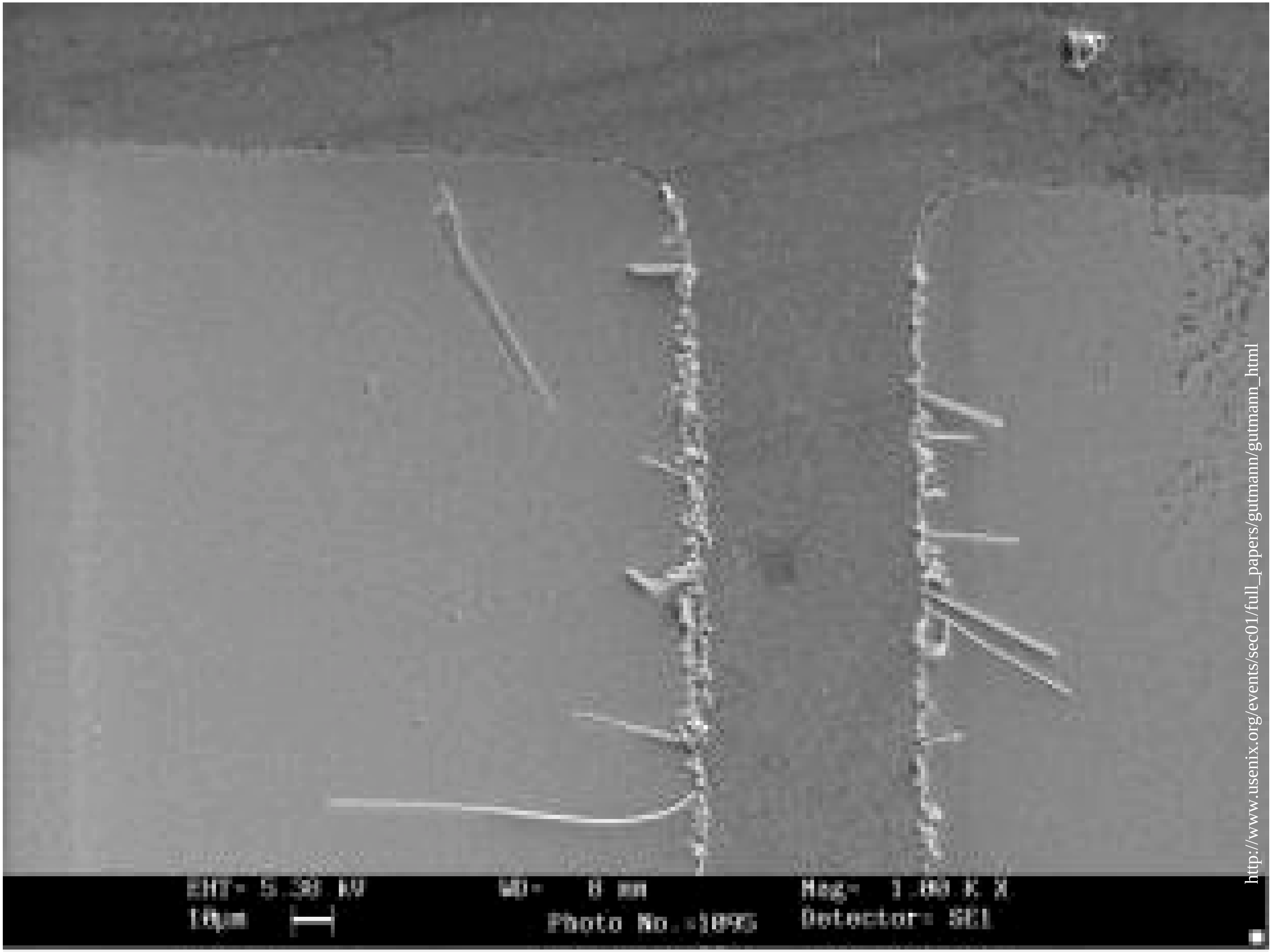
EHT= 5.30 kV
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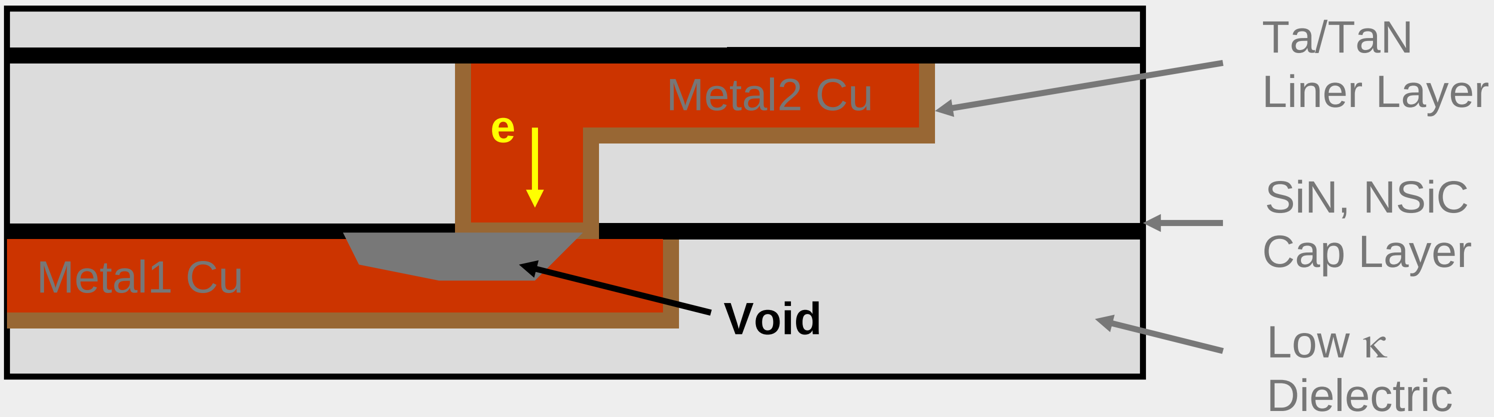
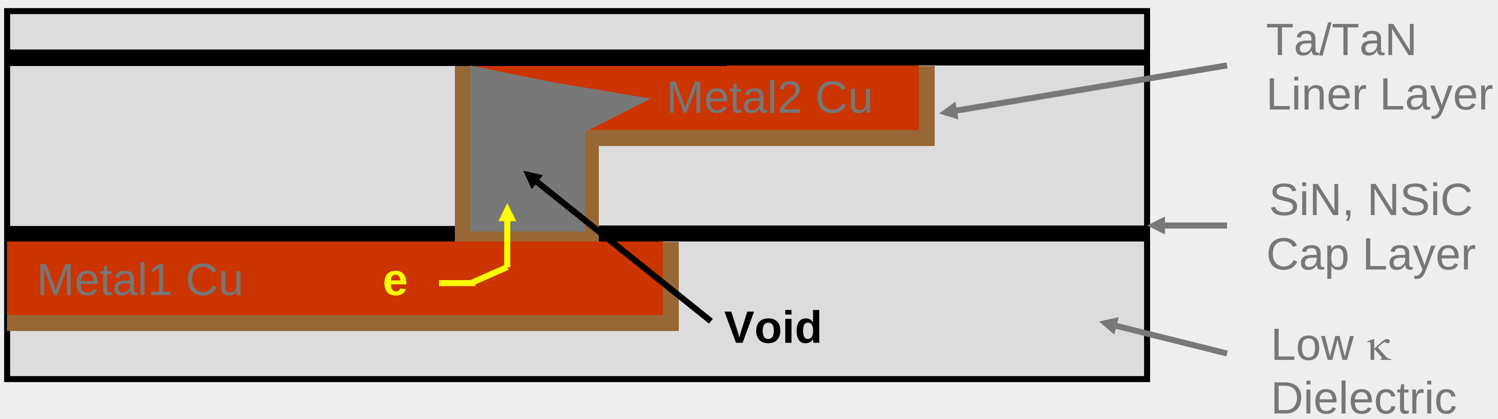
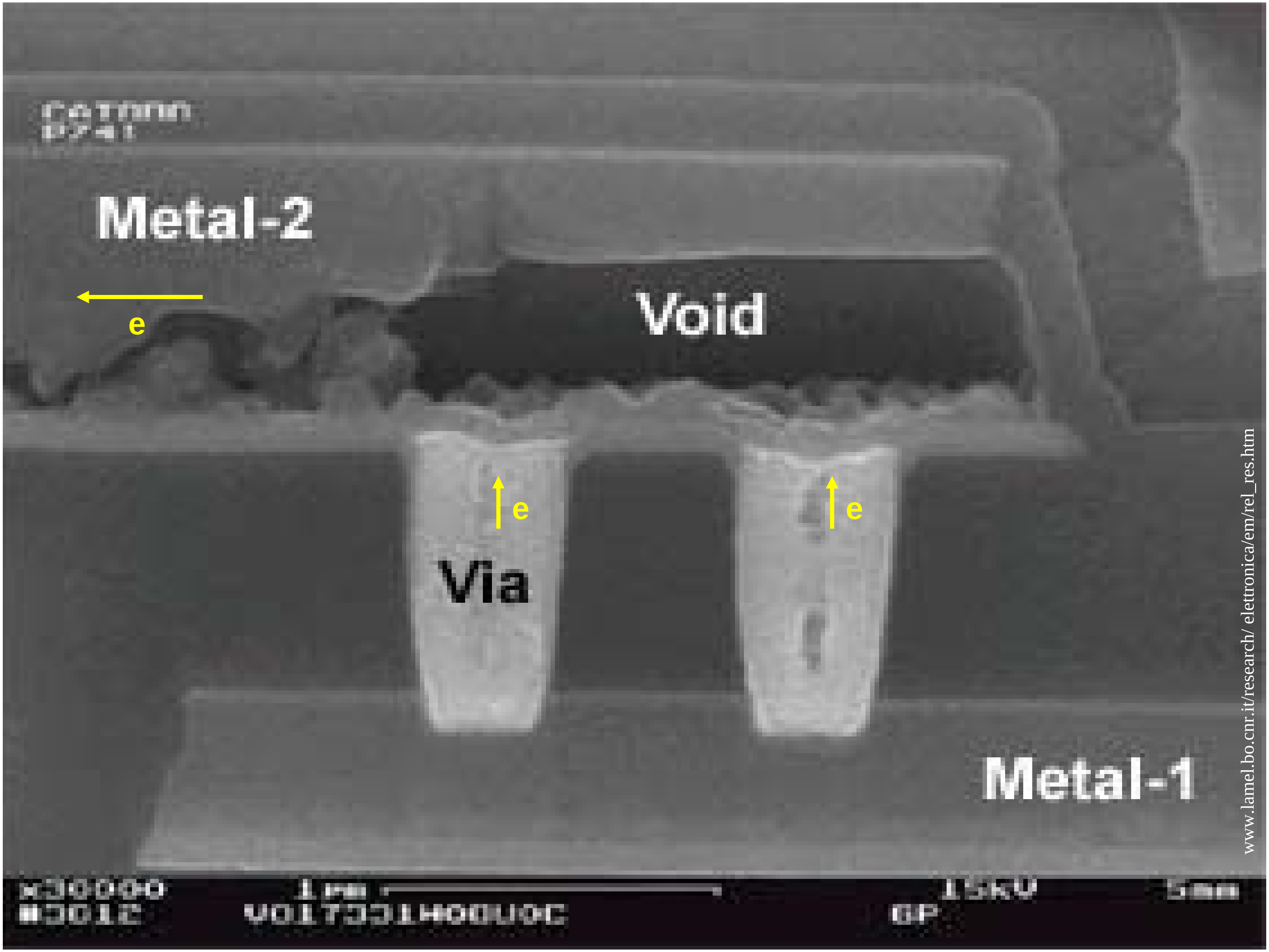
Common Failure Mechanisms in Integrated Circuits

A) Line Depletion



B) Via Depletion

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www.lamel.bo.cnr.it/research/ elettronica/em/rel_res.htm

Electromigration and Current Density

Black‘s Equation [1]:
Mean time to failure of a single wire due to electromigration

Cross-section-area-dependent constant

Activation energy for electromigration

$$MTTF = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{k \cdot T}\right)$$

Temperature

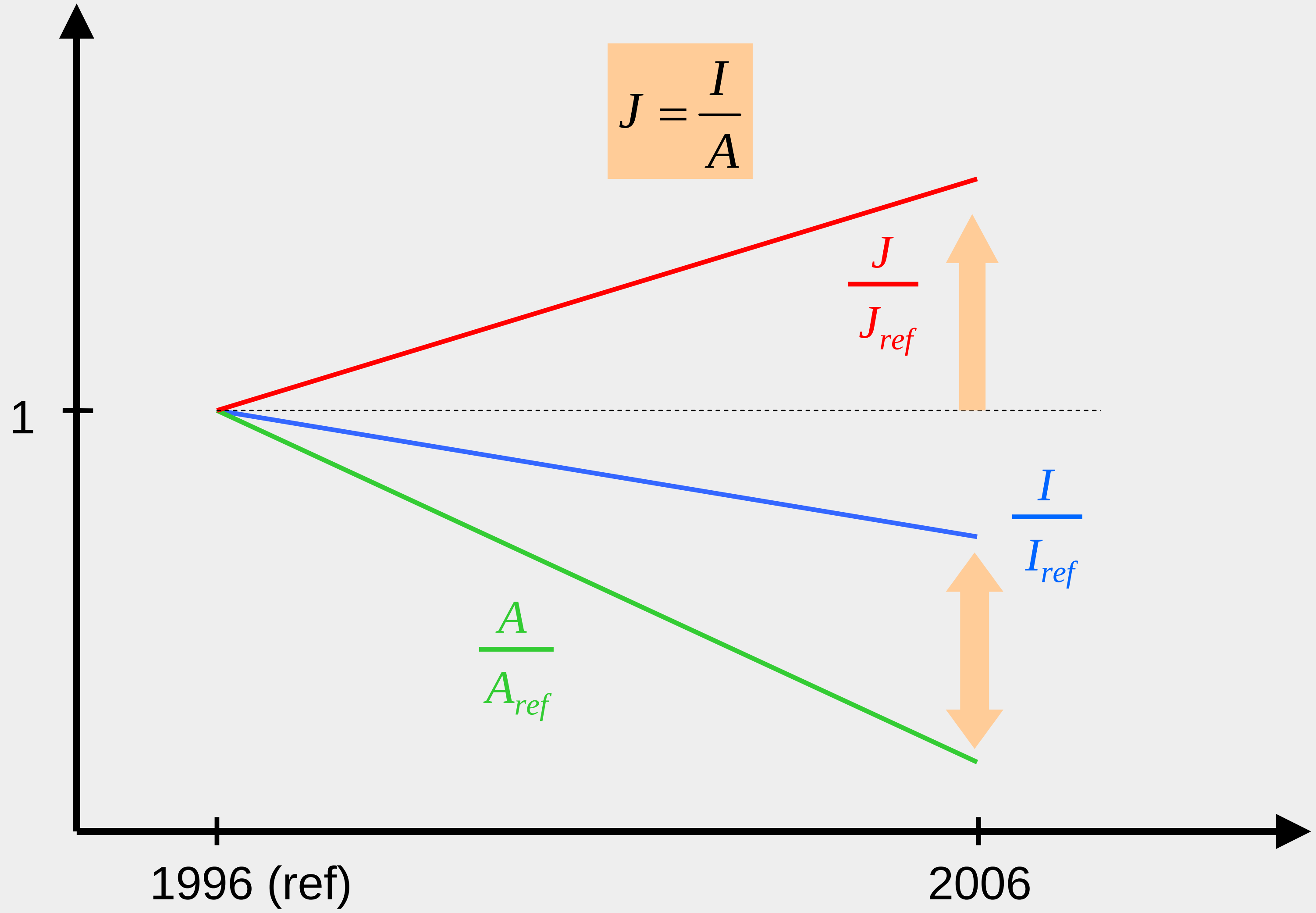
Current density

Scaling factor (usually set to 2)

Boltzmann constant

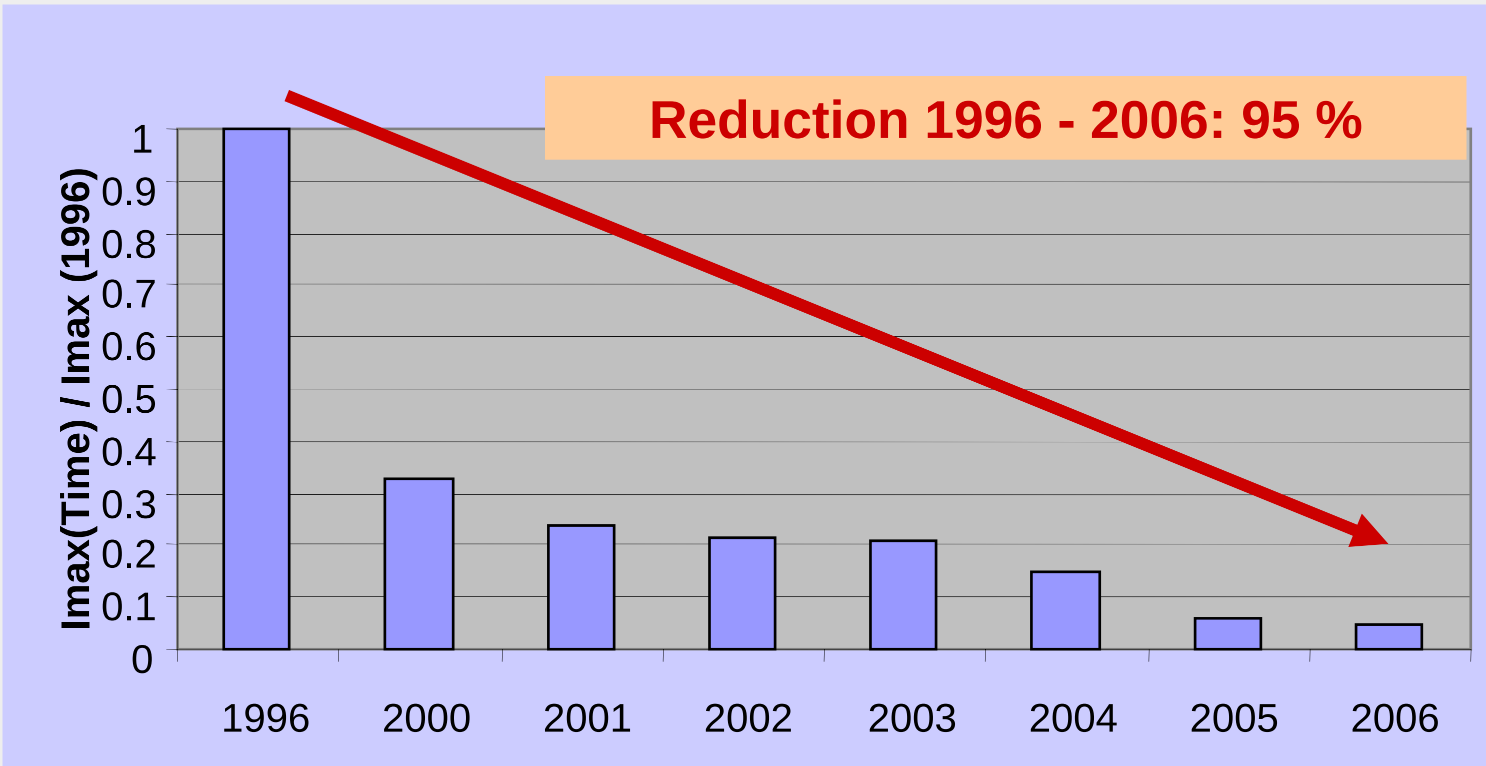
-> Current density is the major parameter in addressing electromigration during physical design

Why is Electromigration Becoming a Problem?



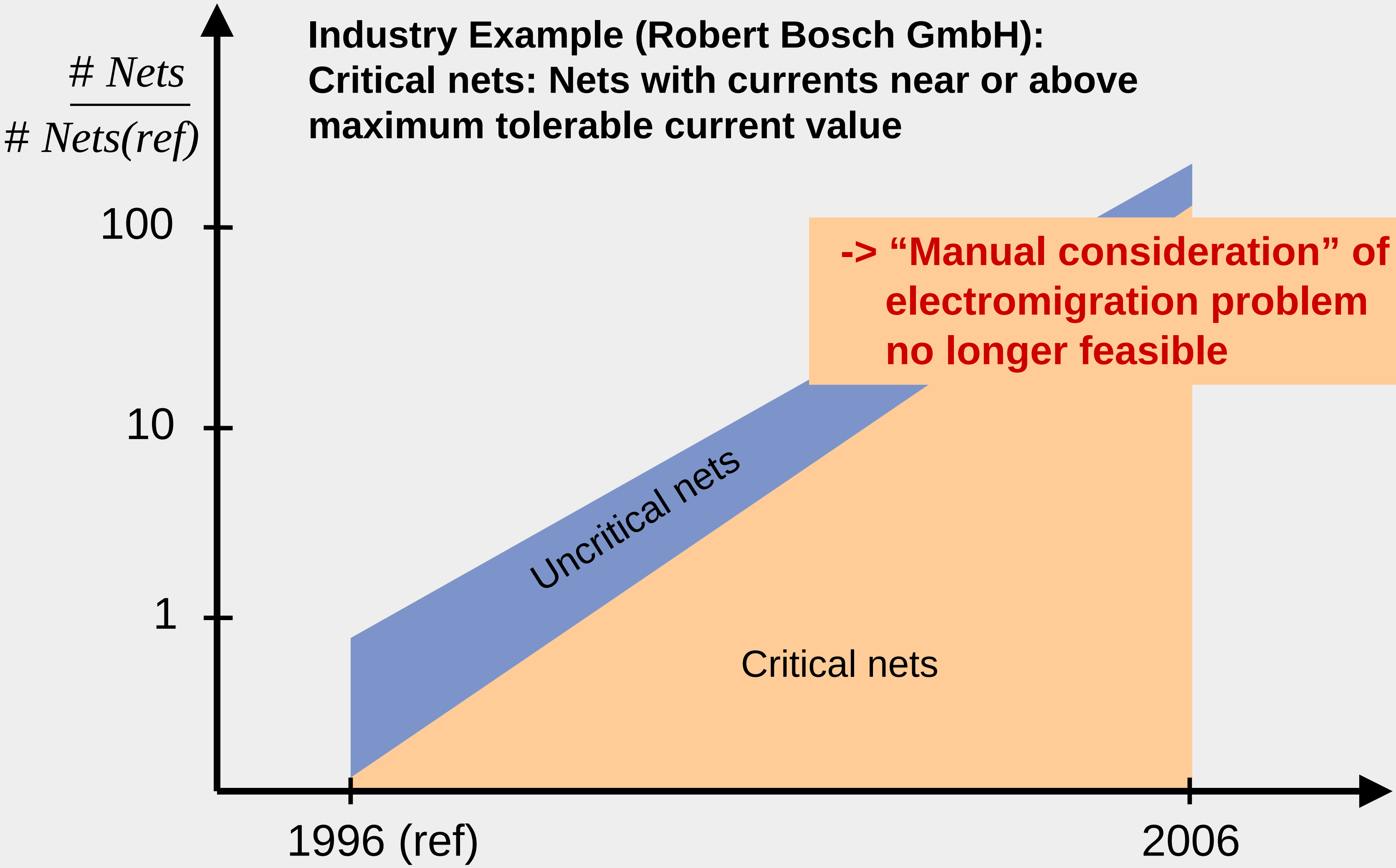
Why is Electromigration Becoming a Problem? (cont'd.)

Industry Example (Robert Bosch GmbH):
Maximum tolerable current in minimum line width interconnect (Metal1, Al) due to technology scaling



Why is Electromigration Becoming a Problem? (cont'd.)

Industry Example (Robert Bosch GmbH):
Critical nets: Nets with currents near or above maximum tolerable current value



-> "Manual consideration" of electromigration problem no longer feasible

Maximum Tolerable Current Densities

- Conventional metal wires (house wiring, etc.)

  Al $\approx$ 19,100 A/cm^2
  Cu $\approx$ 30,400 A/cm^2

  … reaching melting temperature due to Joule heating

Melting temperature limits maximum current densities

- Thin film interconnect on integrated circuits can sustain current densities up to 10^{10} A/cm^2 before reaching melting temperature

  Al $\approx$ 200,000 A/cm^2
  Cu ($J_{max}(Cu) \approx 5^* J_{max}(Al)$) $\approx$ 1,000,000 A/cm^2

  … it reaches its maximum value due to the occurance of electromigration

Electromigration limits maximum current densities

Contents

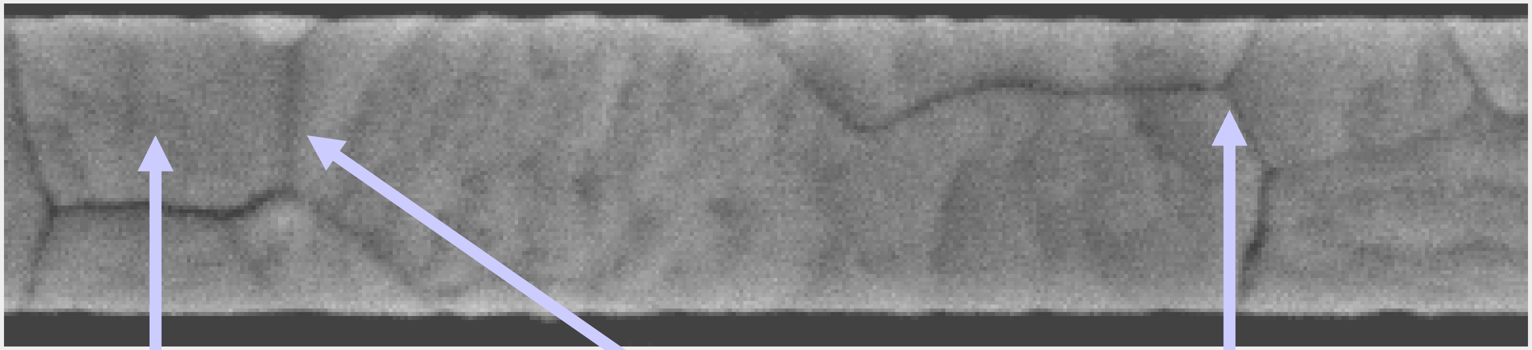
History of Electromigration Research

- 1861 Discovery of electromigration by M. Gerardin
- 1950s First systematic studies of electromigration by W. Seith and H. Wever (Correlation between the direction of the current flow and the material transport)
- 1960s Electromigration is recognized as one of the main reasons for IC failure
- 1967 J. R. Black: Relationship between MTTF (mean time to failure) and current density and temperature (Blacks law [1])
- 1975 I. A. Blech: Discovery of „immortal wires“ by considering the product of current density and wire length (Blech length [2])

Migration in Solid State Materials

- **Stress Migration**
  due to
  mechanical stress
- **Electromigration**
  due to
  electric field
  - Electrolytic electromigration
  - Solid state electromigration
- **Thermomigration**
  due to
  thermal gradient

Diffusion Processes and Activation Energies E_A

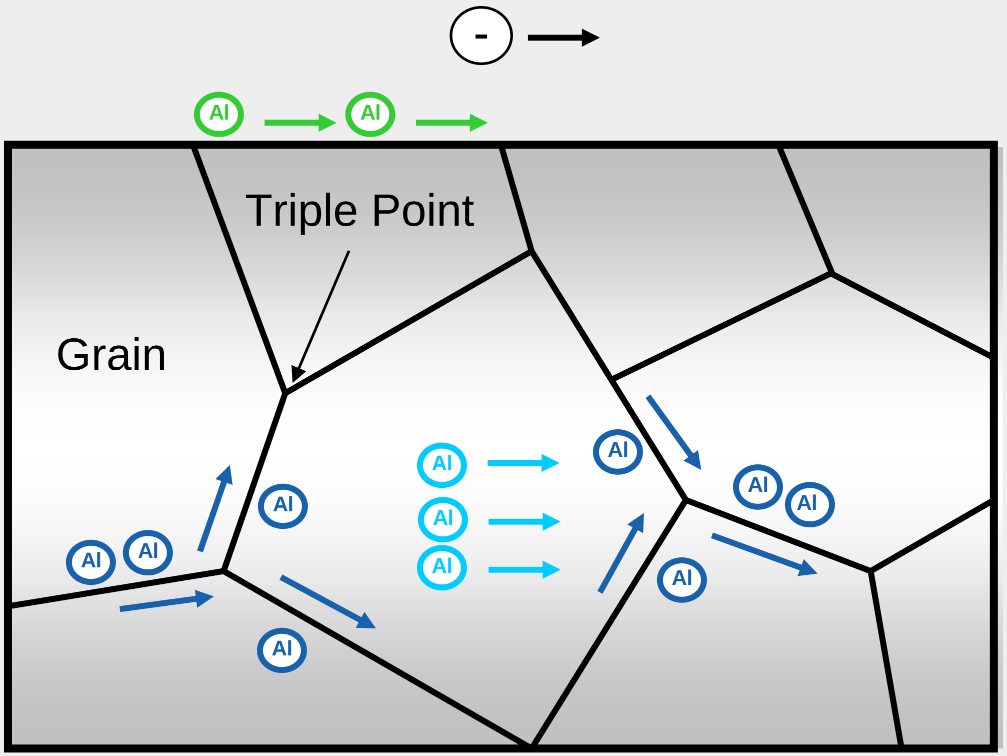


Grain: homogeneous lattice of metal atoms

Grain boundary: shift in the orientation of the lattice

Triple Point

Diffusion Processes and Activation Energies E_A



Grain Boundary Diffusion

E_{A_GRAIN}= 0.7 eV (Al)

E_{A_GRAIN}= 1.2 eV (Cu)

Bulk Diffusion

E_{A_BULK}= 1.2 eV (Al)

E_{A_BULK}= 2.3 eV (Cu)

Surface Diffusion

$E_{A\_SURF.}$= 0.8 eV (Al)

$E_{A\_SURF.}$= 0.8 eV (Cu)

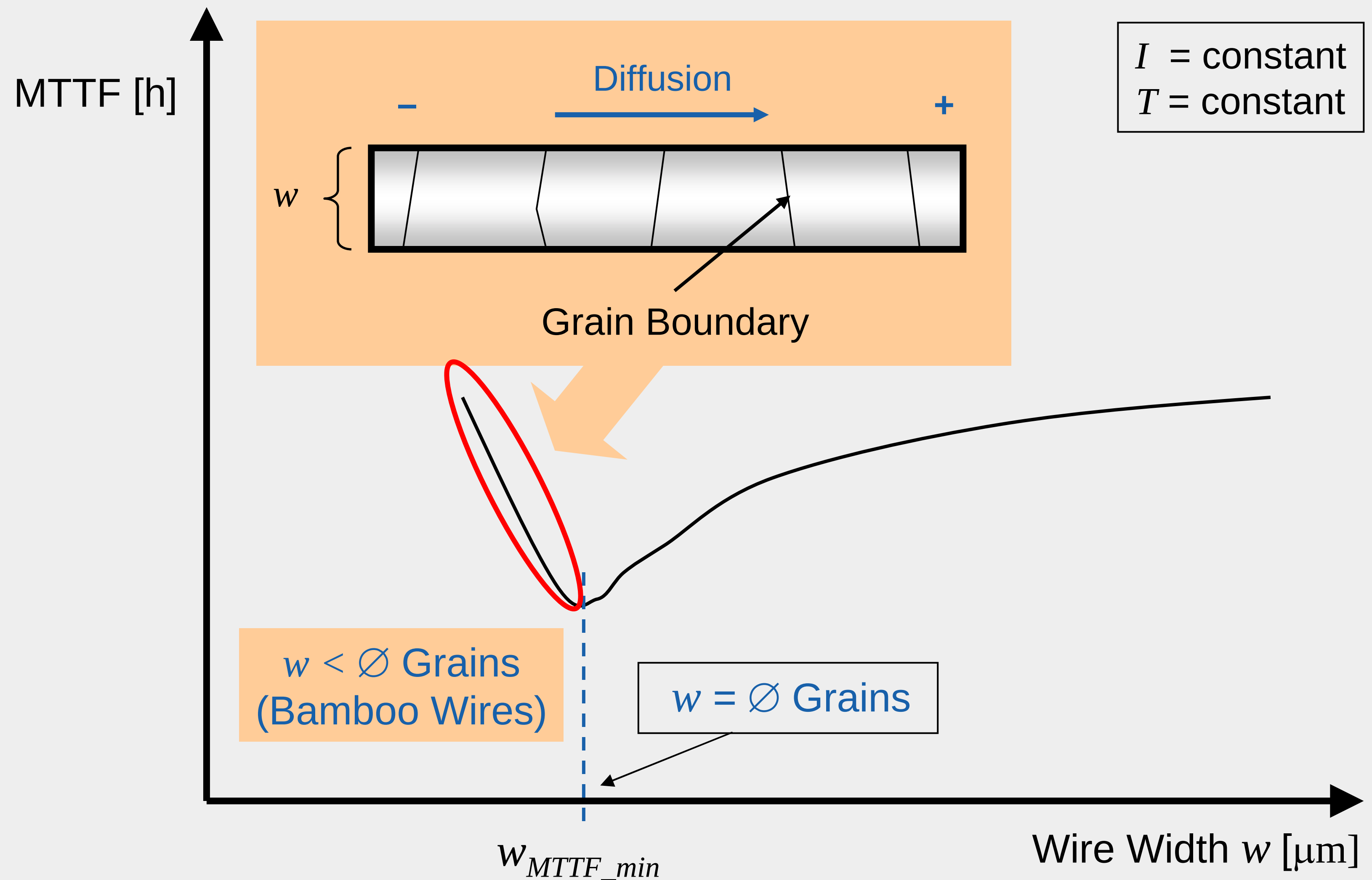
Aluminum:

Grain Boundary Diffusion
+ Surface Diffusion

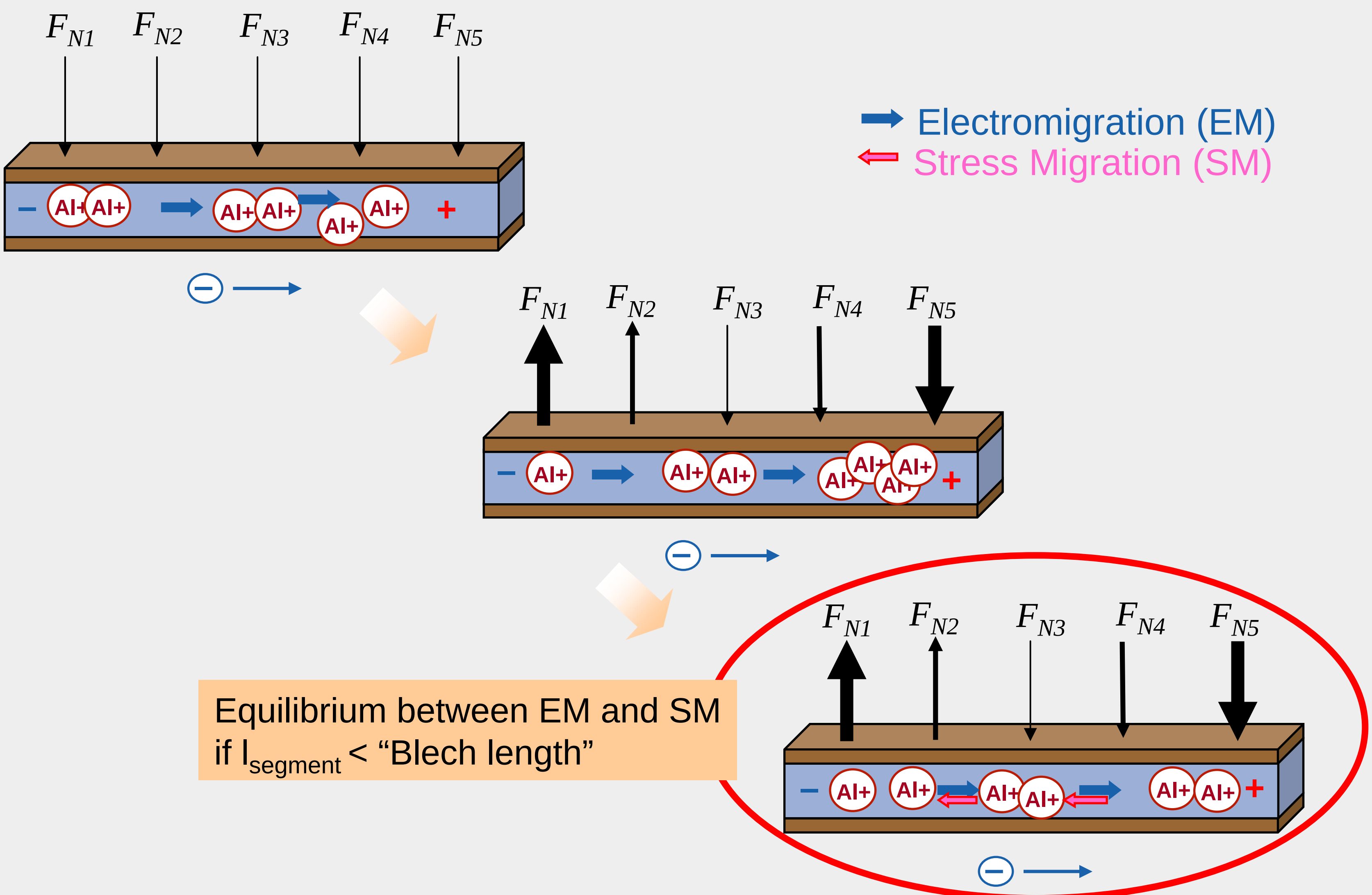
Copper:

Surface Diffusion

Special Effects (1): Bamboo Wires



Special Effects (2): Immortal Wires



Equilibrium between EM and SM if $l_{segment}$ < "Blech length"

Maximum Current Density With Regard to Temperature

Black‘s Equation [1]:
Mean time to failure of a single wire due to electromigration

Cross-section-area-dependent constant

Activation energy

$$MTTF = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{k \cdot T}\right)$$

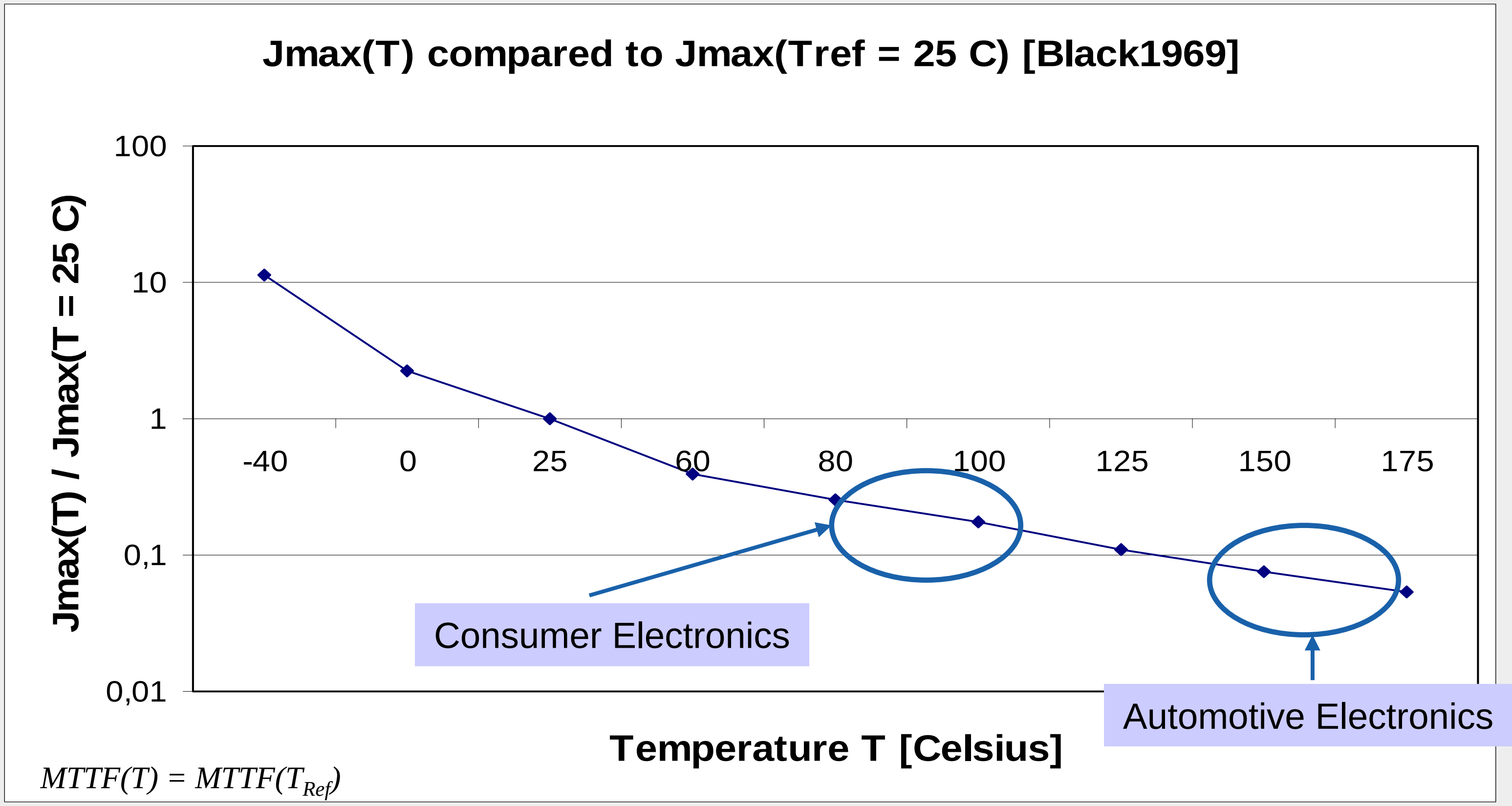
Temperature

Current density

Scaling factor (usually set to 2)

Boltzmann constant

Maximum Current Density With Regard to Temperature



Example: A temperature rise of 100 K in an Al metallization reduces the permissible current density by about 90 %.

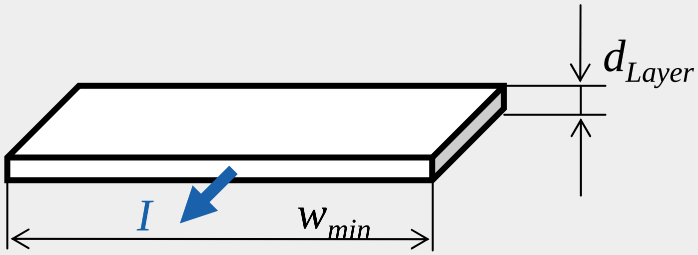
Contents

Which Physical Design Parameters Effect Electromigration?

- Local current density
  - ➢ **Wire widths and via sizes (number of vias)**
- Homogeneity of the current flow
  - ➢ **Wire shapes, corner bends, via arrangements, etc.**
- Current distribution within device pins
  - ➢ **Current-density-correct pin connections**
- Temperature-dependency of the maximum current density
  - ➢ **Temperature of the chip/interconnect**
- Immortal wires
  - ➢ **Segment length below Blech length**

(a) Wire Widths

Minimal wire width w_{min}:



$$w_{min} = \max \begin{cases} \dfrac{I_{RMS/AVG} \cdot f(w)}{d_{Layer} \cdot J_{max}(T_{ref}) \cdot f(T)} \\[2ex] \dfrac{I_{peak} \cdot f(w)}{d_{Layer} \cdot J_{peak}(T_{ref}) \cdot f(T)} \\[2ex] w_{min\_process} \end{cases}$$

$J_{max/peak}$	Layer- and current-type dependent maximum permissible current density at reference temperature T_{ref}
$I_{RMS/AVG}$ I_{peak}	Current (rms, avg, peak)
T	Working temperature
T_{ref}	Reference temperature
$f(w)$	Grain-size-dependent width scaling factor
$w_{min\_process}$	Process-dependent minimum wire width
n	Scaling factor (n = 2 [1])
E_A	Activation energy
k	Boltzmann constant

Temperature scaling $f(T)$, if $T \neq T_{ref}$:

$$f(T) = \exp\left(-\frac{E_A}{n \cdot k \cdot T_{ref}} \left(1 - \frac{T_{ref}}{T} \right) \right)$$

Black‘s law with $MTTF(T) = MTTF(T_{ref})$

(a) Via Sizes

Minimal number of single vias N_{min} per via array:

$$N_{min} = \max \begin{cases} \mathrm{ceil}\left(\dfrac{I_{RMS/AVG} \cdot s}{I_{max\_via}(T_{ref}) \cdot f(T)} \right) \\ \mathrm{ceil}\left(\dfrac{I_{peak} \cdot s}{I_{peak\_via}(T_{ref}) \cdot f(T)} \right) \end{cases}$$

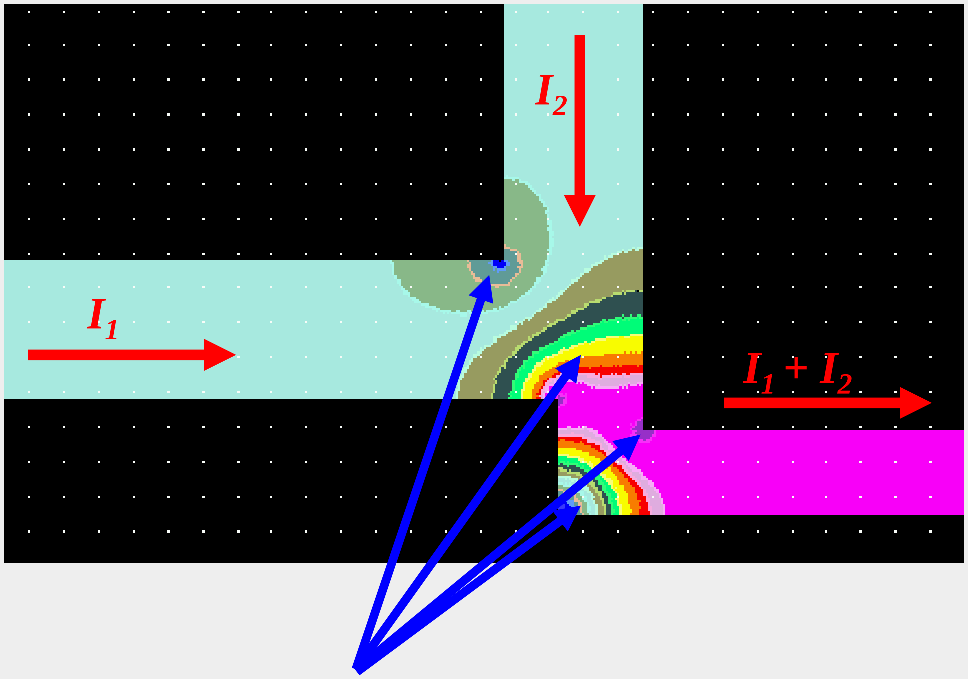
I_{max_via}, I_{peak_via}	Maximum permissible via current at reference temperature T_{ref}
$I_{RMS/AVG}$ I_{peak}	Via current (rms, avg, peak)
s	Safety factor (1.1 … 1.2)
T	Working temperature
T_{ref}	Reference temperature
n	Scaling factor (n = 2 [1])
E_A	Activation energy
k	Boltzmann constant

Temperature scaling $f(T)$, if $T \neq T_{ref}$:

$$f(T) = \exp\left(-\frac{E_A}{n \cdot k \cdot T_{ref}} \left(1 - \frac{T_{ref}}{T} \right) \right)$$

Black‘s law with $MTTF(T) = MTTF(T_{ref})$

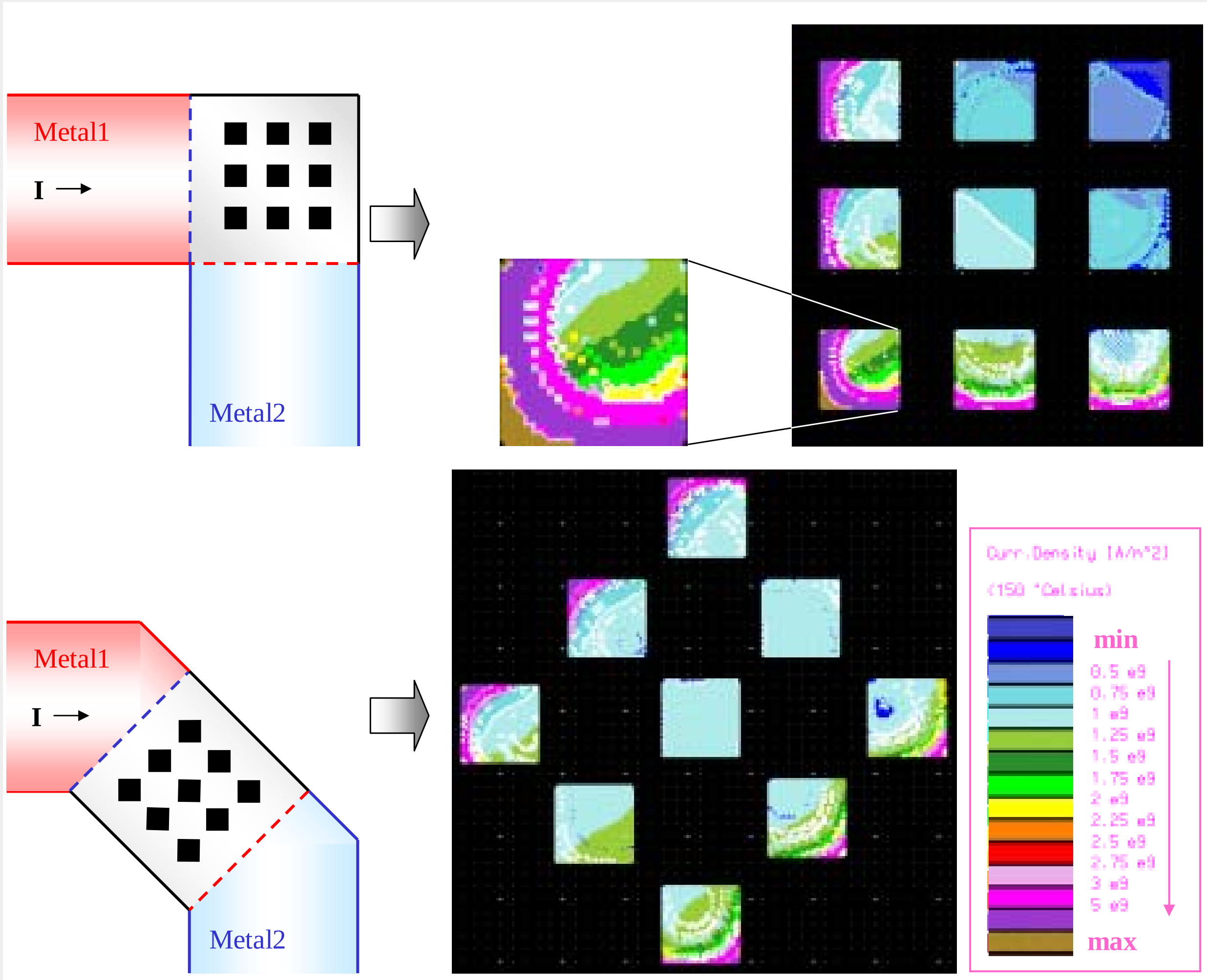
(b) Homogeneity of the Current Flow: Wire Shapes, Corner Bends



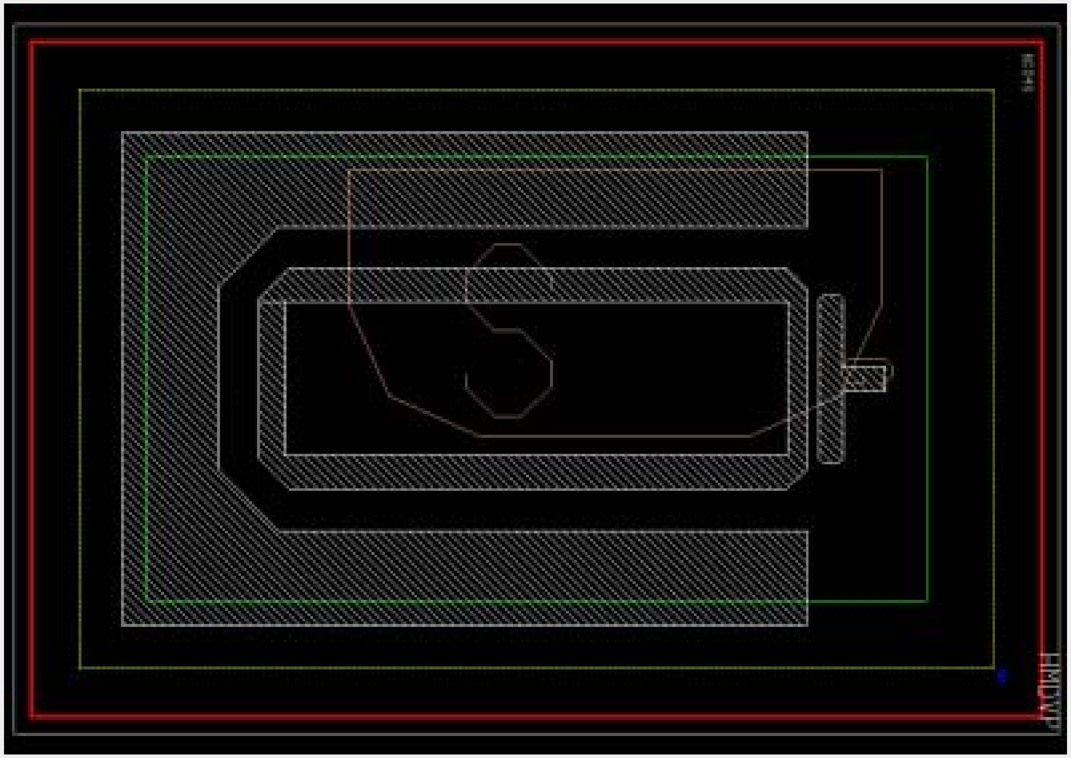
Inhomogeneous current flow

-> Avoiding of 90-degree corners, rapid width changes, etc.

(b) Homogeneity of the Current Flow: Via Arrangements

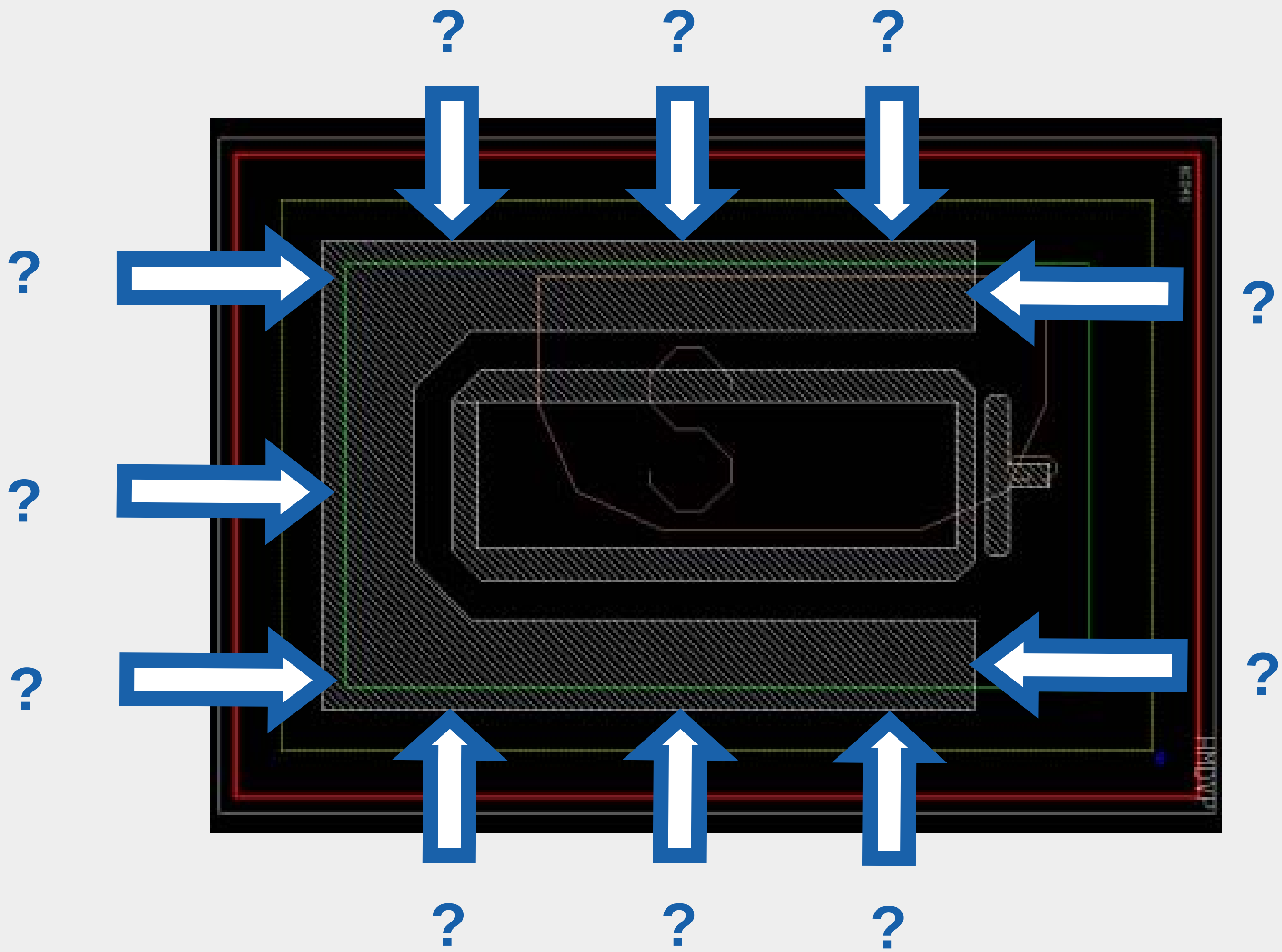


(c) Current-Density-Correct Pin Connections

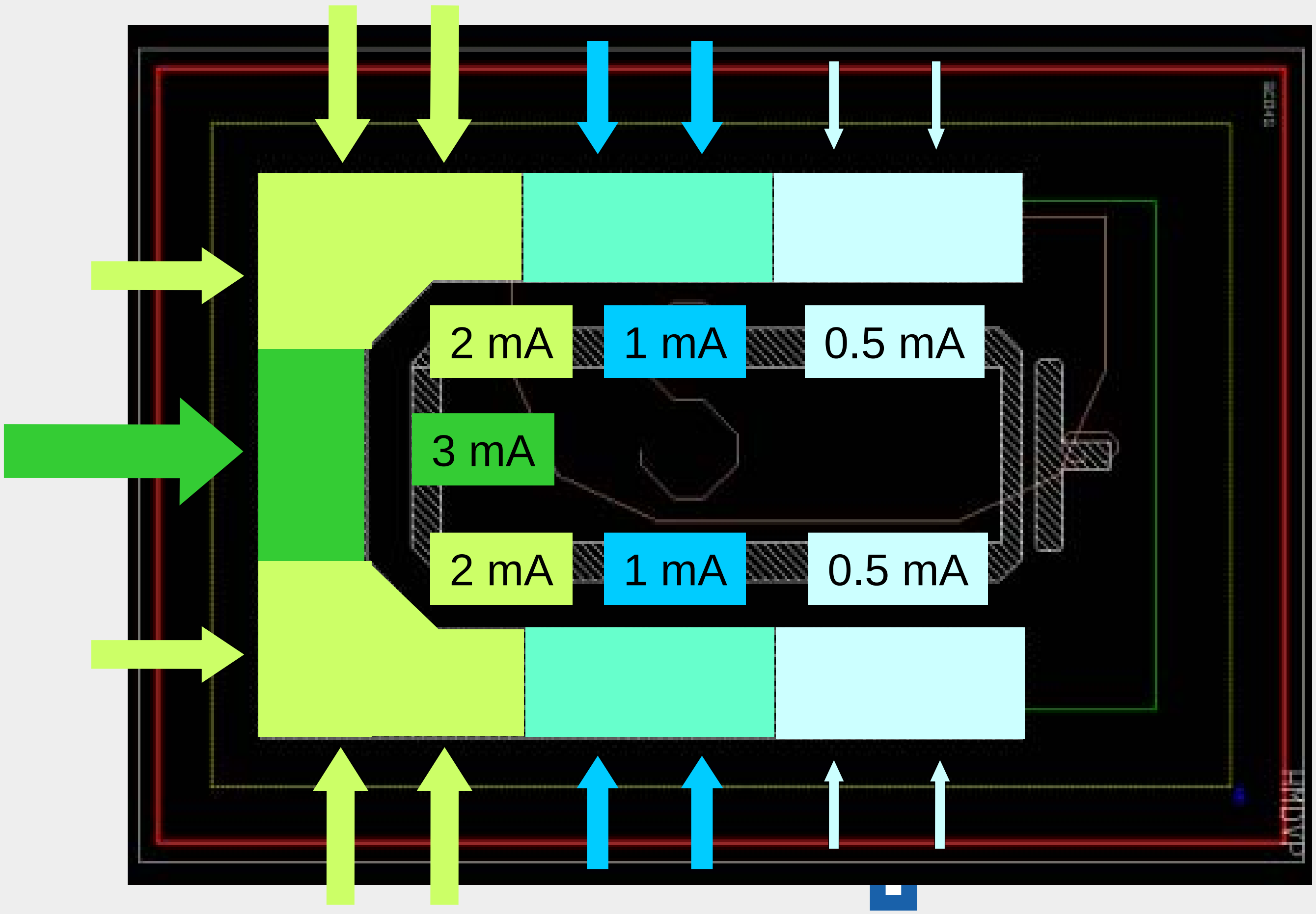


Pin of a DMOS transistor

(c) Current-Density-Correct Pin Connections



(c) Current-Density-Correct Pin Connections



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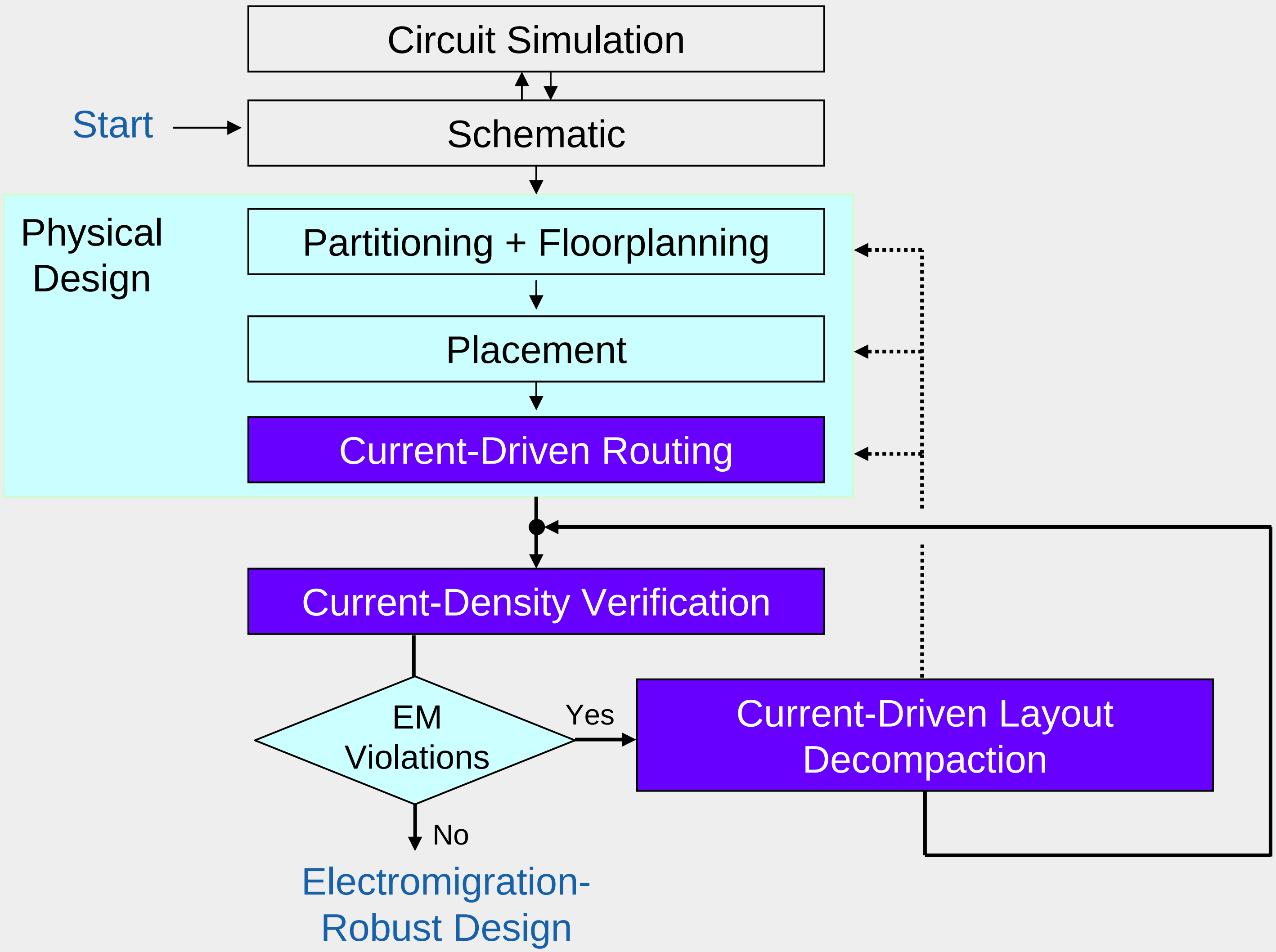
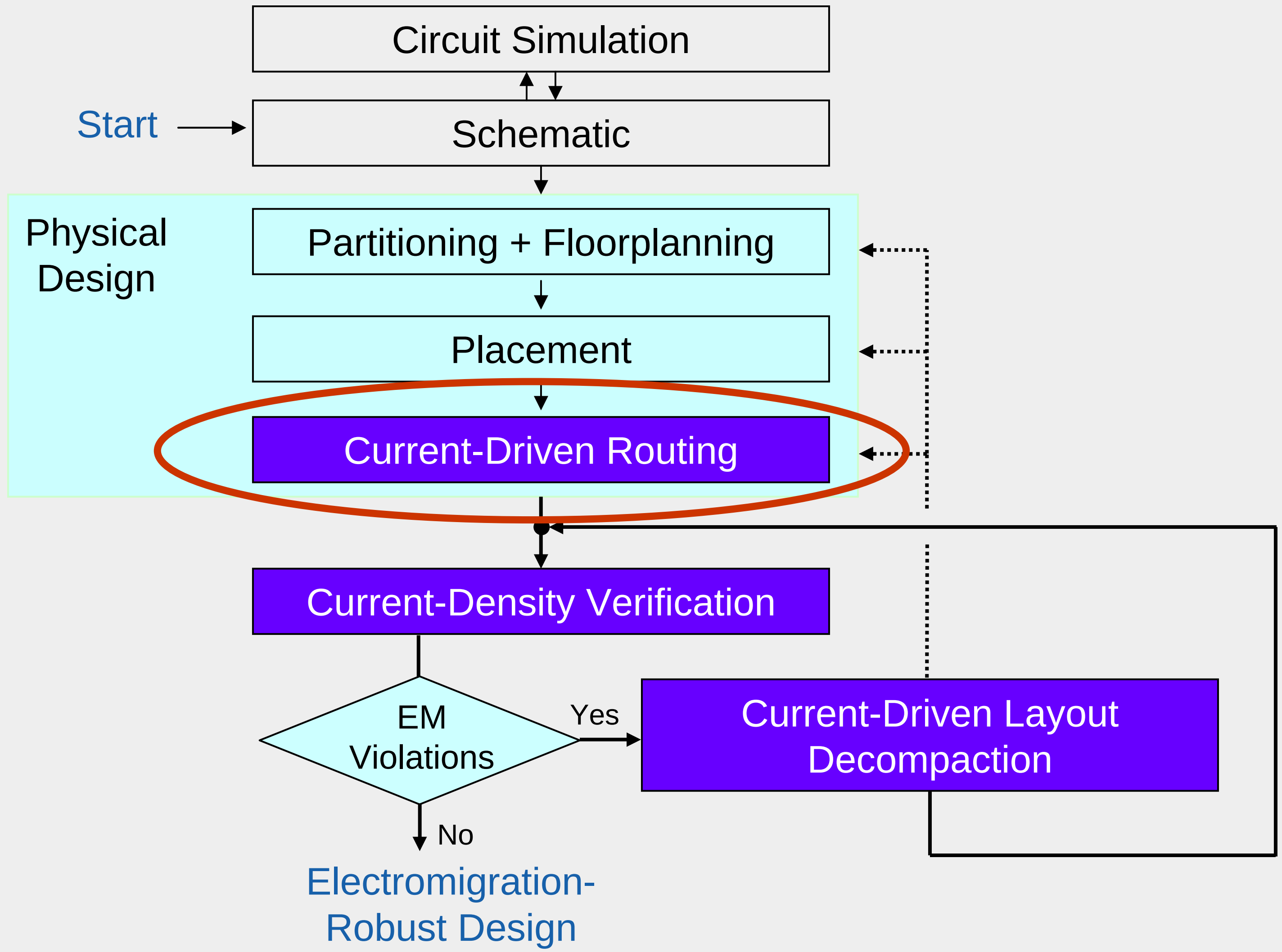
Electromigration-Aware (Analog) Physical Design Flow



Electromigration-Aware (Analog) Physical Design Flow



Current-Driven Routing

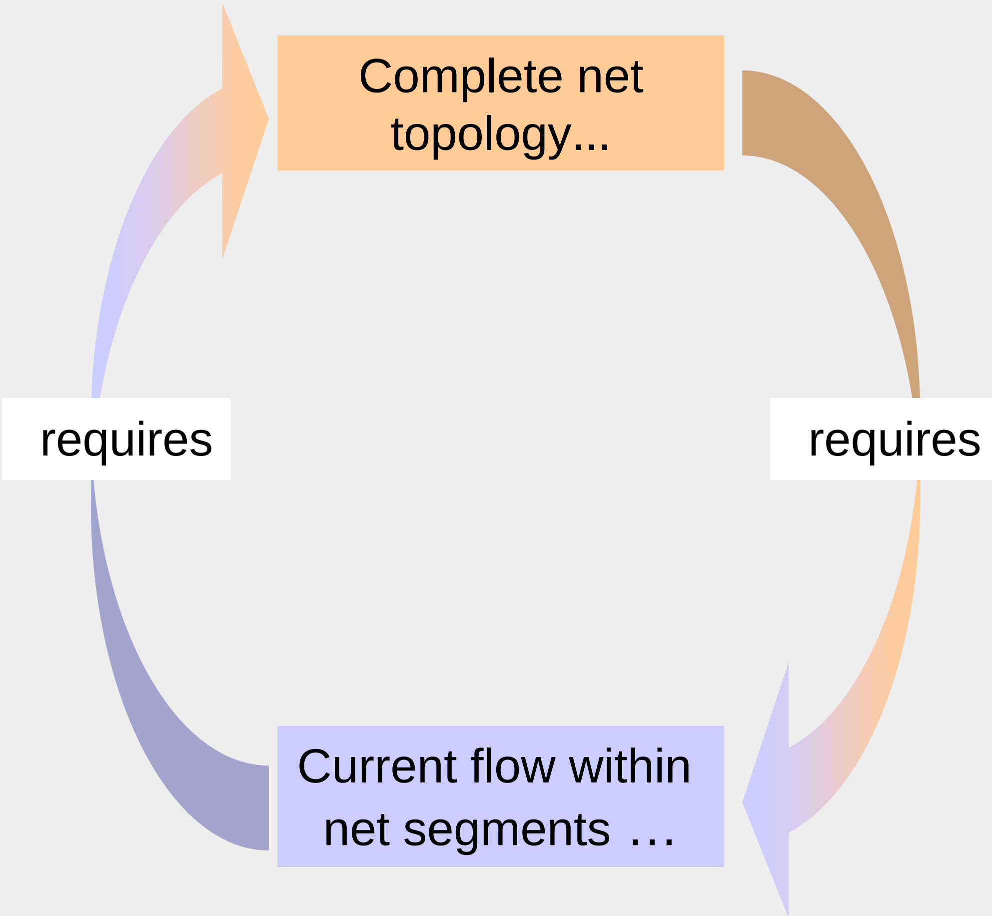
Goals:

- Routing with current-correct wire widths and via sizes
- Minimization of wire area

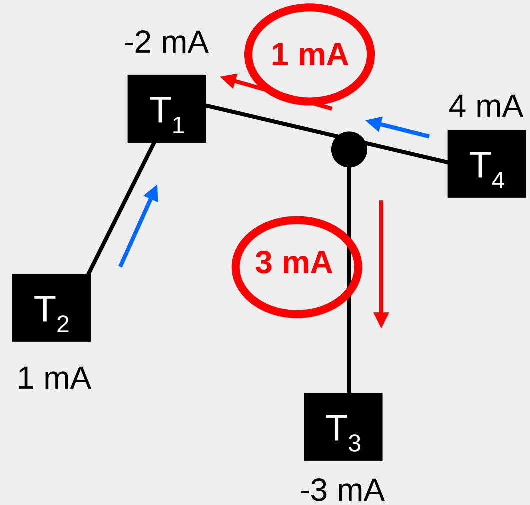
Major steps:

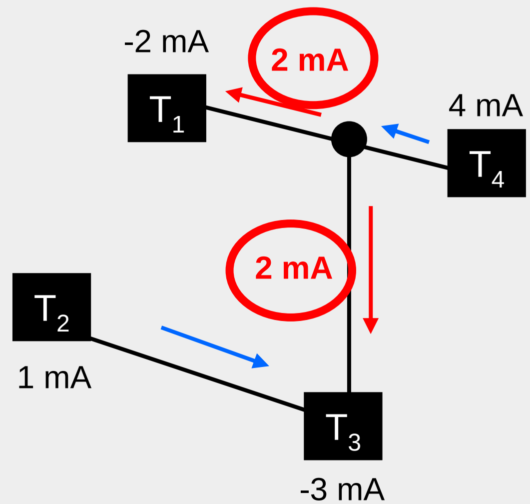
1. Concurrent wire planning and segment current determination
2. Calculation of wire widths and via sizes
3. Two-point detailed routing with provided wire widths and via sizes

Cyclic Conflict in Topology and Current Flow Determination

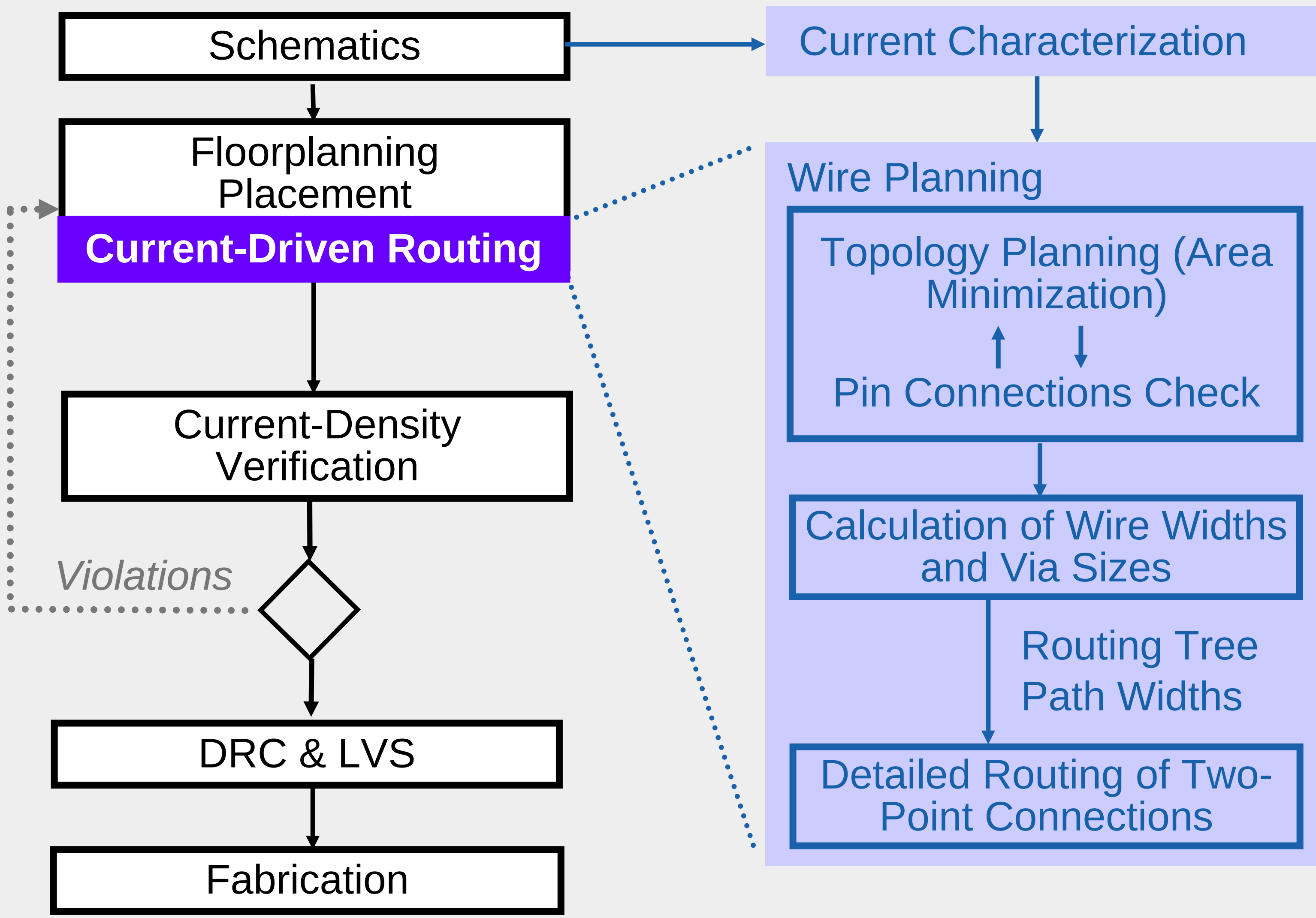


-> (1) Wire planning
(2) Detailed routing

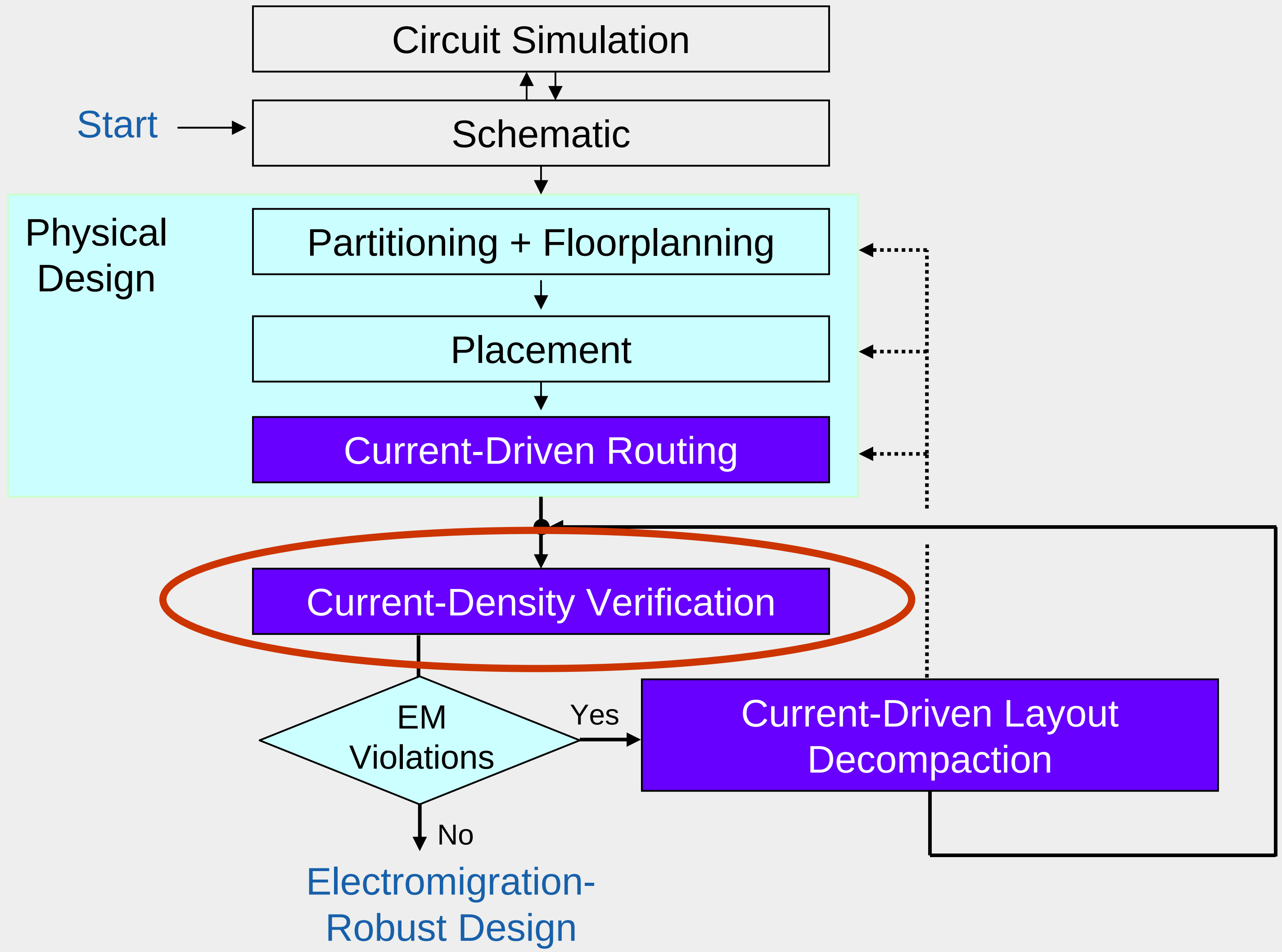




Current-Driven Routing: Algorithm



Current-Density Verification



Current-Density Verification

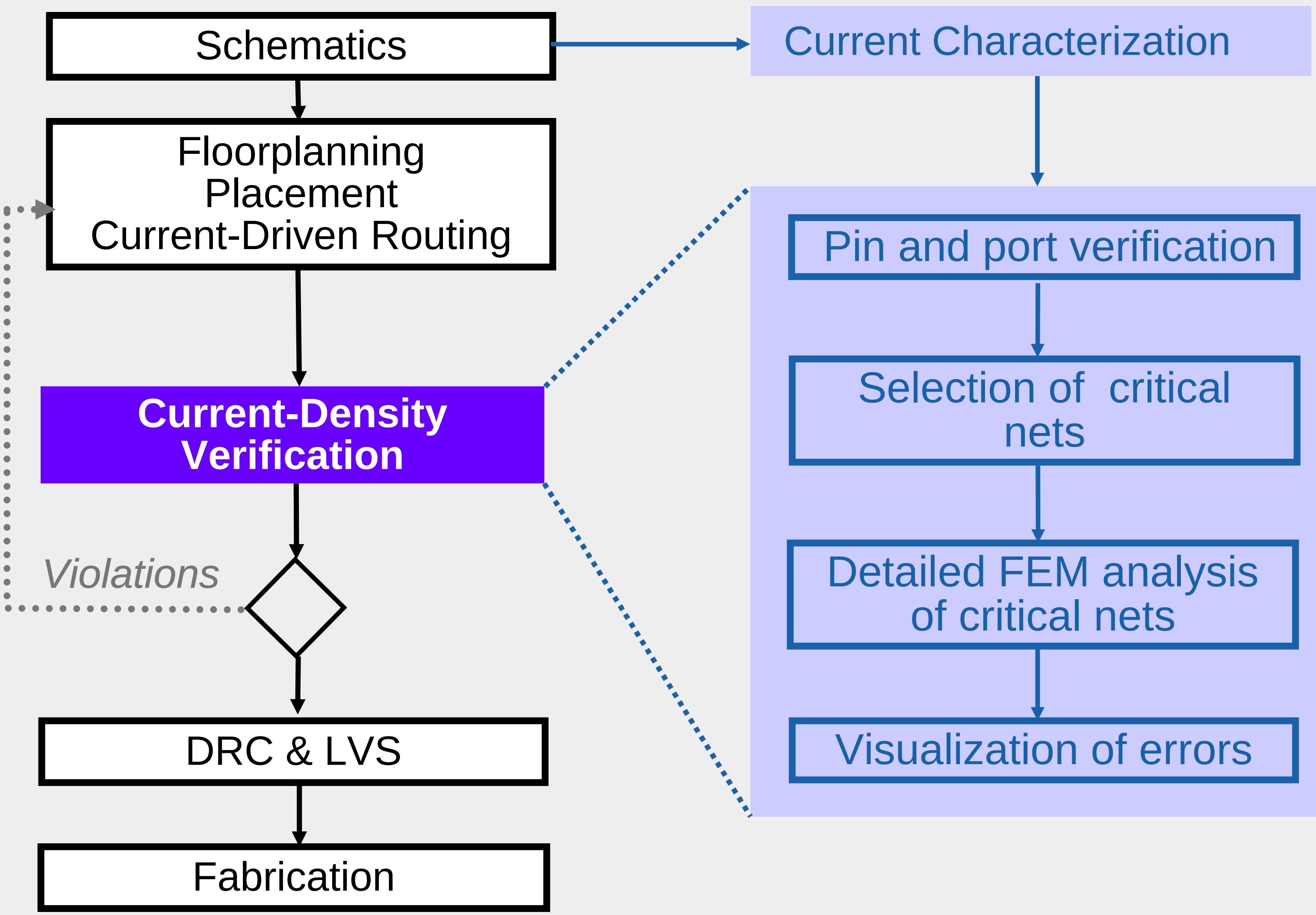
Goal:

- Automatic verification of actual current densities within arbitrarily shaped layout structures: $J_{Wire/Via}(T, Layer) \leq J_{Max}(T, Layer)$

Major steps:

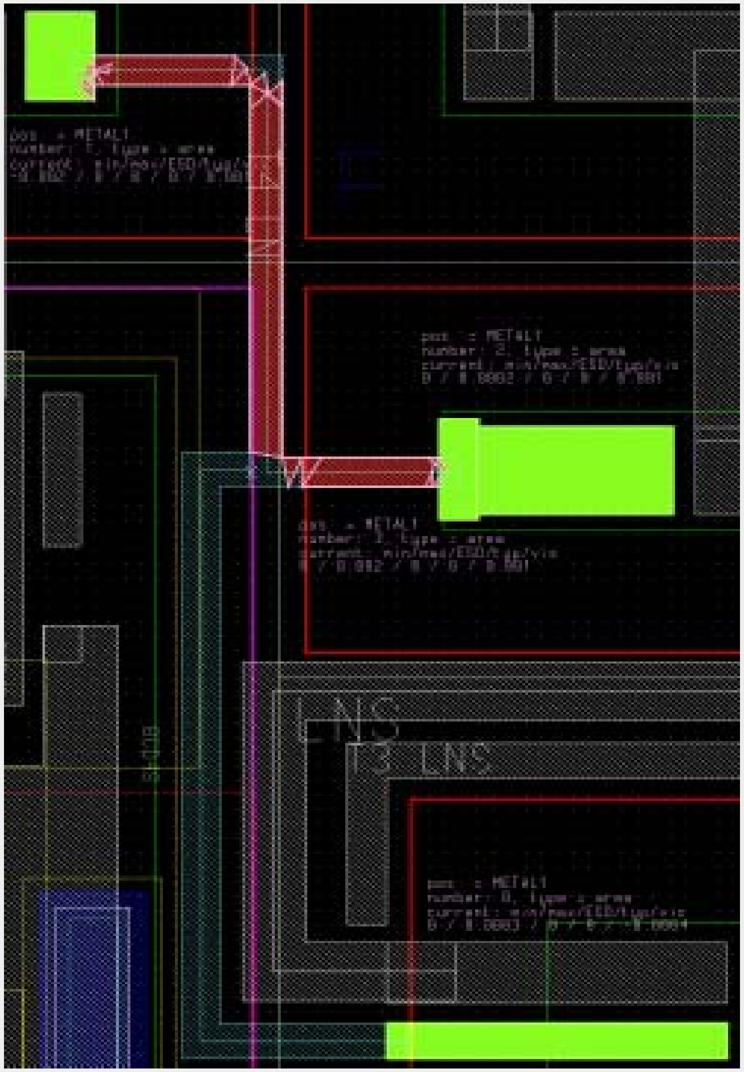
1. Determination of *maximum* current densities in each layer
2. Calculation of *actual* current densities within layout structures
3. If actual current density exceeds maximum value:
   mark violating areas and violation degrees

Current-Density Verification: Algorithm

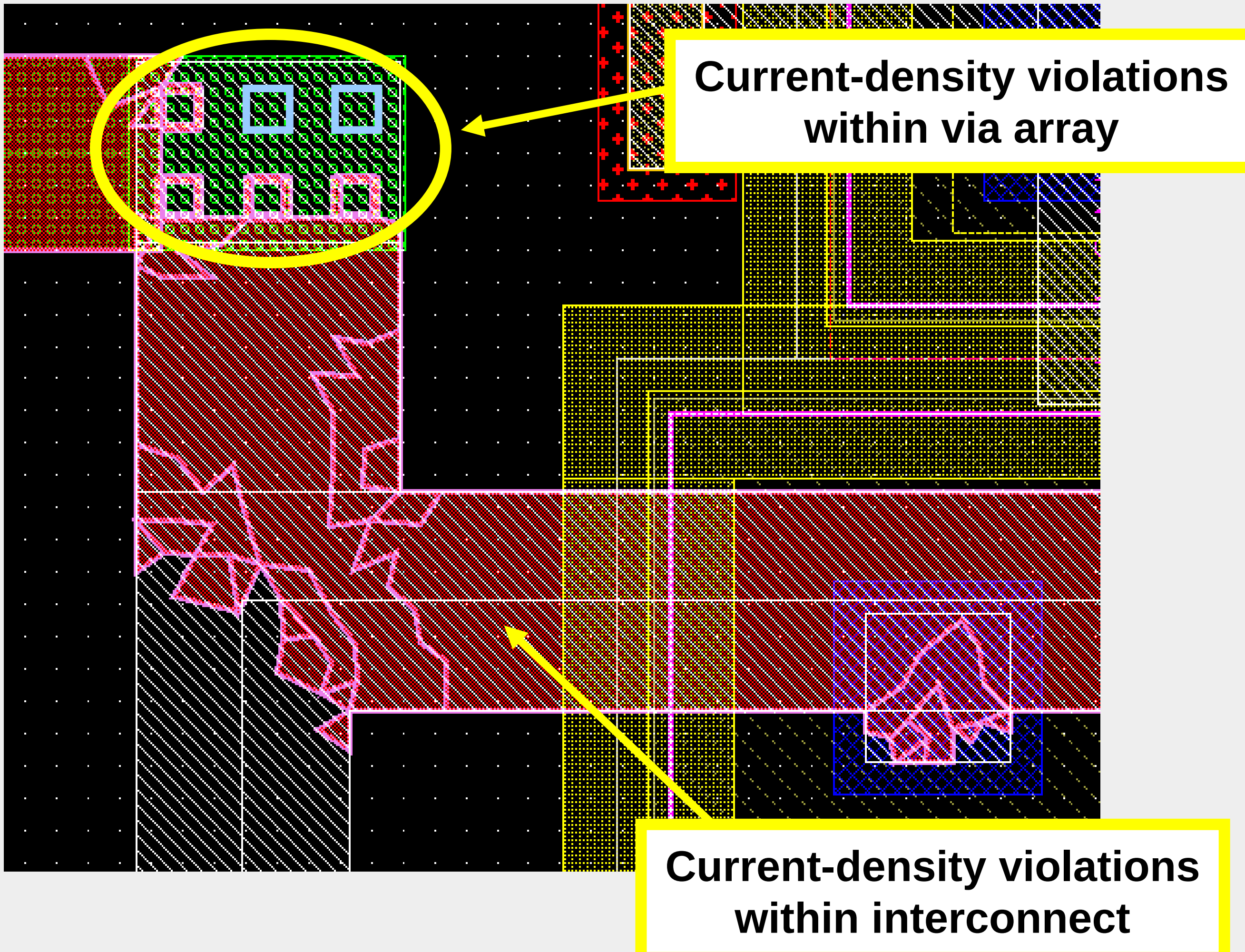


Detailed FEM Analysis of Critical Nets

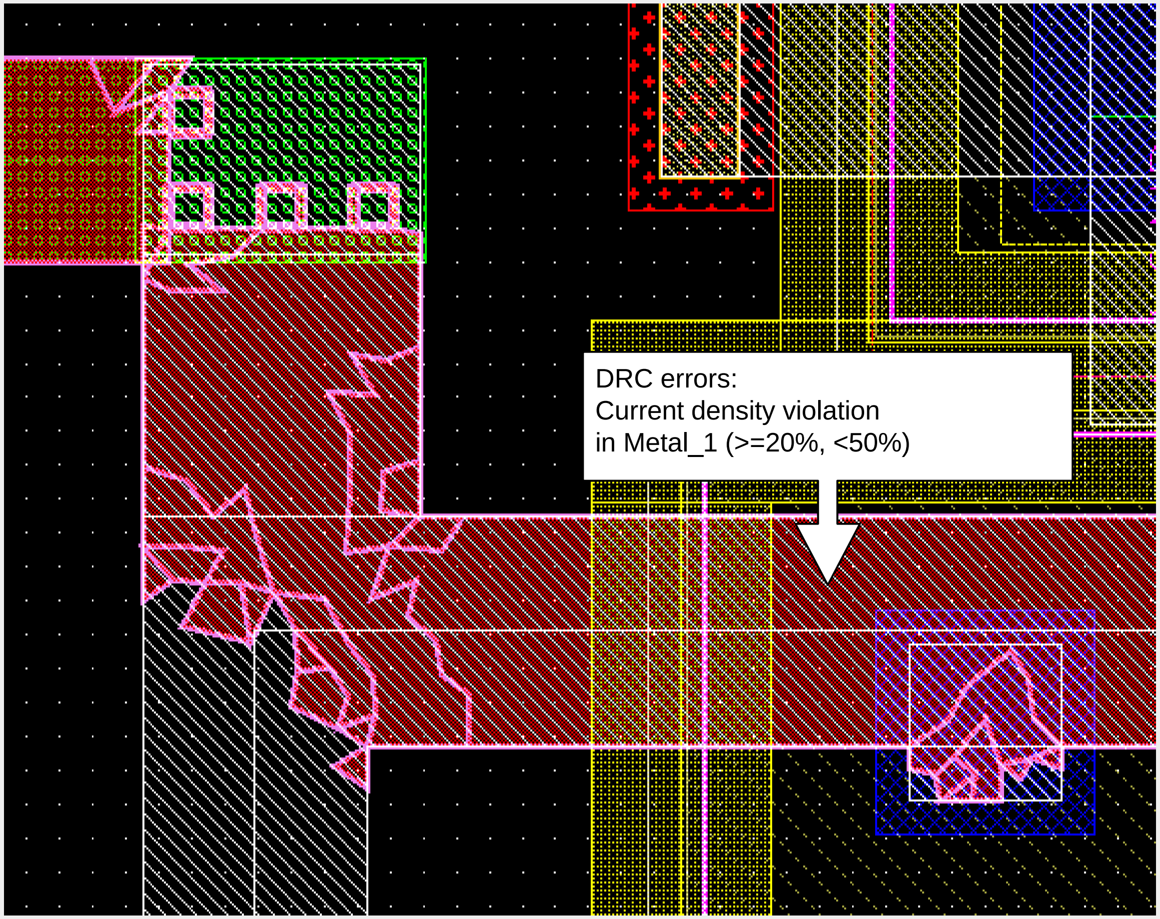
1. Assignment of current values at device pins and net ports
2. Layout segmentation into finite elements (triangles)
3. Calculation of the electric potential field $\varphi(x,y)$ using FEM
4. Calculation of current density J out of potential field gradient J=-$1/\rho \cdot$ grad($\varphi(x,y)$)
5. Comparison of calculated current density in every finite element with its maximum permissible value
6. Visualization of the violating areas



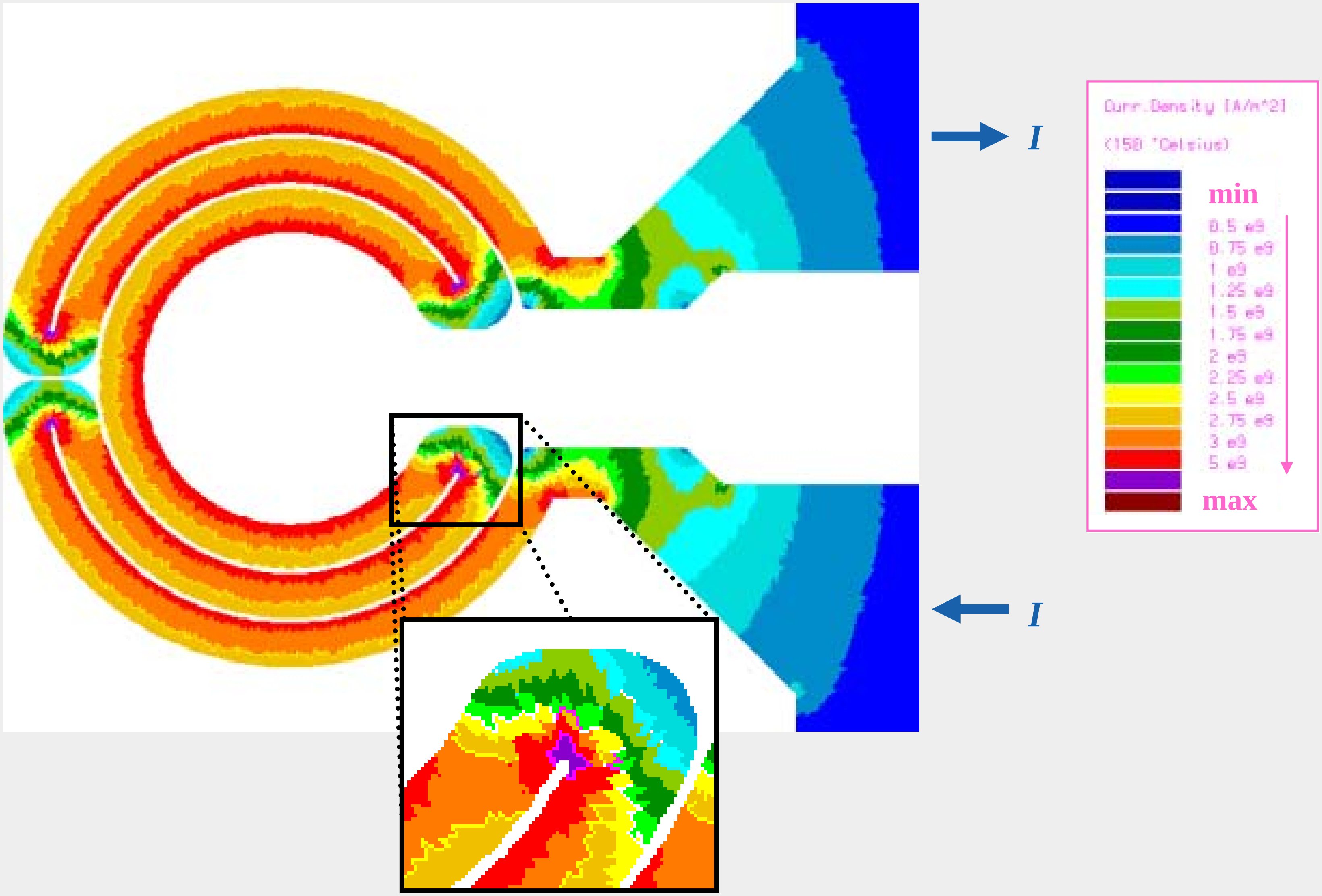
Current-Density Verification



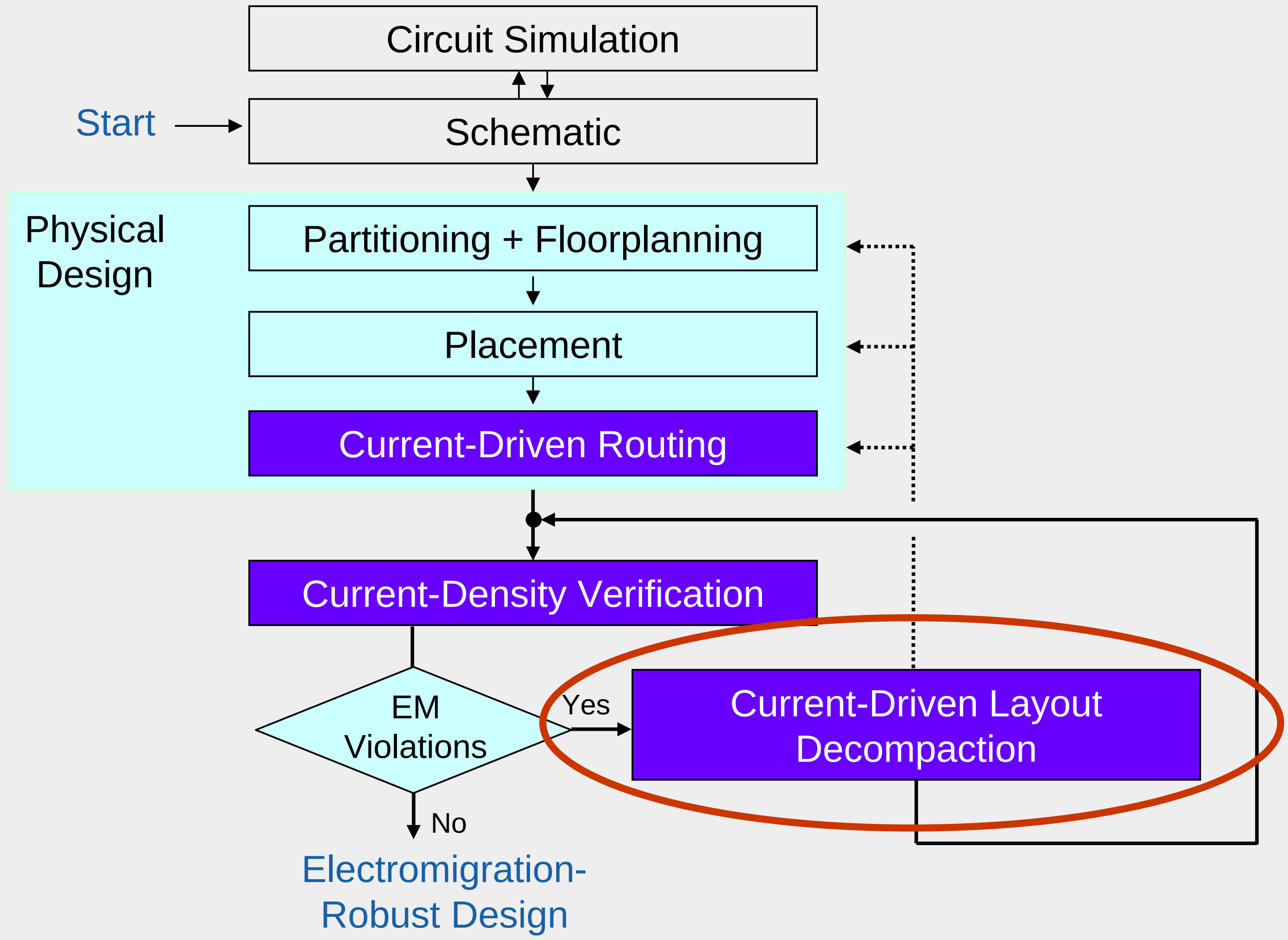
Current-Density Verification



Current-Density Visualization



Current-Driven Layout Decompaction



Current-Driven Layout Decompaction

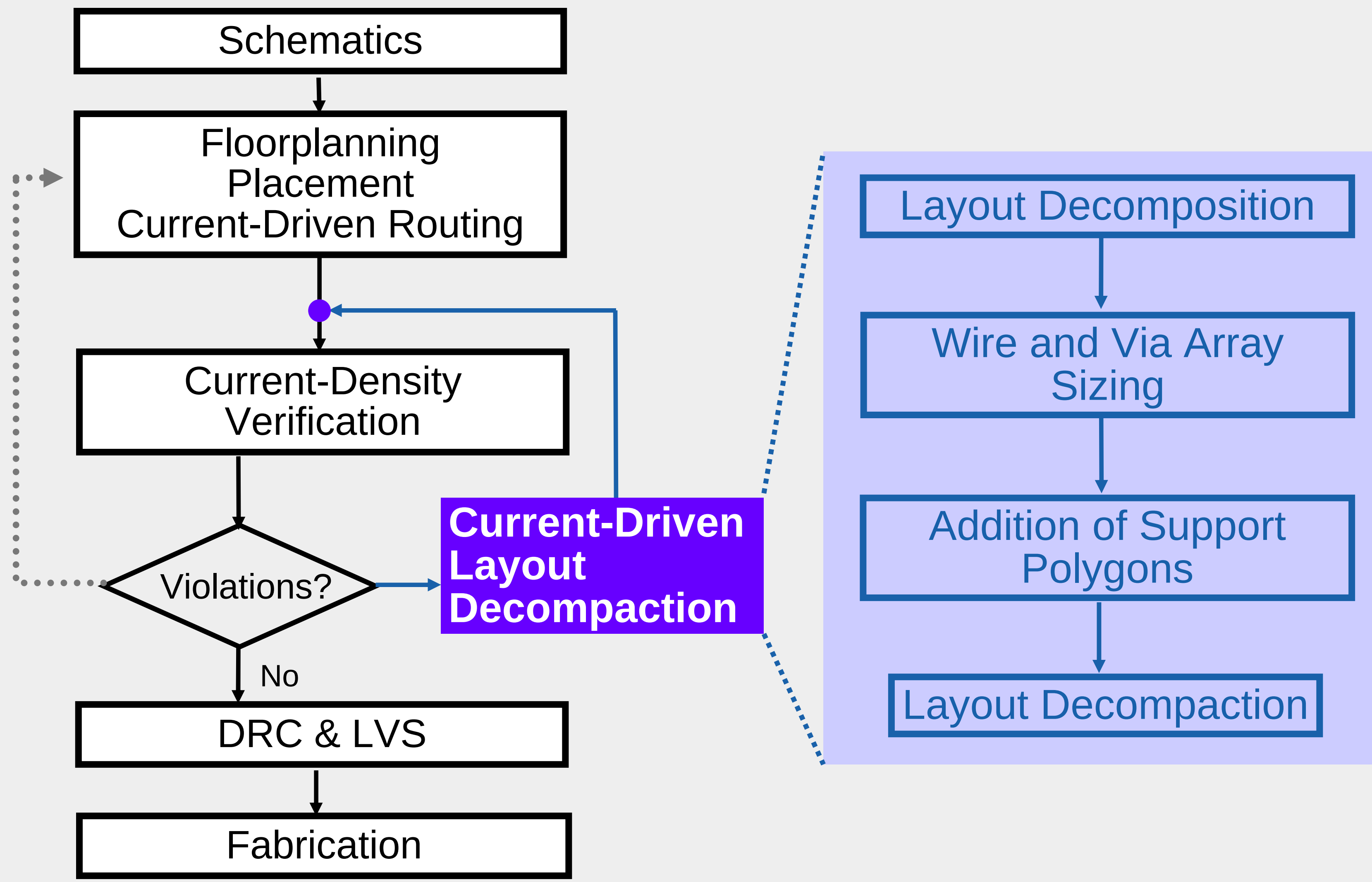
Goals:

- Post-routing adjustment of layout segments according to their actual current density
- Homogenization of the current flow

Major steps:

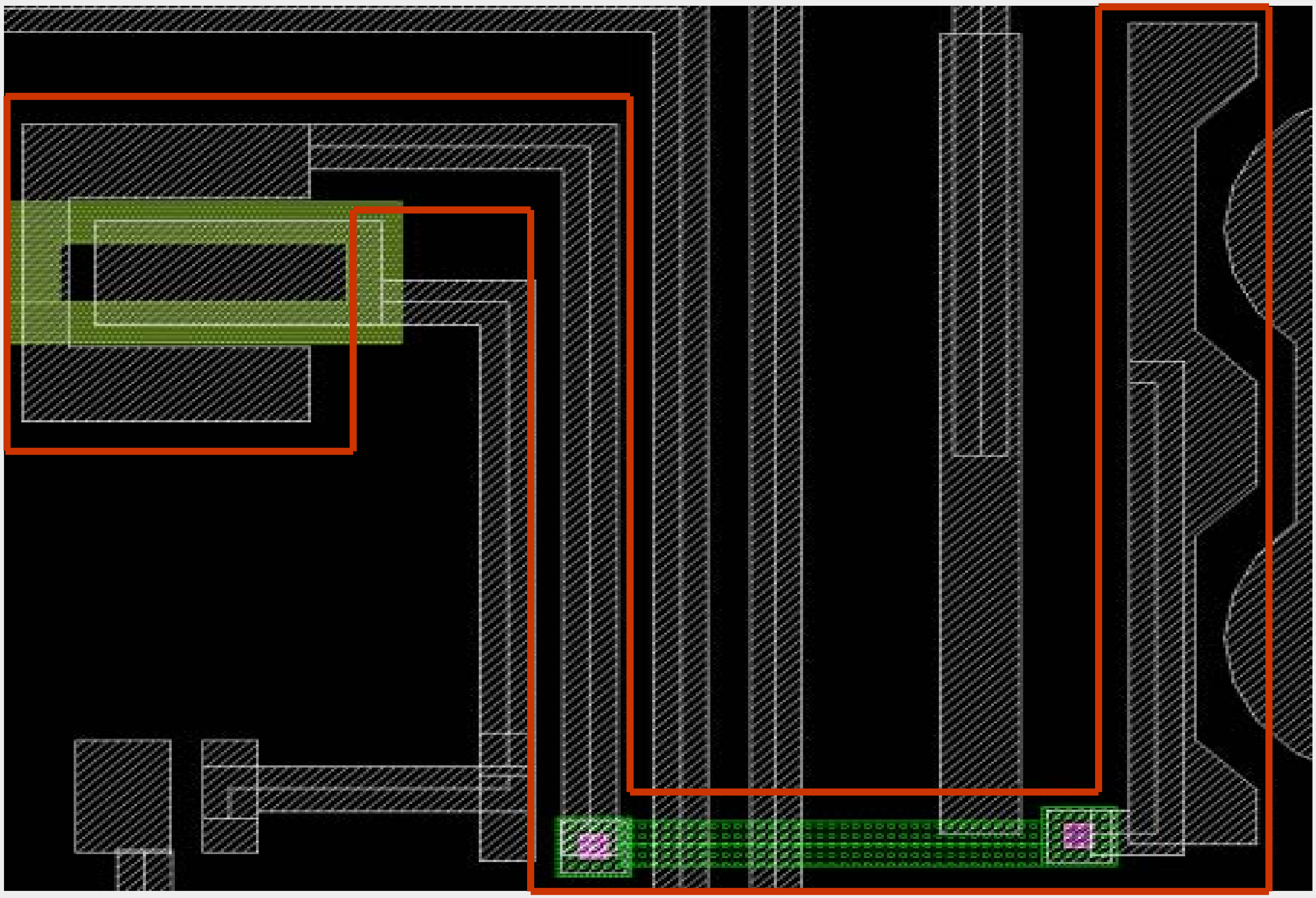
1. Current-density verification
2. Calculation of wire widths and via sizes according to actual currents in violating net segments
3. Addition of support polygons
4. Layout decompaction

Current-Driven Layout Decompaction: Algorithm



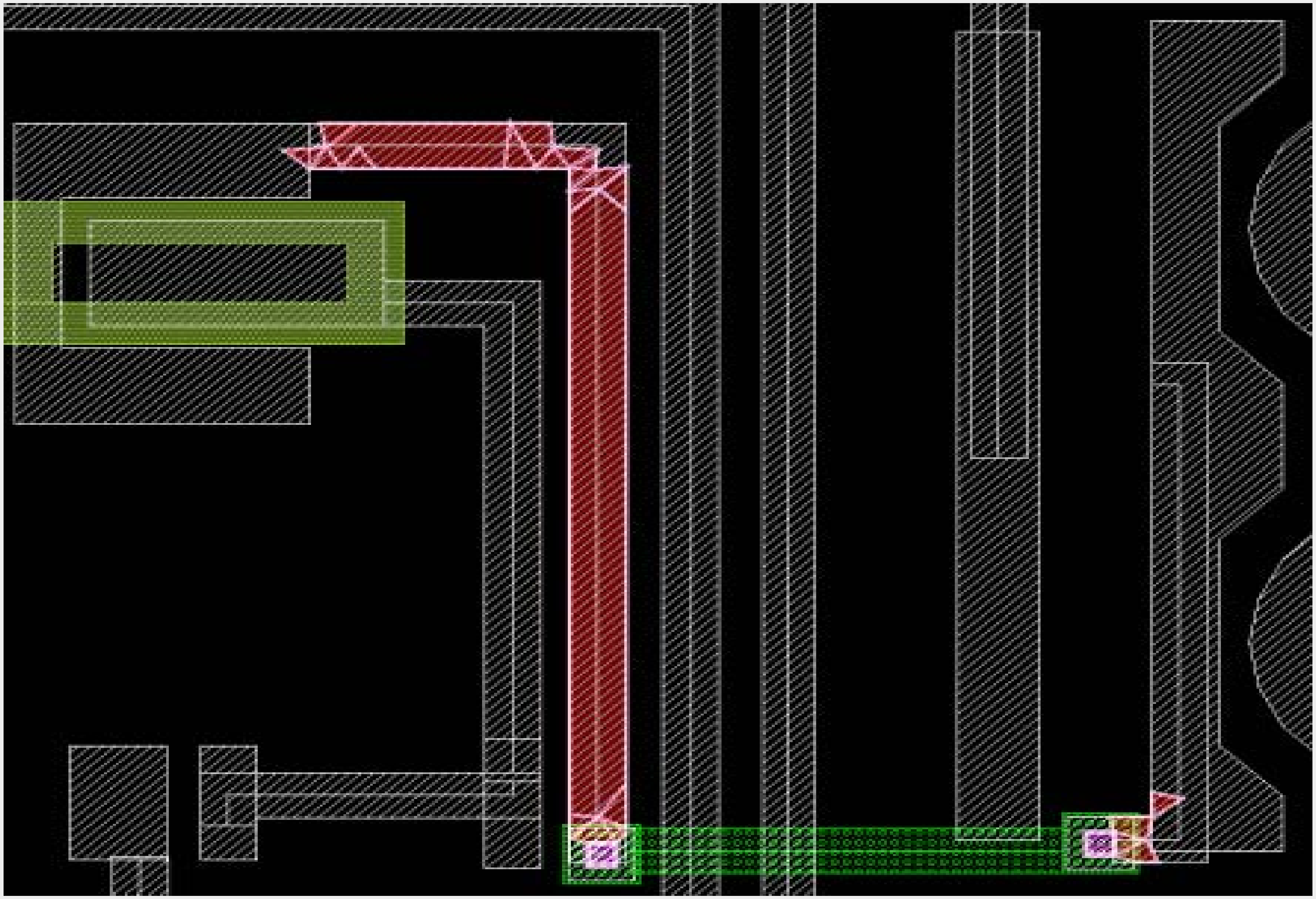
Current-Driven Layout Decompaction: Example

(1) Routed net



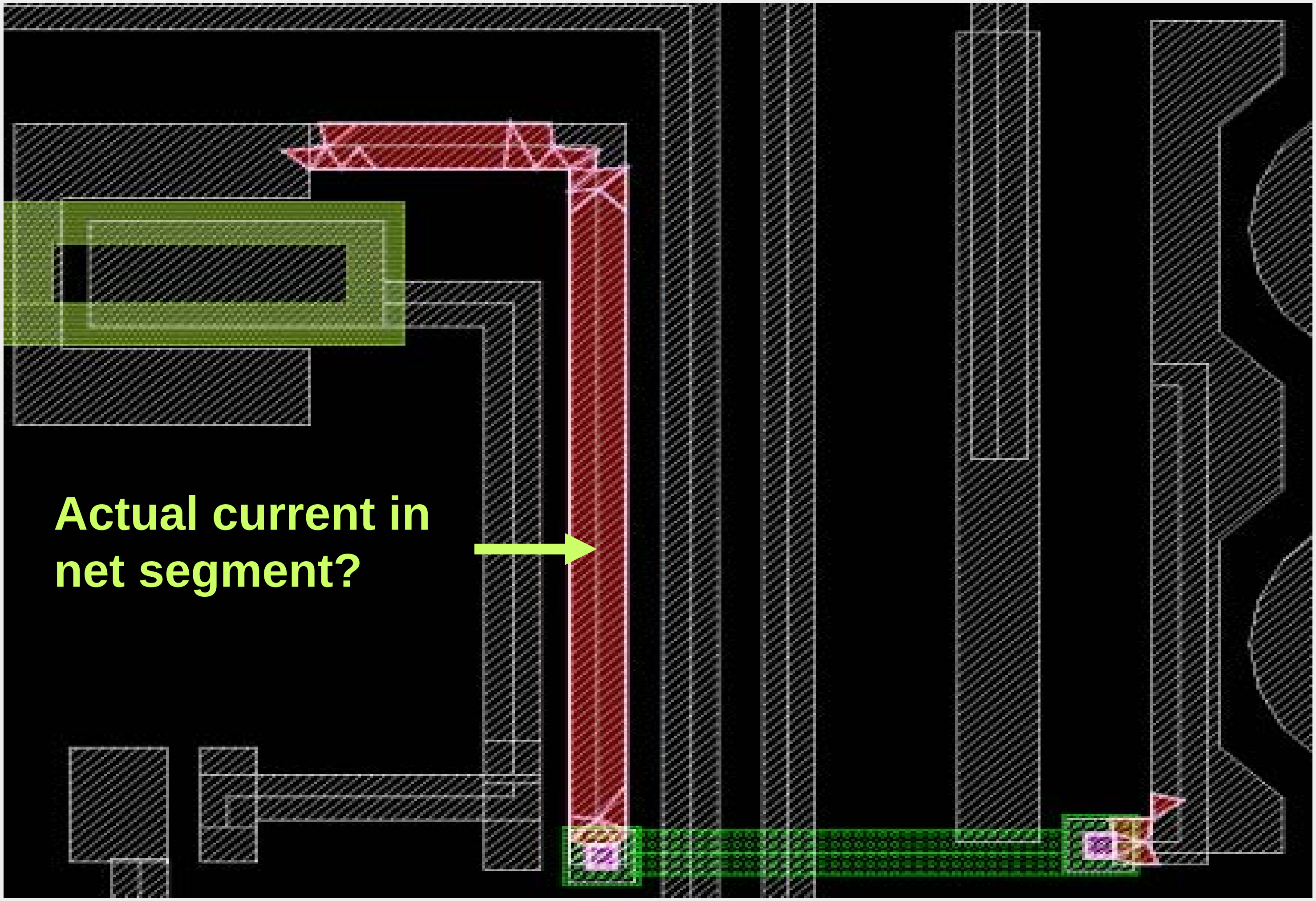
Current-Driven Layout Decompaction: Example

(2) Current-density verification



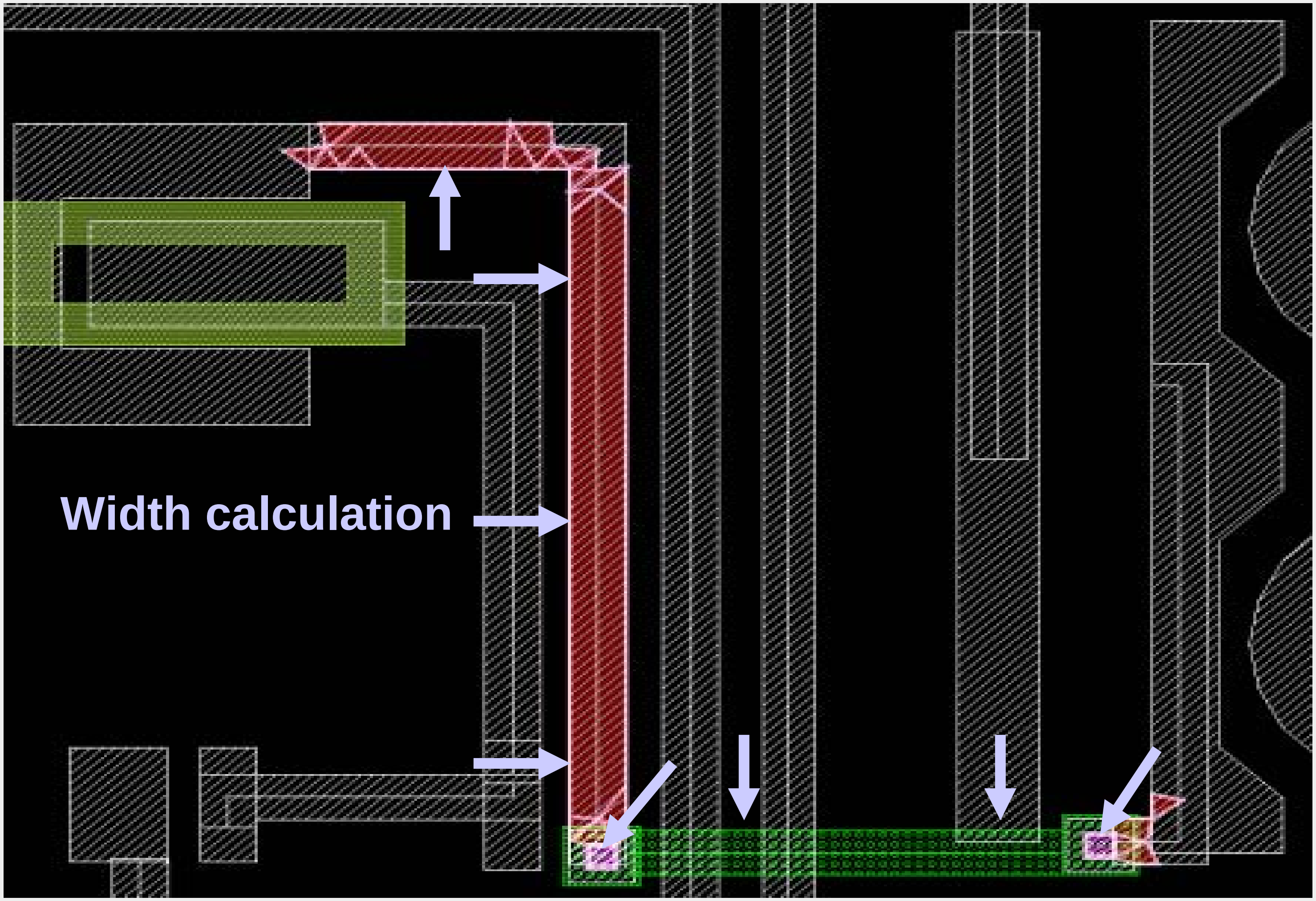
Current-Driven Layout Decompaction: Example

(3) Calculation of currents within violating net segments



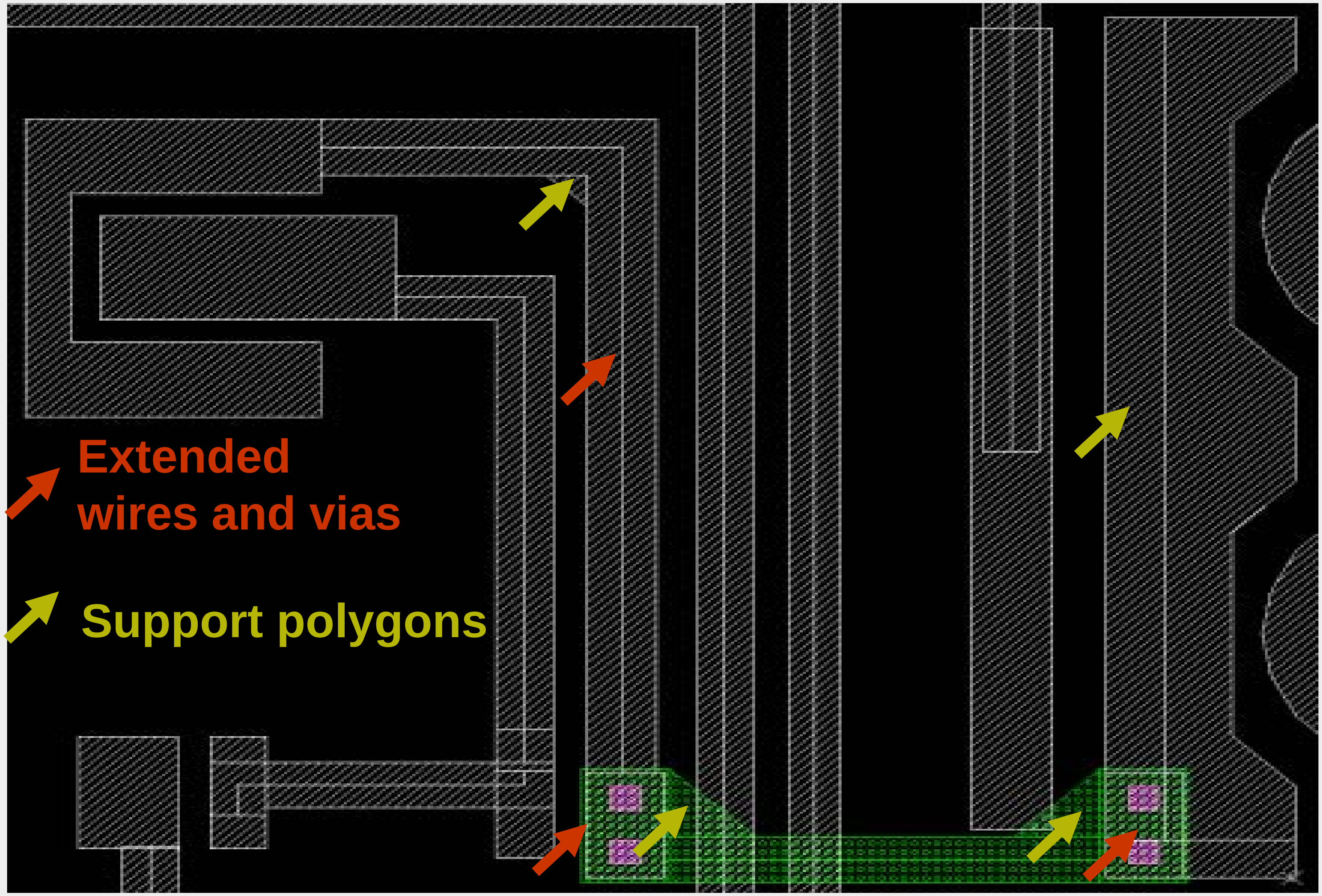
Current-Driven Layout Decompaction: Example

(4) Calculation of wire widths and via sizes according to actual currents



Current-Driven Layout Decompaction: Example

(5) After layout decompaction



Contents

Summary

- Electromigration: migration of atoms due to momentum transfer from conduction electrons
- Al: grain boundary diffusion, Cu: surface diffusion

➢ Electromigration is becoming a design problem due to increased current densities related to IC down-scaling

Technology solutions: (1) Cu instead of Al -> $J_{max}(Cu) \approx 5^* J_{max}(Al)$
(2) Bamboo structures, Blech length, …

Physical design solutions: (1) Current density
(2) Temperature

➢ Model: Black's law [1] (MTTF of interconnect and its relationship to current density and temperature)

Summary (2)

- Two methodologies for current-density correct interconnect generation:
  - Current-driven routing
    - Solving the cyclic topology/current problem via two-step approach: wire planning and subsequent two-point detailed routing
  - Current-driven layout decompaction
    - All currents are known (no cyclic topology/current problem)
    - Requires current-density verification and decompaction tool
- Current-density verification
  - Verification of arbitrarily shaped custom circuit layouts
  - Incorporates thermal simulation data

➢ Current-density verification must be an integral part of any future design flow

References

[1] Black, J.R. : "Electromigration - A brief survey and some recent results"; *Proc. of IEEE Reliability Physics Symposium*, Washington D.C., 1968.

[2] Blech, I.A. : "Electromigration in thin film aluminium films on titanium nitride"; *Journal of Applied Physics*, Vol. 47, No. 4, 1976.

[3] Maiz, J.A.: "Characterization of electromigration under bi-directional (BC) and pulsed unidirectional (PDC) currents"; *Proc. of IEEE-International Reliability Physics Symposium*, pp. 220-223, 1989.

[4] Lienig, J., Jerke, G., Adler, Th.: "Electromigration avoidance in analog circuits: two methodologies for current-driven routing"; *Proc. of the 7th Asia and South Pacific Design Automation Conference*, IEEE Press, Bangalore, India, January 2002.

[5] Lienig, J., Jerke, G.: "Current-driven wire planning for electromigration avoidance in analog circuits"; *Proc. of the 8th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Kitakyushu, Japan, pp. 783-788, 2003.

[6] Jerke, G., Lienig, J.: "Hierarchical current density verification in arbitrarily shaped metallization patterns of analog circuits"; *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, no.1, pp. 80-90, Jan. 2004.

[7] Jerke, G., Lienig, J., Scheible, J.: "Reliability-driven layout decompaction for electromigration failure avoidance in complex mixed-signal IC designs"; *Proc. of the 41st Design Automation Conference*, San Diego, CA, pp. 181-184, 2004.

[8] Adler, T., Barke, E.: "Single step current driven routing of multiterminal signal nets for analog applications"; *Proc. of Design, Automation and Test in Europe (DATE)*, pp. 446-450, 2000.