# Timing Analysis in Presence of Supply Voltage and Temperature Variations

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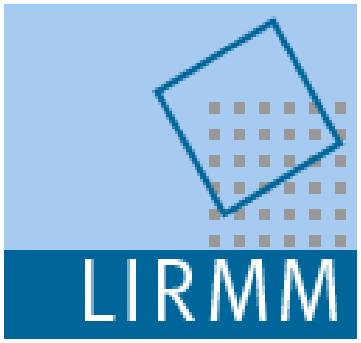


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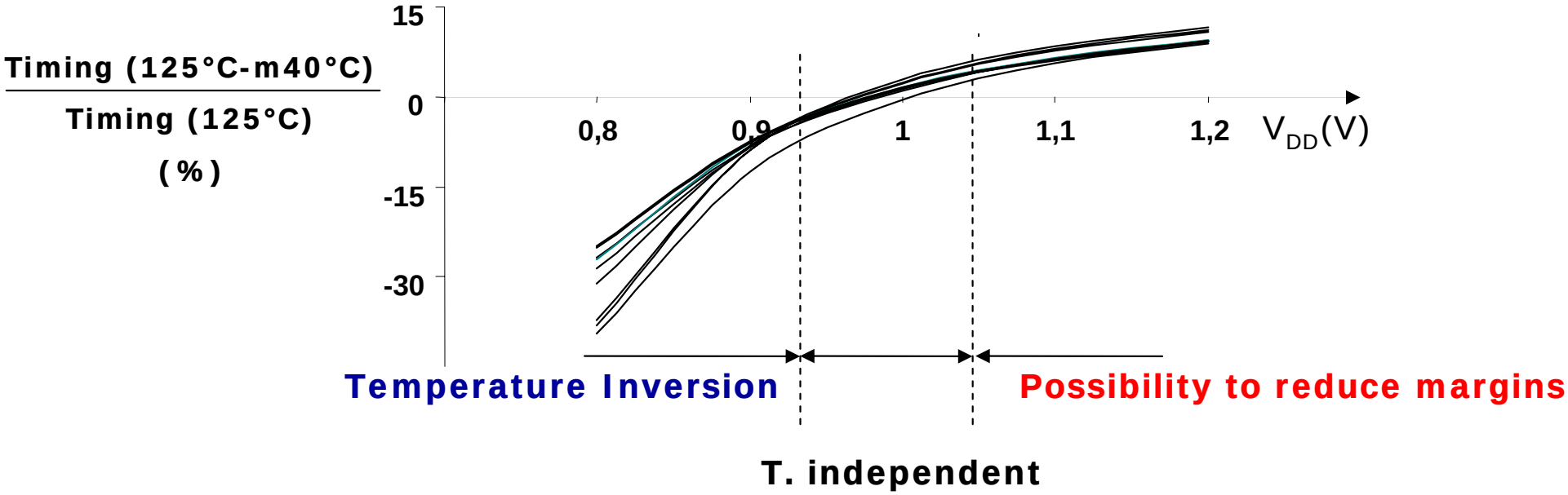
# Motivation

- Delay is strongly dependent on supply voltage
  - +10% Vdd, induce > +20% delay
  - WC/BC drop ±10% of $V_{DD}$, is it accurate?
- Temperature sensitivity depends on domains
  - Function of process and supply voltage value



# Our goal

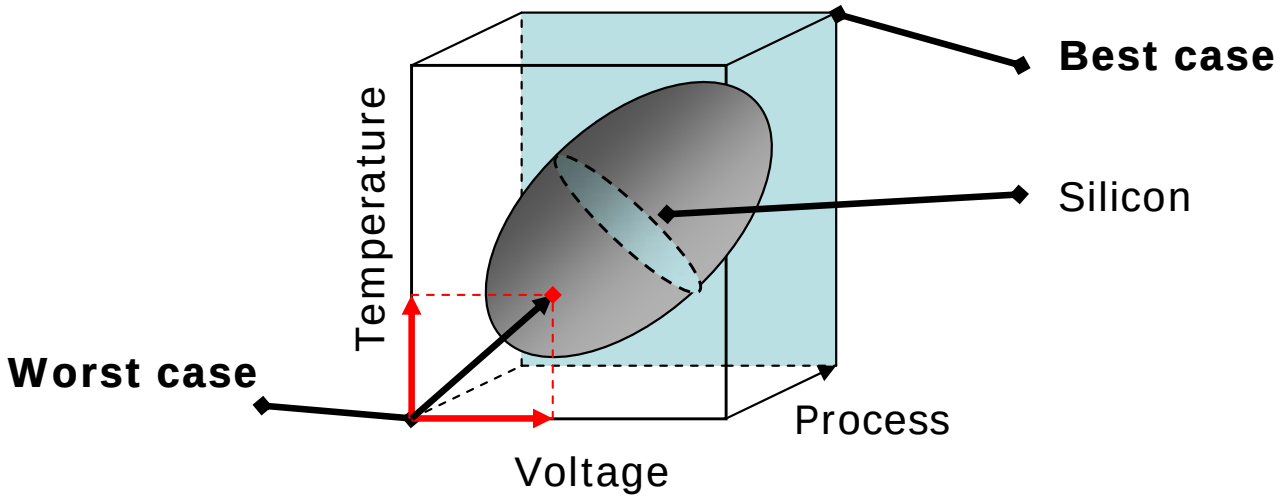
- Reduced margins using “real” V, T values for each cell
- Avoid over-design or re-design steps
- How ?
  - Using Vdrop and T. Gradient maps
  - Non-linear timing derating for each instance

# How ?

- Manage Vdd and θ at cell level ?
  - Popular K-factor method

$$Delay = Do + \overbrace{\frac{\partial D}{\partial V_{DD}}\Delta V_{DD}}^{\text{Voltage}} + \overbrace{\frac{\partial D}{\partial \theta}\Delta\theta}^{\text{Temperature}}$$

  - From a standard corner analysis we estimate timing for any Voltage and Temperature value



# Problem

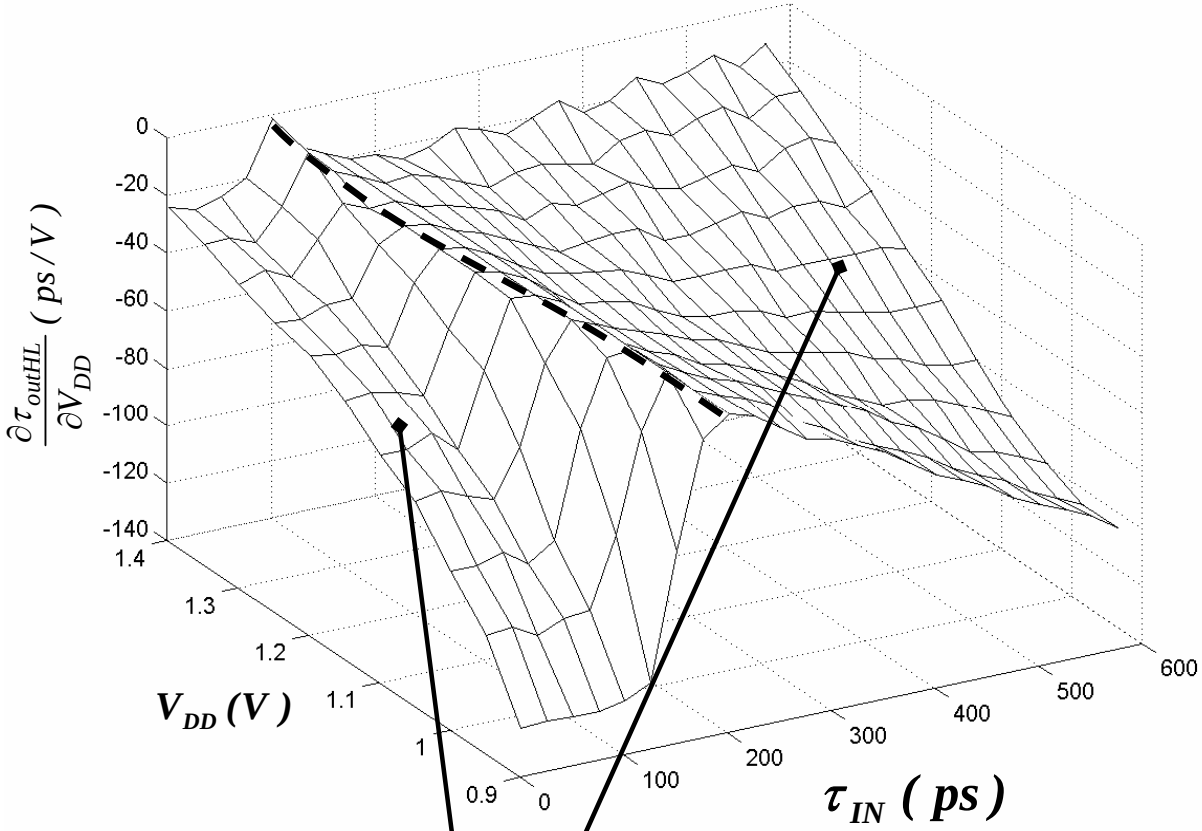
- How to define accurately scaling factors?

$$Delay = Do + \underbrace{\frac{\partial D}{\partial V_{DD}}}_{?}\Delta V_{DD} + \underbrace{\frac{\partial D}{\partial \theta}}_{?}\Delta\theta$$

  - Linear function not enough accurate
  - Polynomial template not enough accurate on large range of $V_{DD}$ and T.

- Scaling must follow physical behavior

# Sensitivity analysis




- Derating factor must characterized:
  - Slow and Fast domains
  - Design dependence

**Input slope**

```
"0.092, 0.247, 0.553, 1.172", \
"0.093, 0.247, 0.556, 1.172", \
"0.103, 0.258, 0.557, 1.166", \
"0.134, 0.275, 0.556, 1.173", \
"0.194, 0.344, 0.597, 1.176" );
```

**Output Capacitance**

**Transition Time LUT**

# Analytical Timing Model – Slope

- Modeling the transistor as a current generator

$$\tau_{out} = \frac{C_L \cdot V_{DD}}{I_{MAX}}$$

- Depending on the input range value
  - Fast input domain: saturation current

$$\tau_{out}^{Fast} = \frac{DW \cdot C_L \cdot V_{DD}}{K \cdot W \cdot \left(V_{DD} - V_T\right)^{\alpha}}$$

  - Slow input domain: current function of slope

$$\tau_{out}^{Slow} = \left( \frac{DW \cdot C_L \cdot \tau_{IN}^{\alpha} \cdot V_{DD}^{1-\alpha}}{\alpha \cdot K \cdot W} \right)^{\frac{1}{1+\alpha}}$$

# Analytical Timing Model – Delay

- Propagation Delay is strongly dependent on:
  - Input slew
  - Output Load
  - Gate size
  - I/O coupling capacitance (Miller effect)

$$t = \frac{\tau_{IN}}{\alpha + 1}\left(\frac{\alpha - 1}{2} + \frac{V_T}{V_{DD}}\right) + \left(1 + \frac{2C_M}{C_M + C_L}\right)\frac{\tau_{out}}{2}$$

# Analytical Timing Model – Temperature

- Supply voltage value appears explicitly
- Temperature acts on Threshold Voltage and Mobility

$$V_T = V_{Tnom} - \delta \cdot (\theta - \theta_{nom}) \qquad K = K_{nom} \cdot \left( \frac{\theta_{nom}}{\theta} \right)^{X_K}$$

$$\tau_{out}^{Fast} = \frac{DW \cdot C_L}{K \cdot \left( \frac{\theta_{nom}}{\theta} \right)^{X_K} \cdot W \cdot (V_{DD} - V_T + \delta \cdot (\theta - \theta_{nom}))^{\alpha}}$$

$$t = \frac{\tau_{in}}{\alpha + 1} \left( \frac{\alpha - 1}{2} + \frac{V_T - \delta \cdot (\theta - \theta_{nom})}{V_{DD}} \right) + \left( 1 + \frac{2C_M}{C_M + C_L} \right) \frac{\tau_{out}}{2}$$

# Derating Coefficient - $V_{DD}$

- From analytical model,
  - We derate formulas with respect to $V_{DD}$
  - We extract design dependency

- For slope in fast input domain,

$$\frac{\partial \tau_{out}^{Fast}}{\partial V_{DD}} = \frac{DW \cdot C_L}{K \cdot W} \cdot \frac{(1-\alpha) \cdot V_{DD} - V_T}{(V_{DD} - V_T)^{1+\alpha}}$$

Becomes

$$\frac{\partial \tau_{OUT}^{Fast}}{\partial V_{DD}} = \frac{a_{Slope}^{Fast}}{V_{DD}^{\ 2}} + \frac{b_{Slope}^{Fast}}{V_{DD}^{\ 2}} C_L$$

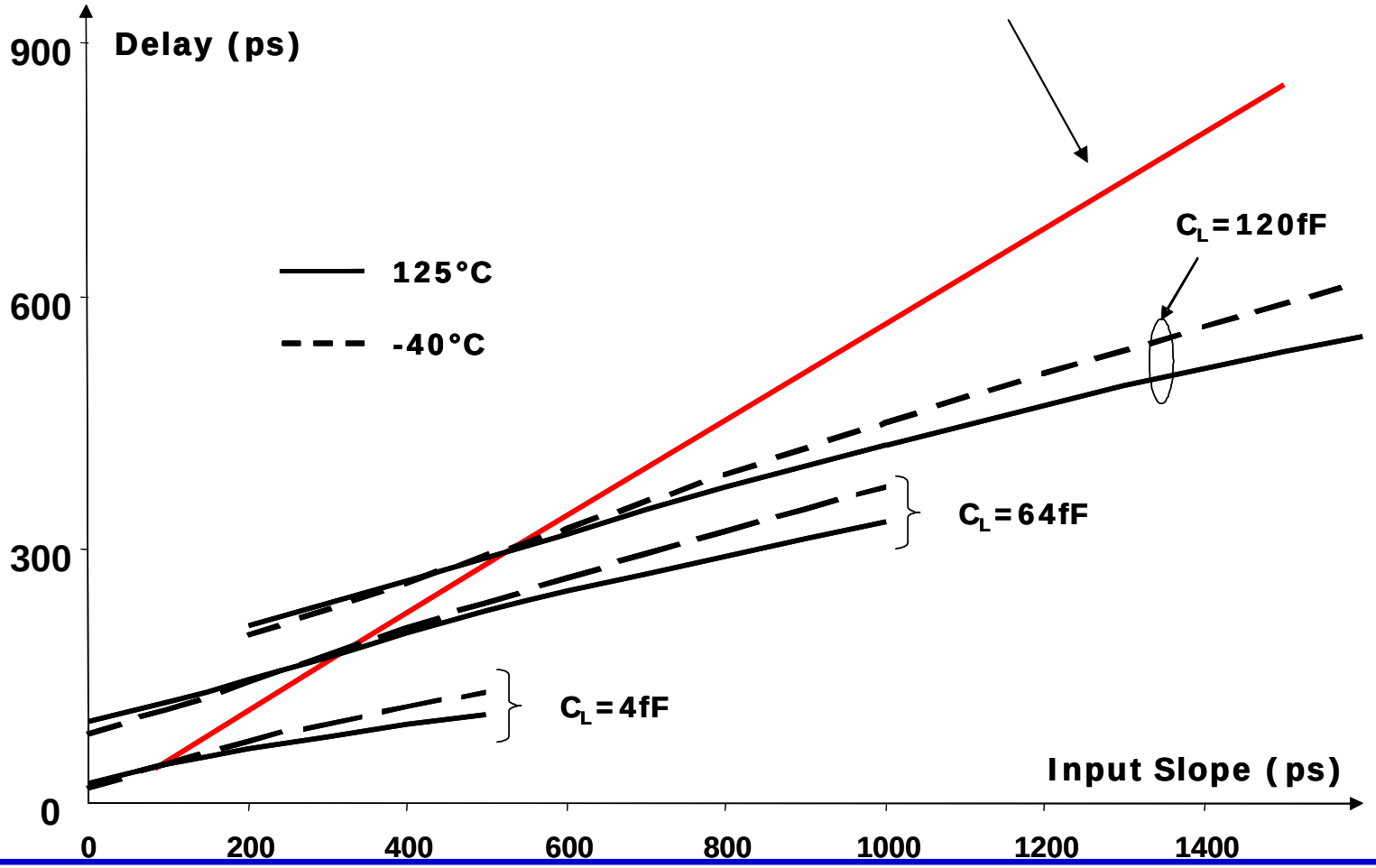
- $a^{Fast}$, $b^{Fast}$ are $V_{DD}$ independent parameters to be calibrated

# Derating Coefficient – Temperature

- Temperature Template

$$\frac{\partial t^{Fast}}{\partial \theta} = a_{Delay}^{Fast} + b_{Delay}^{Fast} \cdot \tau_{IN} + c_{Delay}^{Fast} \cdot C_L$$

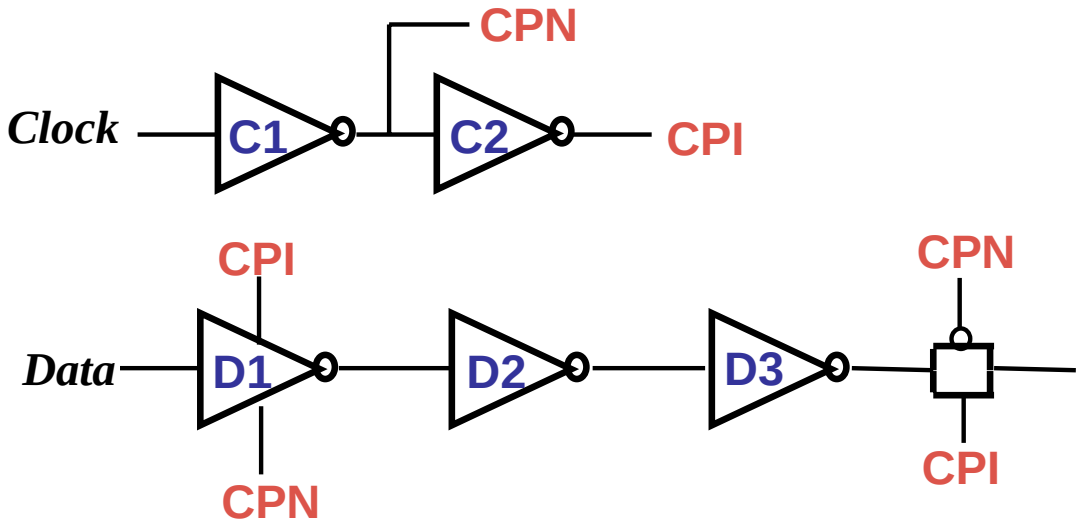
$$\tau_{INinv} = a_{INV} + b_{INV} \cdot C_L$$



# Derating Coefficient – Constraint

- Setup and Hold:
  - Race between Clock and Data paths.

**Setup = (D1+D2+D3) – C1**

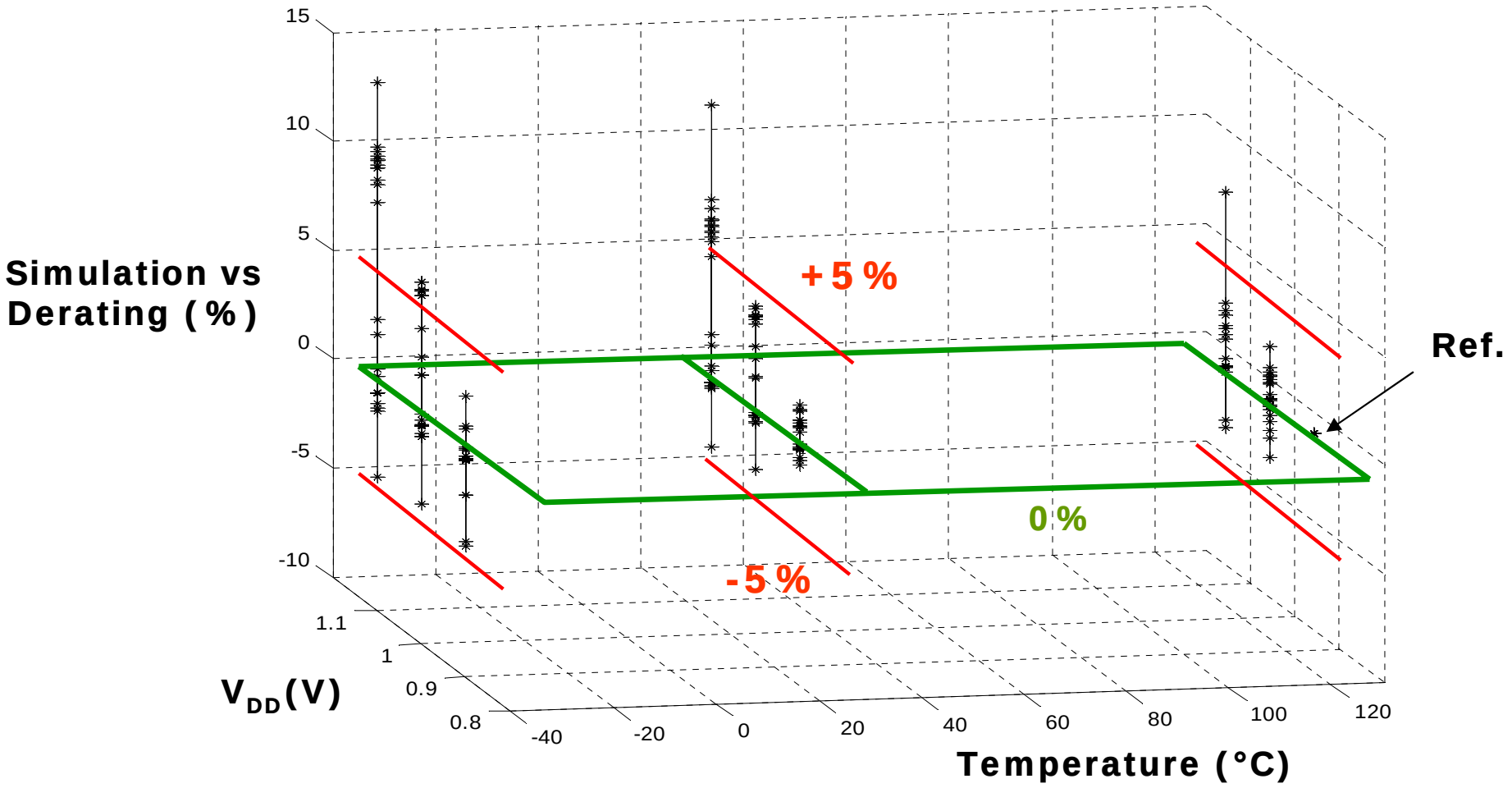



- Ignore Load sensitivity, keep only slope variation

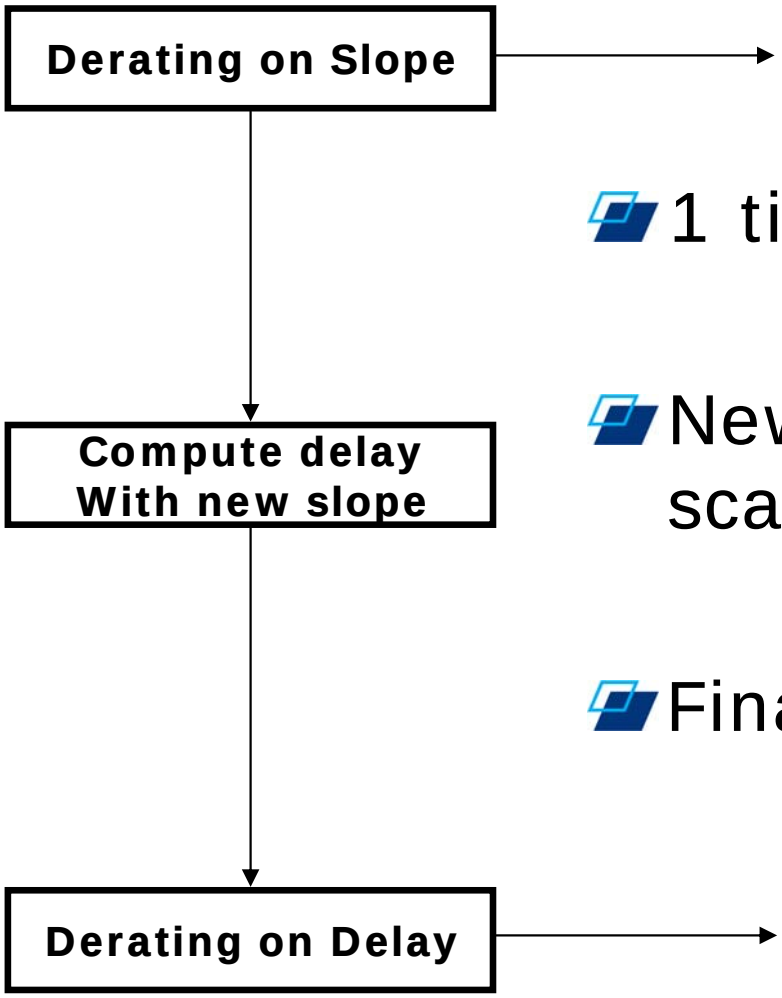
$$\frac{\partial Setup}{\partial \theta} = a_{Setup} + b_{Setup} \cdot \tau_{Data} + c_{Setup} \cdot \tau_{Clock}$$

# Validation – Standard cell

- Template are fitted with 3 corners (1 ref., 1 for Vdd, 1 for T)
- Corner computed for an entire library with derating factor
- Comparison: scaling values versus electrical simulations



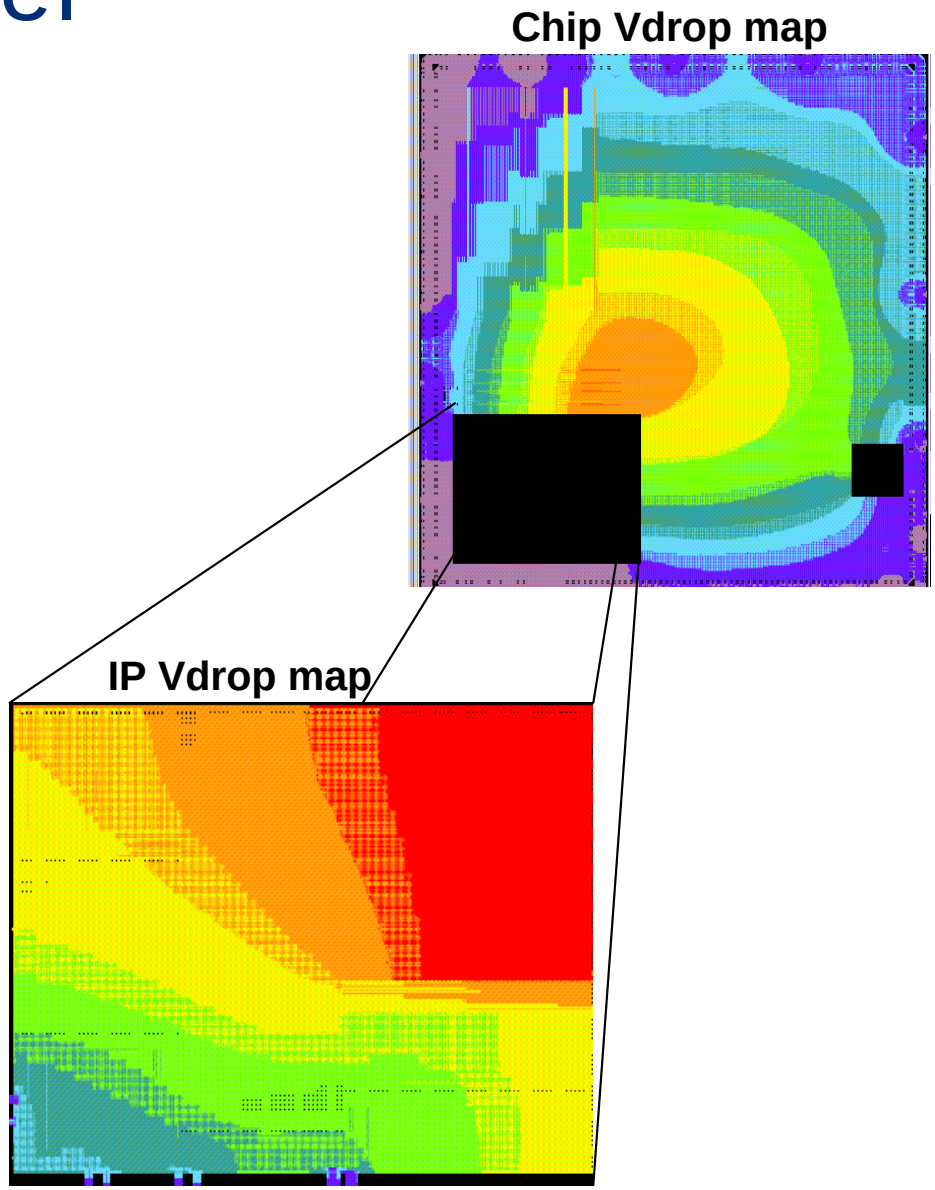
# Application - Chip level




- Slope file (~ SDF)
- 1 timing update with new slope
- New SDF is available (delay can be scaled using internal developed tool)
- Final annotation is done
- Final SDF

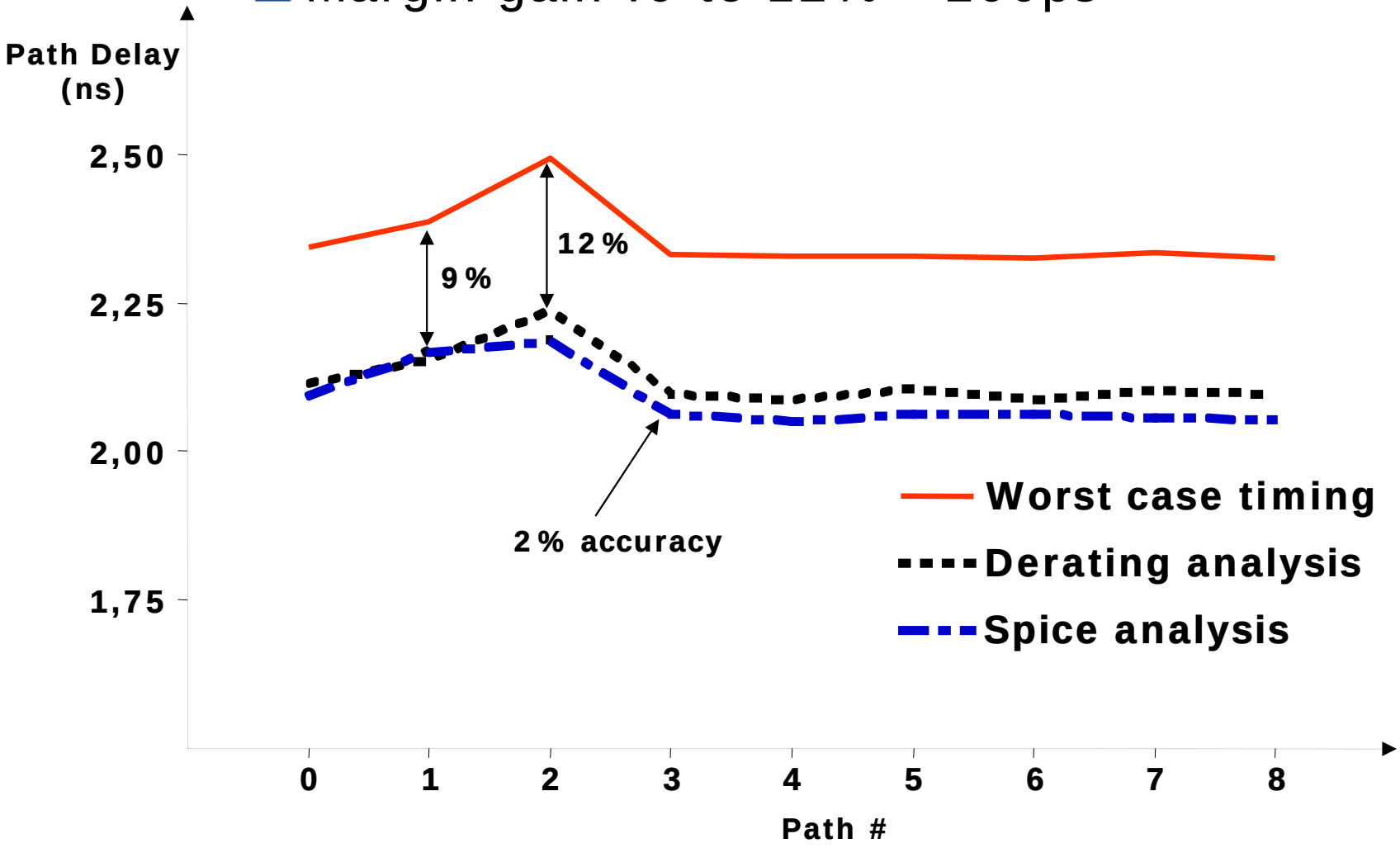
# Application – Chip level

- Timing Analysis with Vdrop data
- From a worst case corner, we update delay with Vdrop maps.
- We compute each Slope and Delay derating (cell by cell)
- Comparison :TA with (Vdd – 10%)
  Versus TA with Vdrop Data



# Results

- Comparison Spice/WC/Derating
  - Margin gain :9 to 12% ~200ps



# Summary

- We propose a method to handle Temperature/$V_{DD}$ variations based on cell by cell scaling factor
  - These deratings are non-linear and function of design conditions
- Taking account Vdrop in TA, highlights a significant gain in margin versus standard worst case method.
- Voltage Derating could be also used to validate Dynamic Voltage, Multi-Voltage feature
- Method has demonstrated for precise Temperature effects such as Temperature inversion and can be used to characterize hot spots.

Thank you !!