Understanding and Addressing the Impact of Wiring Congestion During Technology Mapping

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Motivation

- In DSM wirelength does not scale with feature size
  - Cell area minimization no longer guarantees block/chip size minimization
  - The synthesized netlist may not be routable within the fixed floorplan constraints
- Congestion should be included in the synthesis optimization objectives
  - In the traditional ASIC design flow no physical information is available before layout
  - Physical information can be effectively exploited during technology mapping
- The impact of any synthesis-level congestion minimization approach can be evaluated only after detailed routing

Motivation

- Including congestion in the synthesis optimization objectives yields sub-optimal cell area and/or delay
  - Trade-offs between congestion and cell area and/or delay minimization must be carefully considered
- Congestion-driven technology mapping can effectively reduce congestion globally
- But localized congested regions may still persist after detailed routing
  - Different layout areas may have very different routing demands
  - Both “global” and “local” nets along with the netlist structure and the routing resources impact on routability
- A single-pass congestion minimization approach is not likely to work for all designs

Congestion-driven tech mapping

- Connectivity is captured after initial placement of the tech independent netlist
- Placement coordinates are used during:
  - DAG partitioning
  - Tree covering
- The congestion-driven tree covering cost function attempts to place the fanin gates close to their fanouts

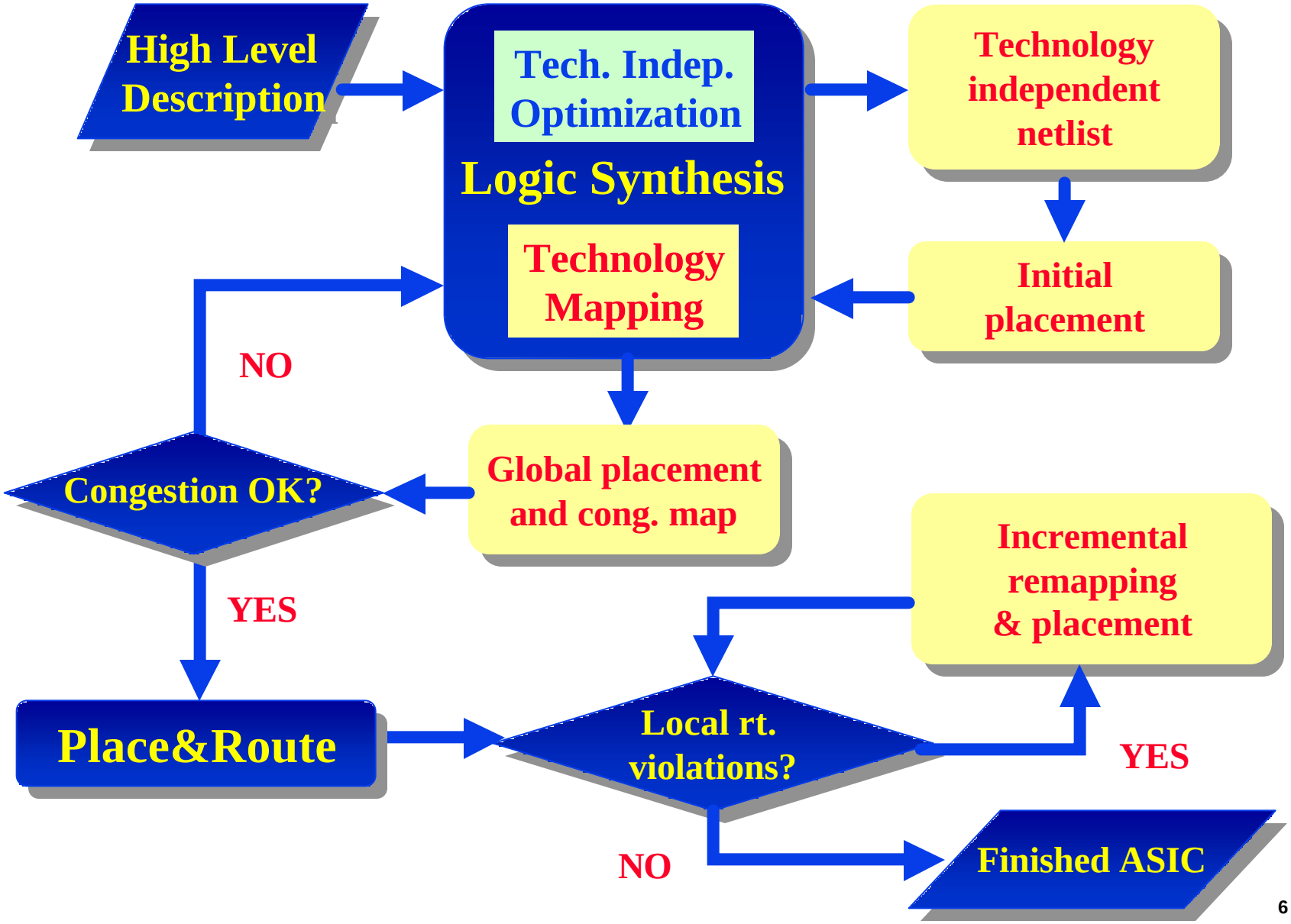
$$COST(m,v) = AREA(m,v) + K \cdot WIRE(m,v)$$

- The impact of wiring cost is controlled by the congestion minimization factor ***K***
  - By increasing ***K*** structurally routable netlists can be efficiently obtained
  - But a purely predictive congestion measure may yield a large cell area and an unroutable design

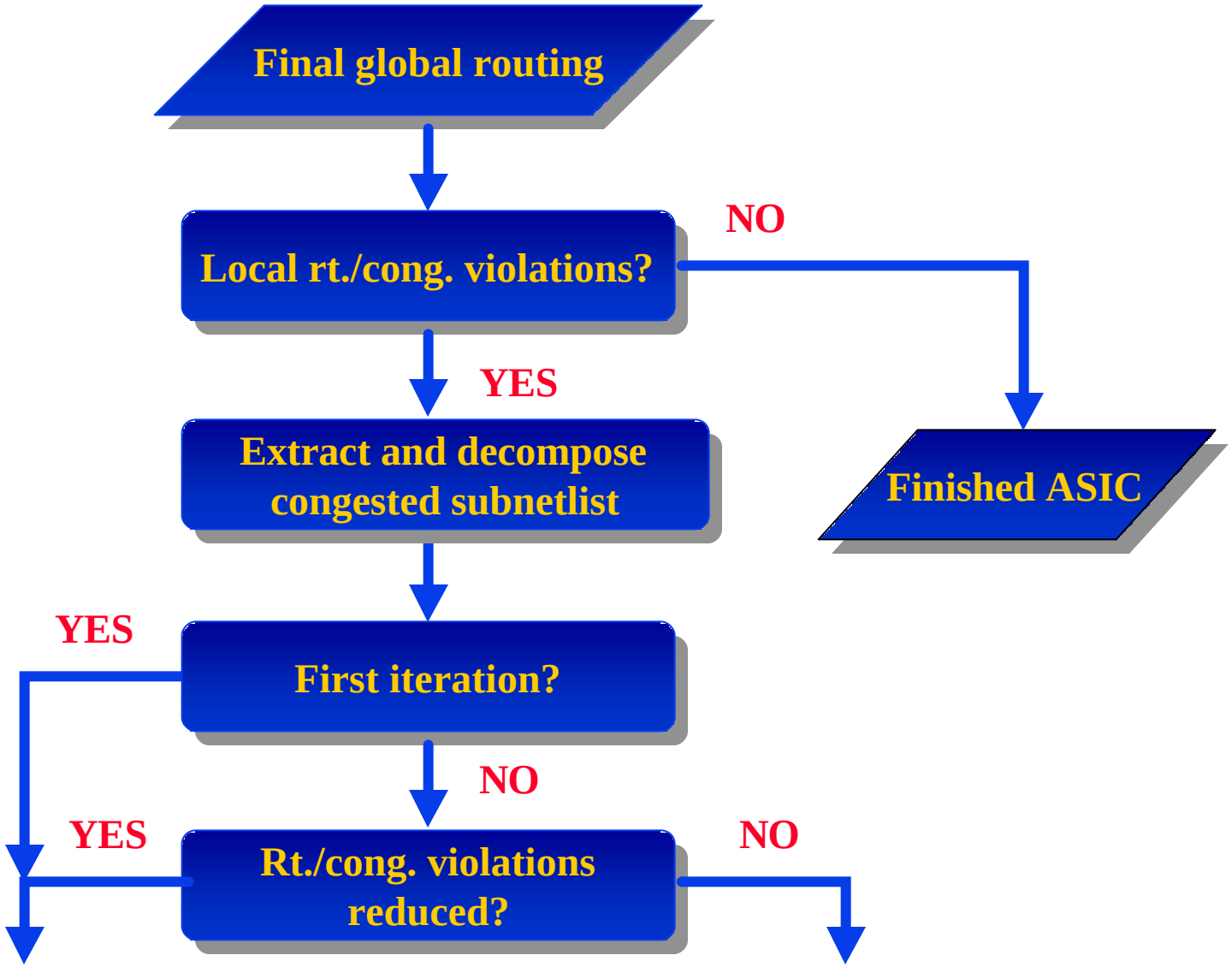
Proposed methodology

- **Our congestion-aware tech mapping approach can be easily integrated into the traditional ASIC design flow**
  - **By increasing the congestion minimization factor *K* structurally more routable netlists can be efficiently generated from the same tech independent netlist and its initial placement**
- **But *a priori* estimation of the optimal *K* value is very difficult**
  - **The optimal *K* value is not constant across the chip layout image**
- **After routing localized congested areas can be incrementally remapped instead of either relaxing the floorplan constraints or resynthesizing the whole circuit**

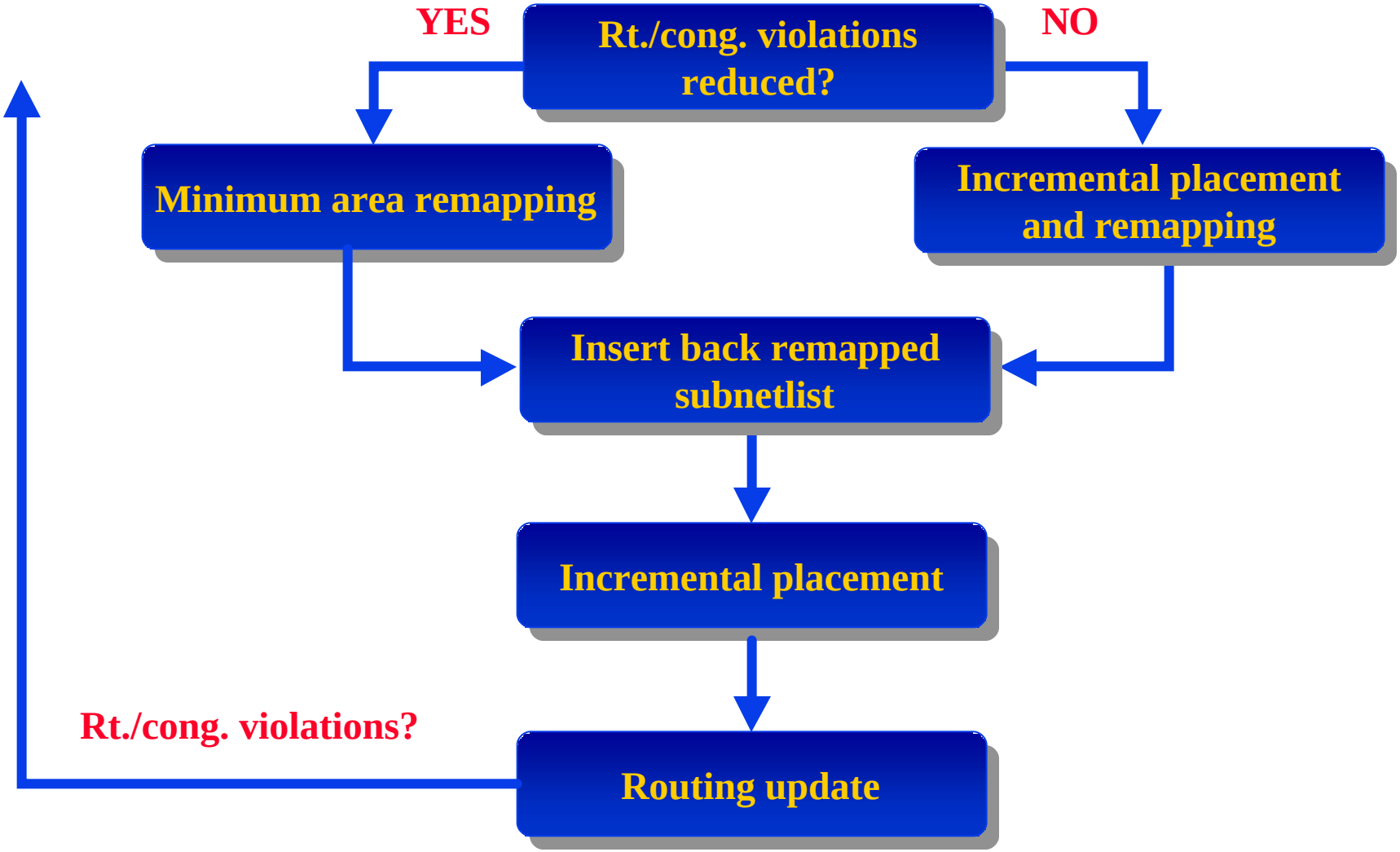
Modified ASIC design flow



Incremental remapping flow (I)



Incremental remapping flow (II)



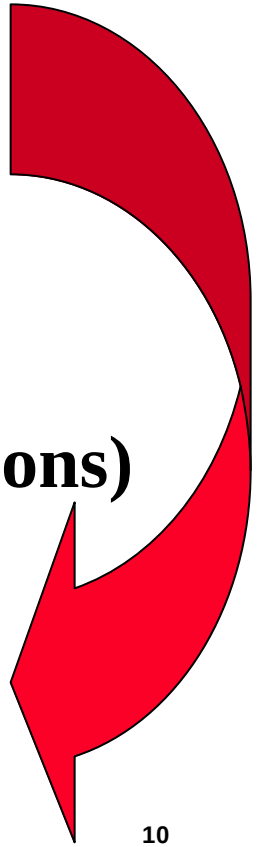
Results

- The incremental flow has been implemented using commercial tools, our congestion-driven tech mapper and various interface utility programs
- The cell library is the CORELIB8DHS™ 2.1, in 0.18㎛m, by STMicroelectronics, Inc., and three metal layers have been used in all experiments
- Circuit PDC (IWLS93)
  - 23K gates
  - Die size == 229786㎛m²
- Industrial circuit (courtesy of Central R&D, STM)
  - 250K gates
  - Die size == 2131133㎛m²

Results

Circuit PDC – Congestion minimization

K	Cell Area (μm²)	Area Utilization %	Rt. violations
0.0	128438	55.89	5447
0.00075	131477	57.22	3673
0.001	132514	57.67	0
0.0025	140161	61.0	28
0.005	147714	64.28	0
0.0075	151769	66.05	0
0.05	163103	70.98	158
0.5	178975	77.89	6270
1.0	180330	78.48	7770



Incremental remapping (28 initial violations)
One iteration

K	Cell Area (μm²)	Area Utilization %	Rt. violations
0.0	139727	60.81	0
0.01	139846	60.86	0

Results

Industrial circuit – Congestion minimization

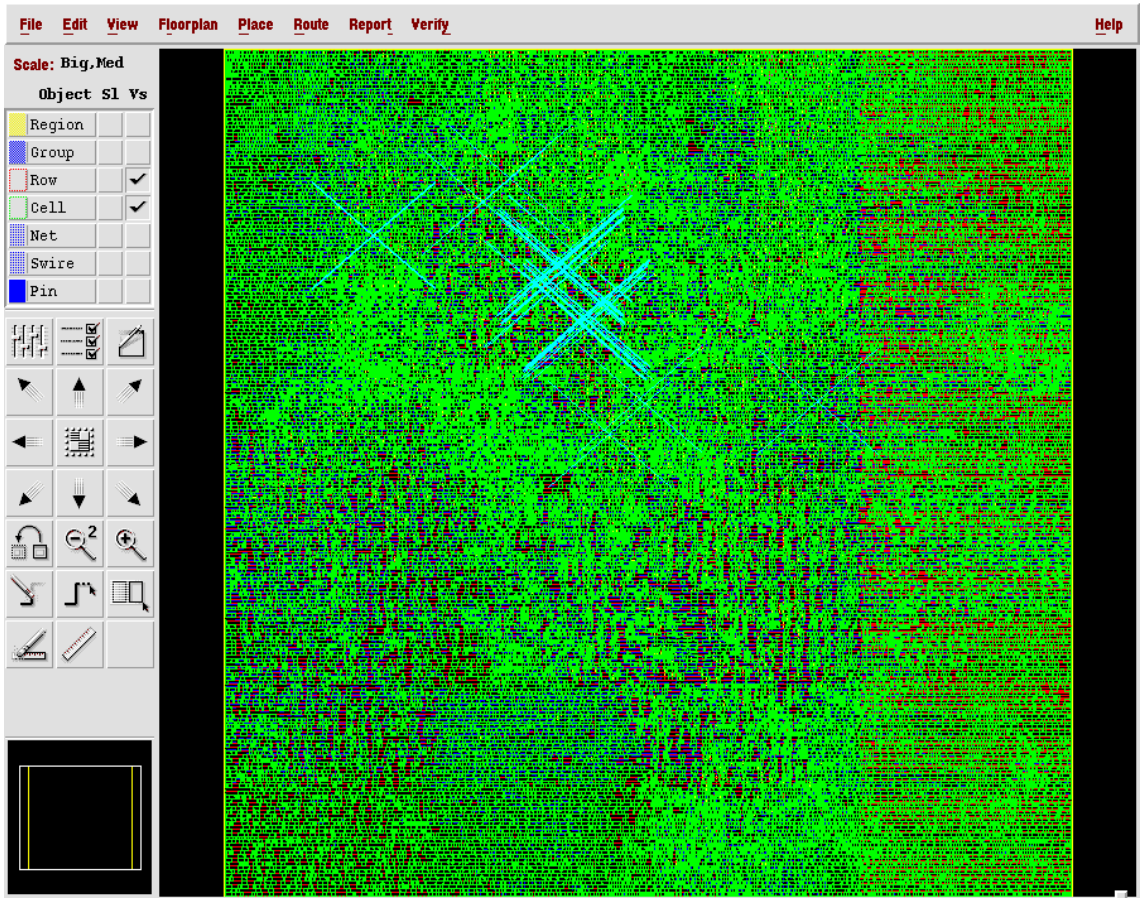
K	Cell Area (μm²)	Area Utilization %	Rt. violations
0.0	1270309	59.61	22466
0.00075	1273250	59.75	29
0.001	1275687	59.86	44

Incremental remapping

Iteration	Cell Area (μm²)	Area Utilization %	Rt. violations
1st	1273225	59.74	25
2nd	1272697	59.72	0

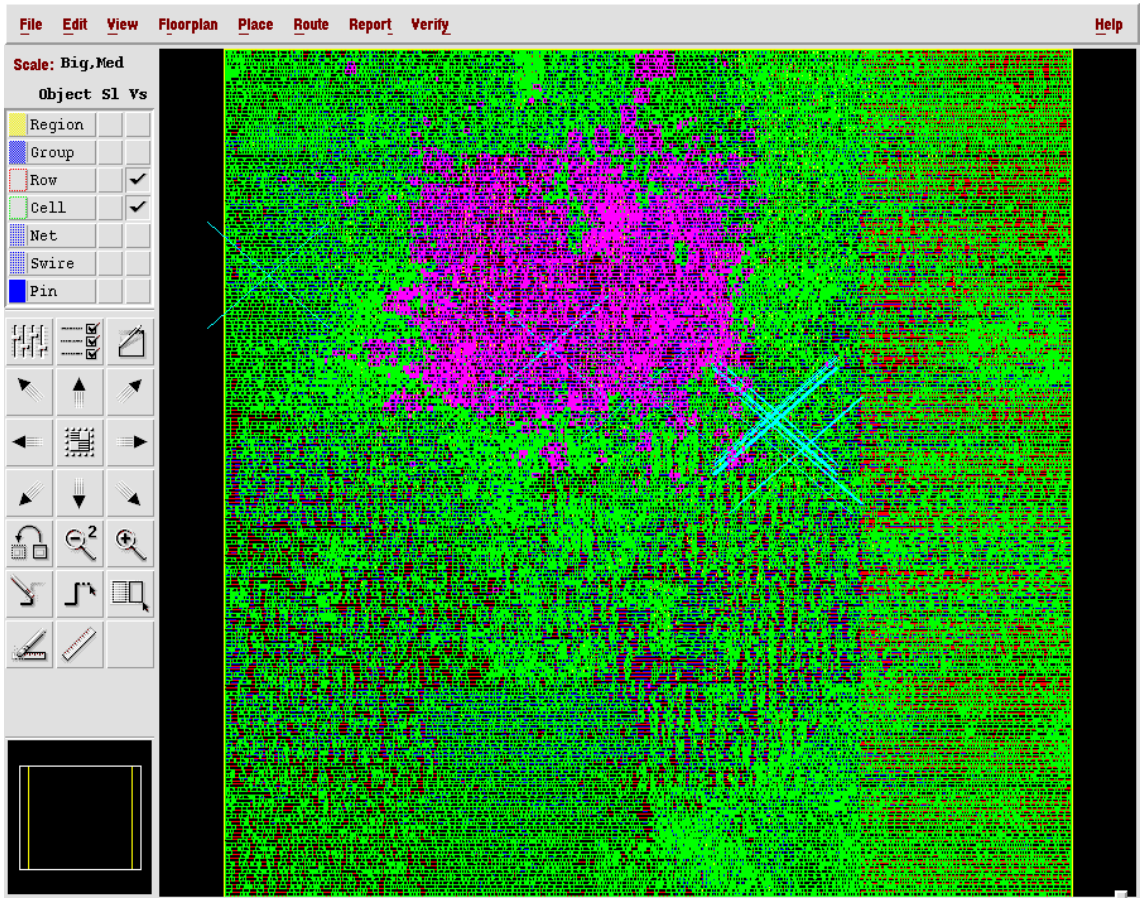
Results

Tech mapping with K == 0.001 – 44 routing violations



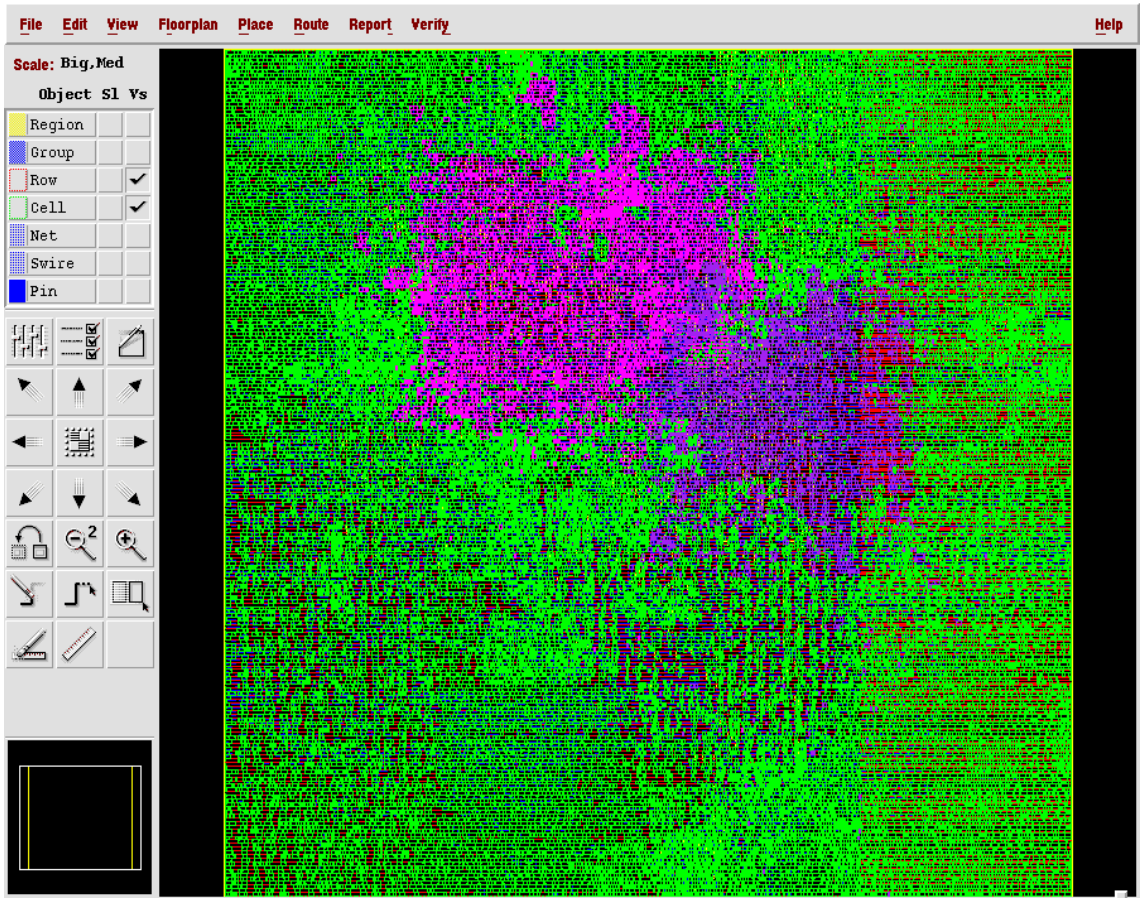
Results

Incremental flow – 1st iteration -- 25 routing violations



Results

Incremental flow – 2nd iteration -- no routing violations



Conclusions

- We proposed a complete, efficient and robust methodology for congestion minimization both at the synthesis and layout stage of the design flow
- Wiring congestion must be considered globally in logic synthesis and locally in physical design
  - The impact of congestion minimization into the synthesis optimization objectives must be carefully evaluated
  - Different layout regions can have very different routing demands
- A single-pass approach for congestion minimization is unlikely to work for all circuits and it will be successful only in a random, unpredictable way