# RC(L) Interconnect Sizing with Second Order Considerations via Posynomial Programming

**Tao Lin and Lawrence T. Pileggi**
**Dept. Electrical and Computer Engineering**
**Carnegie Mellon University**

Electrical & Computer ENGINEERING

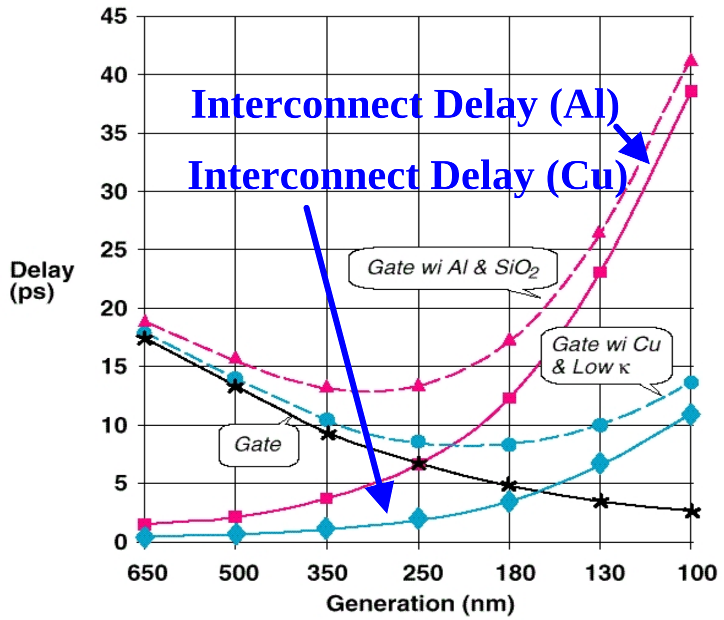
# Outline

- Elmore delay based formulation
- Central moment metrics
- Posynomiality of central moments
- Extension to inductive interconnects
- Applications
- Experiment results

# Interconnect Problem

- The delay due to the *global* RC(L) interconnects is becoming a dominant portion of the overall path delay

- Practical interconnect optimization methods are required for global nets



# Optimization Via Elmore Delay

- Interconnect sizing formulations based on the Elmore delay model:

$$\begin{aligned} &\textit{minimize} && \mathit{Area}(W) && \text{— Minimize the area} \\ &\textit{subject to} && \mathit{Elmore}_k(W) < d_0 && \text{— Delay constraints} \\ &\textit{and} && \underline{w}_i \le w_i \le \overline{w}_i \quad i = 1,\ldots N && \text{— Width bounds} \end{aligned}$$

- Many efficient algorithms have been developed:
  - Lagrange relaxation method
  - Sensitivity based convex programming
  - Local refinement algorithm
  - Sequential quadratic programming

Electrical & Computer ENGINEERING

# Posynomiality of Elmore Delay

- Elmore delay is the first order metric of RC interconnect delay
  - The first moment: $H(s) = m_0 + m_1 s + m_2 s^2 + \ldots$
  - Sum of RC products: $Elmore_k = \sum_{i \in P(k)} R_i \sum_{j \in D(i)} C_j$
  - Function of width: $R_i \propto \frac{1}{w_i} \quad C_i \propto w_i$

$$Elmore_k(w) = \sum_{i \in P(k)} \left(\frac{1}{w_i}\right) \sum_{j \in D(i)} a_{ij} w_j$$

- Posynomial function of sizes:
  - Posynomiality: $f(w_1 \cdots w_n) = \sum a_i (\Pi w_j^{b_{ij}}), a_i > 0$

Electrical & Computer ENGINEERING

# Posynomial Programming

- Posynomial geometric programming:

$$
\begin{array}{lll}
\textit{minimize} & Area(W) & \text{— } \textit{Sum of } w_i{*}l_i \\
\textit{subject to} & Elmore_k(W) < d_0 & \text{— } \textit{Delay constraints} \\
\textit{and} & \underline{w}_i \le w_i \le \overline{w_i} \quad i = 1,\ldots N & \text{— } \textit{Width bounds}
\end{array}
$$

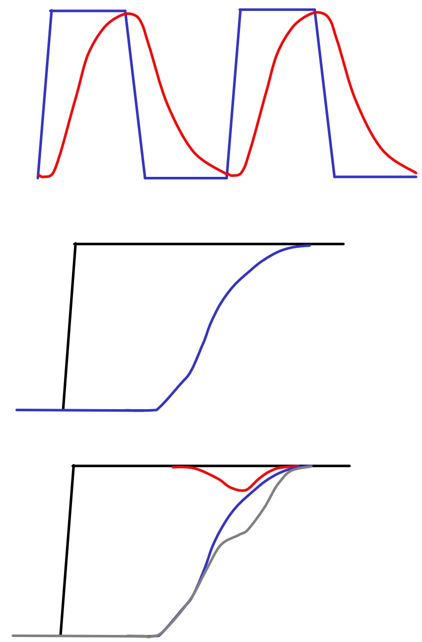
  - A posynomial function can be transformed into a convex function under the exponential substitution:

$$w_j = exp(x_j)$$

  - The interconnect sizing problem is a *convex programming* problem under exponential substitution

# Signal Integrity Problems

- Signal integrity becomes an important issue in giga-scale DSM design
  - Signal quality
    - Clock attenuation
    - Signal transition time
  - Signal uncertainty
    - Noise peak
    - Extra-delay due to noise



# Higher Order Moments

- Limitation of first order metrics
  - Incapable of modeling integrity
  - Incapable of modeling noise
- High order moments:
  - It is trivial to show that higher order moments (RC trees) are also posynomial

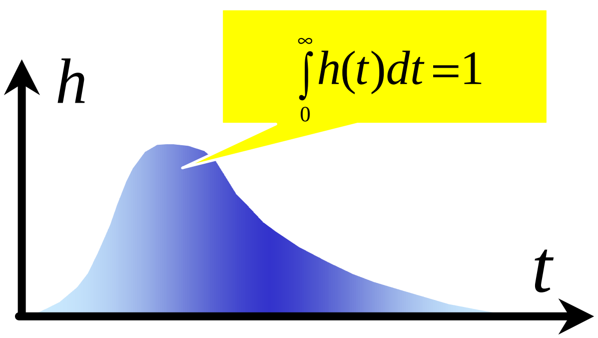
$$m_{2,k} = \sum_{i \in P(k)} R_i \sum_{j \in D(i)} m_{1,j}$$

  - But reduced order models in terms of higher order moments do not preserve posynomiality

$$0.5 = 1 - a_1 e^{-p_1 t} - a_2 e^{-p_2 t} - \ldots$$

# Central Moments

- Definition of the central moments

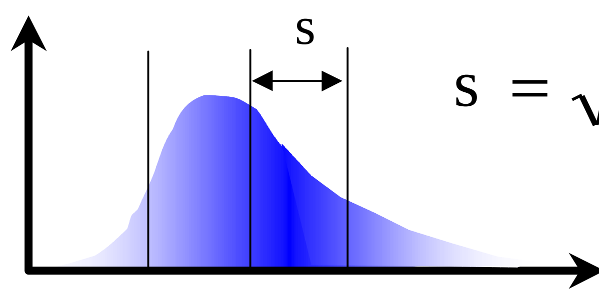



$$m = m_1 \equiv mean$$

$$m_2 = 2m_2 - m_1^{\;2} \quad (variance)$$

$$m_3 = -6m_3 + 6m_1 m_2 - 2m_1^{\;3} \; (skewness)$$

- $\mu_2$ is a natural metric for signal quality/shape
  - Standard deviation
  - Dispersion



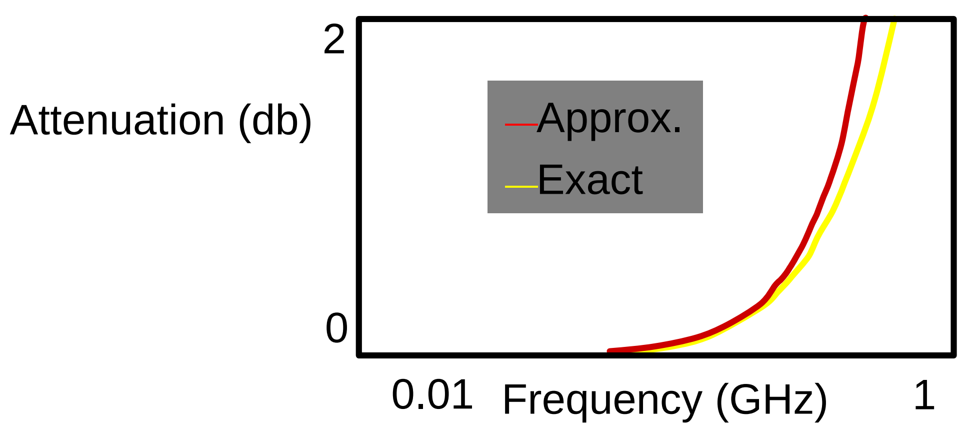

$$s = \sqrt{\mu_2}$$

# Signal Attenuation

- An accurate model for signal attenuation in RCL clock tree [Celik99]

$$a(w) = -10\log(1 - m_2 w^2) \quad (db)$$

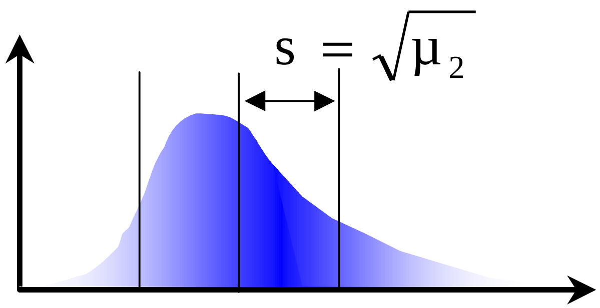
- A provable upper bound for RC responses

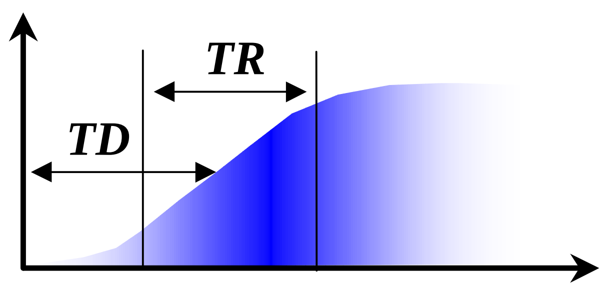



- An upper bound for overdamped cases (RCL)

# Signal Transition

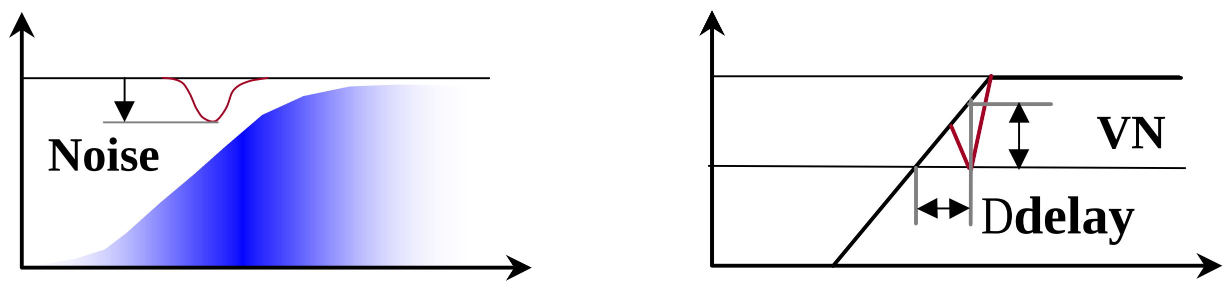
- $\mu_2$ as a metric of RC signal transition time [Elmore48]:
  - Transfer function: $g(s) = 1 - sTD + 0.5s^2(TR^2/2 + TD^2)$
  - Signal transition time: $TR = \sqrt{2pm}\ _2$



# Delay Due To Crosstalk

- $\mu_2$ is a metric of delay uncertainty due to crosstalk noise
  - Assuming a finite ramp input TR and an environment noise Vn
  - Worst case alignment: $\Delta$delay=TR*Vn/Vdd



# Posynomiality Proof

- Is $\mu_2$ a posynomial function of wire widths?

$$m_2 = 2m_2 - m_1^{\;2}$$

  - $m_1$ and $m_2$ in an RC tree are posynomial functions of wire widths
  - $\mu_2$ is provable positive for RC tree response [Gupta97]
- Prove by induction: $\mu_2$ of RC tree response is a posynomial function of wire widths

# For Inductive Interconnect

- High order moments for RCL circuits:
  - $M_2$ is not guaranteed to be positive for RCL circuit responses

$$m_{2,k} = \sum_{i \in P(k)} R_i \sum_{j \in D(i)} m_{1,j} - \sum_{i \in P(k)} L_i \sum_{j \in D(i)} C_j$$

- Modeling of on-chip inductance
  - A simple linear model for embedded wire

$$L \approx mt / w$$

- Posynomial condition of $\mu_2$ (sufficient condition) which can be verified before solving the problem

$$R_k R_D C_L + \frac{1}{4} R_k^{\ 2} C_k \geq L_k$$

# Sizing Formulations

- A posynomial interconnect sizing formulation with second order constraints:

$$
\text{(I)}\quad
\begin{array}{ll}
\textit{minimize} & Area(W) \\
\textit{subject to} & m_{1,k}(W) \le d_0 \\
\textit{and} & \mu_{2,k}(W) \le s_0 \\
\textit{and} & \underline{w}_i \le w_i \le \overline{w}_i \quad i = 1, \ldots N
\end{array}
$$

- The inequality constraints on $\mu_2$ represent the constraints on signal quality
  - Attenuation: $a(w) = -10 \log(1 - m_2 w^2) \le a_0$
  - Transition time: $TR = \sqrt{2 p m_2} \le TR_0$

Electrical & Computer ENGINEERING

# Sizing Formulations

- For clock tree sizing problems, the delay constraints are equality constraints in order to achieve zero skew solutions

$$\begin{array}{ll} \text{minimize} & Area(W) \\ \text{subject to} & m_{1,k}(W) = d_0 \\ \text{and} & \mu_{2,k}(w) \leq s_0 \\ \text{and} & \underline{w}_i \leq w_i \leq \overline{w}_i \quad i = 1,\ldots N \end{array}$$

- Given the posynomiality of the constraints, the above problem can be solved via a multi-stage approach. Each stage involves solving a problem of (I). [Celik99][Kay97]

# Sizing Formulations

- The posynomiality can be applied to other type of sizing formulations

(II)

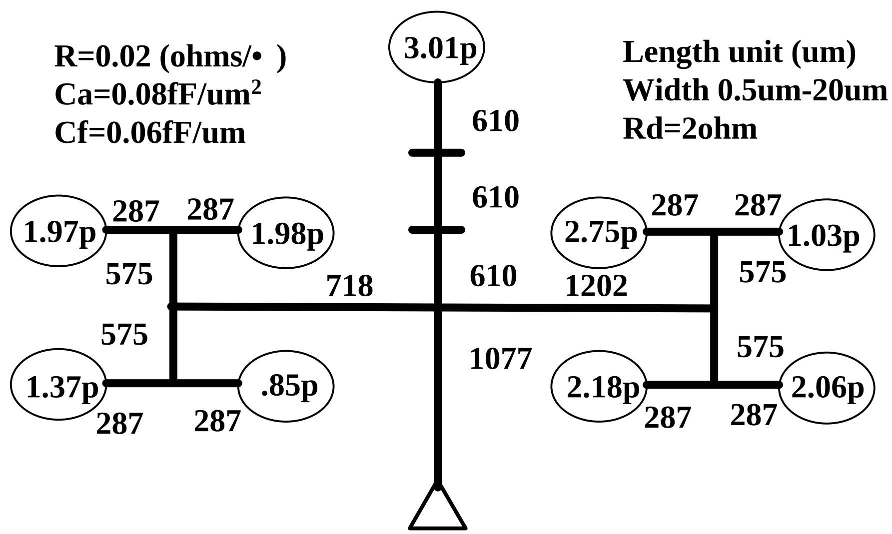
$$
\begin{array}{lll}
\text{minimize} & Max\ delay\,(W) & \\
\text{subject to} & Area\ (W) \le a_0 & \\
\text{and} & \mu_{2,k}(W) \le s_0 & \\
\text{and} & \underline{w}_i \le w_i \le \overline{w}_i & i = 1,\ldots N
\end{array}
\quad \Rightarrow \quad
\begin{array}{lll}
\text{minimize} & dmax & \\
\text{subject to} & Delay_{1,k}(W) \le dmax & \\
\text{and} & Area\ (W) \le a_0 & \\
\text{and} & \mu_{2,k}(W) \le s_0 & \\
\text{and} & \underline{w}_i \le w_i \le \overline{w}_i & i = 1,\ldots N
\end{array}
$$

- Sizing formulations (I) and (II) are both posynomial programs as the Elmore delay based sizing problems

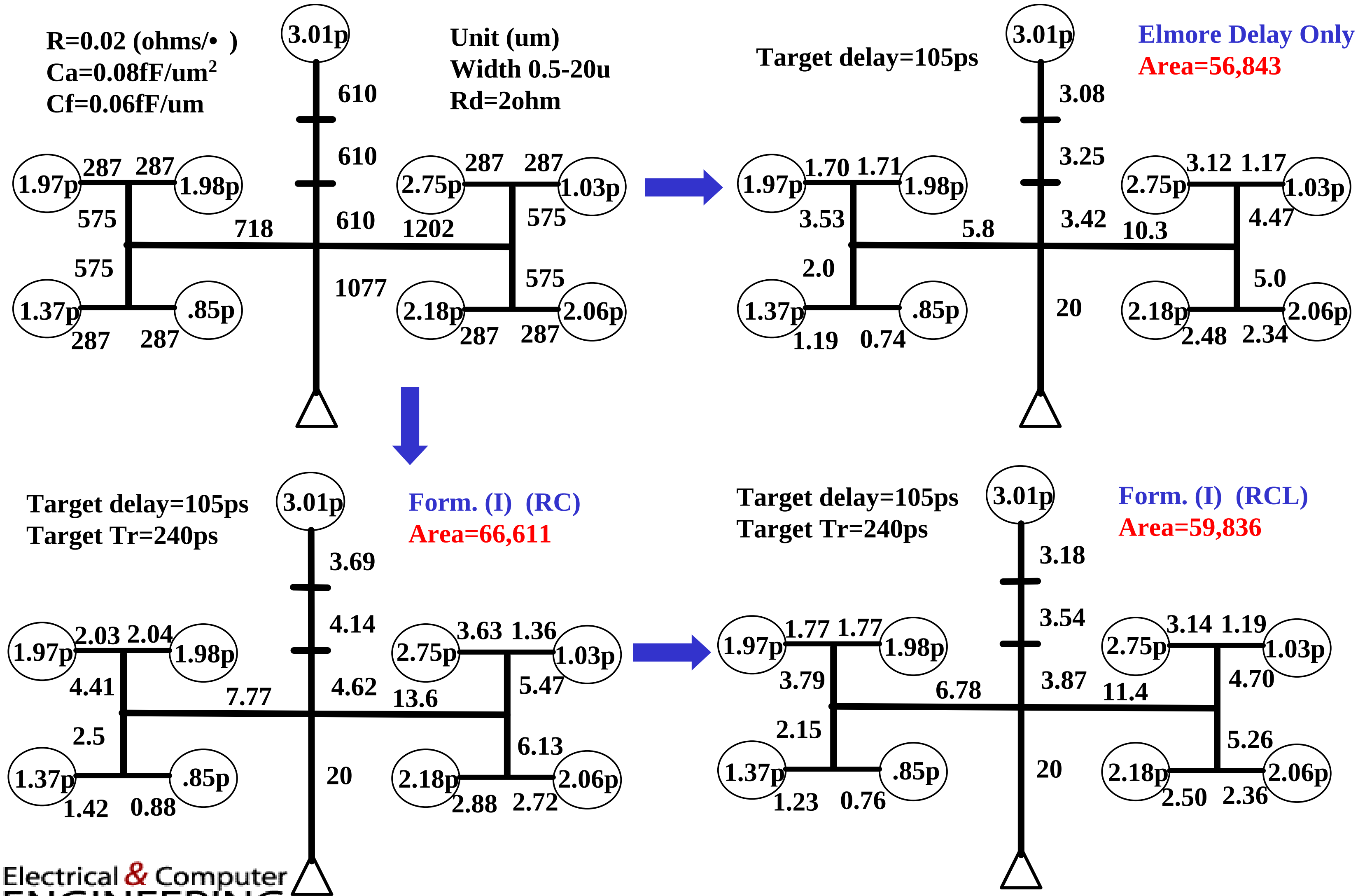
# Experiments

- Extend sequential quadratic programming wire sizing algorithm (ORCIDS)
  - Provable convergence
  - Compute $\mu_2$ in $o(n)$ complexity by path tracing
  - Match the  second order moments of transmission line models [Yu95]
- Example:
  - Design Constraints:

$$Delay \le 105 \; ps$$
$$TR \le 240 \; ps$$



# Experiment Results




Electrical & Computer ENGINEERING

# Conclusions

- The second central moment is a posynomial metric of interconnect signal integrity
- Interconnect sizing problems with second order signal integrity constraints are formulated as posynomial programs
- The existing algorithms can be extended to solve the new sizing problems with provable convergence