Overcoming Wireload Model Uncertainty in Physical Design

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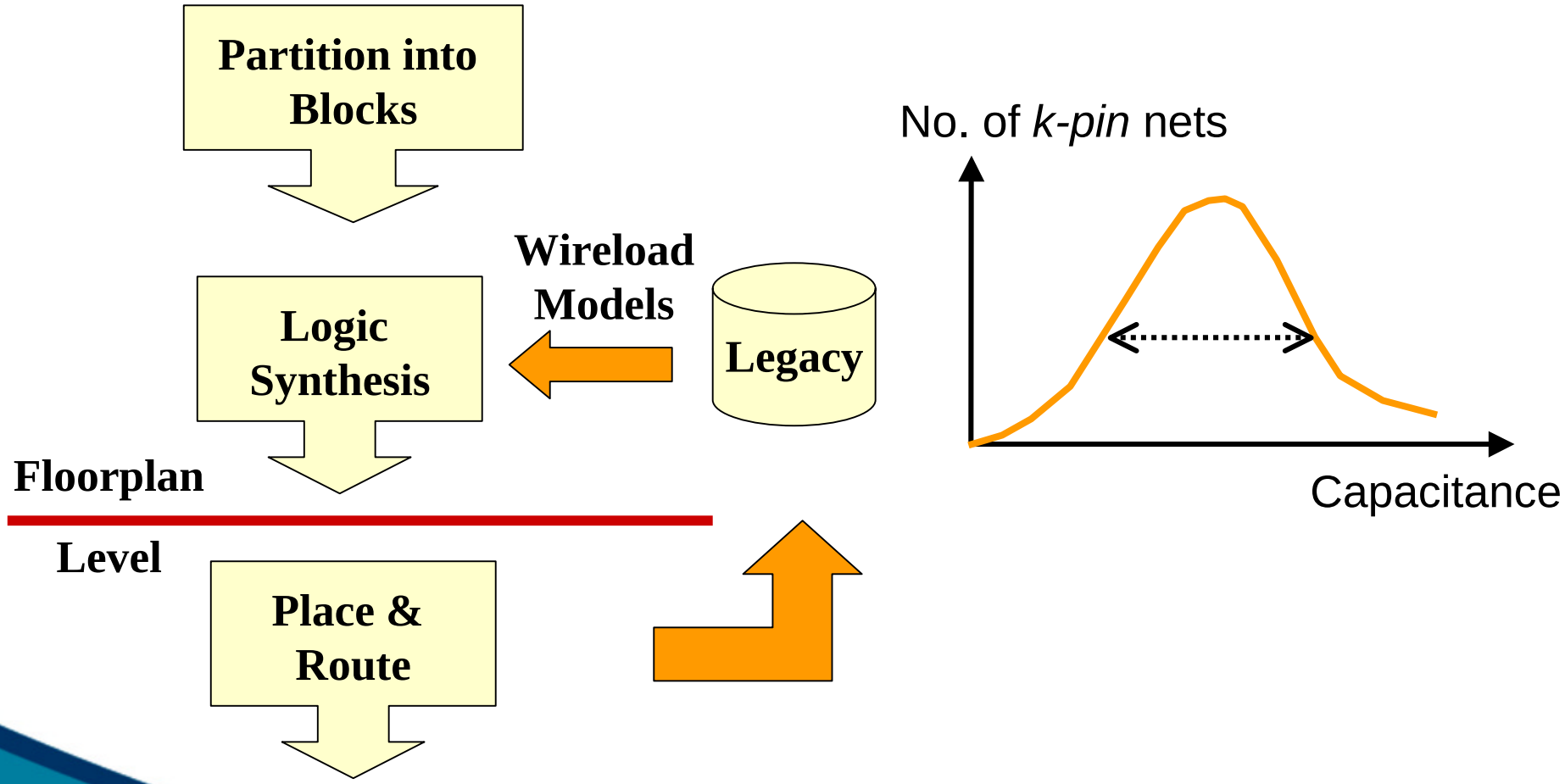
Acknowledgements

- **Monterey R&D**

Outline

- Motivation
- The truth about interconnect dominance
- Uncertainty in interconnect estimation
- Will it change design flows?
- Conclusions

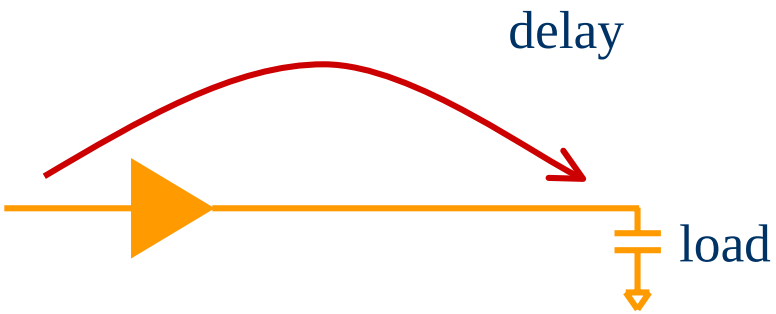
Block Based Design



Interconnect Estimation

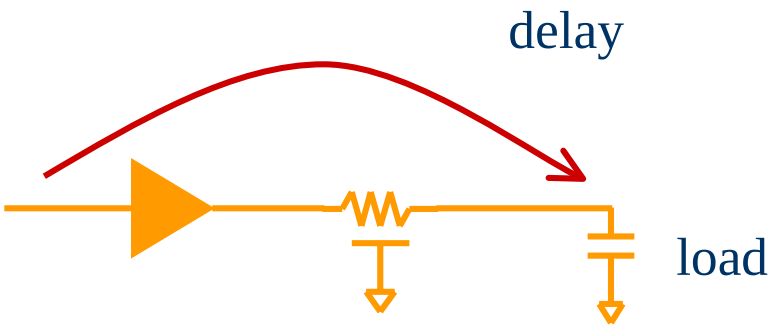
- Need early estimation
- Need accurate estimation
- Estimation error and stage delay
- What does it depend on?

Impact of Interconnect on Delay



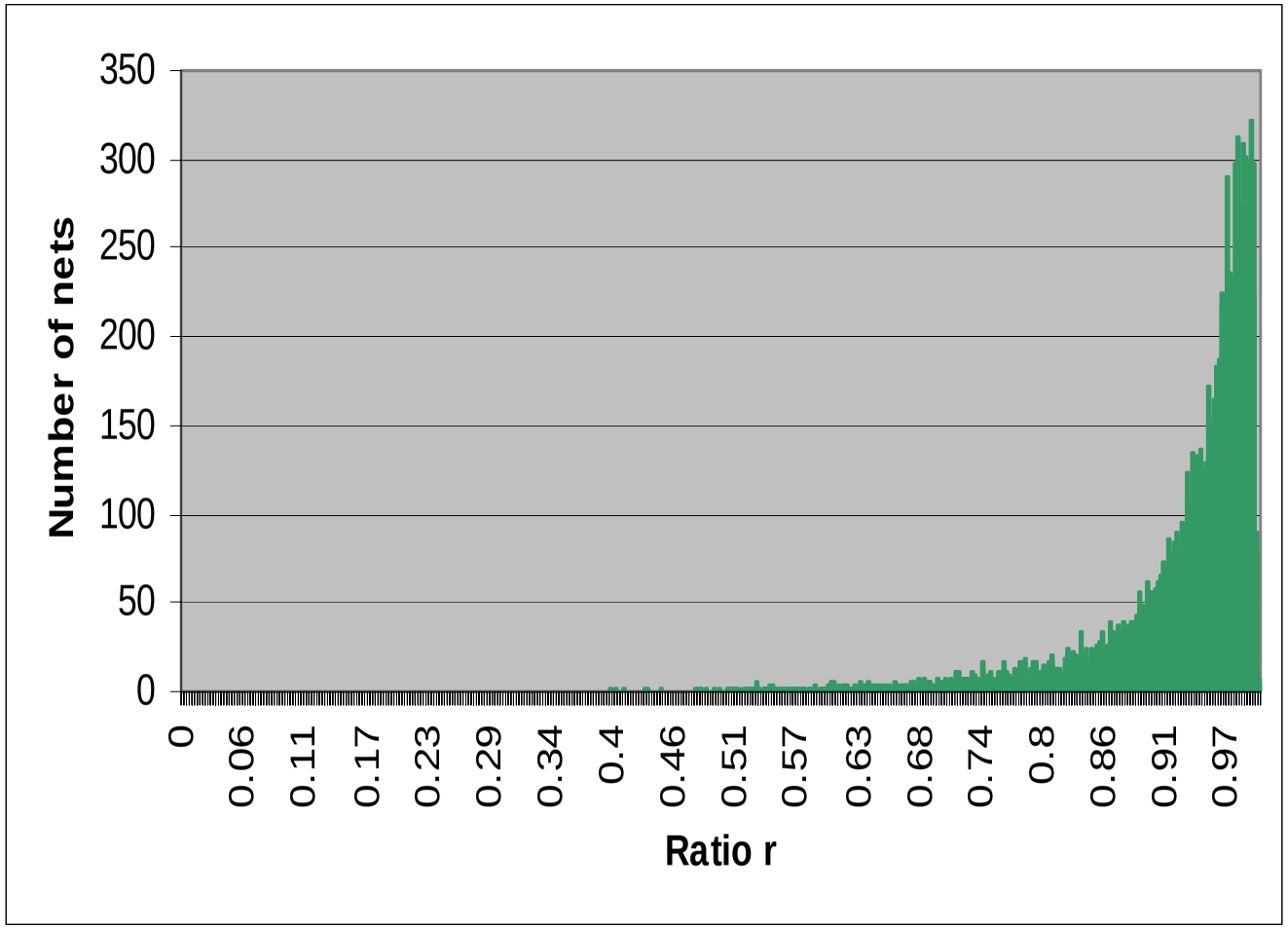
delay without interconnect

Impact of Interconnect on Delay



$$r = \frac{\text{delay without interconnect}}{\text{delay with interconnect}}$$

Impact of Interconnect on Delay

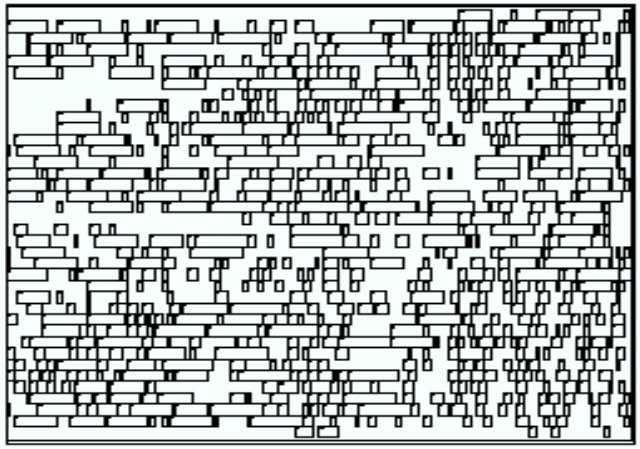


Interconnect Estimation Error

- **Estimation error and stage delay**
- **Best case**
  - Get estimate from actual values
- **Compare estimates with real values**

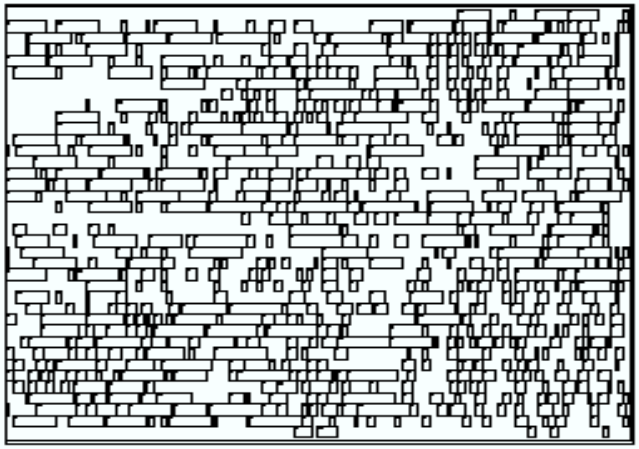
An Experiment

- **Consider a placed and routed design**
- **Meets constraints**



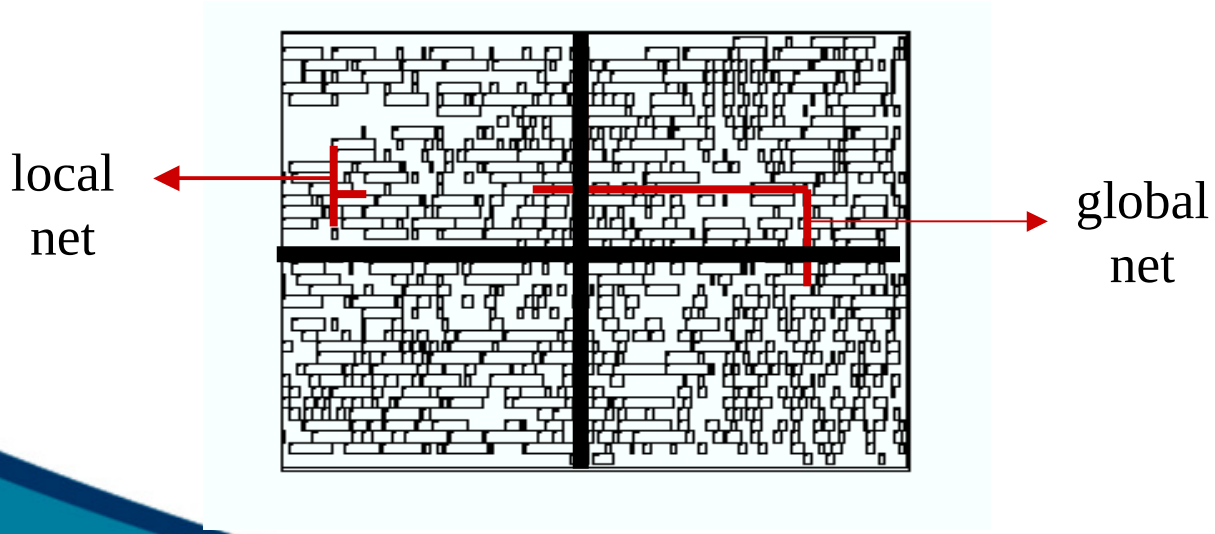
An Experiment

- **Design partitioned into blocks**



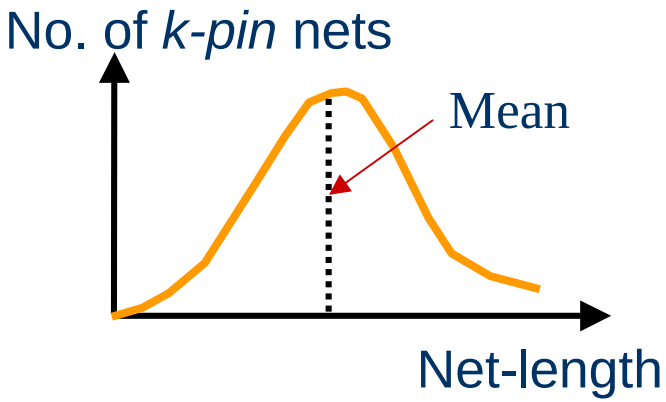
An Experiment

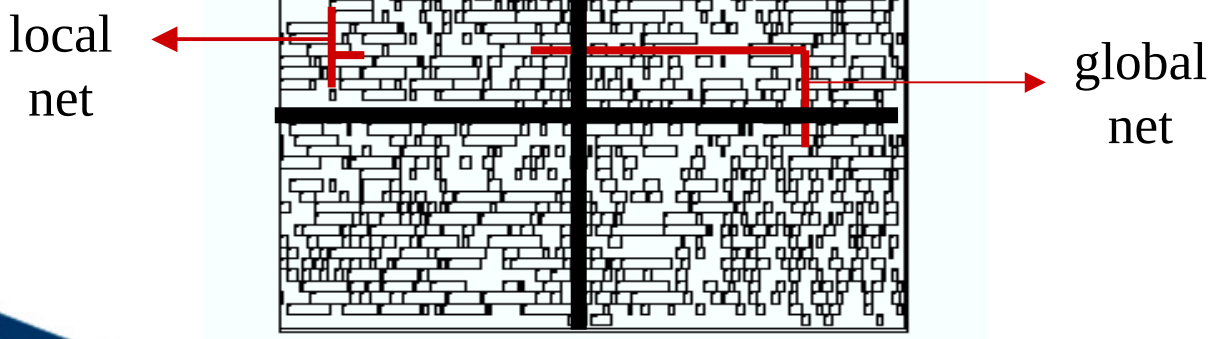
- **Design partitioned into blocks**



An Experiment

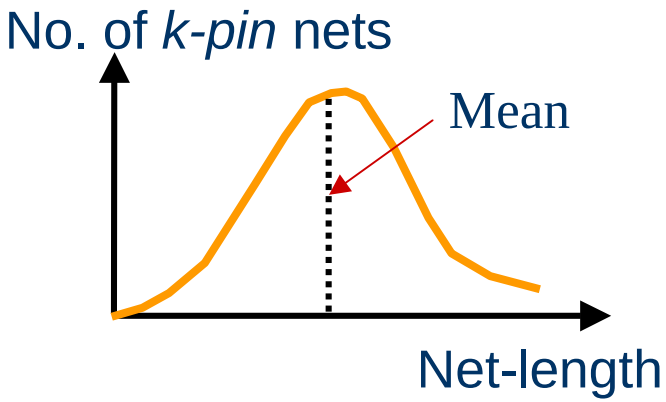
- **Use actual detailed placement**
- **Steiner model for nets**

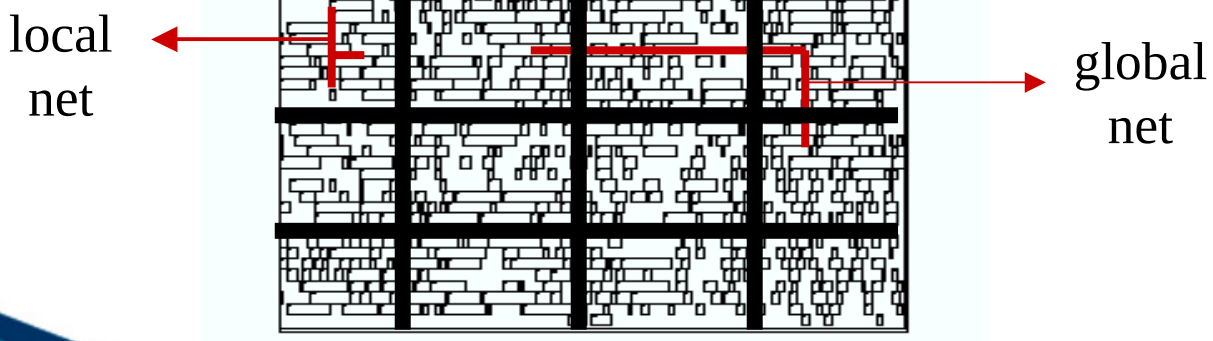




An Experiment

- **Consider different block sizes**



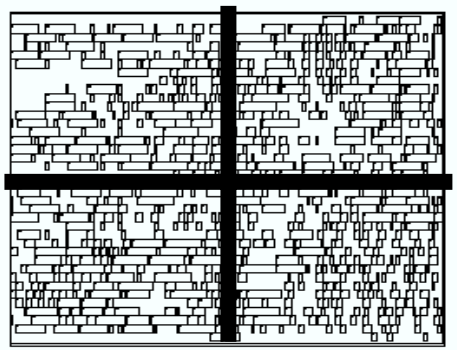


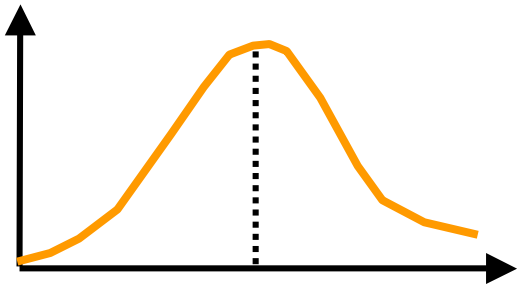
Best-case Wireload Model

- **Estimated capacitance**
  - Mean wirelength from detailed placement
- **Actual capacitance**
  - Actual wirelength from detailed placement

$$r_1 = \frac{\text{delay with estimated capacitance}}{\text{delay with actual net capacitance}}$$

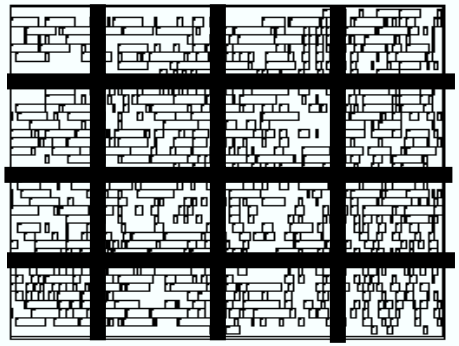
Best-case Wireload Model

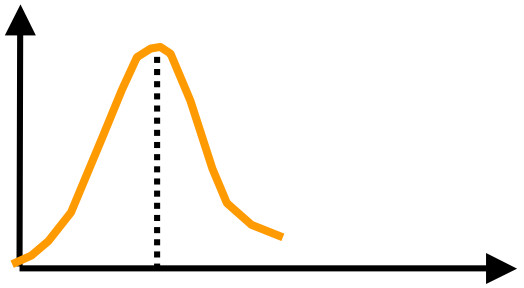




$$r_1 = \frac{\text{delay with estimated capacitance}}{\text{delay with actual net capacitance}}$$

Best-case Wireload Model





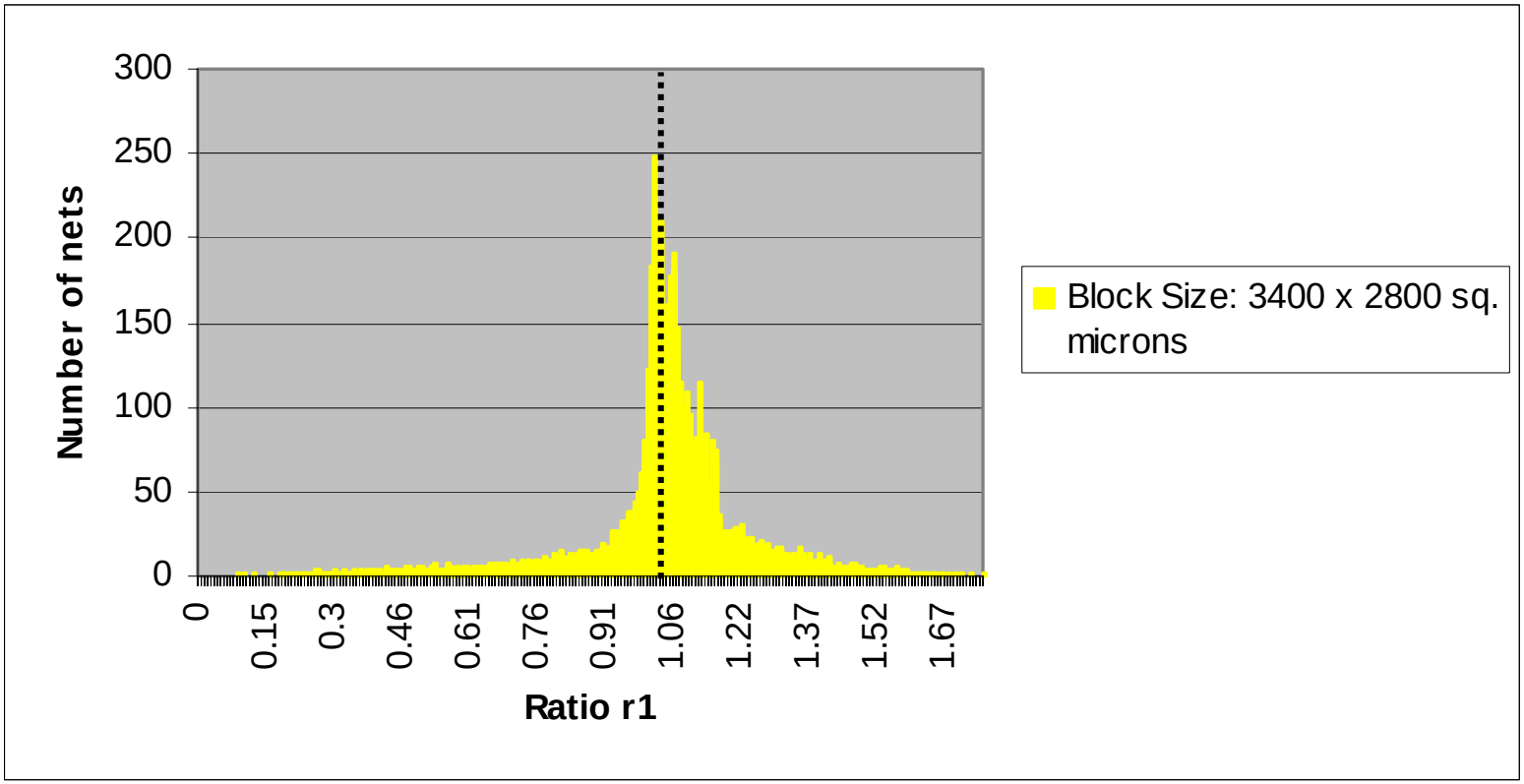
$$r_1 = \frac{\text{delay with estimated capacitance}}{\text{delay with actual net capacitance}}$$

Best-case Wireload Model

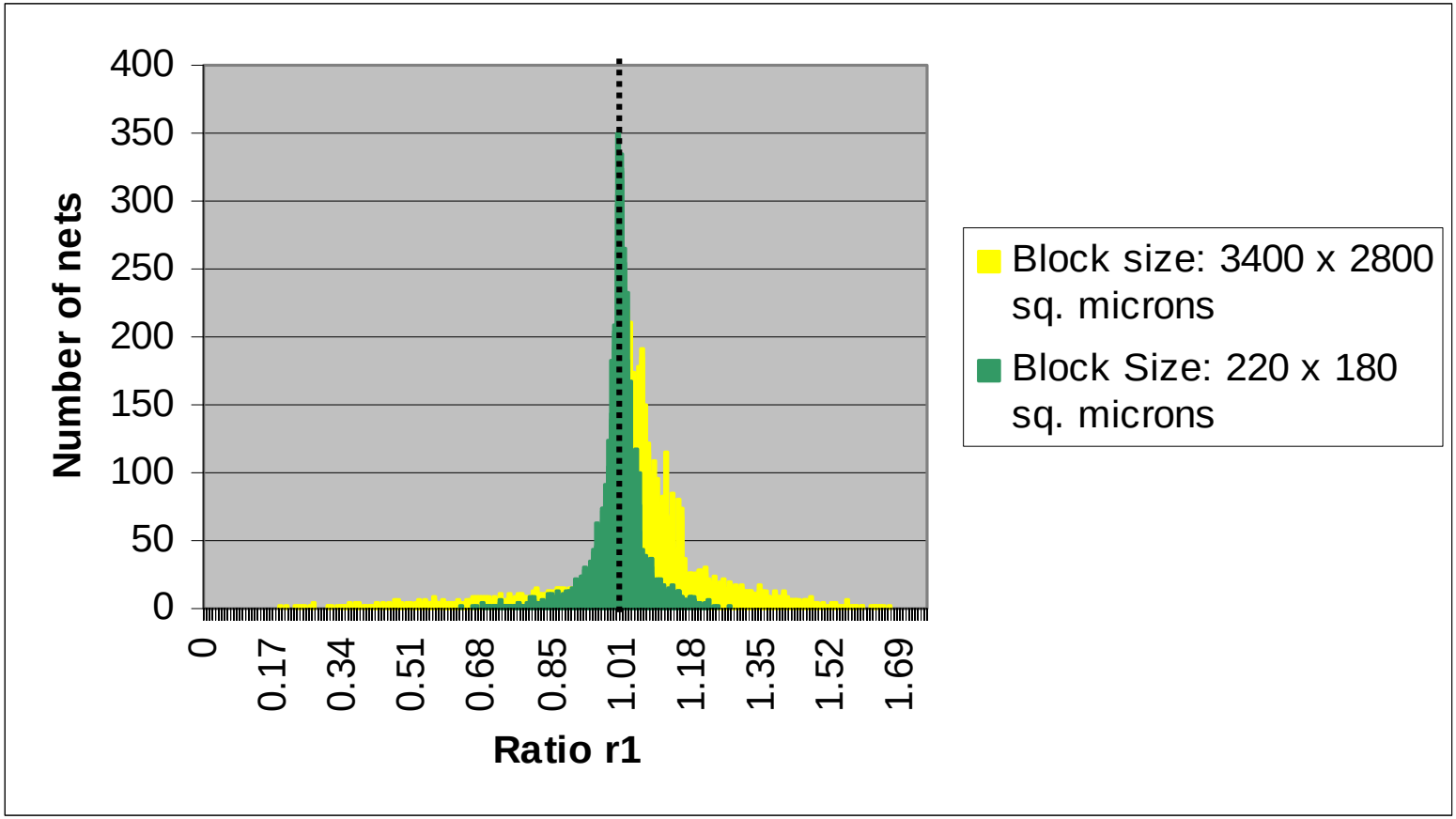
- **Profiles for an industry design**
  - 0.18 micron, 144k gates
  - Distribution of ratio r_1 over 2 pin ‘local’ nets
  - Different block sizes

$$r_1 = \frac{\text{delay with estimated capacitance}}{\text{delay with actual net capacitance}}$$

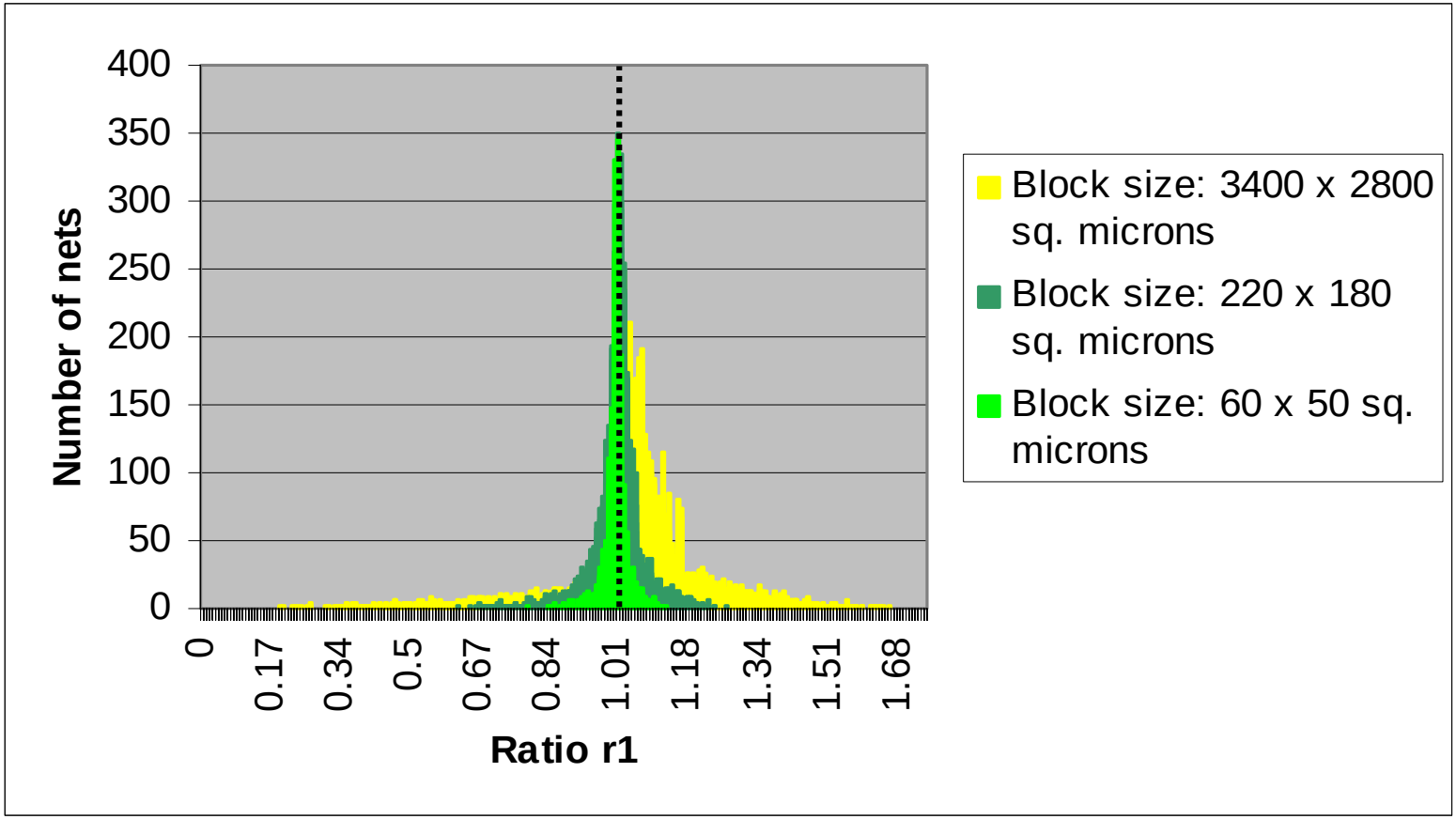
Best-case Wireload Model



Best-case Wireload Model



Best-case Wireload Model



As Good As It Gets

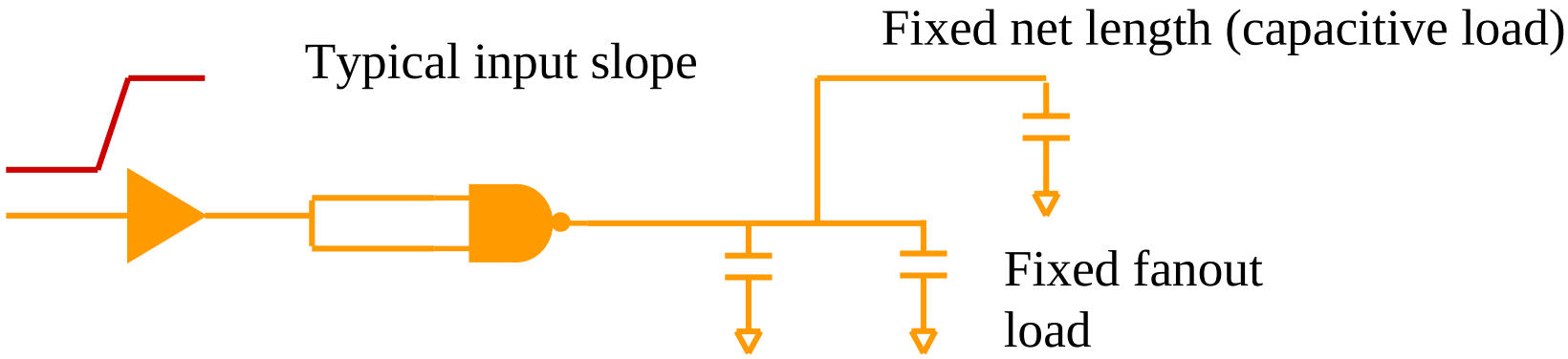
- **Actual and estimated delays differ**
- **Not surprising!**
  - Use mean of distribution
  - What about deviation?
- **Breaks down for large block sizes**
- **Improves for smaller block sizes**

As Good As It Gets

- **Best-case model breaks down at some block size**
- **Error in gate-level synthesis?**
- **Ignored routing issues**
  - congestion, obstacles, layer assignments, vias and jogs
  - extracted (and more exact) capacitances and resistances

Who's driving?

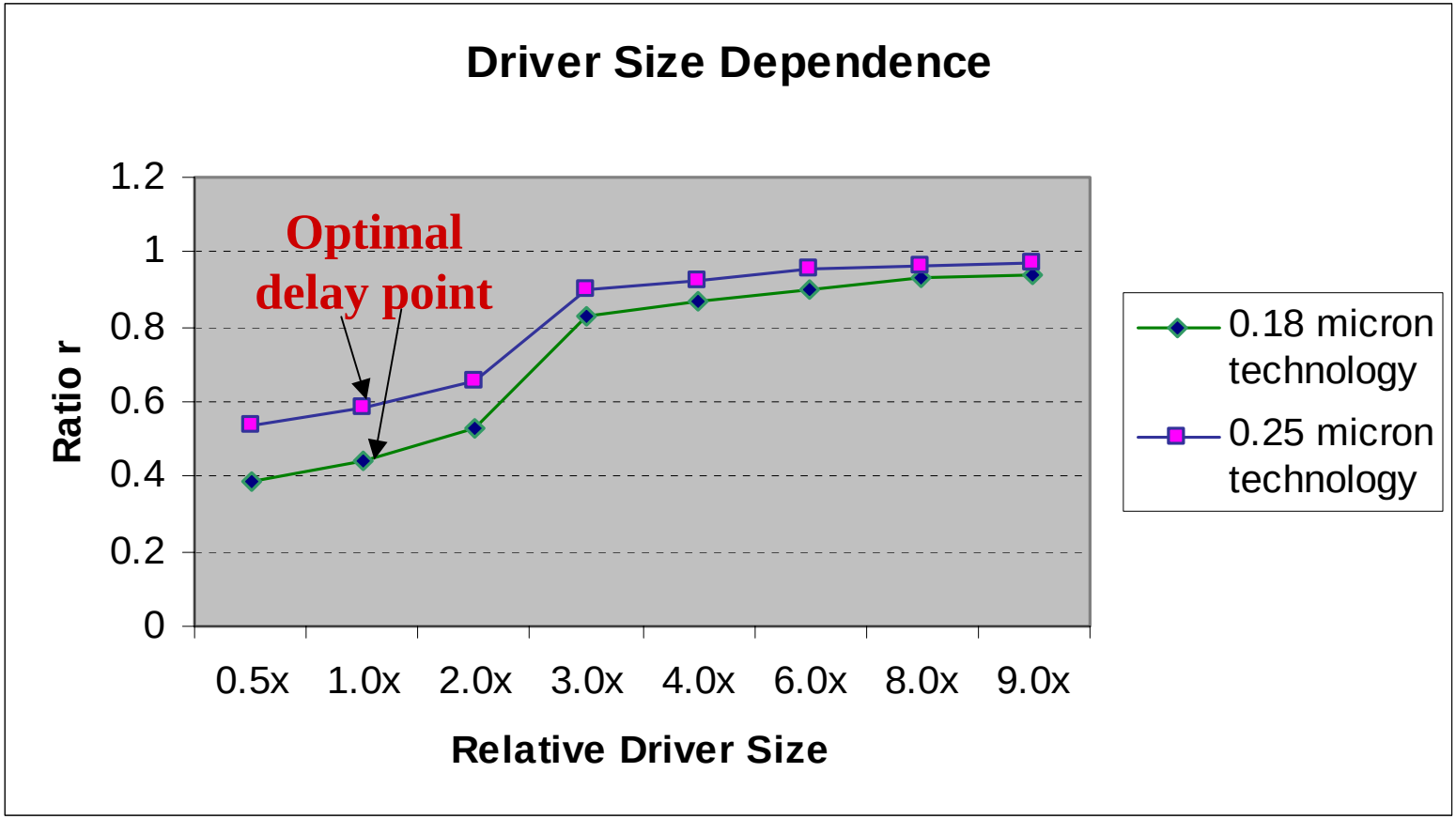
- **Experiment : vary driver sizes**



$$r = \frac{\text{Fanout delay without interconnect}}{\text{Fanout delay with interconnect}}$$

- **Only capacitive effects seen here**

Who's driving?



Choice of Driver Sizes

- **Optimal choice of driver ?**
  - Minimum delay, reasonable output slope
  - Low value of *r*
- **Strong driver**
  - Neglect interconnect capacitance
  - May be sub-optimal!
- **Longer net $\Rightarrow$ resistive effects dominate**

Criticality of Layer Assignment

- **Layer assignment impact is process specific**
- **Variations affect wireload model error**
- **Via resistances**
- **Coupling capacitances**
  - Neighboring routes and switching

Design-specific Dependencies

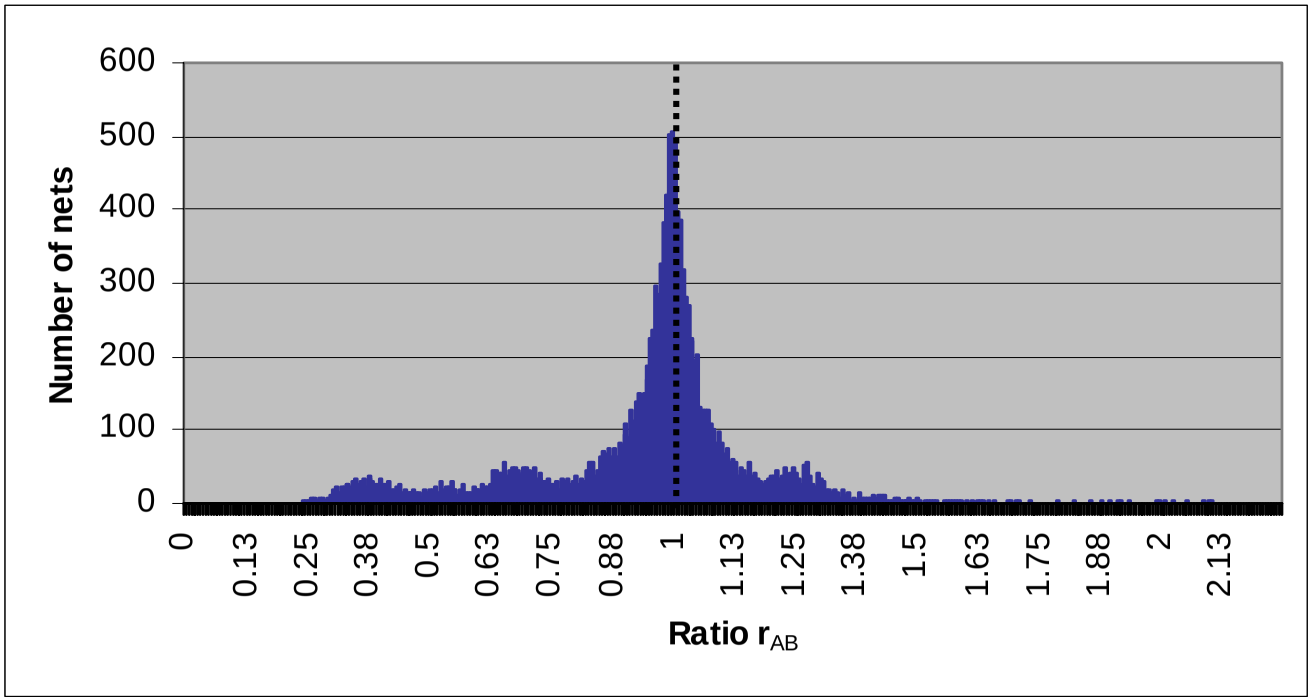
- Depends on congestion
- Depends on netlist connectivity

Design-specific Dependencies

- **Experiment:**
  - Re-order IO pins for a datapath design
  - 48k gates, 0.25 micron
  - Compare net delays from placed and routed results in both cases

$$r_{AB} = \frac{\text{delay with floorplan A}}{\text{delay with floorplan B}}$$

Dependence on Floorplan



In Summary

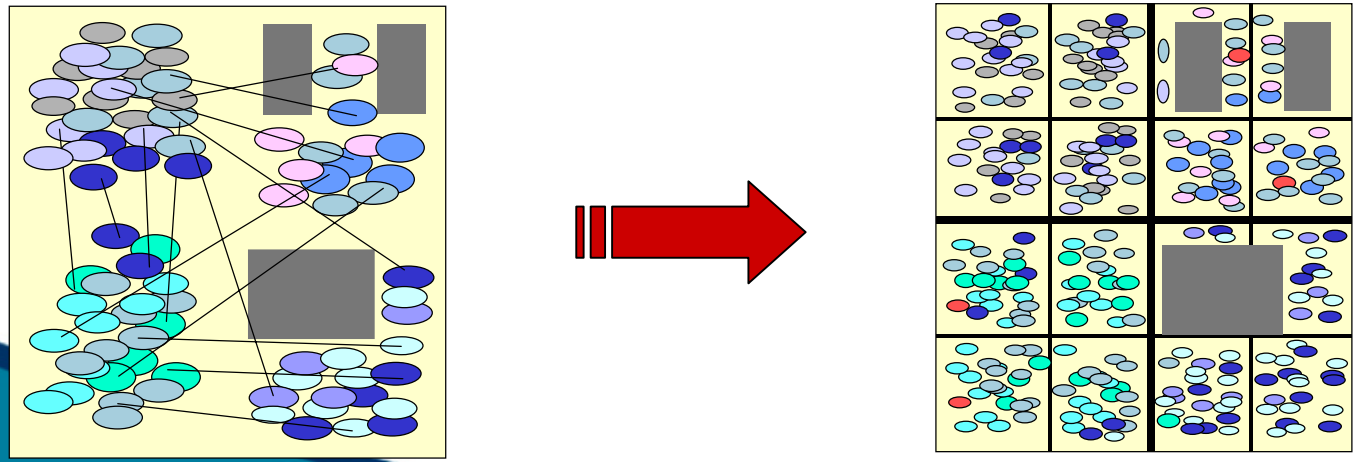
- **Interconnect estimation error**
  - process specifics
  - driver sizes chosen
  - layer assignment, vias
  - coupling capacitances
  - meandering routes, congestion

Design Methodologies Impact

- **Block sizes suitable for synthesis**
- **Synthesis-placement loop**
- **Use strong drivers**
  - [ICCAD98] Sylvester and Keutzer, "*Getting to the Bottom of Deep Sub-micron*"
- **Constant delay synthesis**

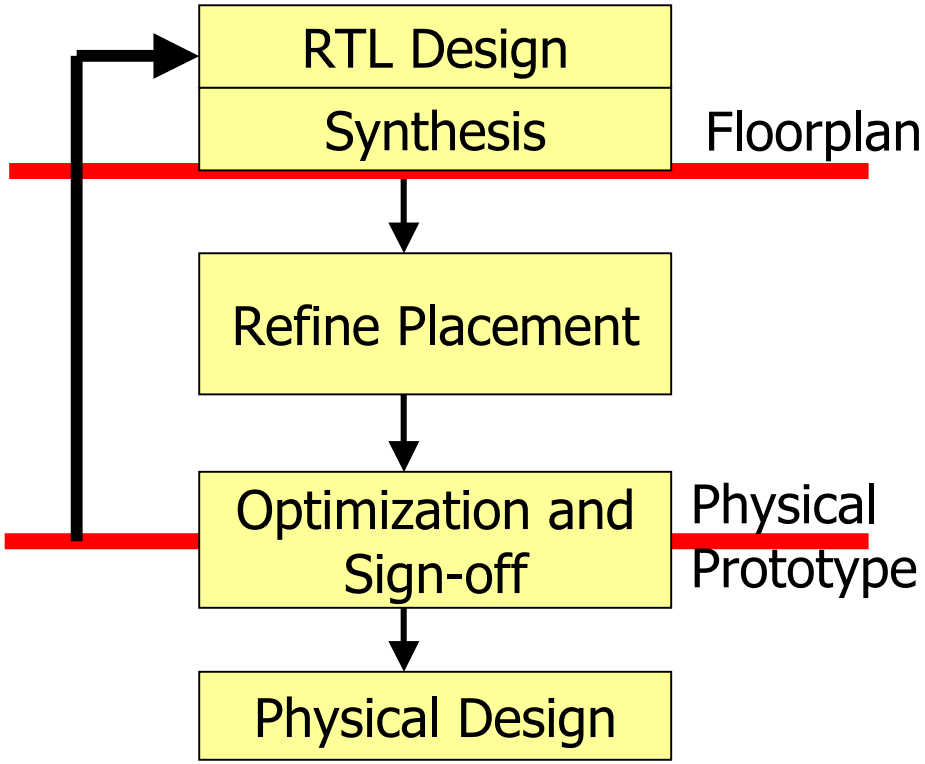
Physical Prototyping

- **Enough detail to sign-off on design**
  - Interconnect estimate/delays make sense
  - Also estimate congestion, power, clock-tree
- **Enough abstraction to explore design**

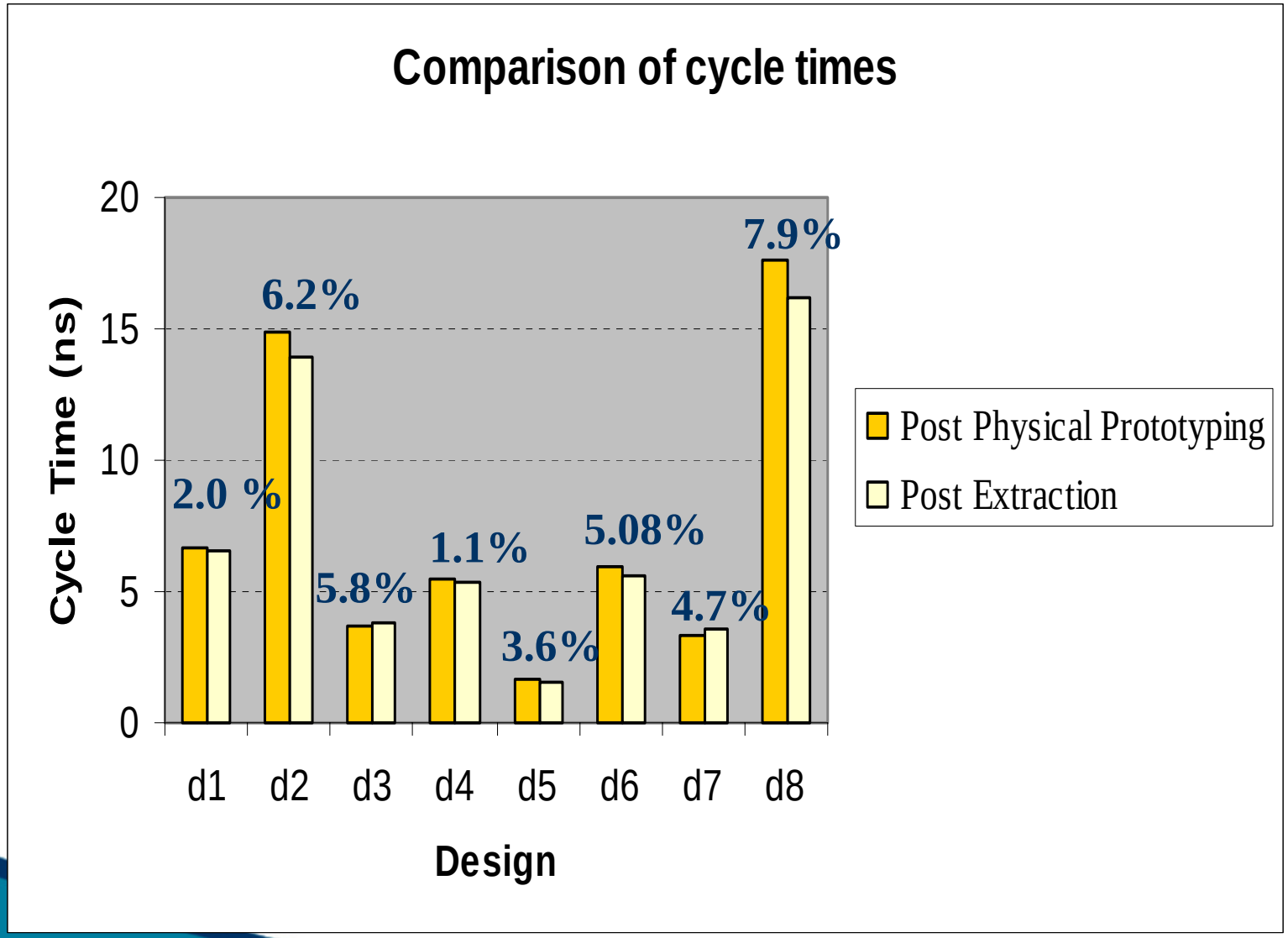


Physical Prototyping

- **RTL Exploration**
- **Floorplan/constraint changes**



Some Results



Conclusions

- **Interconnect estimation**
  - Never fully accurate
  - More refined as physical detail increases
- **Design sign-off**
- **Physical prototyping**
- **Enables new hierarchical design methodology**