Synthesis of Low Power Clock Trees for Handling Power-supply Variations

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Outline

- Clock distribution networks and challenges
- Problem definition
- Parameters affecting clock skew in clock trees
  - Analyze the parameters, variations and their effect on clock skew.
  - Propose techniques to reduce the clock skew.
- Our approach
- Experimental setup and Results
- Conclusions

Clock distribution networks

- **Challenges of clock network synthesis**
  - Satisfy clock skew constraints in the presence of variations.
  - Reduce the power dissipated. (Metric: Capacitance.)

- **Popular structures**
  - Clock trees - Relatively low variation-tolerance, Low capacitance.
  - Clock meshes - High variation-tolerance, High capacitance.
  - Hybrid (mesh + tree, tree + cross-links)

- **Focus of our work: Clock tree structures**
  - Analyze the parameters and variations affecting clock skew.
  - Propose techniques to reduce the clock skew.

Problem definition

Terminology

- **Local sink pairs**
  - Sink pairs closer than a specified distance (*L*).

    L : Local skew distance.

- **Local clock skew (LCS)**
  - Clock skew between any local sink pair.

- **Maximum local clock skew (MLCS)**
  - Many such local sink pairs.
  - Maximum LCS among them.

Problem definition

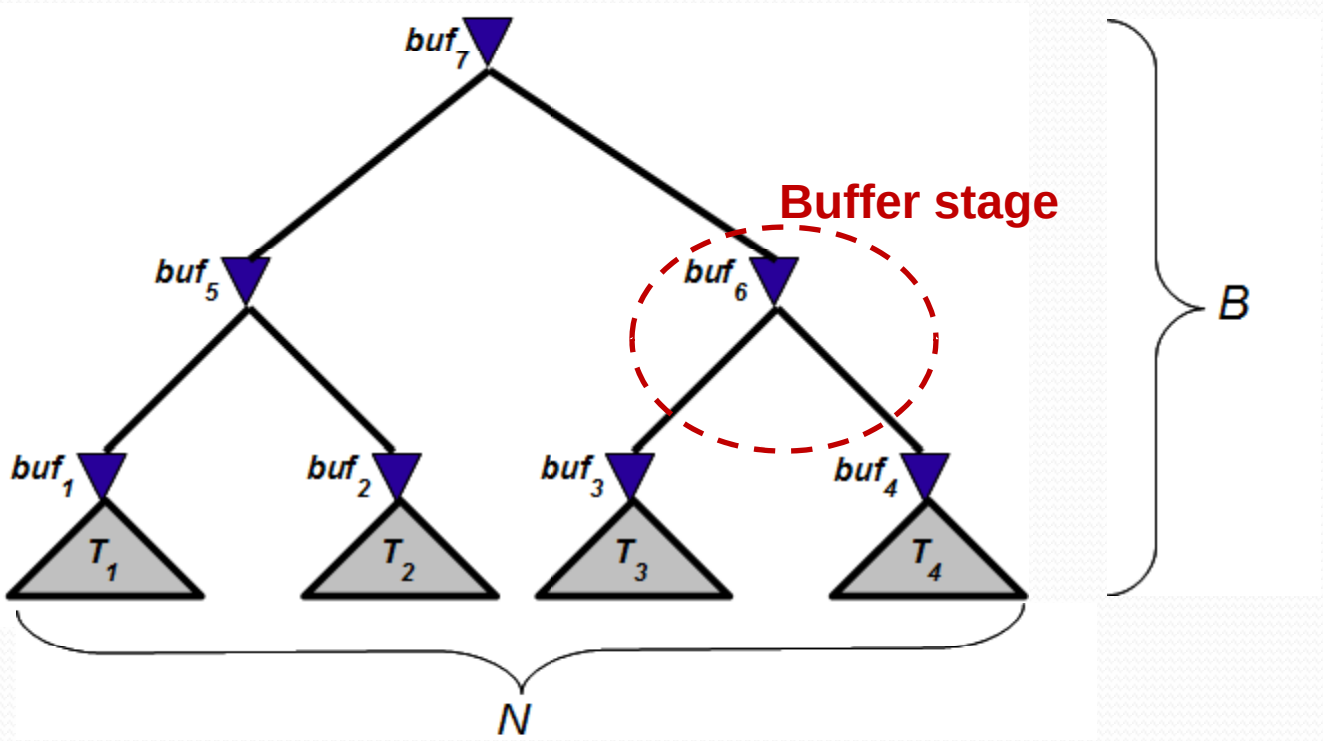
Based on ISPD 2010 contest problem

- **Given**
  - Clock source, sink and blockage locations.
  - Local skew distance, *L*.
  - MLCS limit.
  - Slew limit.
  - Inverter and wire library.
  - Power-supply and wire-width variations (Uniform distribution).

- **Construct a low capacitance (power) clock tree**
  - **Satisfy slew constraint:** Signal slew < Slew limit.
  - **Satisfy blockage constraint:** Inverters cannot be placed over blockages.
  - **Satisfy MLCS constraint:** 95th percentile of MLCS, $MLCS_{95\%}$ < MLCS limit.

Parameters affecting clock skew

- **Clock skew parameters**
  - Number of sinks, *N*.
  - Number of buffer levels, *B*.
  - Delay variation per buffer stage, σ_0.
    - Buffer stage = Buffer + Interconnect it drives.
    - σ_0 is the standard deviation of delay per buffer stage.

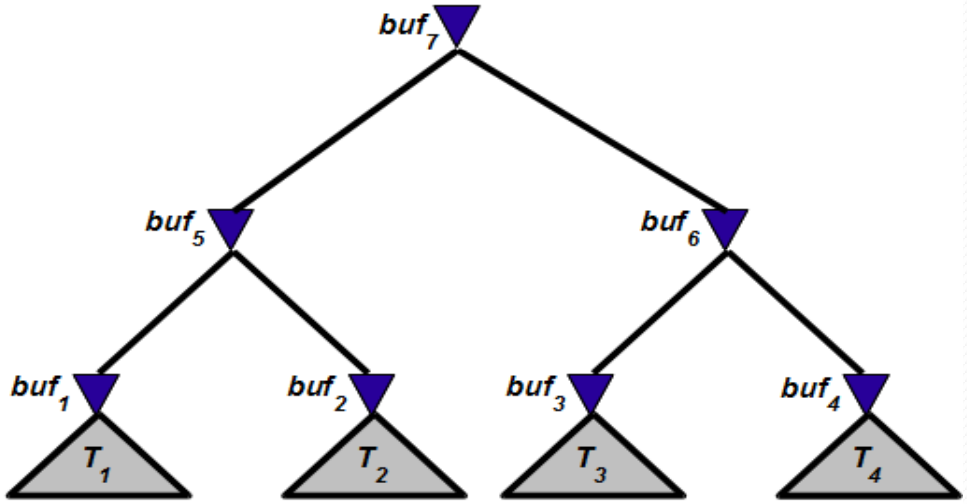


Parameters affecting clock skew

Clock skew under variations

- **Clock tree T_D**
  - Identical path delays from source to sinks.
    - Normal distribution with same mean and variance.
  - Possible overlapping paths.
  - Clock skew is R_D.

- **Clock tree T_I *(Hypothetical)***
  - Similar to T_D.
  - Assume: No overlapping paths.
  - Clock skew is R_I.



- $P(R_D < z) \geq P(R_I < z)$ => $E(R_I) \geq E(R_D)$ (from [4] and [5])

  $P(R_D < z) \geq P(R_I < z)$ => $R_{I,\,95\%} \geq R_{D,\,95\%}$

  $R_{D,\,95\%} = \alpha . R_{I,\,95\%}$ (where $0 \leq \alpha \leq 1$)

[4] Kugelmass et al., "Probabilistic model for clock skew", *Proc. Intl Conf Systolic Arrays*, 1988.

[5] Kugelmass et al., "Upper bound on expected clock skew", *IEEE Trans. Computers*, 1990.

Parameters affecting clock skew

Clock skew under variations

- $\boldsymbol{R_{D,\,95\%} = \alpha . R_{I,\,95\%}}$ **(where $0 \leq \alpha \leq 1$)**
  - Asymptotic formulae for $E(R_I)$ and $Var(R_I)$. (from [4] and [5])

    - For given N, B and σ_0.
  - Sample set large => Assume normal distribution for R_I.

    $R_{I,\,95\%} \sim E(R_I) + 2.\sqrt{Var(R_I)}$
  - $\boldsymbol{R_{D,\,95\%} \sim \alpha . [\, E(R_I) + 2.\sqrt{Var(R_I)}\,]}$

- **Formula for 95 th percentile of clock skew (R) for general clock tree.**
  - Include nominal clock skew (NCS).

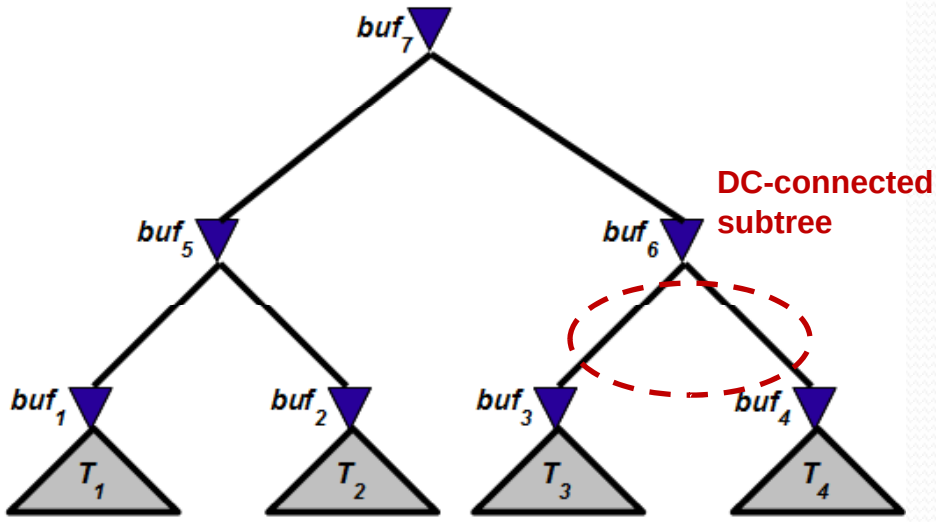
    $\boldsymbol{R_{95\%} \sim NCS + \alpha . [\, E(R_I) + 2.\sqrt{Var(R_I)}\,]}$
  - Empirically estimate α.

Parameters affecting MLCS

- **Wire-width variations (vs) Power-supply variations**
  - Low slew => Small DC-connected subtrees.
  - Effect of wire variations relatively small compared to power-supply variations .

- **Our focus: Power-supply variations**
  - **Delay variation per buffer stage, σ_0:**

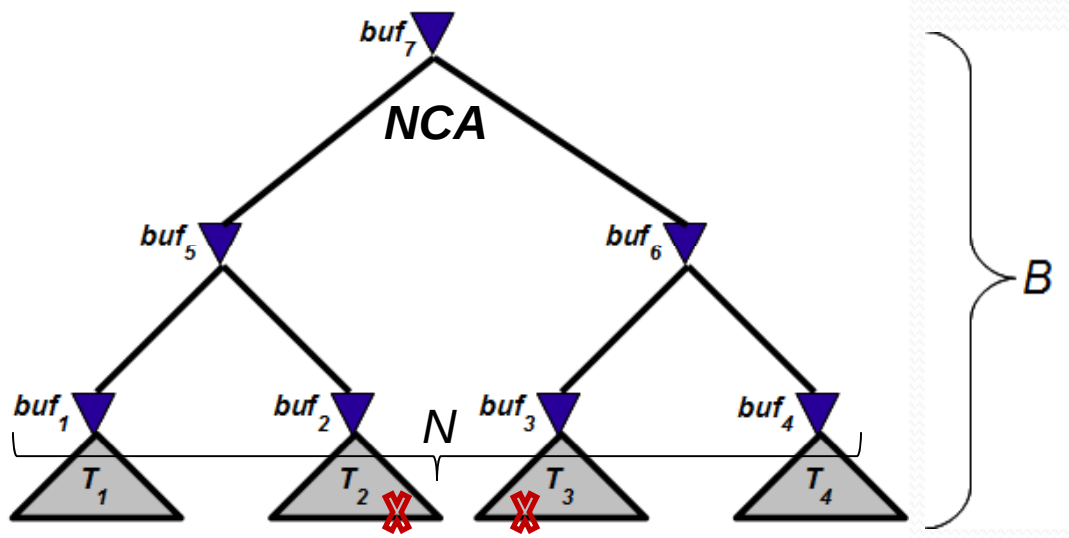
    - σ_0 of buffer stage ~ σ_0 of buffer.



Parameters affecting MLCS

- **LCS parameters**
  - **Number of buffer levels, *B*:**
    - Subtree of the NCA (nearest common ancestor) of local sink pair.
  - **Number of sinks, *N*:**
    - Subtree of the NCA of local sink pair.
    - Number of level 1 buffers (bottom-up from sinks).

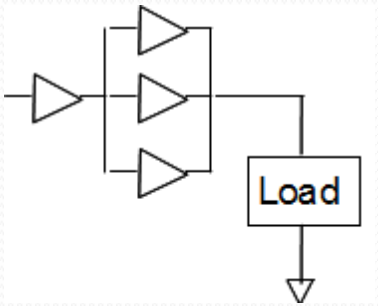
- **MLCS parameters**
  - σ_0, *N* and *B* values that give the highest 95% LCS among all local sink pairs.



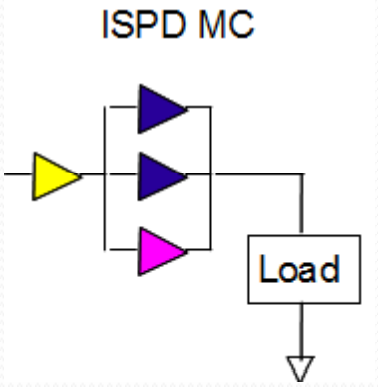
Parameters affecting MLCS

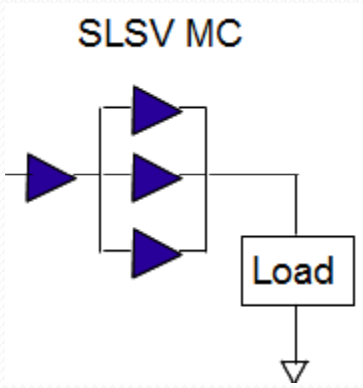
Power-supply variations

- **ISPD 2010 contest**
  - Inverter modeled as a single point.
  - Many inverters can be placed at a single location.
    - Parallel inverters to increase the drive strength.
    - Buffers.



- **Types of Monte-Carlo (MC) simulations**
  - **ISPD MC simulations**. (ISPD problem.)
    - Inverters placed at same location could get different voltages.
    - Same as the contest simulations.
  - **SLSV MC simulations**. (SLSV problem.)
    - Inverters placed at same location get identical voltages.
    - SLSV : Single Location Single Voltage.





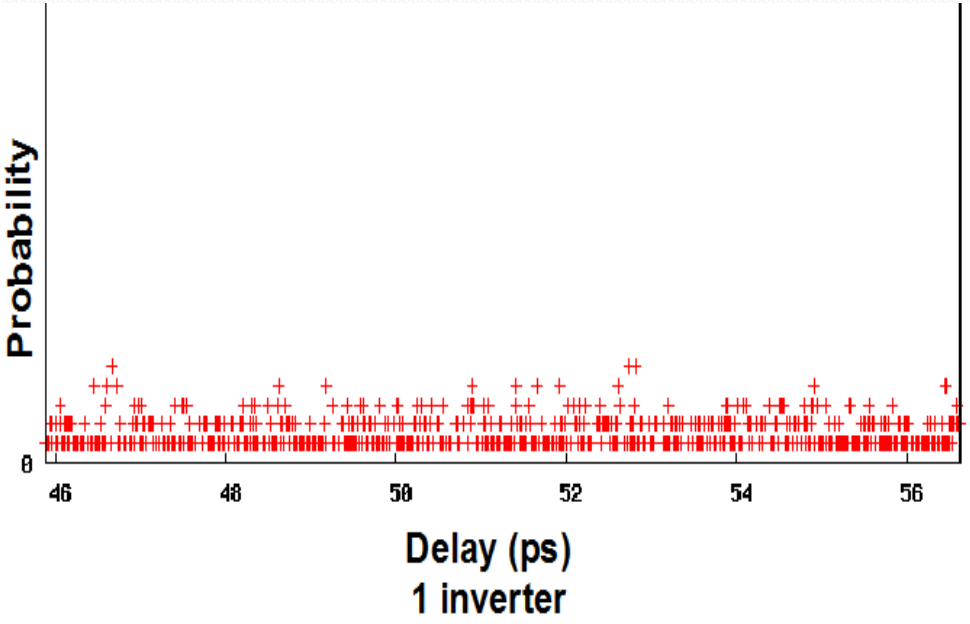
Observations on σ_0

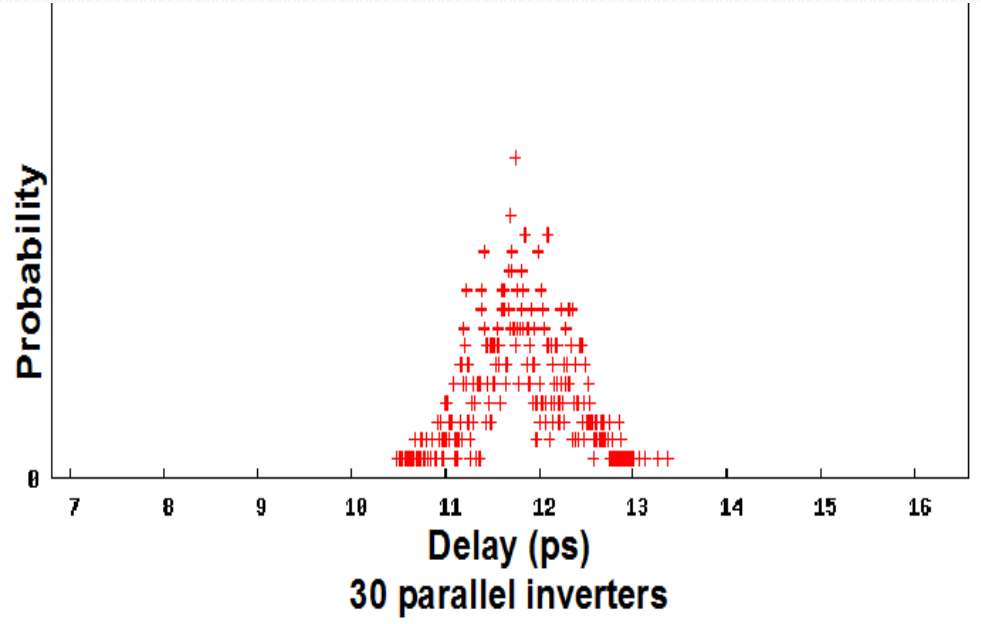
Key Technique - ISPD problem

- **Use parallel inverters to reduce σ_0 :**

  Note: Short circuit power dissipation could increase.

  - Not captured if only capacitance is used as metric for power dissipation.





Observations on σ_0

Key Techniques - SLSV problem

- Buffers (chain of 2 inverters) have lower σ_0 than inverters.
  - Inverters of a buffer (chain of 2 inverters) get identical power-supply voltages.
  - Use buffers (chain of 2 inverters).

- Lower buffer input slew => Lower σ_0.
  - Try to maintain low slew in the clock tree.

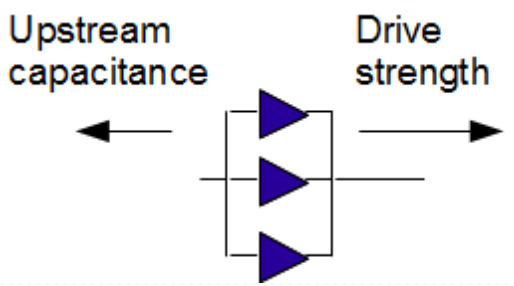
- No significant change in σ_0 for different buffer sizes.
  - At low input slews.
  - For loads at which buffers are inserted to avoid slew constraint violations.

  In our work: A single buffer size is used in entire clock tree (for simplicity).

Observations on *N* and *B*

Key Techniques

- However, buffer size determines *N* and *B.*
  - ISPD and SLSV problem.



- Lower values of *N* and *B* => Lower $MLCS_{95\%}$.
  - Difficult to estimate the buffer size that gives lower *N* and *B*.
    - Non-uniform sink distribution.
    - Blockages.
    - Drive strength (vs) Upstream capacitance presented.
  - We perform a linear search to find the desired buffer size.

Our approach

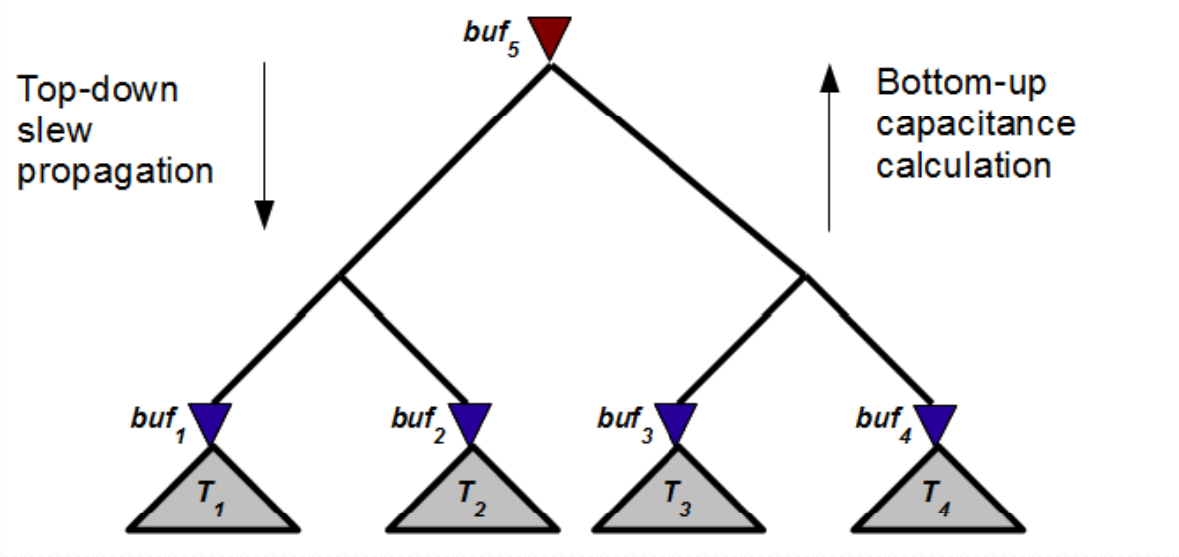
Given a buffer size

- **Construct low nominal skew clock tree**
  - **Deferred Merge Embedding (DME) algorithm**
    - Merging strategy
    - Buffer insertion strategy
      - Avoid slew and blockage constraint violations
    - Buffer modeling
- **Use the formula for $R_{95\%}$ to estimate $MLCS_{95\%}$**

Our approach

Buffer modeling

- Use fast buffer modeling from [6] with minor modification.
  - Iterative approach to model buffer.



- Use NGSPICE for buffer modeling.
  - Stringent MLCS constraints.

[6] R.Puri et al., “Fast and accurate wire delay estimation for physical synthesis of large ASICs”, in *Proc. GLSVLSI*, 2002.

Our approach

Two stages

<u>Stage 1</u> : Perform a linear search for the desired buffer size

Given a buffer size

- Construct low nominal skew tree (DME algorithm)
  - Merging
  - Buffer insertion strategy
    - Avoid slew and blockage constraint violations
  - Buffer modeling **(Use fast buffer modeling)**
- Use the formula for $R_{95\%}$ to estimate $MLCS_{95\%}$

Reason:
Using NGSPICE while searching for desired buffer size - **Expensive!**

<u>Stage 2</u> : Construct low nominal skew tree

(use buffer size determined from stage 1)

- Similar to above EXCEPT
  - Buffer modeling **(use NGSPICE)**
  - Fine tune nominal clock skew **(use NGSPICE)**

Experimental setup

- **Benchmark circuits**
  - ISPD 2010 contest benchmark circuits [7].
  - More than 1000 sinks. (MLCS constraint of 7.5ps or less.)
  - Based on Intel and IBM microprocessor designs (scaled to 45nm).

- **Variations**
  - Power-supply variations: ±7.5%.
  - Wire-width variations: ± 5%.

- **Power-supply variation (±7.5%)**
  - Only V_{dd}.
    - We present the results for these simulations.
  - Share between V_{dd} and V_{ss}.
    - Similar or lower $MLCS_{95\%}$.

[7] "ISPD 2010 High Performance CNS contest" *http://archive.sigda.org/ispd/contests/10/ispd10cns.html*

Results

Using parallel inverters to solve ISPD problem

BM	MLCS limit (ps)	MLCS (ps)							Cap (fF)	Runtime (secs)
		nom	ISPD MC			SLSV MC				
			mean	max	95%	mean	max	95%		
01	**7.50**	2.13	4.01	7.45	**5.79**	17.47	31.30	***25.76**	177.46	2790
02	**7.50**	2.67	4.98	7.50	**6.69**	20.29	29.54	***27.83**	329.92	7787
03	**4.999**	1.41	2.44	4.24	**3.46**	10.40	16.66	***14.54**	50.81	2094
04	**7.50**	1.54	2.84	4.21	**3.79**	12.18	23.41	***18.13**	57.44	2763
05	**7.50**	1.99	2.72	4.69	**3.68**	8.94	16.37	***13.35**	28.93	1100
06	**7.50**	2.32	3.03	4.69	**4.01**	11.19	19.63	***15.28**	36.12	1142
07	**7.50**	2.83	3.81	5.91	**5.65**	12.12	18.80	***16.46**	57.93	2968
08	**7.50**	1.73	2.89	5.13	**4.24**	12.12	19.09	***16.34**	40.43	1498

Results

Using buffers (2 layers of parallel inverters) to solve SLSV problem

BM	MLCS limit (ps)	MLCS (ps)							Cap (fF)	Runtime (secs)
		nom	ISPD MC			SLSV MC				
			mean	max	95%	mean	max	95%		
01	**7.50**	1.47	4.21	8.60	**5.58**	6.96	11.40	***10.29**	189.06	2324
02	**7.50**	1.42	4.60	6.85	**6.27**	7.99	14.66	***11.61**	341.08	6723
03	**4.999**	0.64	1.96	3.42	**2.96**	3.47	5.80	**4.95**	69.15	1269
04	**7.50**	0.81	3.38	7.34	**5.69**	5.27	8.32	**7.17**	56.59	2711
05	**7.50**	0.81	2.32	5.27	**3.67**	3.64	5.64	**5.00**	26.25	1057
06	**7.50**	0.66	2.80	5.94	**4.58**	4.25	6.40	**5.97**	32.57	1027
07	**7.50**	1.09	3.20	6.29	**4.91**	5.03	8.99	**7.07**	56.13	2917
08	**7.50**	0.94	3.10	5.29	**4.83**	4.60	7.39	**6.53**	37.40	1427

Results

Using parallel inverters to solve ISPD problem
500 MC simulations

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06	7.50	2.32	3.10	5.06	4.14	11.22	18.72	*16.06	36.12	1142
07	7.50	2.83	3.60	6.28	4.85	12.14	19.79	*16.54	57.93	2968
08	7.50	1.73	2.79	5.32	3.86	11.69	20.38	*16.02	40.43	1498

Results

Using buffers (2 layers of parallel inverters) to solve SLSV problem
500 MC simulations

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			mean	max	95%	mean	max	95%		
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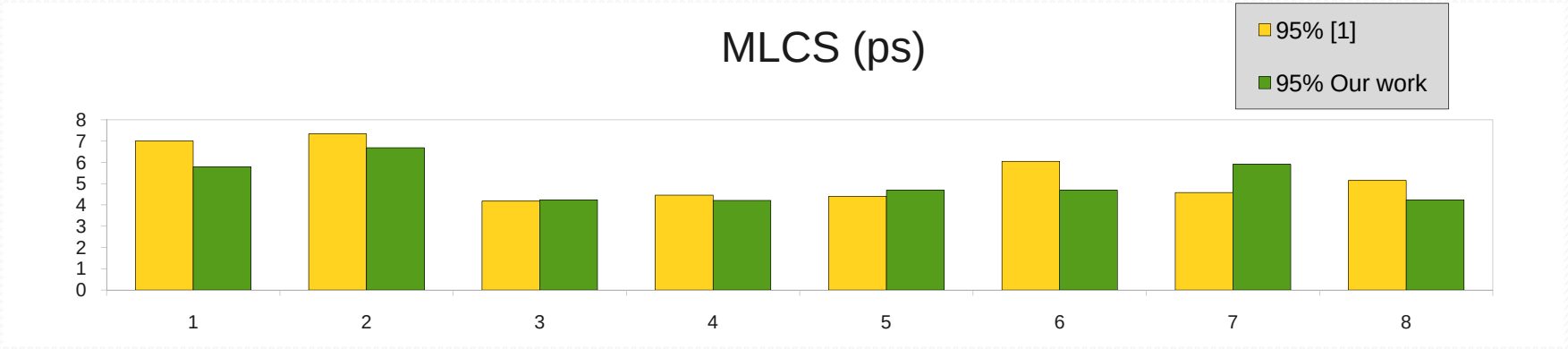
05	**7.50**	0.81	2.42	5.98	**3.91**	3.61	6.96	**5.20**	26.25	1057
06	**7.50**	0.66	2.70	5.70	**4.49**	4.19	7.13	**5.74**	32.57	1027
07	**7.50**	1.09	3.30	8.90	**5.72**	5.10	9.22	**7.40**	56.13	2917
08	**7.50**	0.94	3.05	7.34	**4.91**	4.72	9.11	**6.85**	37.40	1427

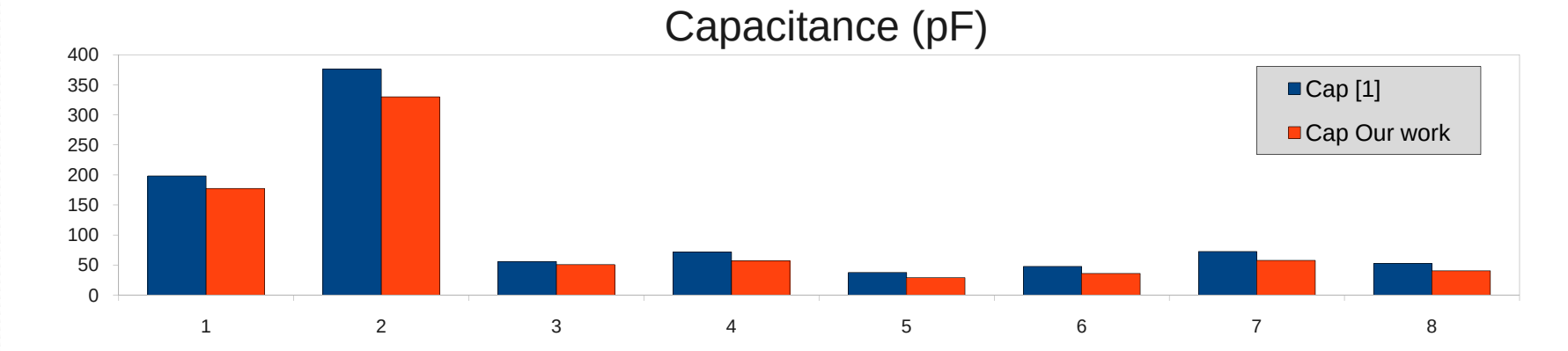
Results

Comparison of ISPD MC using inverters

- [1] D. Lee, M. Kim, I. Markov , “Low Power Clock Trees for CPUs”, *ICCAD*, 2010.
  - Tree structure.
  - Best results among the top three teams.

- On an average: Cap of our work = 1.00, Cap of [1] = 1.22x.



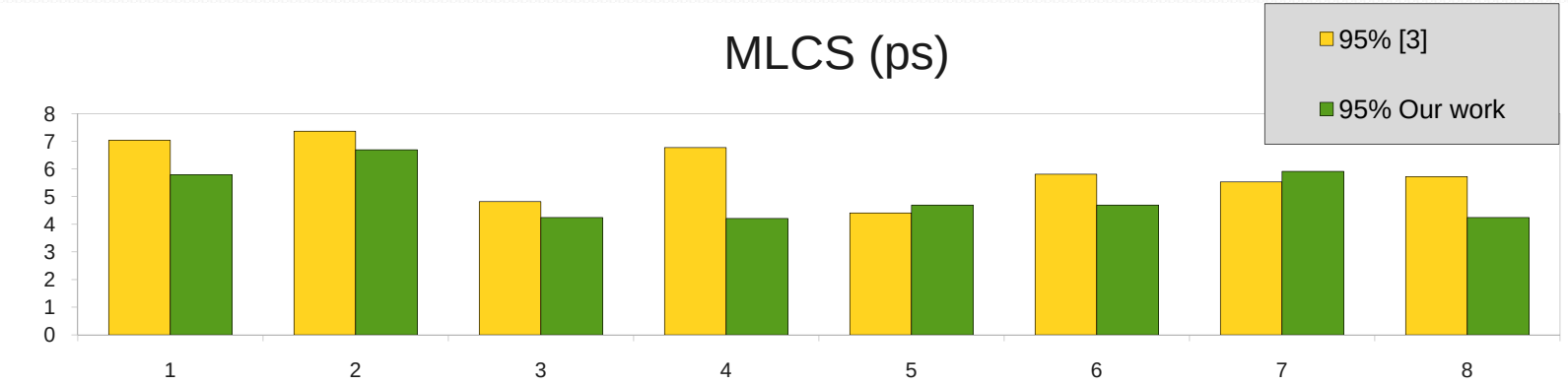


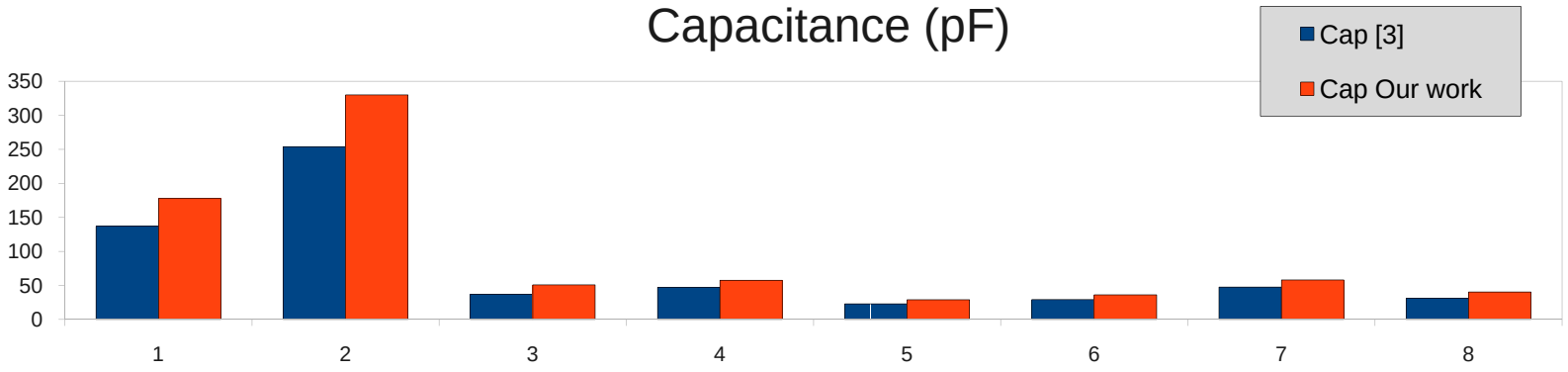
Results

Comparison of ISPD MC using inverters

- [3] T. Mittal and C-K. Koh, "Cross Link Insertion for Improving Tolerance to Variations in Clock Network Synthesis", *ISPD*, 2011.
  - Tree + cross-links structure.
  - Use inverters.

- On an average: Cap of our work = 1.00, Cap of [3] = 0.79x.



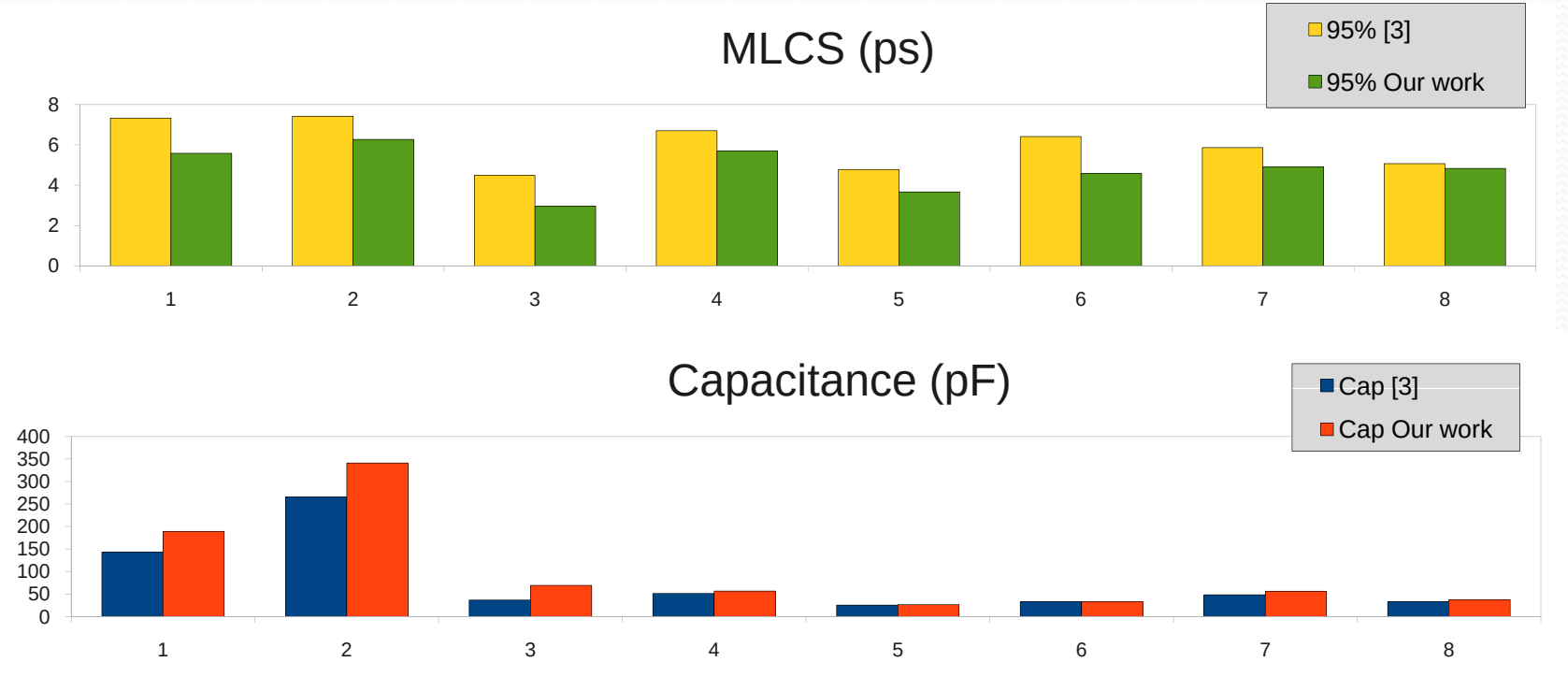


Results

Comparison of ISPD MC using buffers

- [3] T. Mittal and C-K. Koh, "Cross Link Insertion for Improving Tolerance to Variations in Clock Network Synthesis", *ISPD*, 2011.
  - Tree + cross-links structure.
  - Use buffers.

- On an average: Cap of our work = 1.00, Cap of [3] = 0.83x.

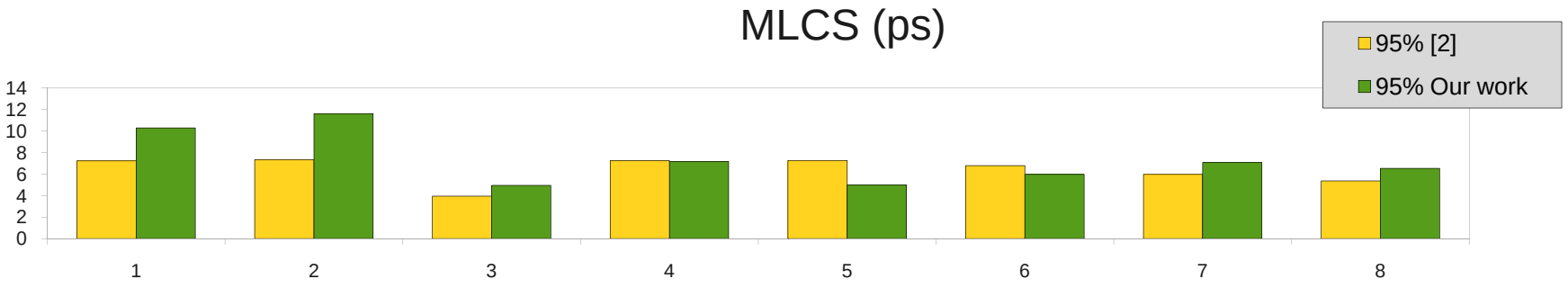


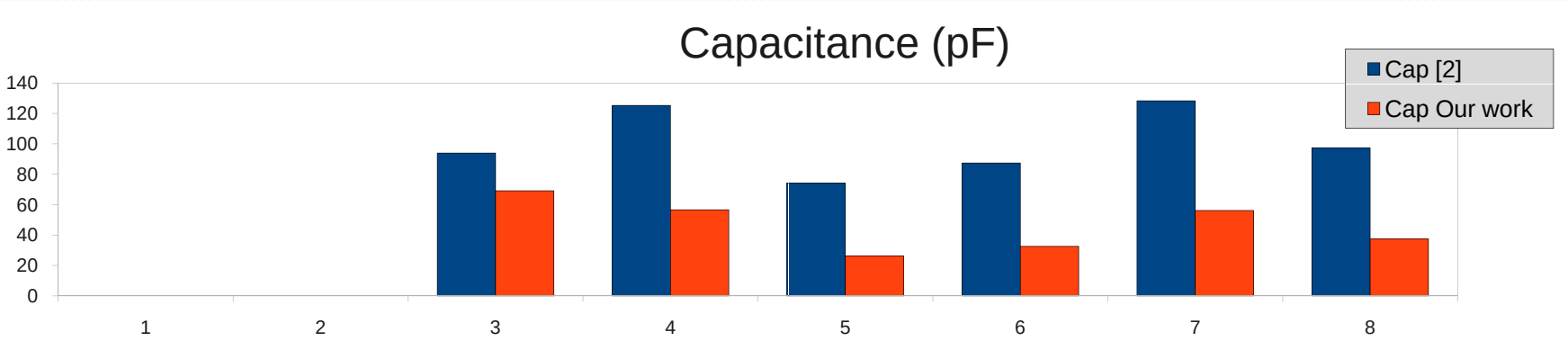
Results

Comparison of SLSV MC using buffers

- [2] L. Xiao, Z. Xiao, Z. Qian, Y. Jiang, T. Huang, H. Tian, and E. Young, "Local clock skew minimization using blockage-aware mixed tree-mesh clock network, *ICCAD*, 2010.
  - Mixed tree-mesh structure.
  - Note: They use single buffer at any location.

- On an average: Cap of our work = 1.00, Cap of [2] = 2.33x.





Conclusions

- **Our contributions**
  - Identified, analyzed parameters that have high impact on MLCS.
  - Quick estimate of MLCS using these parameters.

    - Avoid expensive MC simulations.
  - Simple two-stage technique to meet MLCS constraints.

- **Clock tree structure**
  - Can handle stringent MLCS constraints for most of the contest benchmarks.
  - Analysis of the variations

    - Helps to check if clock tree structures satisfy skew constraints.

Thank you