# Synthesis of Clock Networks with a Mode Reconfigurable Topology and No Short Circuit Current

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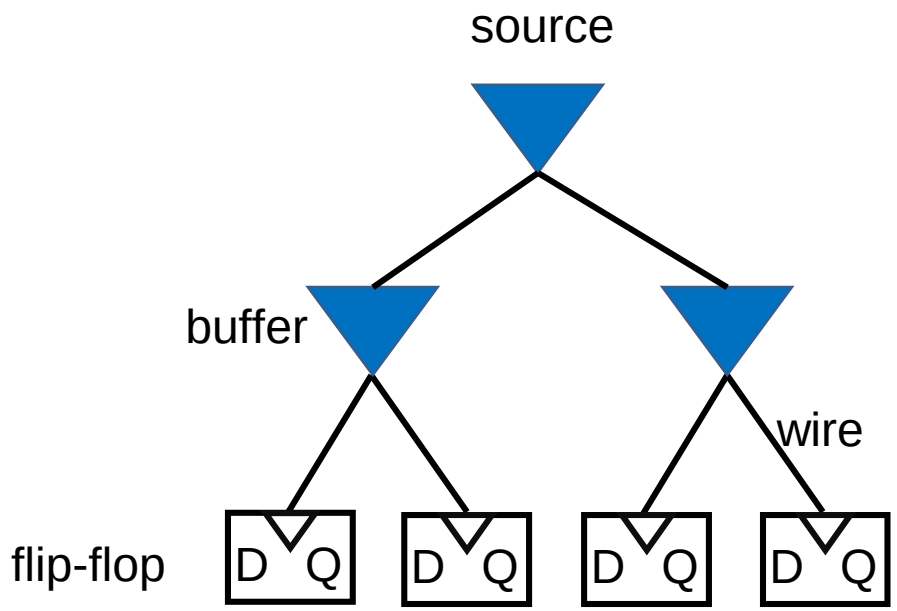
# Outline

- Introduction
- Preliminaries
- Proposed Structure
- Proposed Techniques
- Experimental Results

# Introduction

- Clock network
  - Source
  - Flip-flops
  - Buffers
  - Wires
- Challenges
  - Power consumption
  - Robustness to process, voltage and temperature (PVT) variations
  - Multiple modes (low and high performance)



# Preliminaries

- High performance mode
  - High frequency
  - Tight timing constraints
  - Requires higher robustness to variations
- Low performance mode
  - Low frequency
  - Looser timing constraints
  - Minimize power consumption

# Timing Constraints

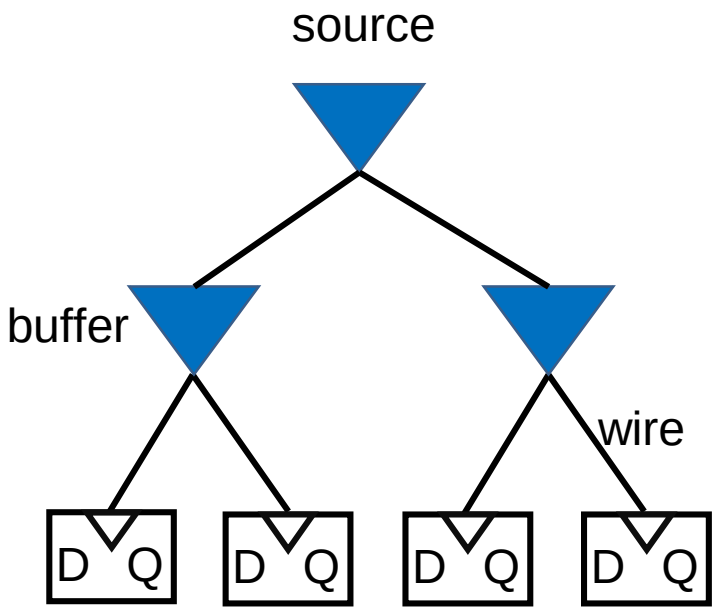
- Skew

  $t_{ij} = t_i - t_j$

- Uniform Skew constraints

  $t_i - t_j <= B$

- Variations introduce skew
  - Not easy to satisfy timing constraints




| | $t_1$ | $t_2$ | $t_3$ | $t_4$ | Skew |
|---|---|---|---|---|---|
| Nominal | 55 | 53 | 57 | 56 | 4 |
| Under variation | 52 | 55 | 65 | 54 | 10 |

# Power Optimization

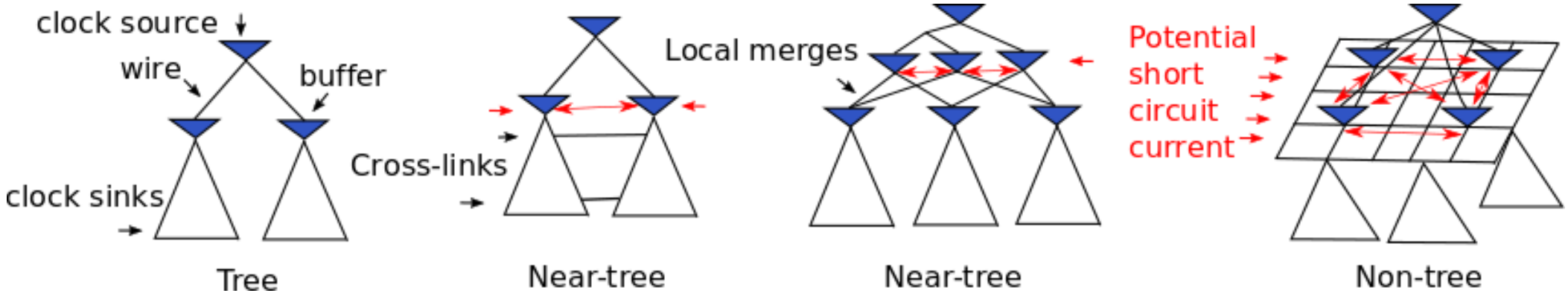
- Dynamic power consumption
  - $P = C_{comb} \cdot V_{DD}^{2} \cdot f \cdot \alpha_{comb} + C_{clk} \cdot V_{DD}^{2} \cdot f \cdot \alpha_{clk}$

  $V_{DD}$ ↓ , f ↓ , $C_{clk}$ ↓ → P ↓

- Voltage and frequency scaling
  - Update the frequency
  - Reduce the supply voltage until timing constraints are not satisfied.

$C_{comb}$ : capacitance of combinational logic
$V_{dd}$ : supply voltage
f : frequency
$C_{clk}$ : capacitance of clock network
$\alpha_{comb}$ : activity factor of combinational logic
$\alpha_{clk}$ : activity factor of clock network
T : clock period

# Clock Network Topologies




Tree topology

+ Low power consumption
+ No short circuit current
- Vulnerable to variations

Non-tree (near-tree) topology

+ Robust to variations
- High power consumption
- Short circuit current

# Previous Works

| Topology | Work | Robustness to variations | Power | Compatible with | | |
|---|---|---|---|---|---|---|
| | | | | Voltage scaling | EDA tools | Reconfiguration |
| Tree | [1,24] | low | small | Yes | Yes | No |
| Near-tree | [8,16] | high | medium | No | No | No |
| Non-tree | [20,26] | high | very large | Yes | Yes | No |
| MRT (near-tree) | This work | **high** | medium | **Yes** | **Yes** | **Yes** |


[1]Kenneth Boese and Andrew B. Kahng. 1992. Zero-Skew Clock Routing Trees With Minimum Wirelength.
In Proc. of International ASIC Conference and Exhibit.17–21.
[8] Rickard Ewetz and Cheng-Kok Koh. 2015. Cost-Effective Robustness in Clock Networks Using Near-Tree Structures. TCAD34, 4 (2015), 515–528.
[16] Anand Rajaram et al.2004. Reducing clock skew variability via cross links(DAC).18–23
[20] Xin-Wei Shih et al.2010. High variation-tolerant obstacle-avoiding clock mesh synthesis with symmetrical driving trees. ICCAD. 452–457.
[24] R.-S. Tsay. 1991. Exact zero skew(ICCAD). 336–339.
[26] Ganesh Venkataraman et al.2006. Combinatorial algorithms for fast clock mesh optimization(ICCAD). 563–567.

# High Level Solution

- **Question:** Can we construct a clock network that has a near-tree/non-tree topology in high performance modes and a tree topology in low performance modes?

- **Our Solution:** Synthesize a clock network with a reconfigurable topology.

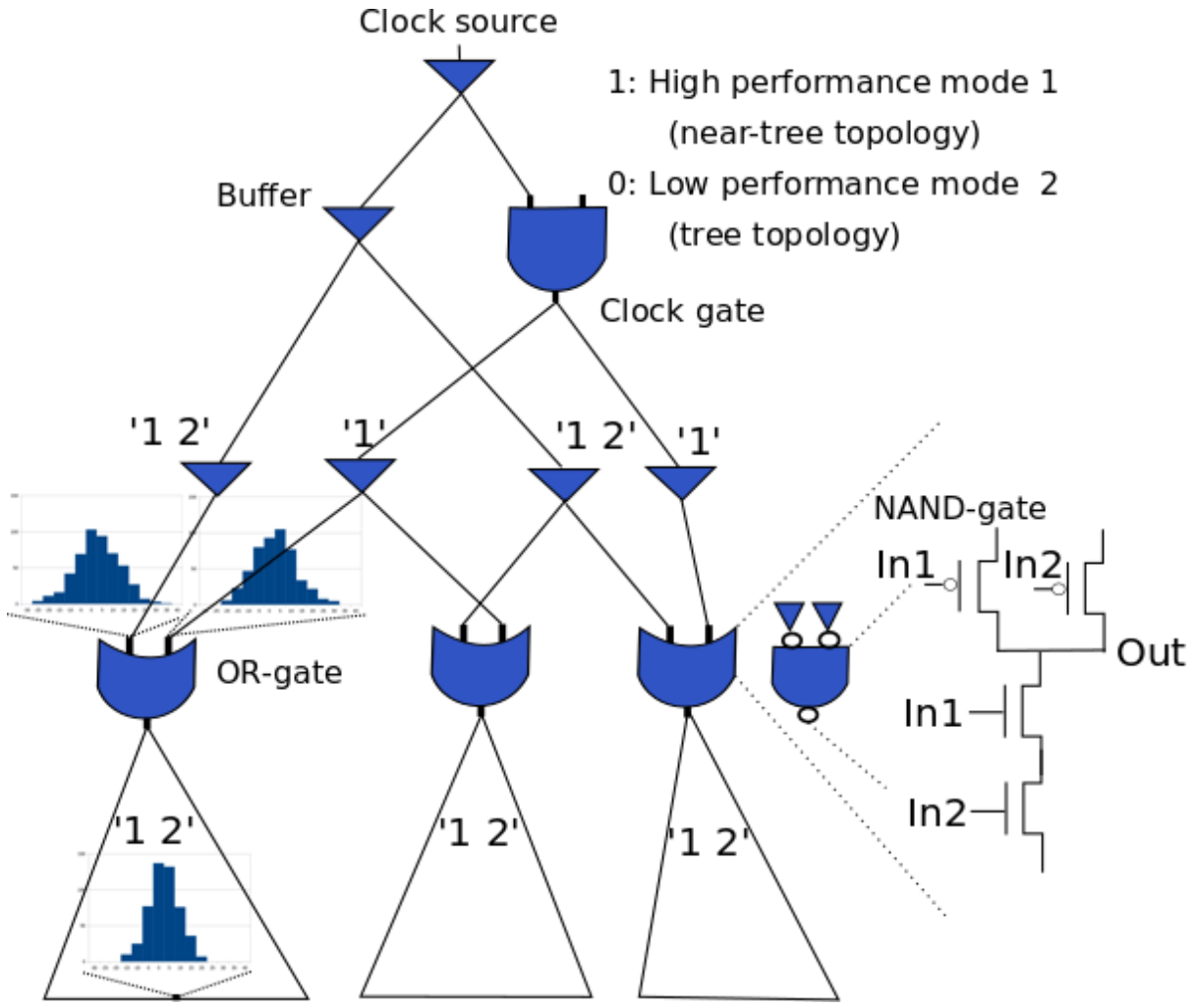
# Problem Formulation

Clock network synthesis for circuits with multiple modes of operation and positive-edge triggered flip-flops

- Objective: To route the clock source to clock sinks while meeting tight timing constraints under variations in the high performance mode and minimizing the power consumption in the low performance mode
- Inputs
  - Flip-flop locations
  - Device and layer library
- Constraints
  - Timing constraints in high performance mode
  - Timing constraints in low performance mode
  - Slew constraint

# Proposed MRT Structure

- High performance mode
  - Near-tree topology
- Low performance mode
  - Reconfiguring the topology into tree
  - Voltage scaling

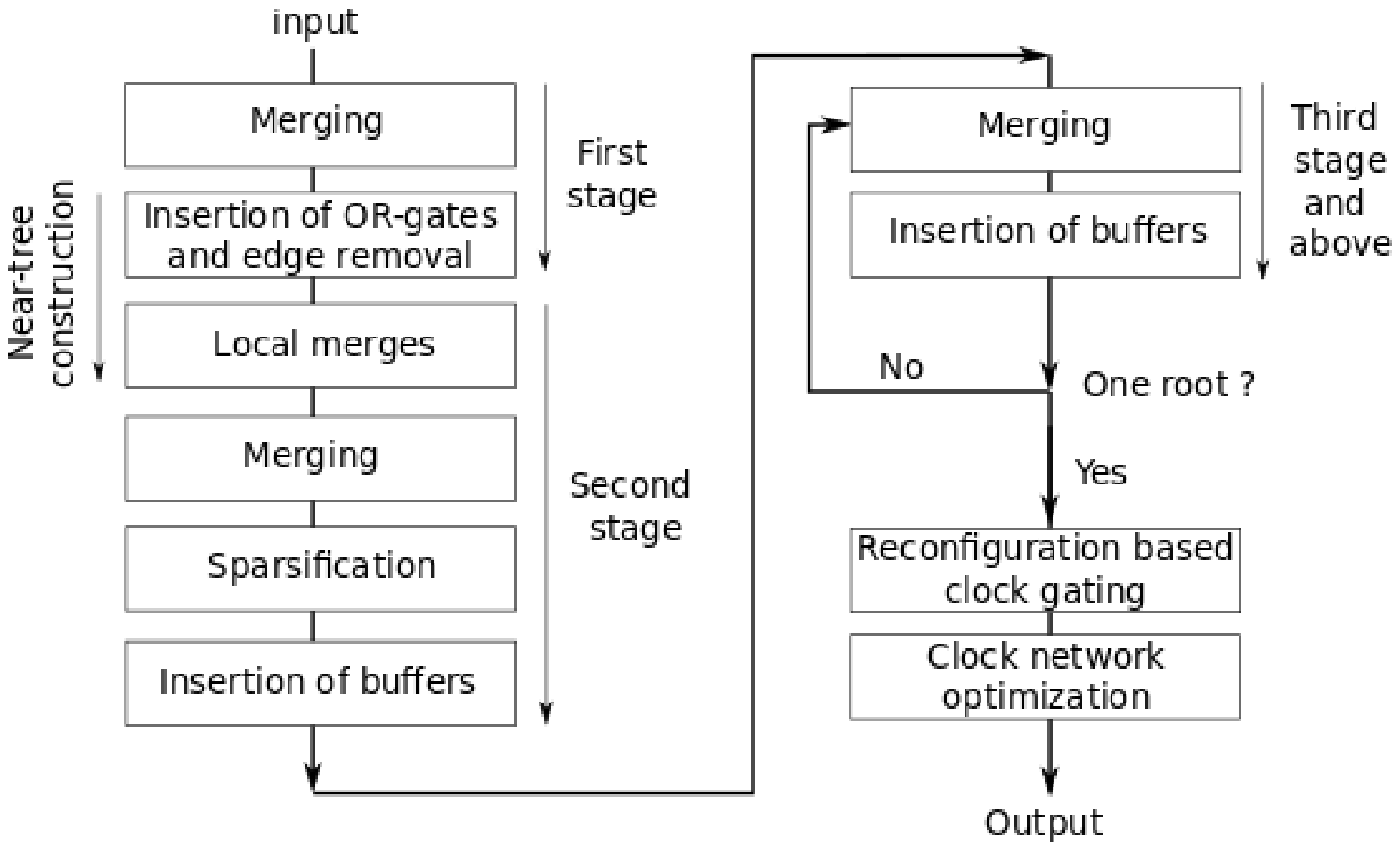


# Advantages and Weaknesses

- Advantages
  - Robust to variations in high performance mode
  - Reduces the switching capacitance in the low performance mode
  - No short circuit current

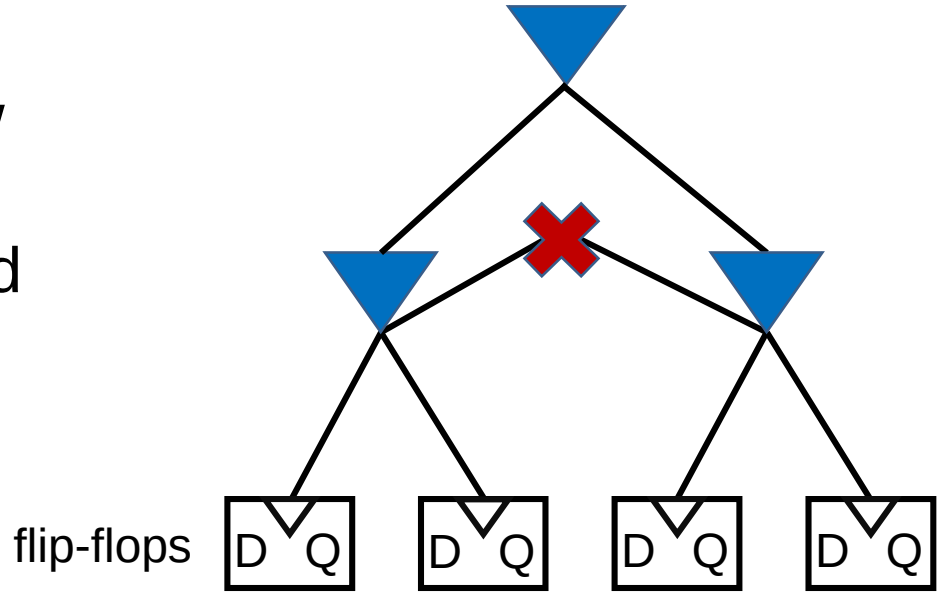
- Weakness
  - Designed for only positive-edge triggered flip-flops

# Methodology



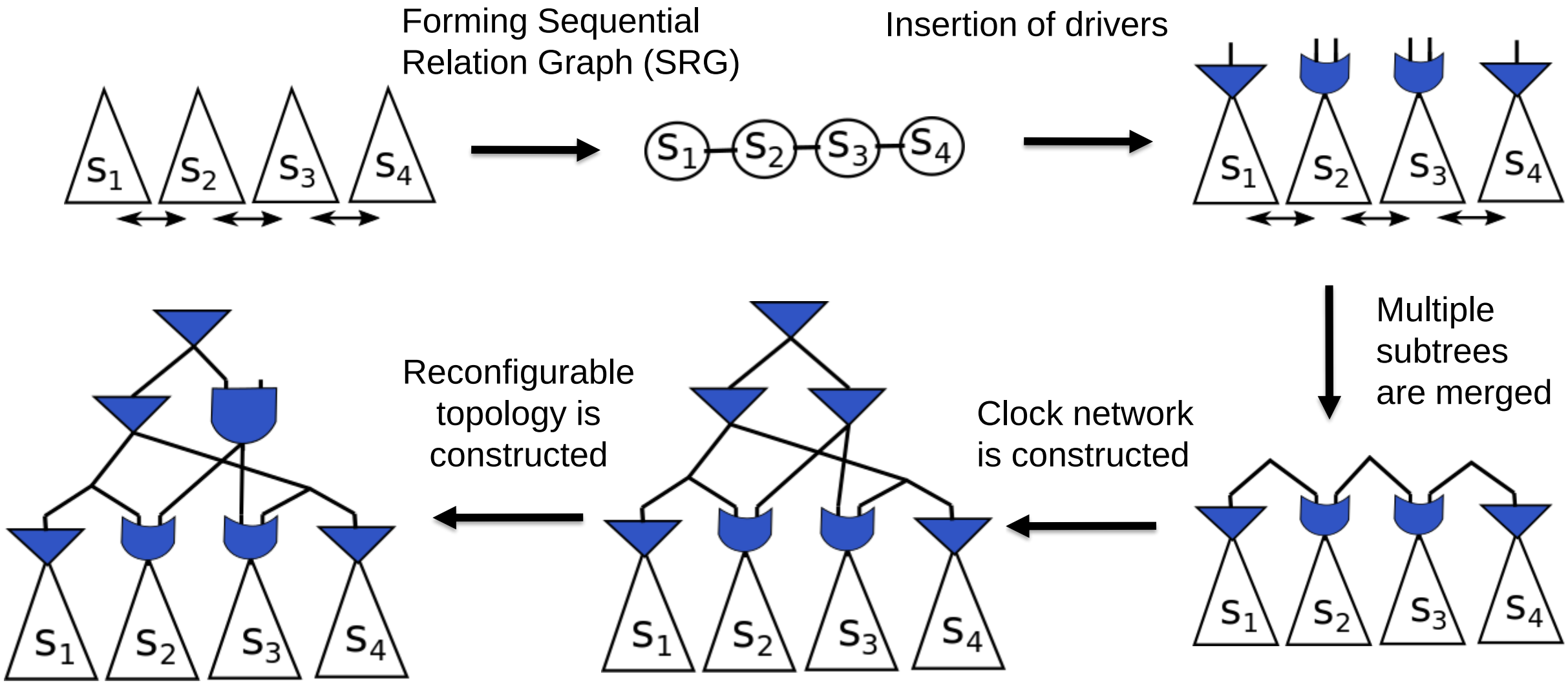
# Zero Skew Clock Tree Synthesis [24]

- Merging subtree pairs that requires minimum wirelength to obtain zero skew
- Subtrees are locked from merging if slew constraint is violated
- Insert buffers after all subtrees are locked
- Perform merging and buffer insertion iteratively until there is one root.



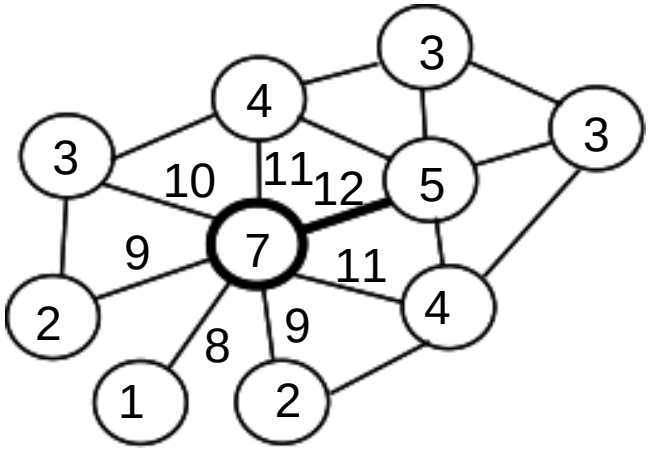

[24] R.-S. Tsay. 1991. Exact zero skew (ICCAD). 336–339.

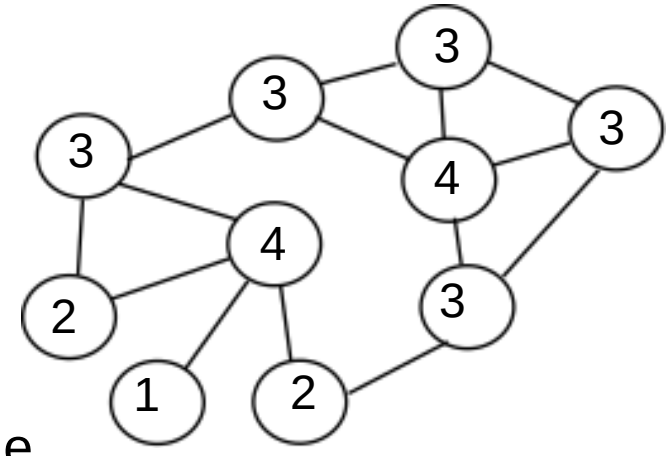
# Flow of the Construction



# Edge Removal

- Maximum number of input pins of OR-gate is limited
- No vertices can have more than 4 edges
- An edge must be removed if it cannot be realized due to slew constraint



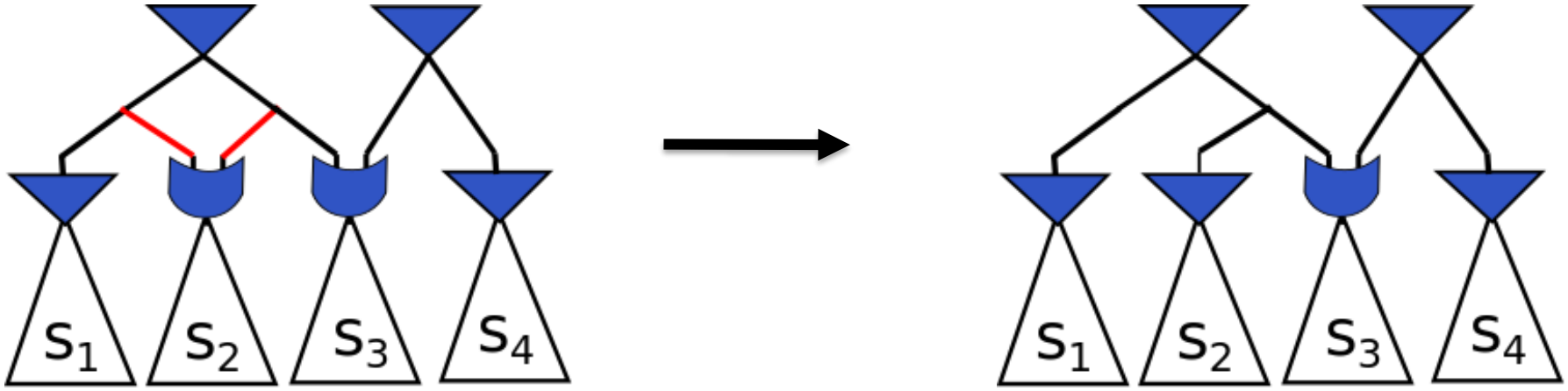

$|\mathrm{v_i}| = \sum_{\forall e_{ij}} 1$

$|e_{ij}| = |v_i| + |v_j|,$

Remove the highest weighted edge of the highest weighted vertex until there are 4 incident edges left.

# Sparsification [8]

- Excessive amount of redundant paths introduce additional variations
- No need for redundant paths from the same second stage driver to an OR-gate




First and second stage subtrees

Subtrees after sparsification

[8] Rickard Ewetz and Cheng-Kok Koh. 2015. Cost-Effective Robustness in Clock Networks Using Near-Tree Structures. TCAD 34, 4 (2015), 515–528.

# Constructing the Reconfigurable Topology

- Turning-off redundant paths to save power in the low performance mode
- A set of buffers are selected to be converted into clock gates based on the following objective function:

$$\min \ \alpha C_H + \beta C_L + \gamma N_g$$

$C_H$: switching cap. in high performance mode
$C_L$ : switching cap. in low performance mode
$N_g$ : number of inserted clock gates
α, β, γ : parameters to regulate different terms

# Experimental Setup

- Benchmarks [6] are synthesized by Synopsis DC & ICC
- Buffer and wire library from 45nm tech.
- Transition time constraint is 100 ps
- Two modes operate in different frequencies ( 5GHz and 1GHz)
- Evaluation in timing
  - 250 Monte Carlo simulations
  - NGSPICE simulations
  - Skew bound for 95% and 100% yield, $B_{95}$ and $B_{100}$.
- Evaluation in power consumption
  - NGSPICE simulations

| **Circuit** | **Sinks** | **Skew constraints** | **Clock period (ps)** | |
|---|---|---|---|---|
| (name) | (num) | (num) | $T_H$ | $T_L$ |
| s1423 | 74 | 78 | 200 | 1000 |
| s5378 | 179 | 175 | 200 | 1000 |
| s15850 | 597 | 318 | 200 | 1000 |
| msp | 683 | 44990 | 200 | 1000 |
| fpu | 715 | 16263 | 200 | 1000 |
| usbf | 1765 | 33438 | 200 | 1000 |
| pci bridge32 | 3582 | 141074 | 200 | 1000 |
| des peft | 8808 | 17152 | 200 | 1000 |

[6] Rickard Ewetz et al.2015. Benchmark circuits for clock scheduling and synthesis([Available Online] https://purr.purdue.edu/publications/1759)

# Evaluated Structures

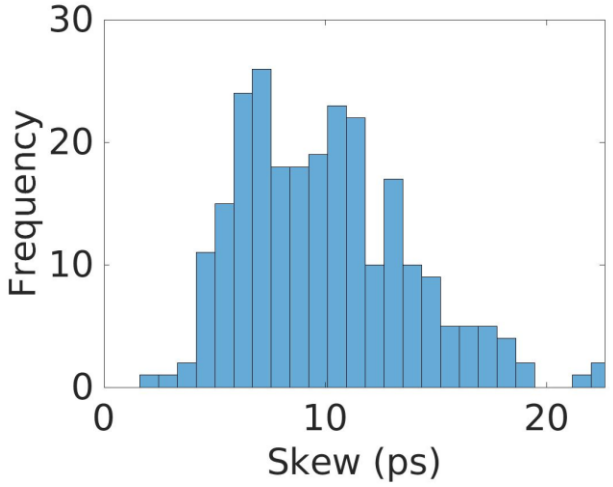
- Tree :  Clock Tree structure in [24] with zero skew
- Near-Tree : Locally merged structure in [8] which has near-tree topology
- MRT: Clock network with mode reconfigurable topology (This work)

[8] Rickard Ewetz and Cheng-Kok Koh. 2015. Cost-Effective Robustness in Clock Networks Using Near-Tree Structures. TCAD 34, 4 (2015), 515–528.
[24] R.-S. Tsay. 1991. Exact zero skew (ICCAD). 336–339.

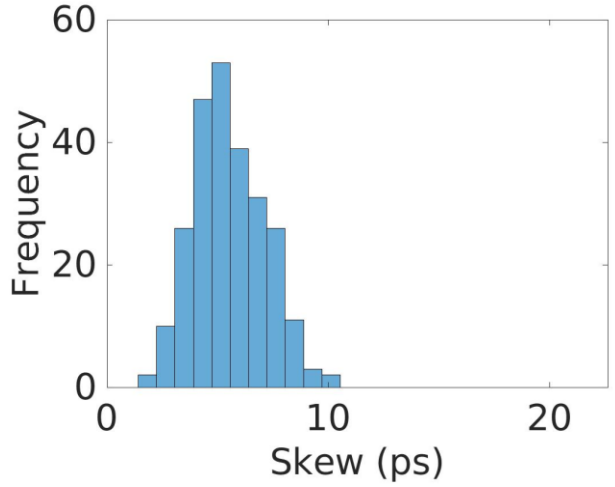
# Experimental Results

Histogram of skews from 250 Monte Carlo simulations on *usbf*

- Joining multiple paths using OR-gates reduces the affect of variations
- MRT structure has a tighter skew distribution.




Tree



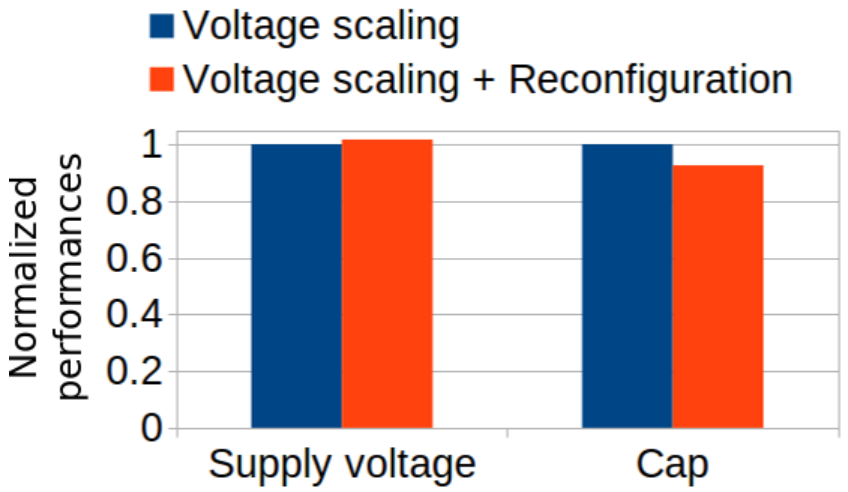

MRT

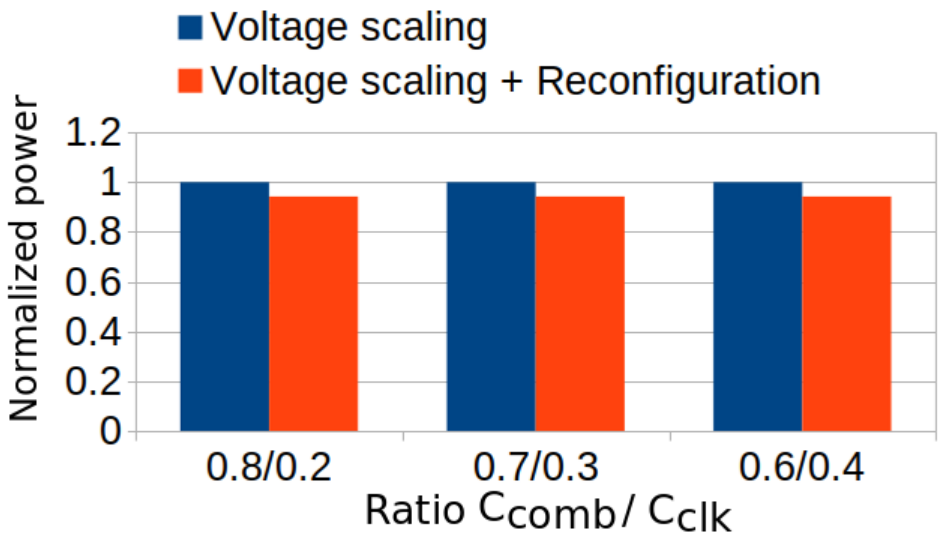
# High Performance Mode

| Benchmark | Structure | Power (mW) | Timing Yield | | Run-time (min) |
|---|---|---|---|---|---|
| | | | $B_{100}$ (ps) | $B_{95}$ (ps) | |
| **msp** | **Tree** | 14.91 | 16.93 | 12.06 | 8 |
| | **Near-tree** | 27.28 | 5.76 | 4.81 | 9 |
| | **MRT** | 21.20 | 7.33 | 5.90 | 9 |
| **des** | **Tree** | 153.96 | 34.03 | 19.94 | 79 |
| | **Near-tree** | 254.28 | 22.59 | 15.96 | 216 |
| | **MRT** | 193.12 | 14.4 | 11.26 | 105 |
| **usbf** | **Tree** | 37.88 | 22.63 | 17.10 | 6 |
| | **Near-tree** | 57.55 | 8.66 | 7.31 | 10 |
| | **MRT** | 50.15 | 10.52 | 8.09 | 9 |
| **Norm.** | **Tree** | 1.00 | 1.00 | 1.00 | 1.00 |
| | **Near-tree** | 1.54 | **0.58** | **0.63** | 1.61 |
| | **MRT** | 1**.42** | **0.59** | **0.62** | 1.68 |

# Low Performance Mode

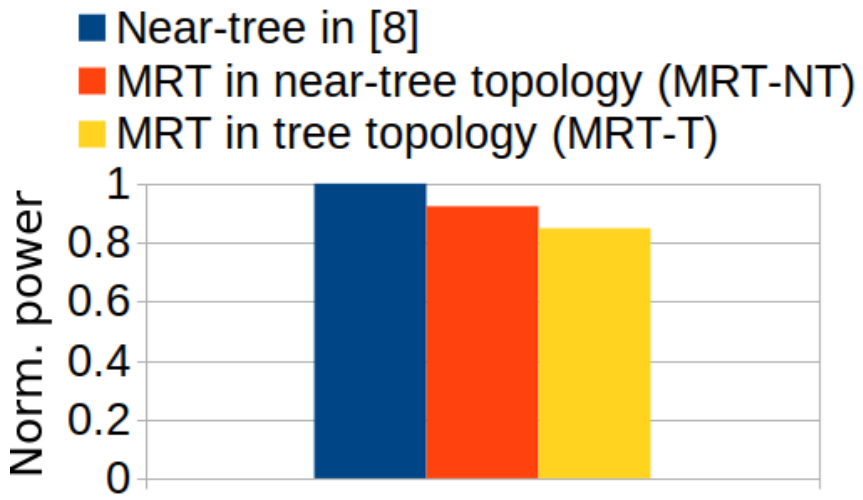
- Reconfiguration of the topology  and voltage scaling
  - reduces the switching capacitance by 8%
  - have 6% lower power consumption than voltage scaling



# Evaluation of Power Consumption

- MRT structures  vs.  Near-Tree
  - MRT-NT has 8% lower power consumption
  - MRT-T has 16% lower power consumption




[8] Rickard Ewetz and Cheng-Kok Koh. 2015. Cost-Effective Robustness in Clock Networks Using Near-Tree Structures. TCAD 34, 4 (2015), 515–528.

# Conclusion

- A clock network structure with a Mode Reconfigurable Topology
  - Similar robustness with lower costs when compared with state-of-the-art near-tree structures
  - Operates in multiple modes using different topologies
  - No short circuit current
  - Compatible with EDA tools

# QUESTIONS ?

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