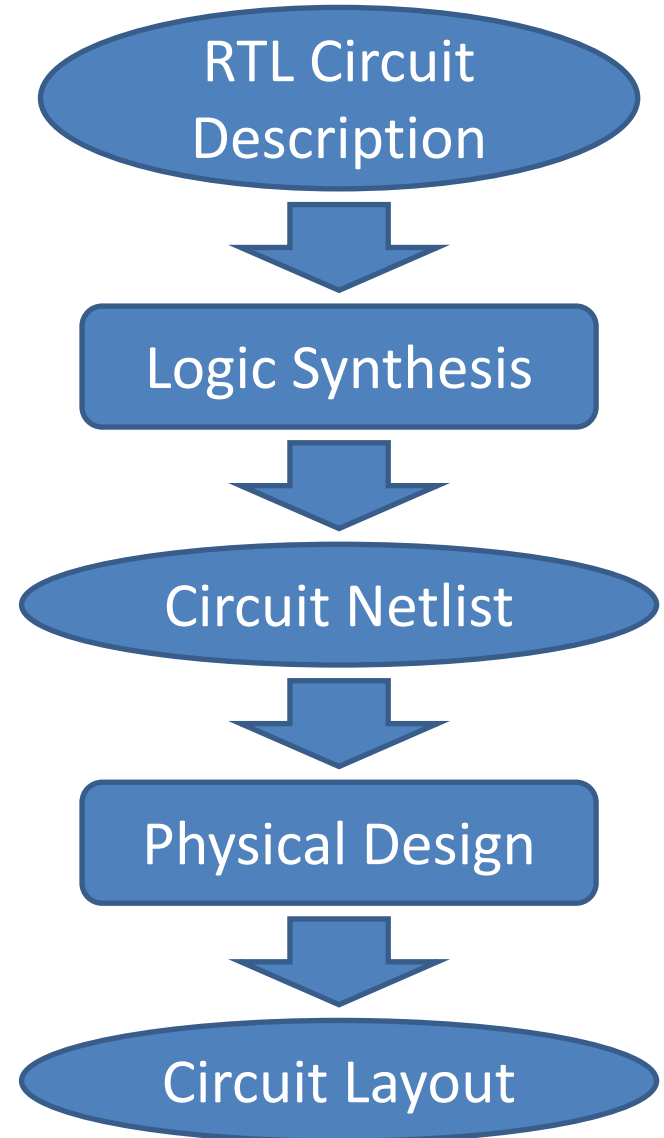


Towards a VLSI Design Flow Based on Logic Computation and Signal Distribution

André Reis

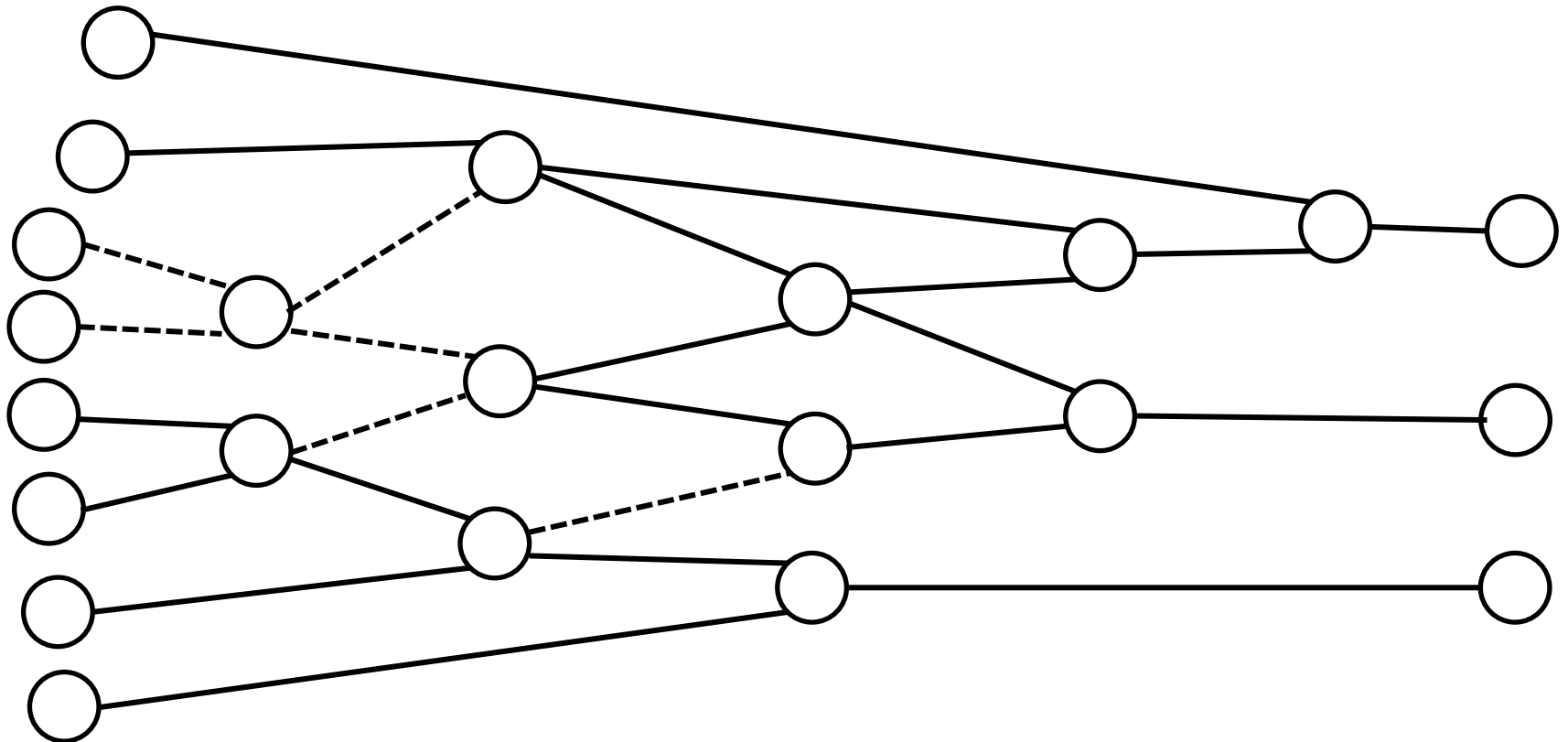
“Usual” Flow

- To be taken with care, but:
 - Separate teams
 - Separate cultures
 - Separate conferences
 - IWLS/ISPD



Logic Synthesis: AIG And-Inverter-Graph

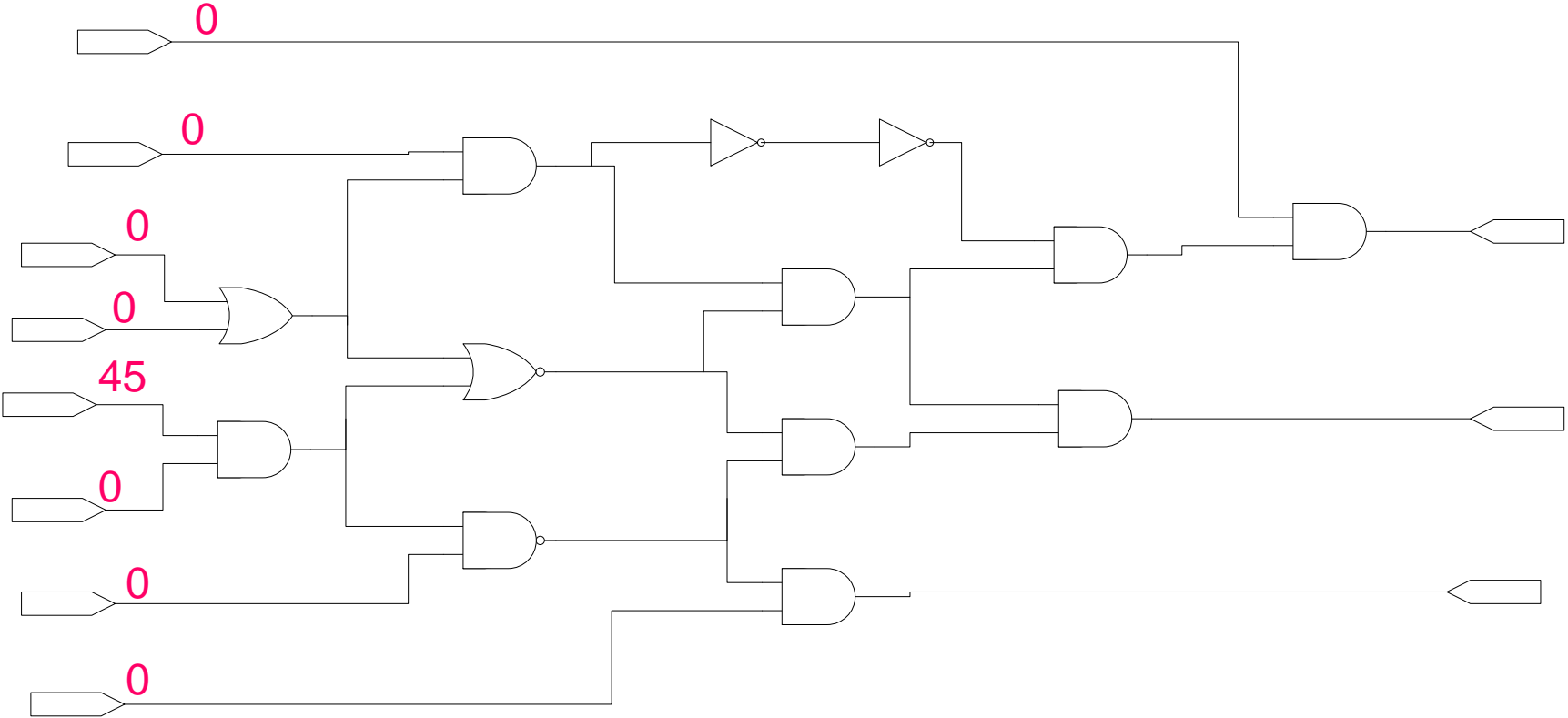
- Set of interconnected nodes



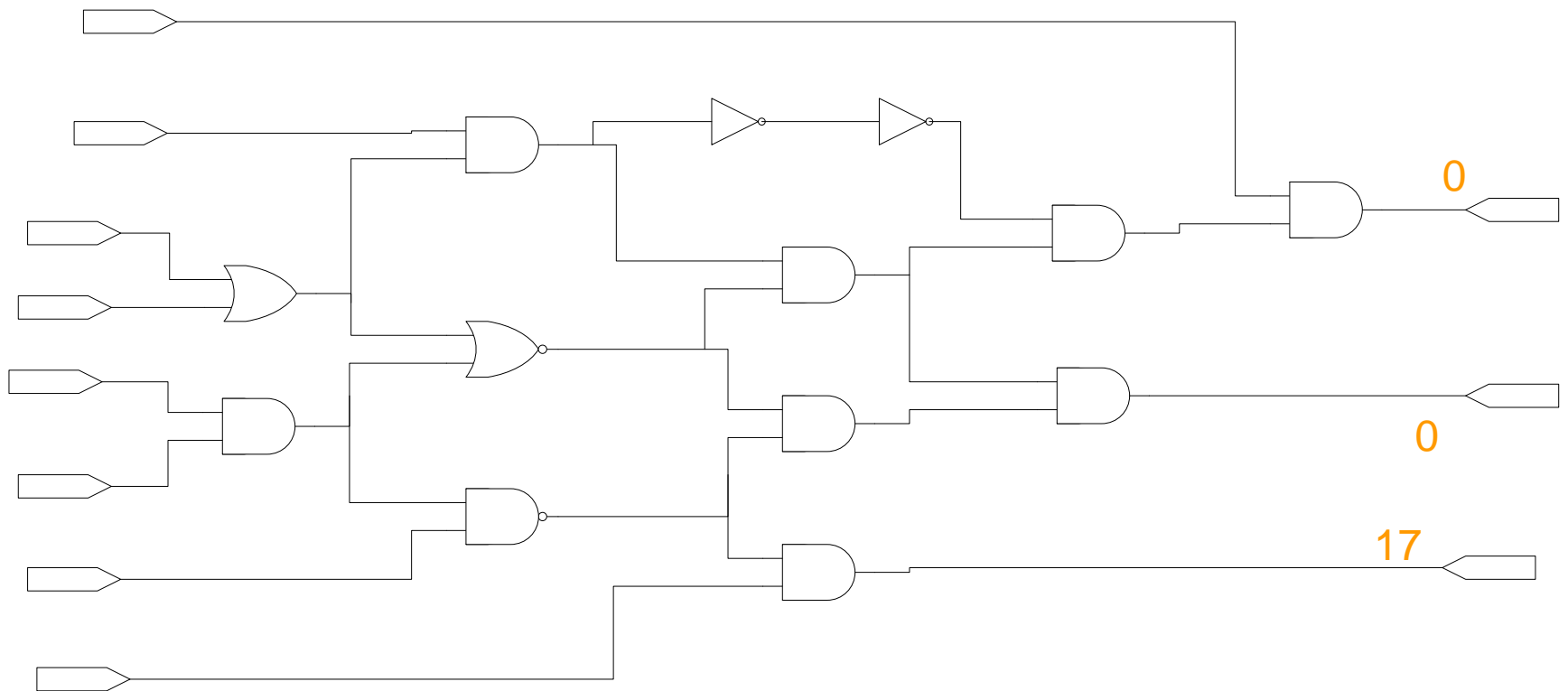
Logic Synthesis vs. Physical Design

- AIG
- Implicit inverters
- Cuts
- Netlist
- Explicit inverter
- Partitioning

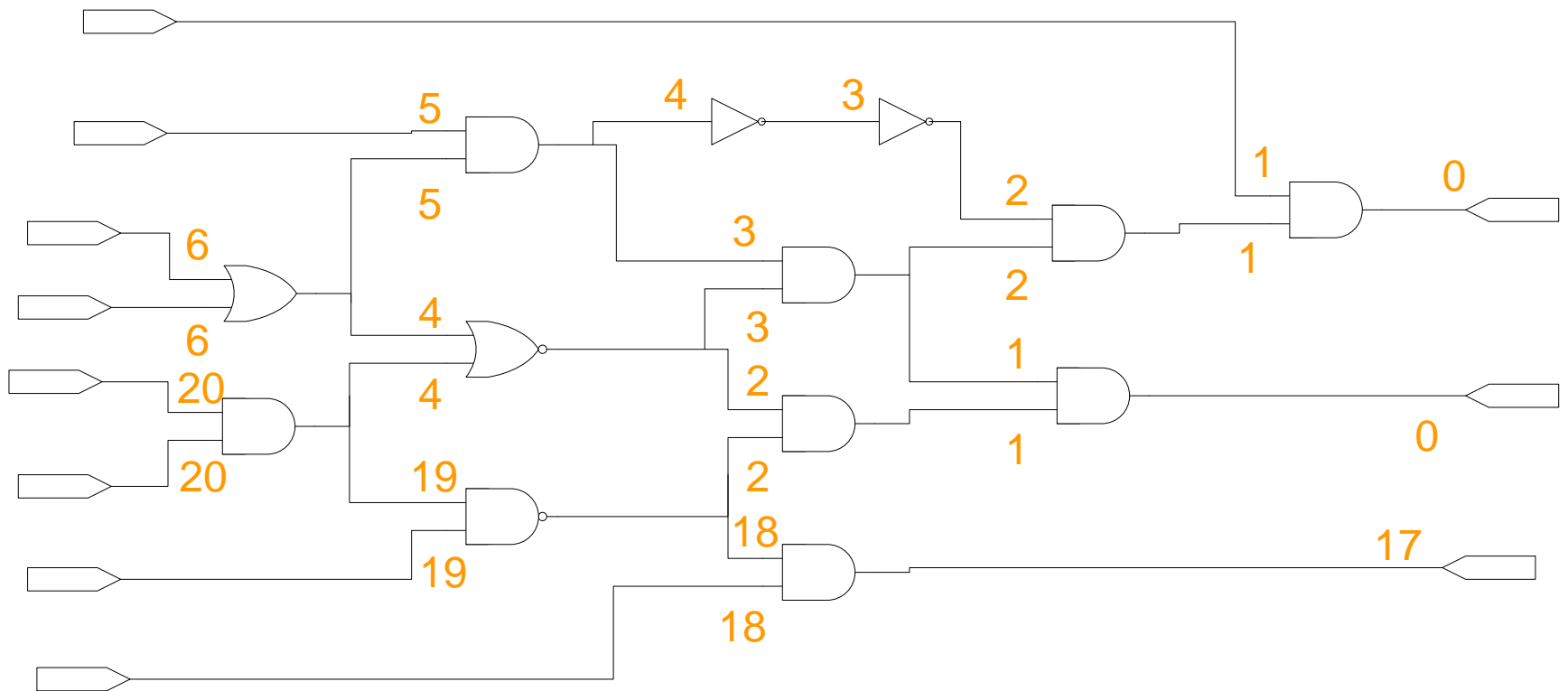
Design constraints: Late arrival times



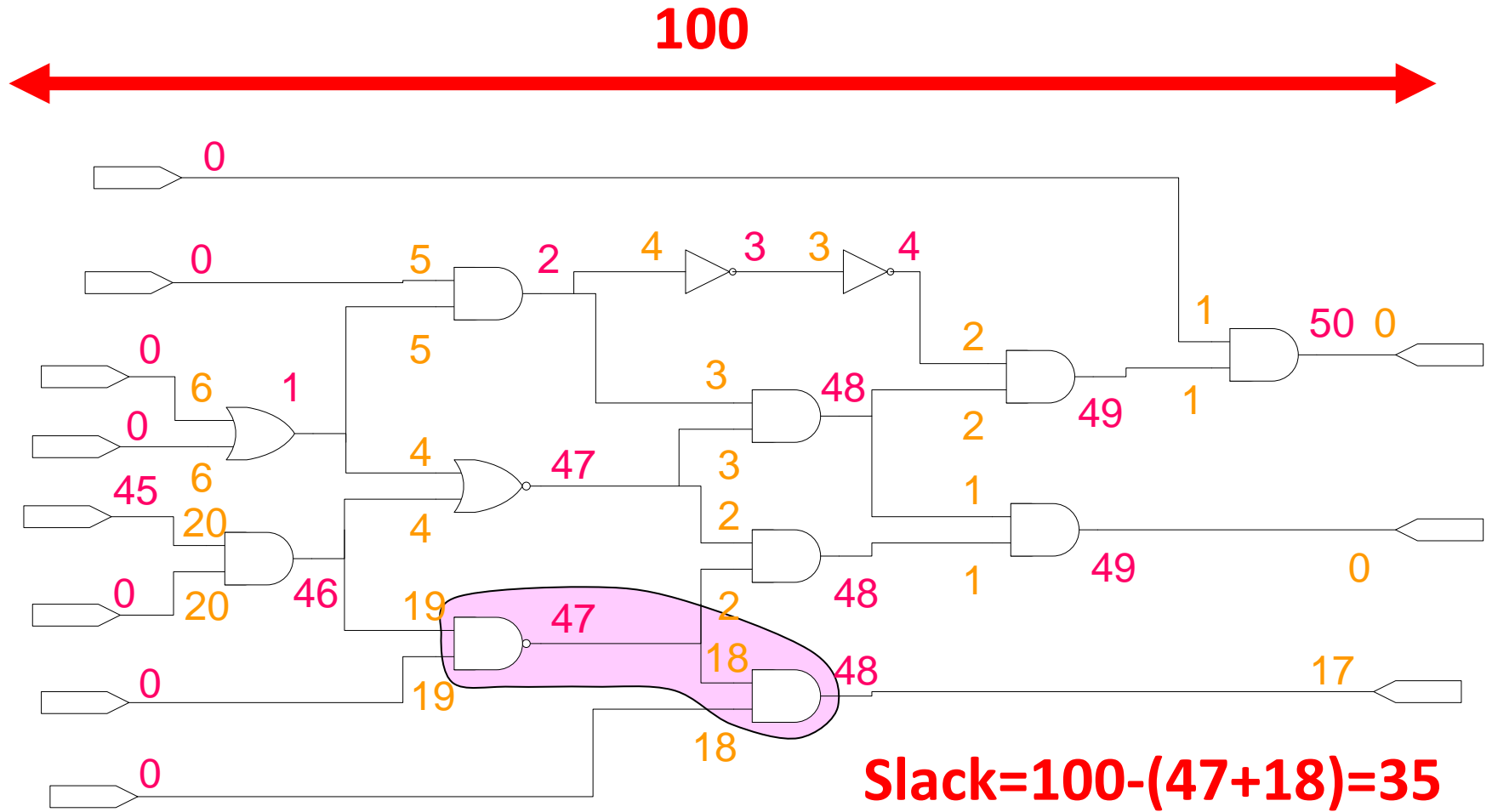
Design constraints: Early request



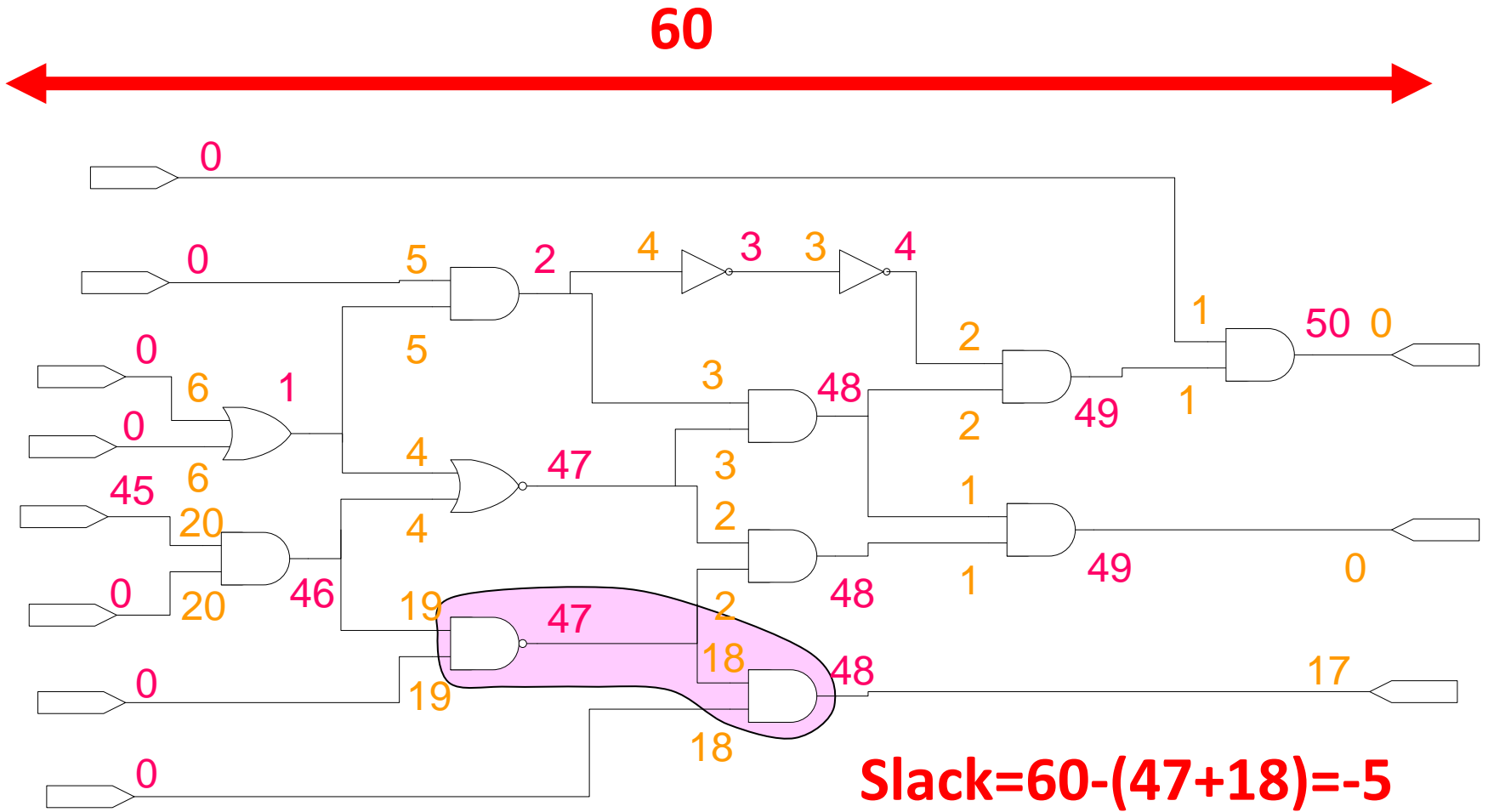
Backward delay



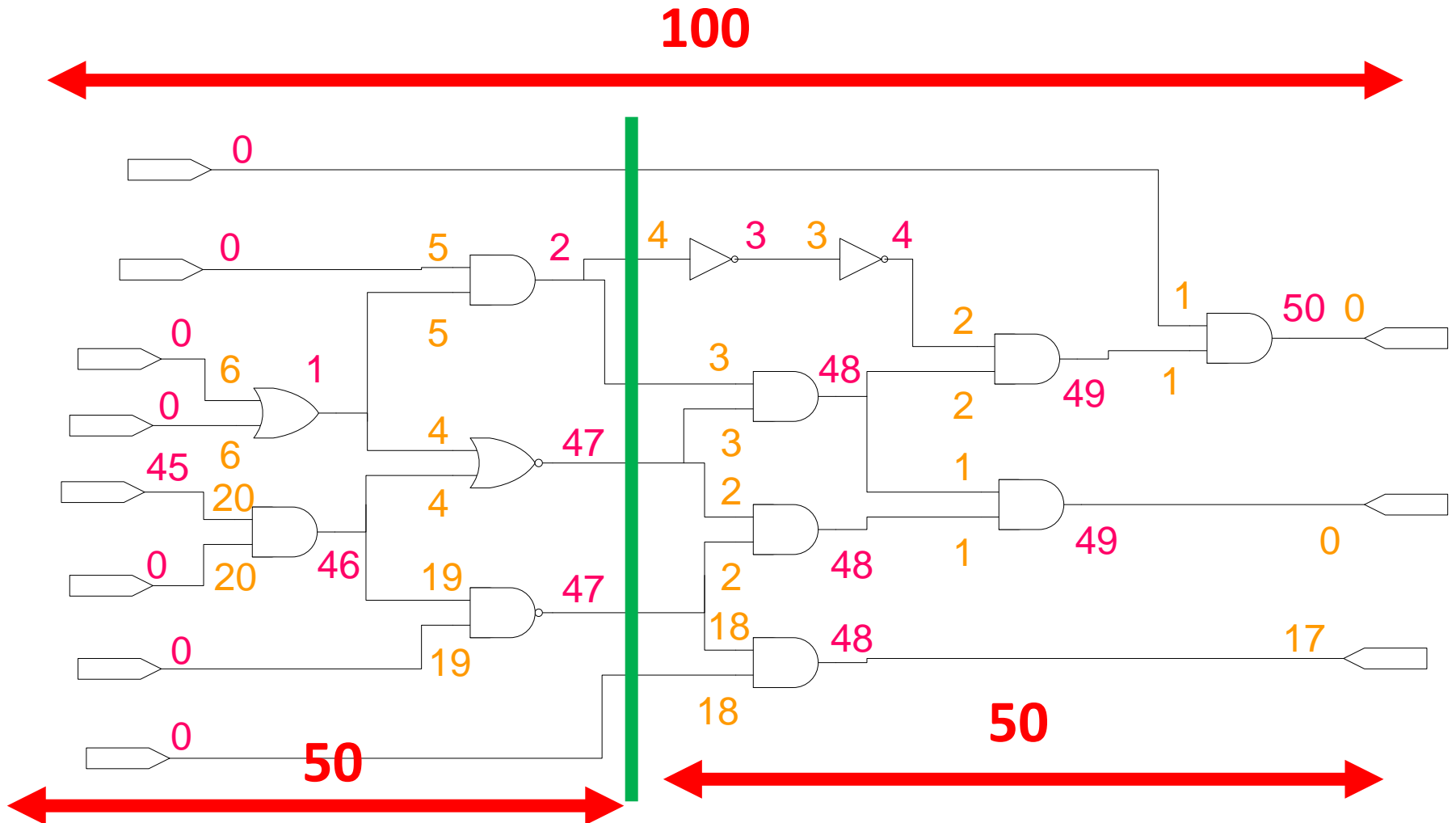
Design Constraints: Target Frequency



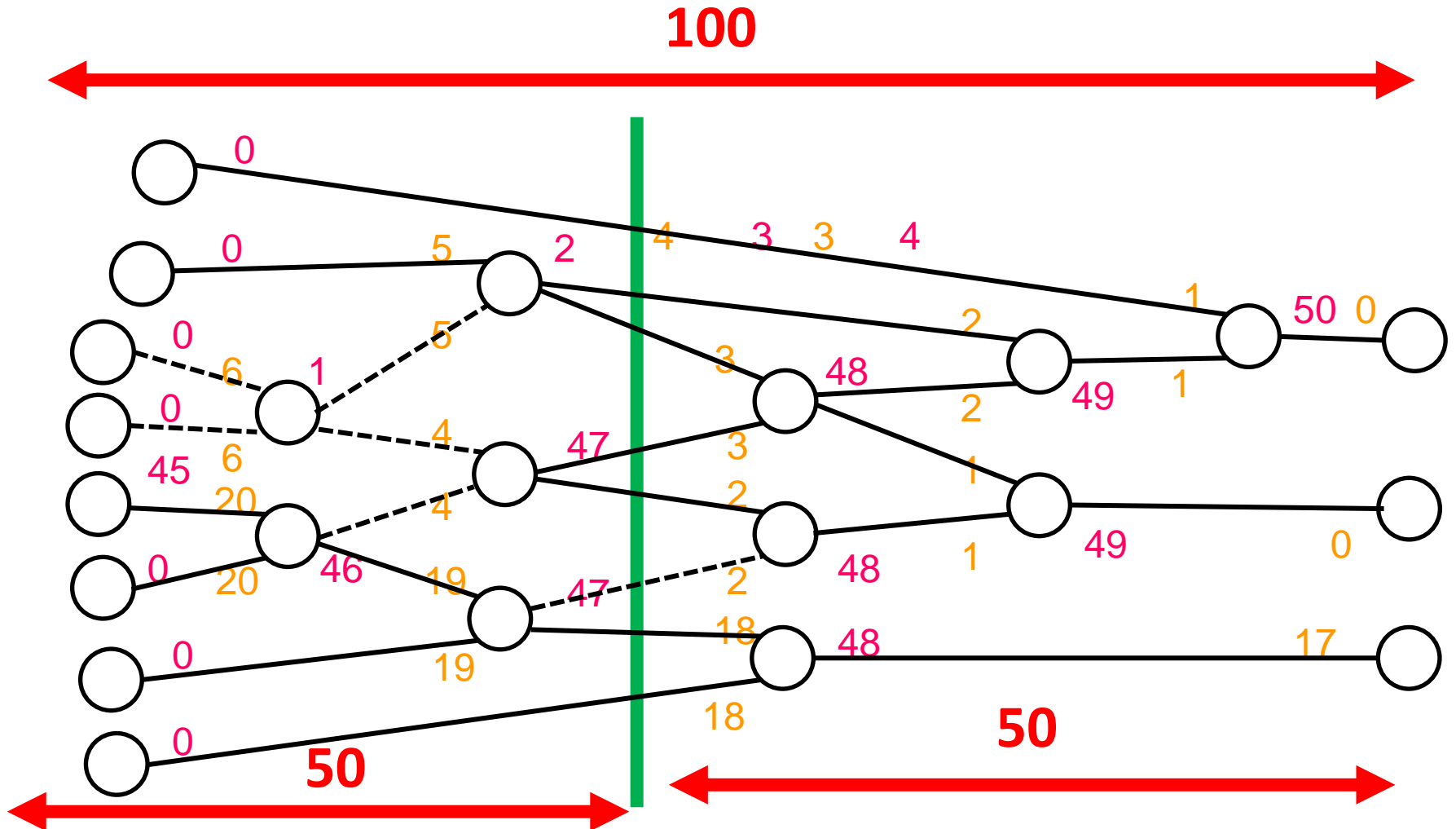
Design Constraints: Target Frequency



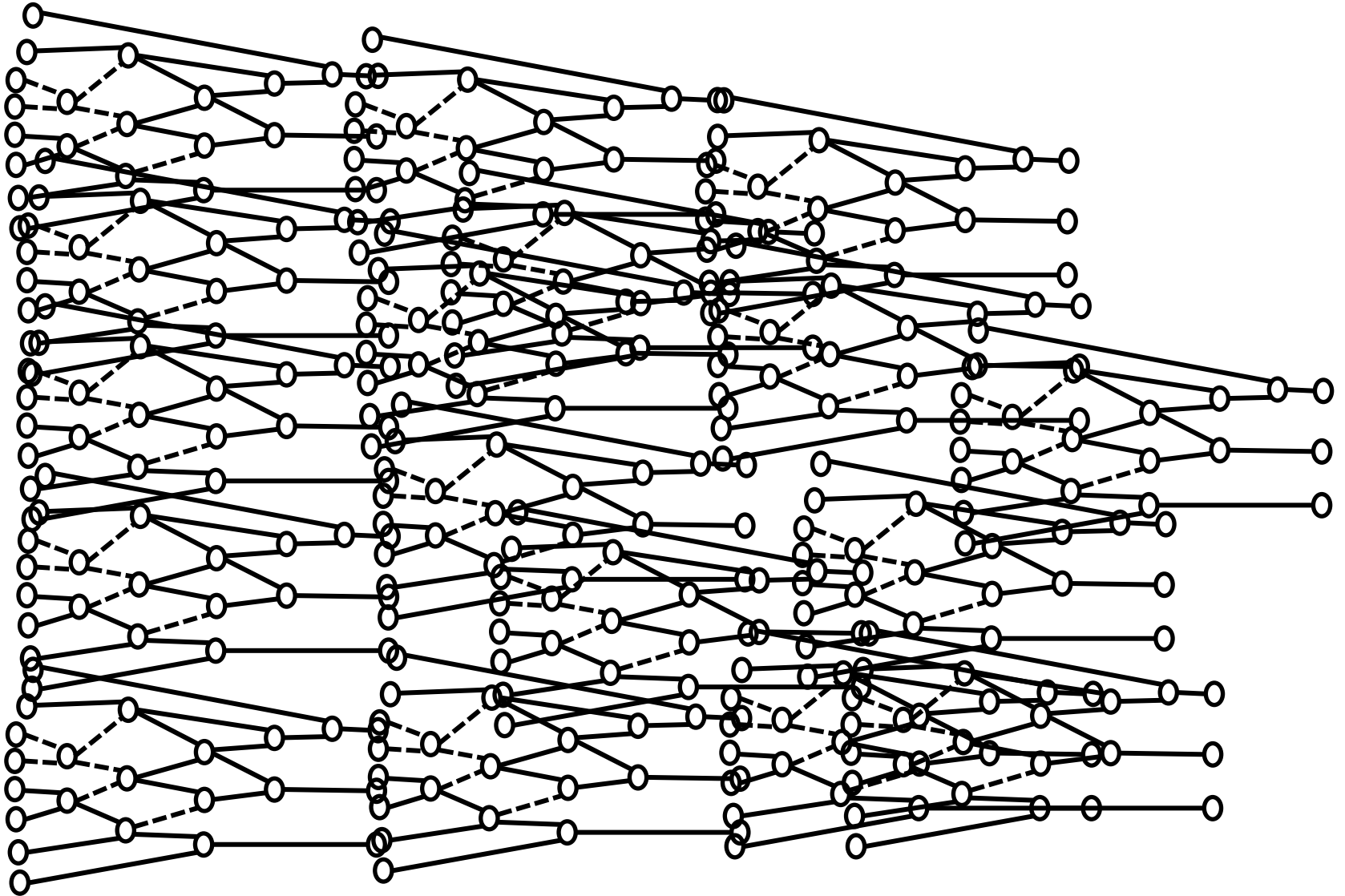
Design Constraints: Timing Budget



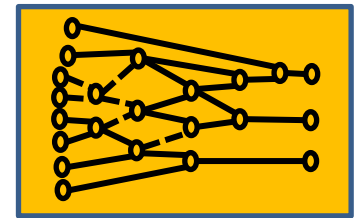
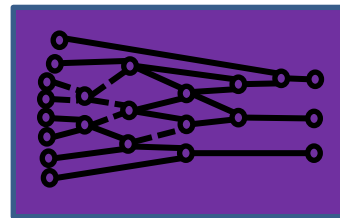
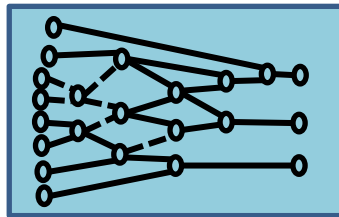
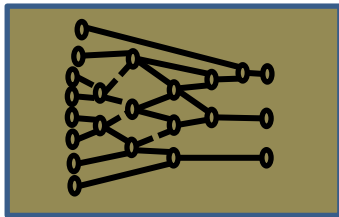
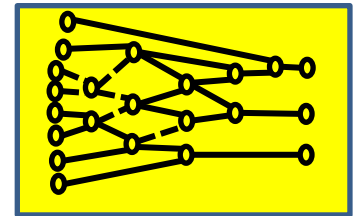
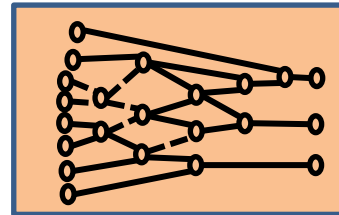
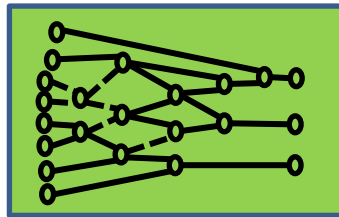
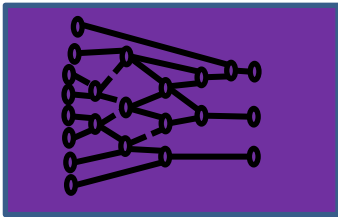
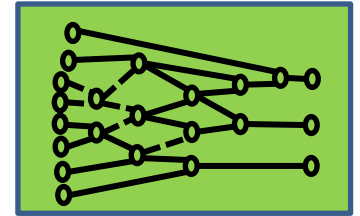
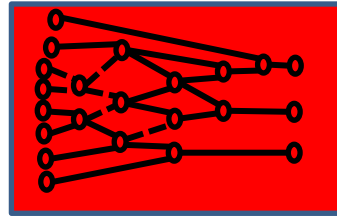
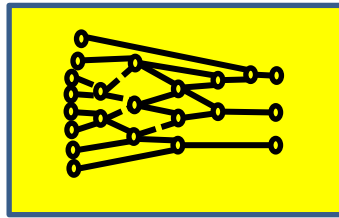
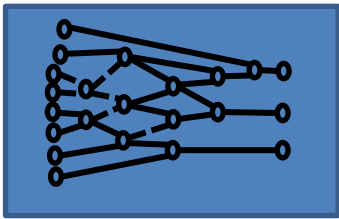
Design Constraints: Timing Budget



KL-cuts in AIGs

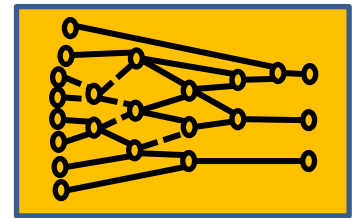
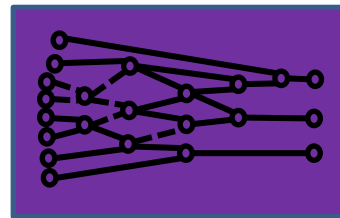
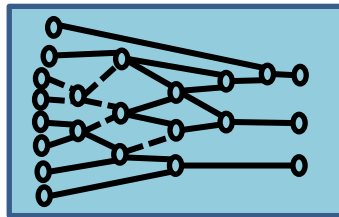
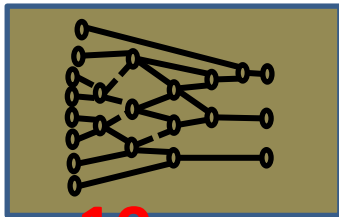
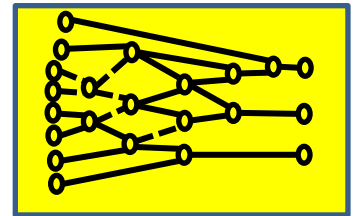
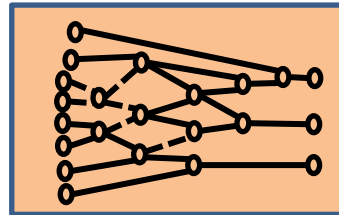
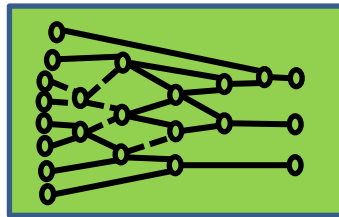
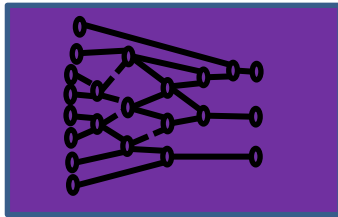
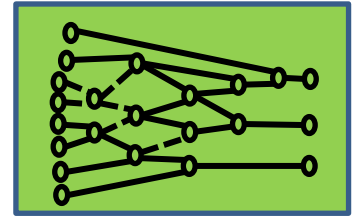
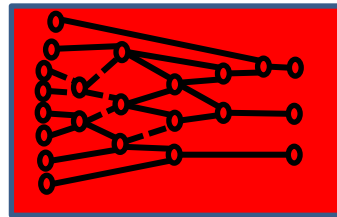
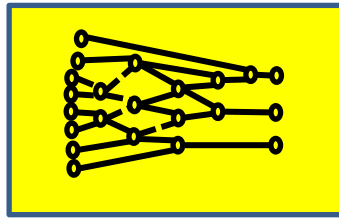
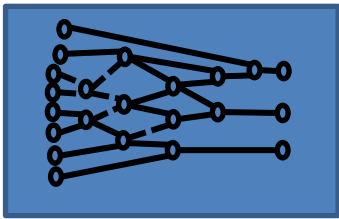


KL-cuts in AIGs



KL-cuts in AIGs

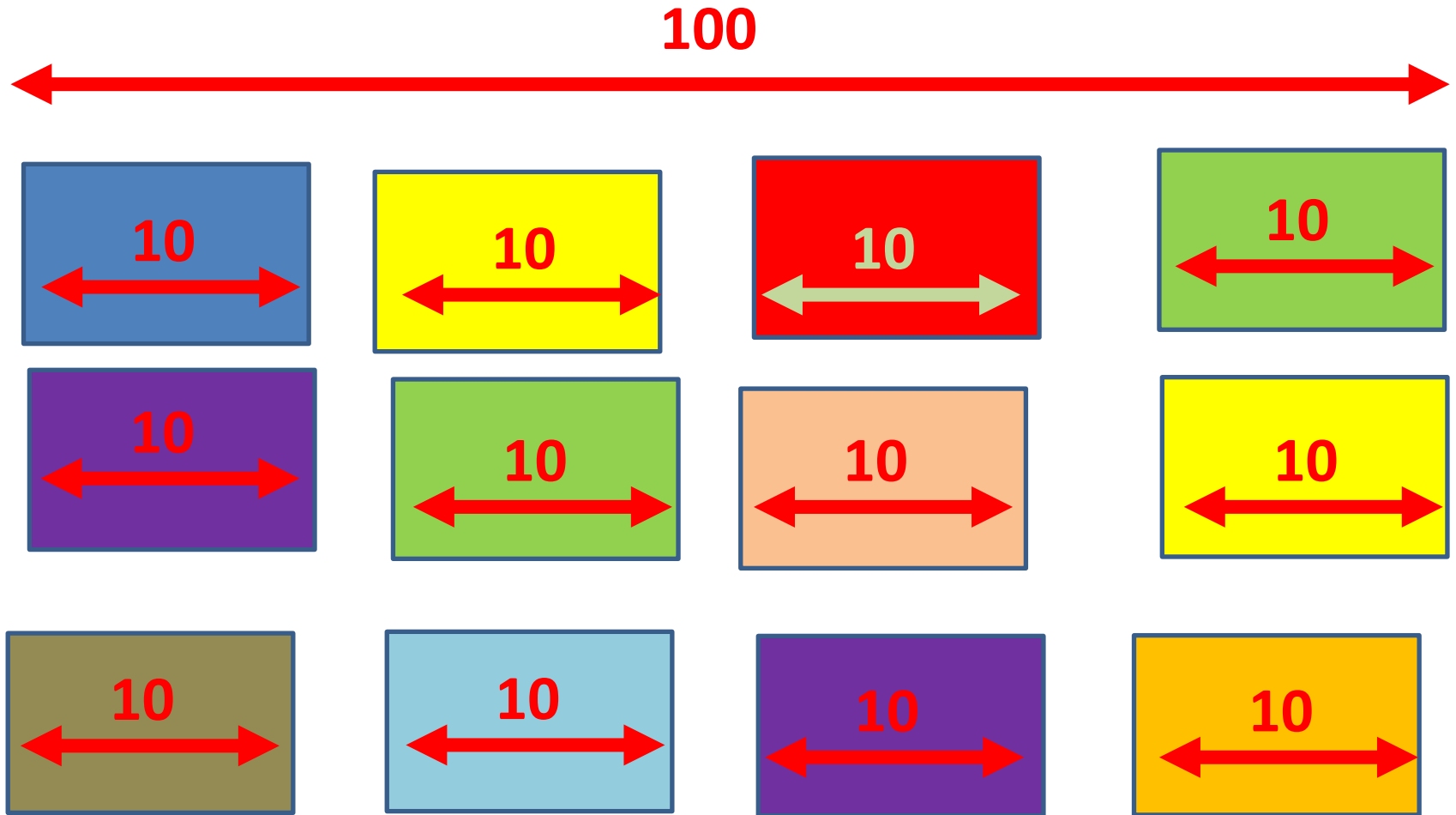
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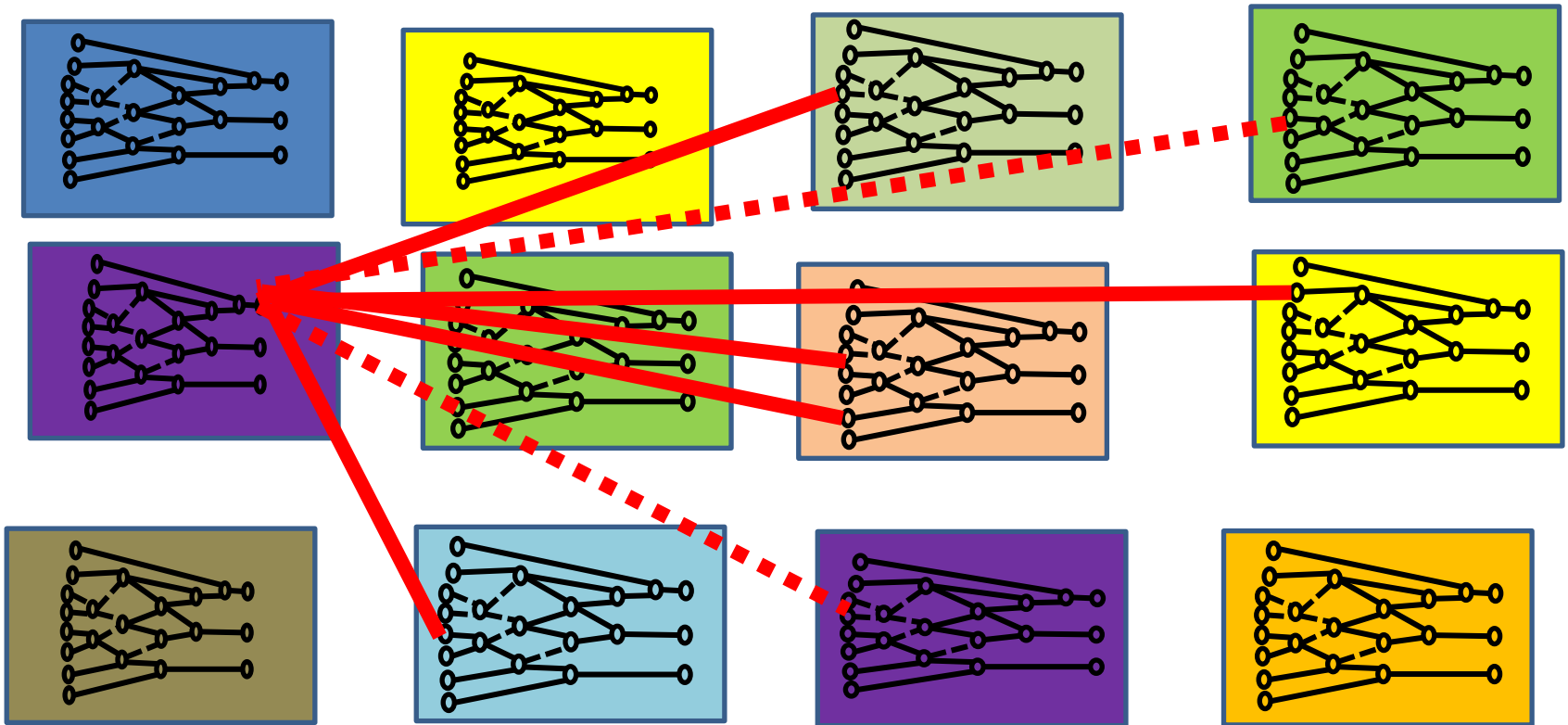
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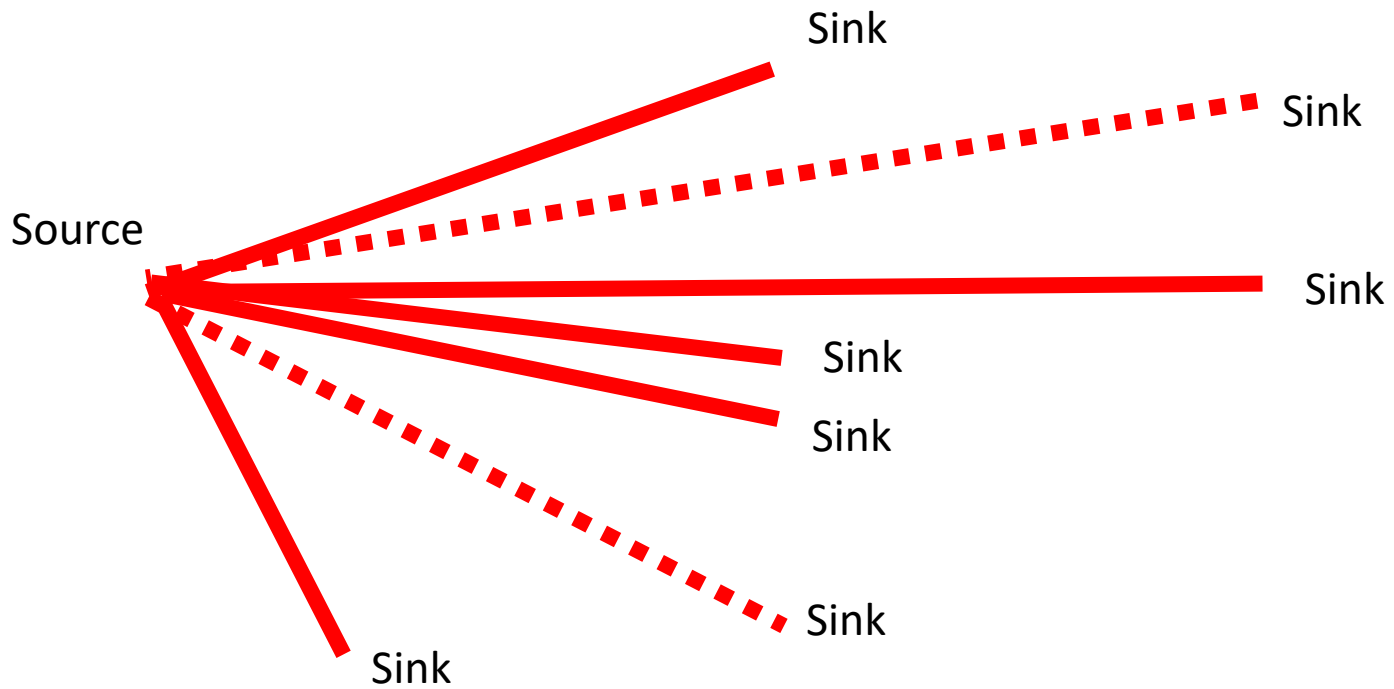
KL-cuts in AIGs



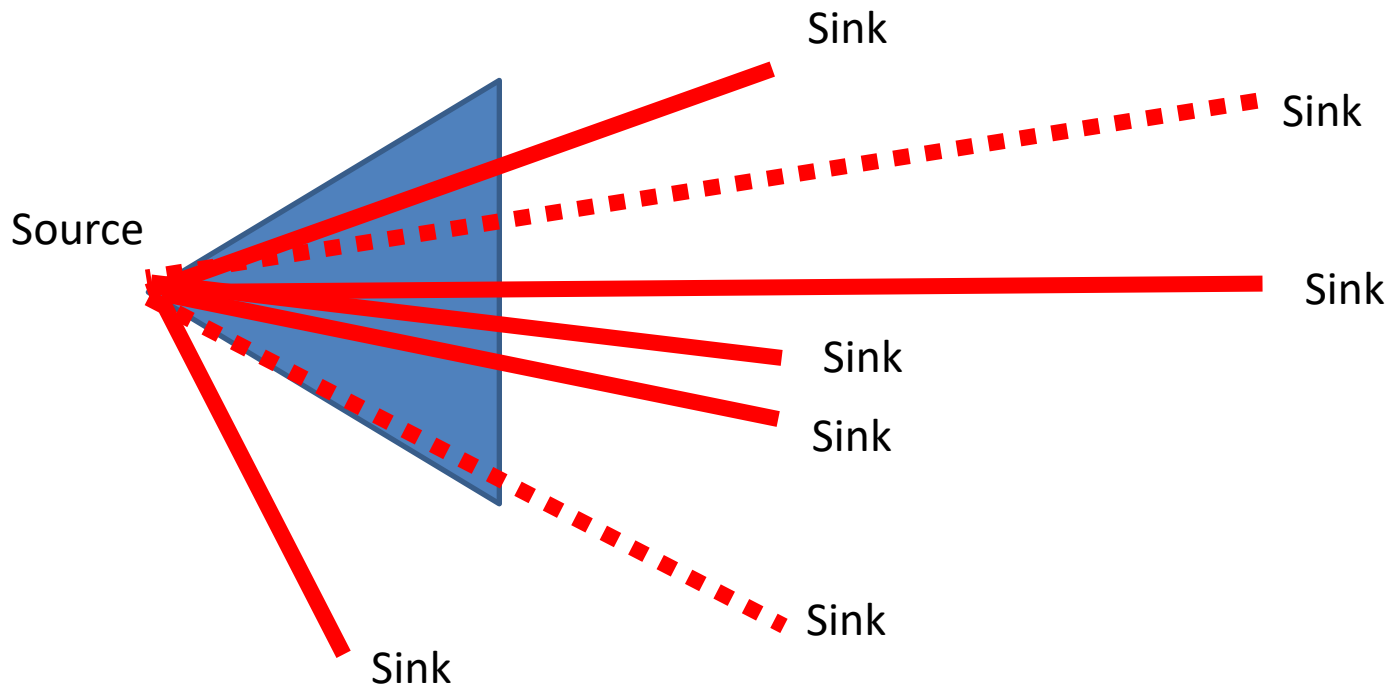
KL-cuts in AIGs: Signal Distribution



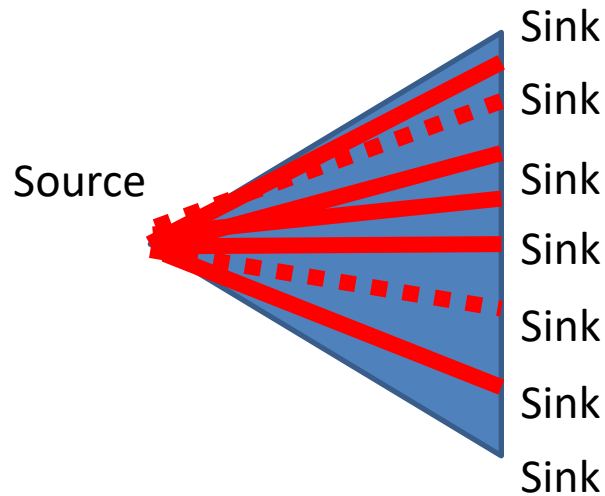
KL-cuts in AIGs



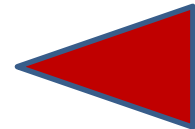
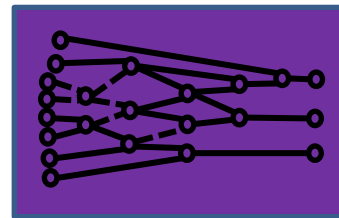
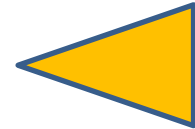
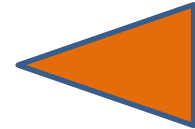
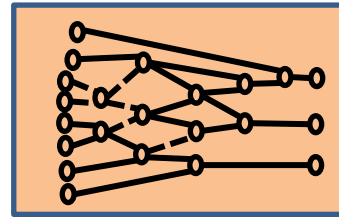
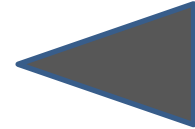
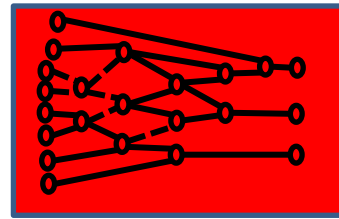
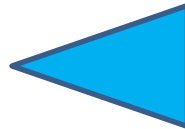
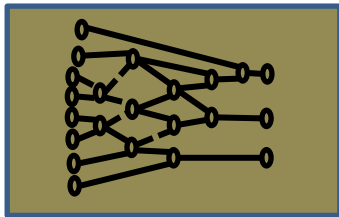
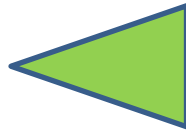
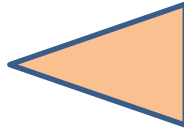
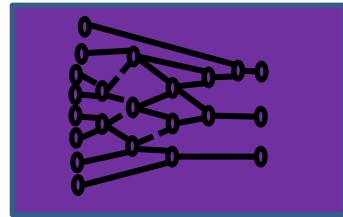
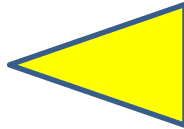
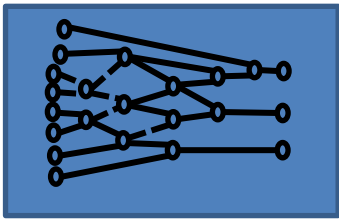
KL-cuts in AIGs



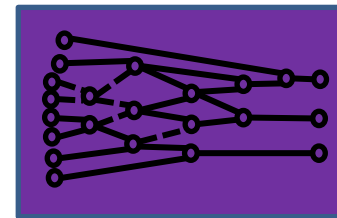
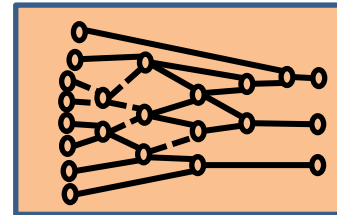
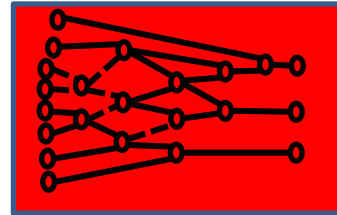
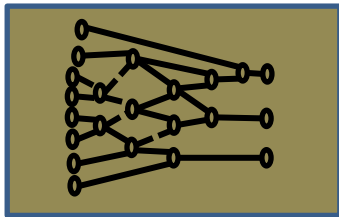
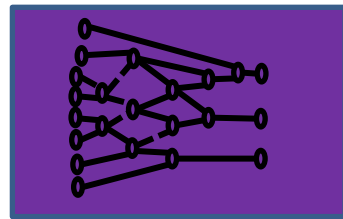
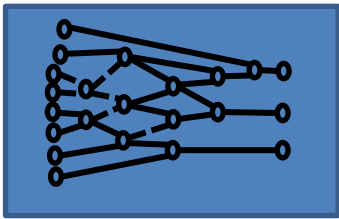
Signal distribution 1L-cuts in AIGs



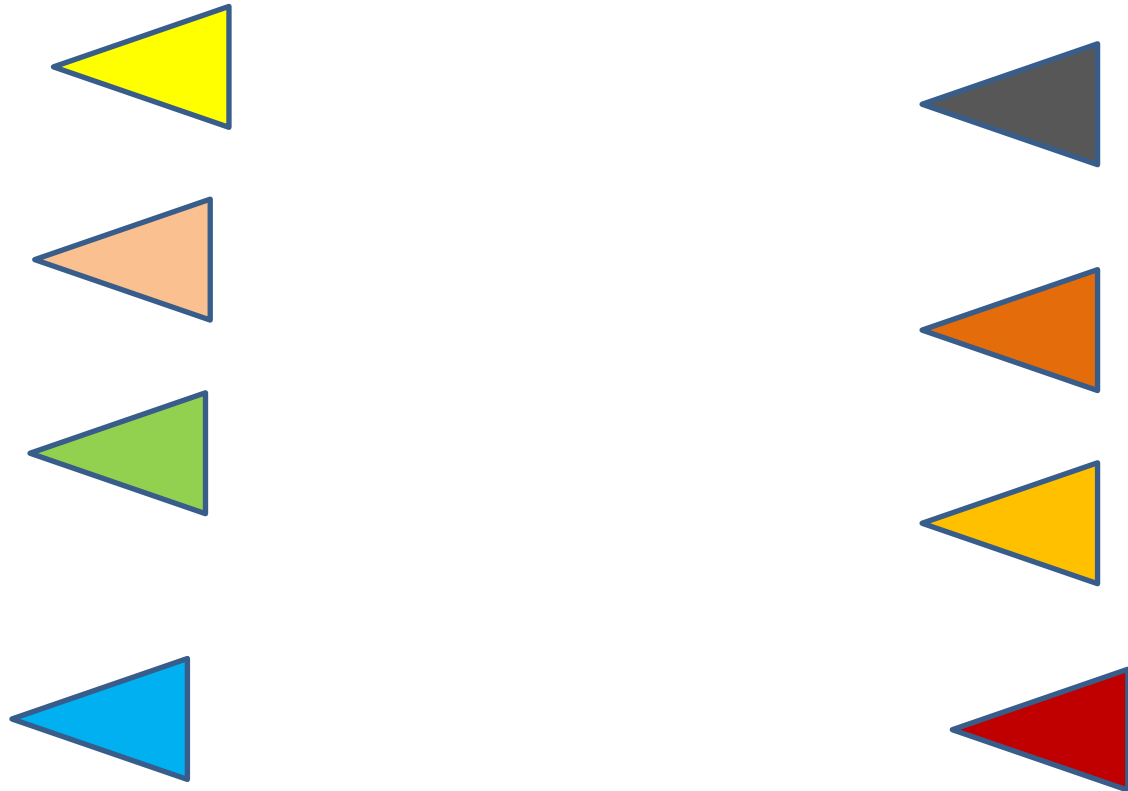
KL-cuts in AIGs



Logic Computation KL-cuts in AIGs



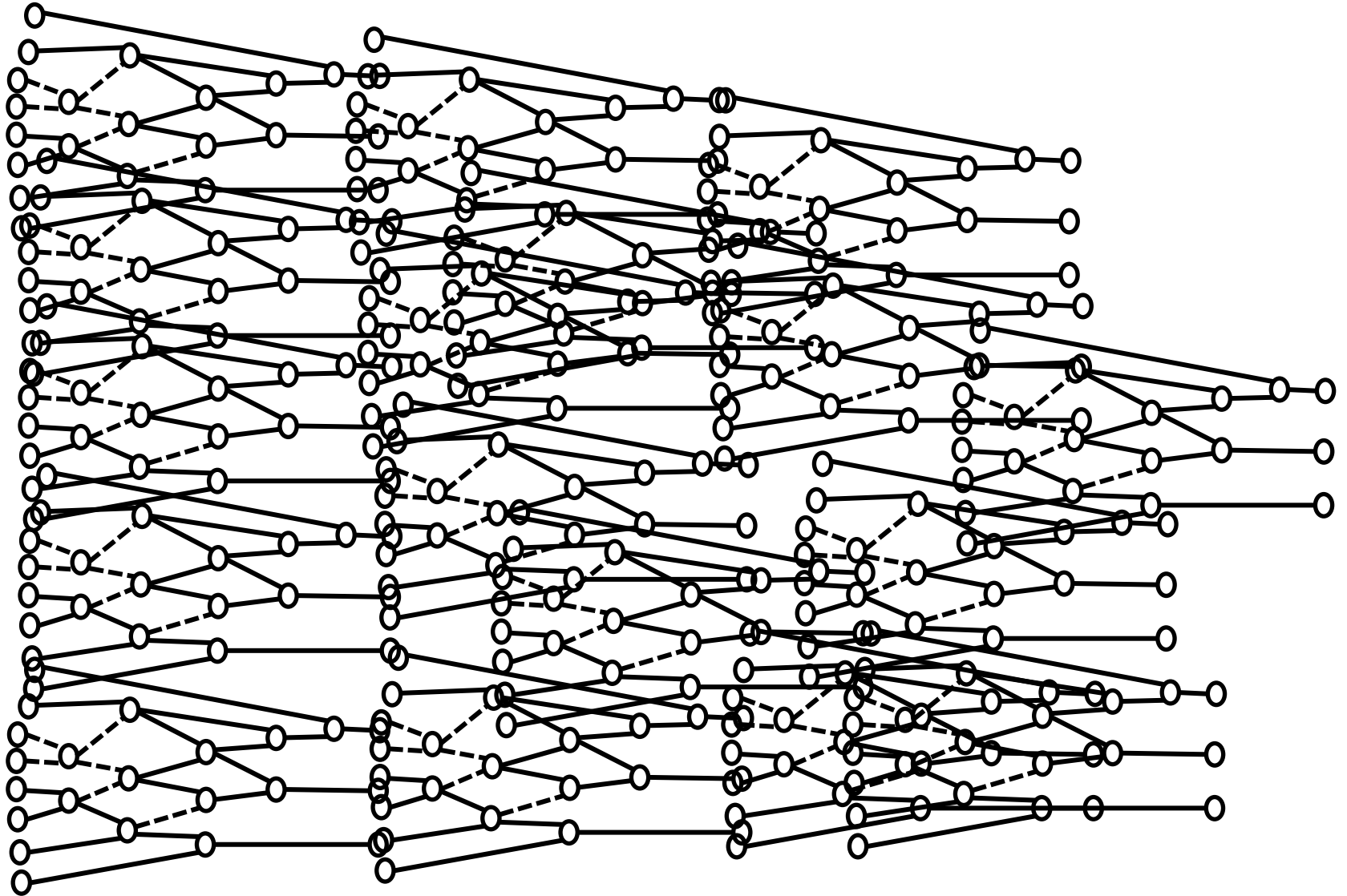
Signal Distribution 1L-cuts in AIGs



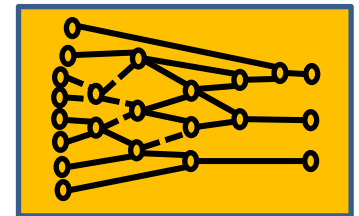
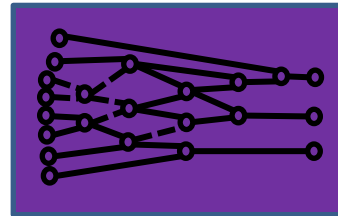
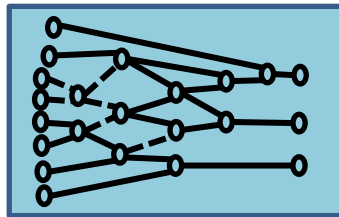
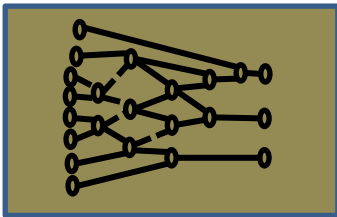
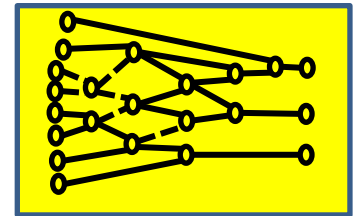
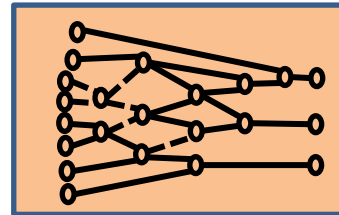
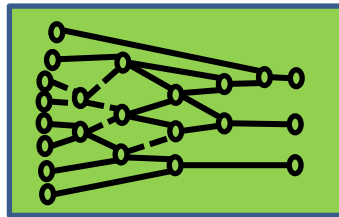
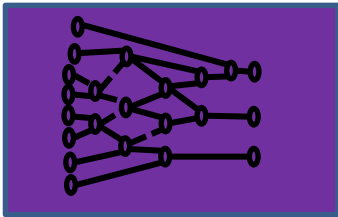
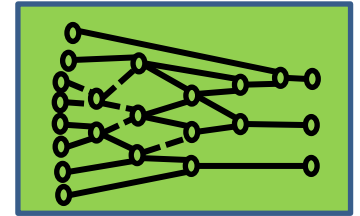
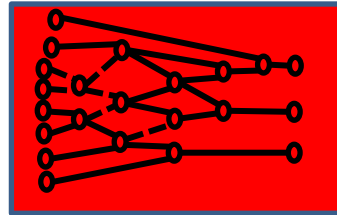
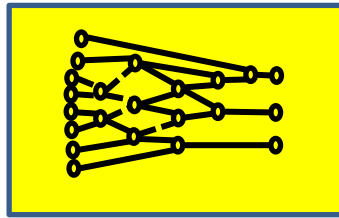
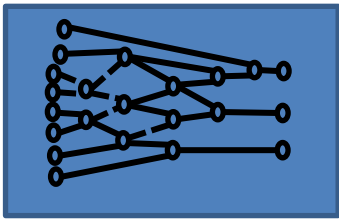
What about a design flow?

- This talk was supposed to bring technology information on early steps of logic synthesis!!!!

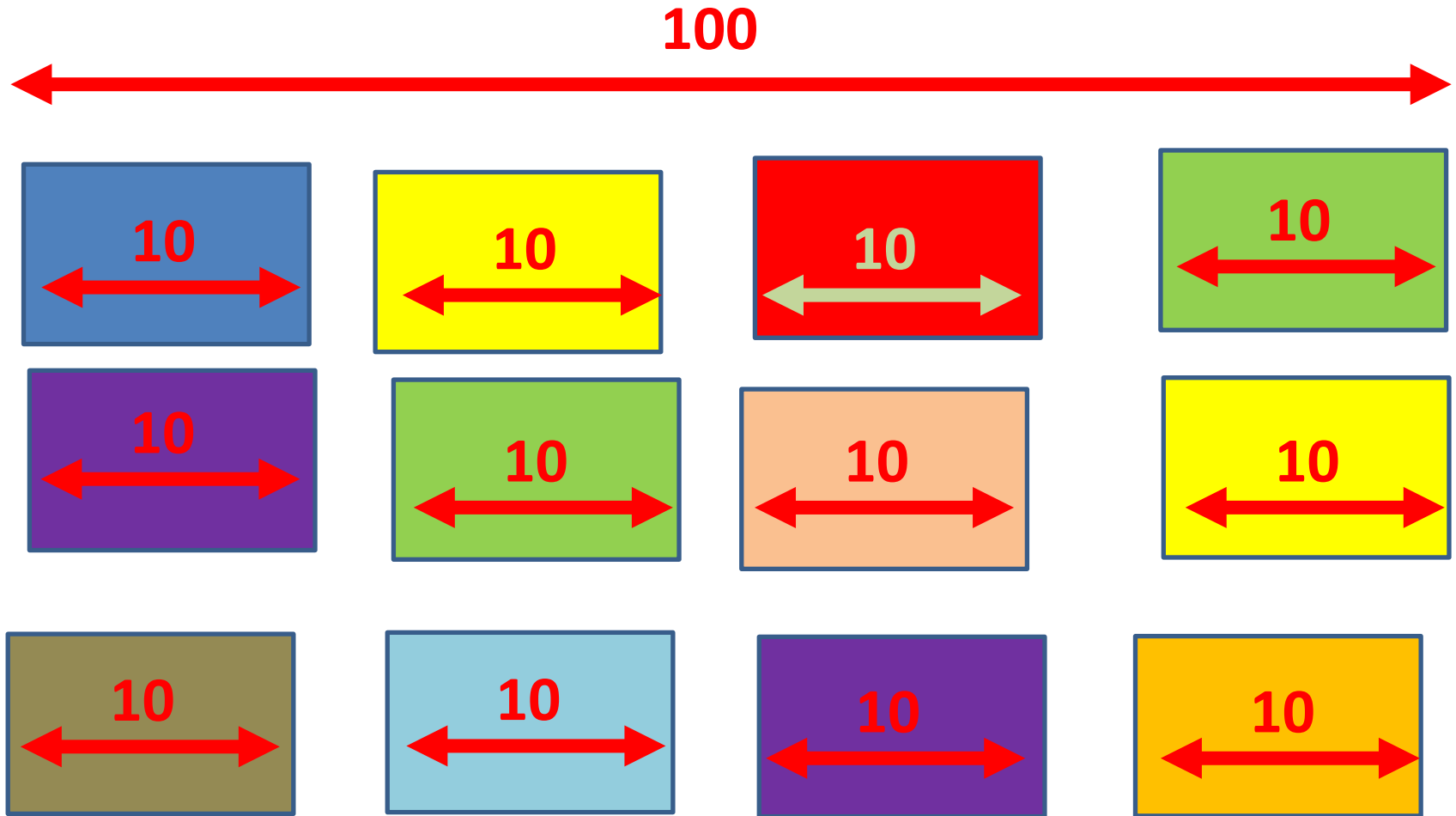
Step 1: Receive Input AIG



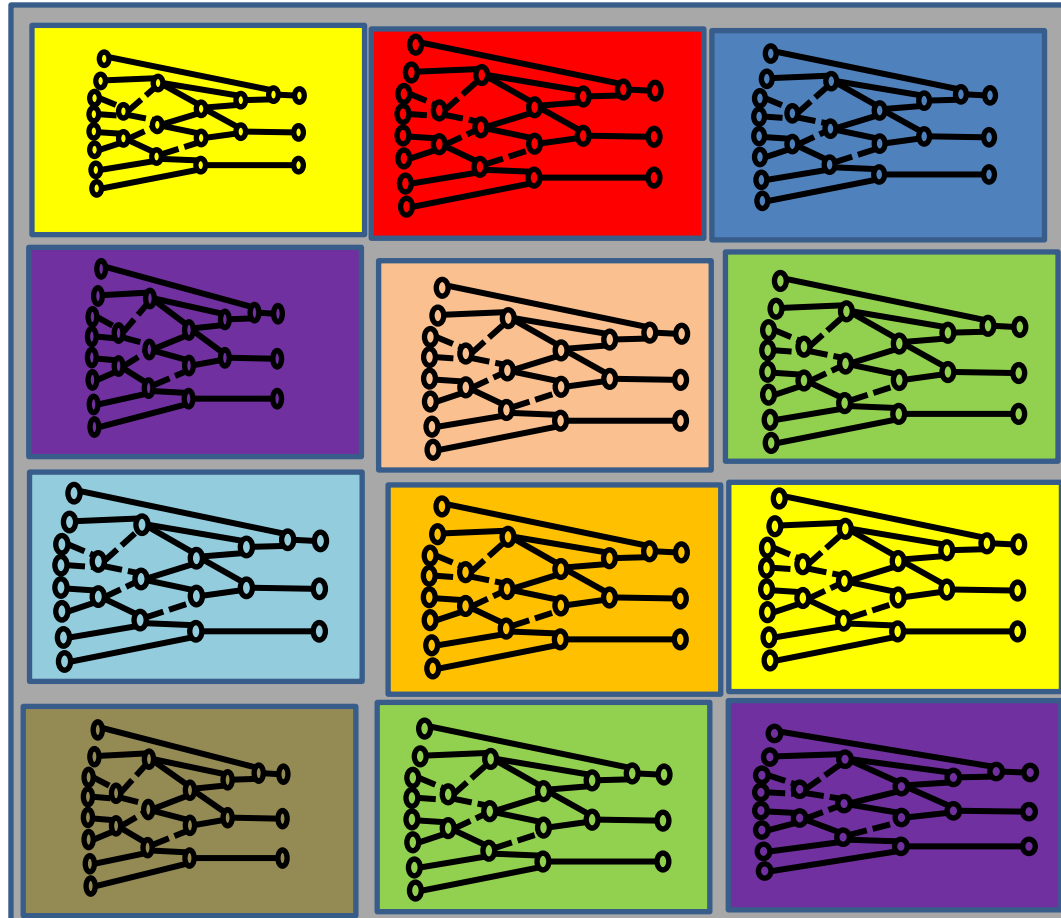
Step 2: Compute KL-cuts



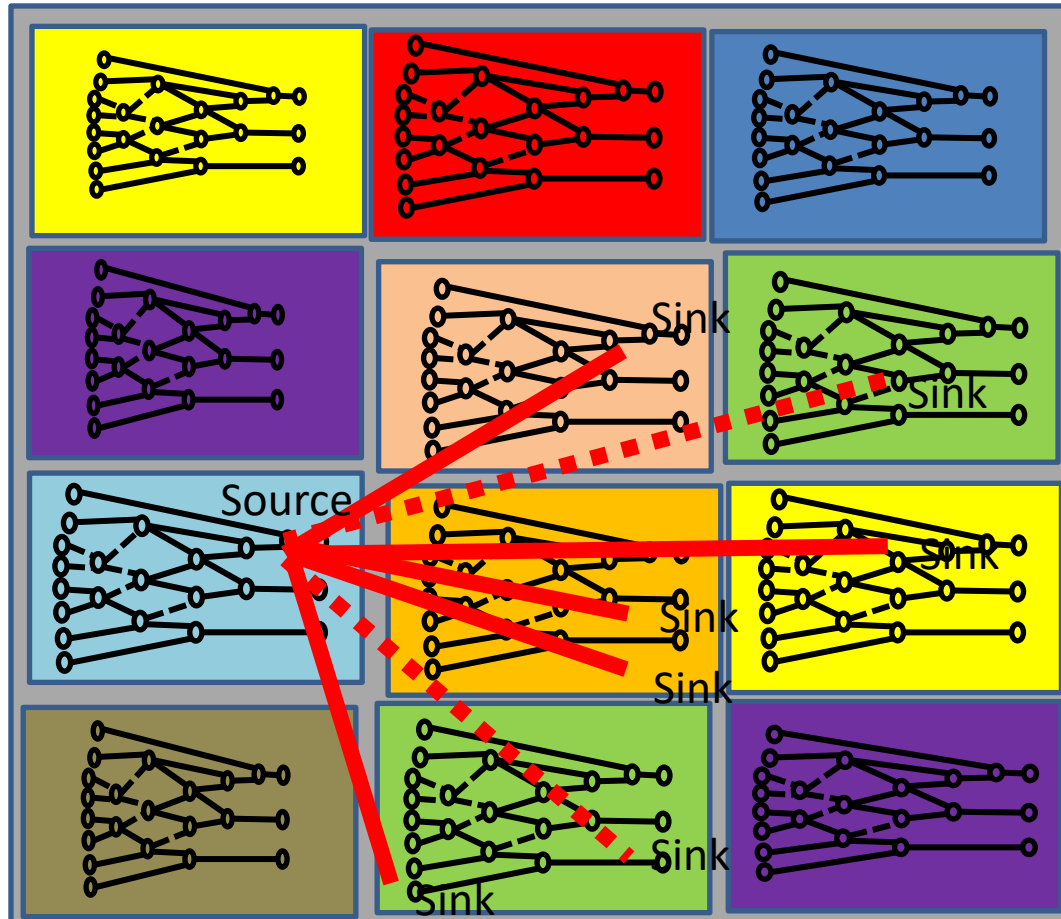
Step 3: Timing budget KL-cuts



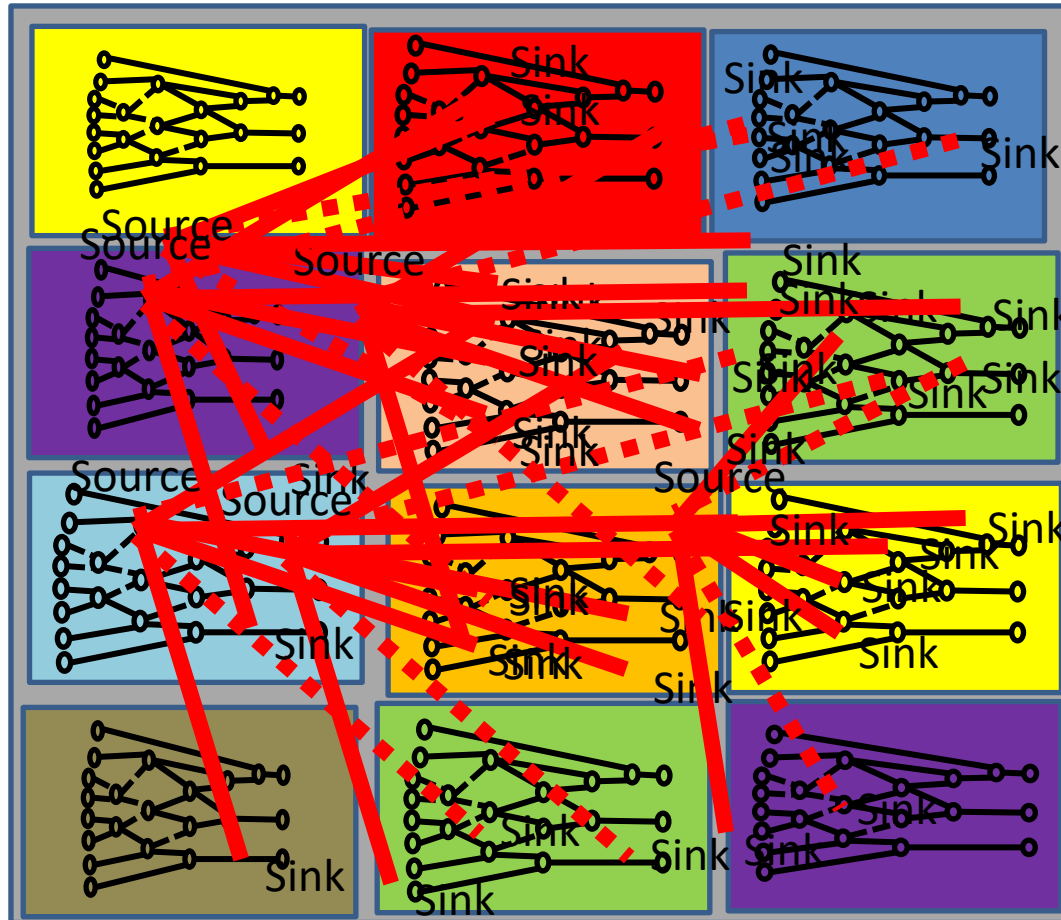
Step 4: Place KL-cuts



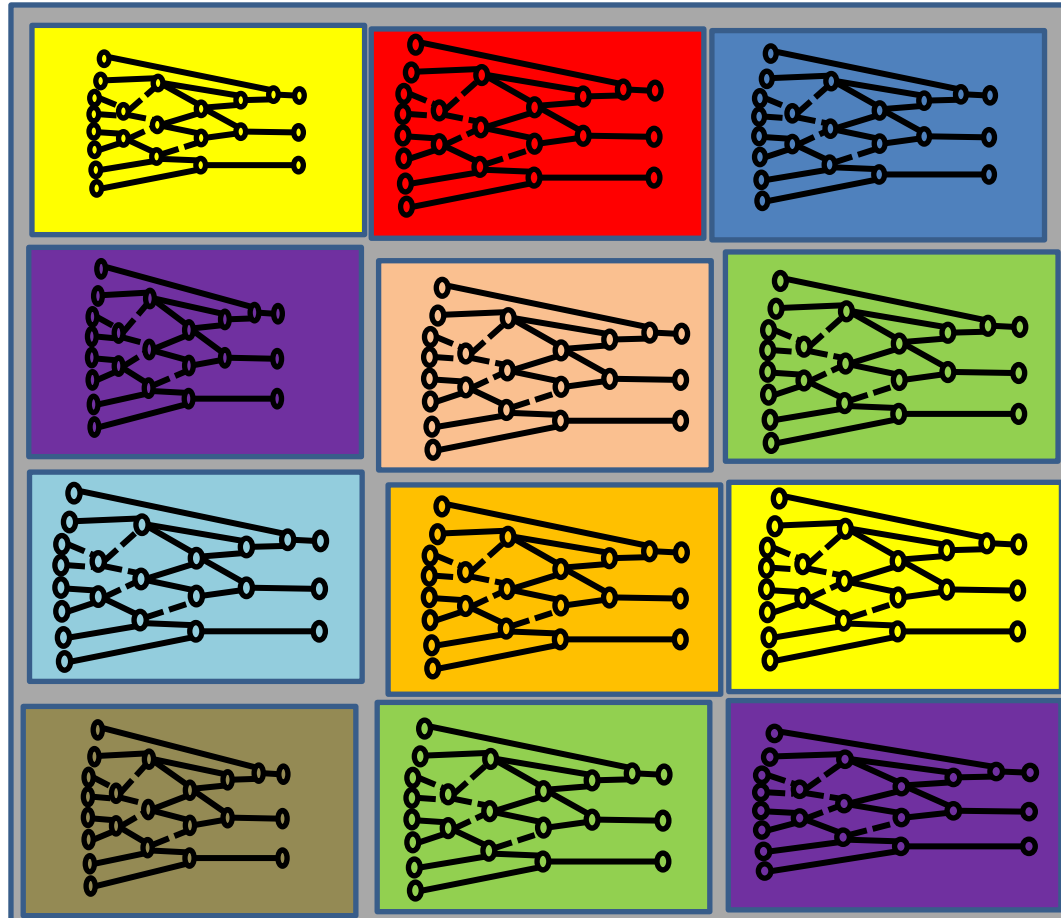
Step 5: Physical Design of 1L-cuts



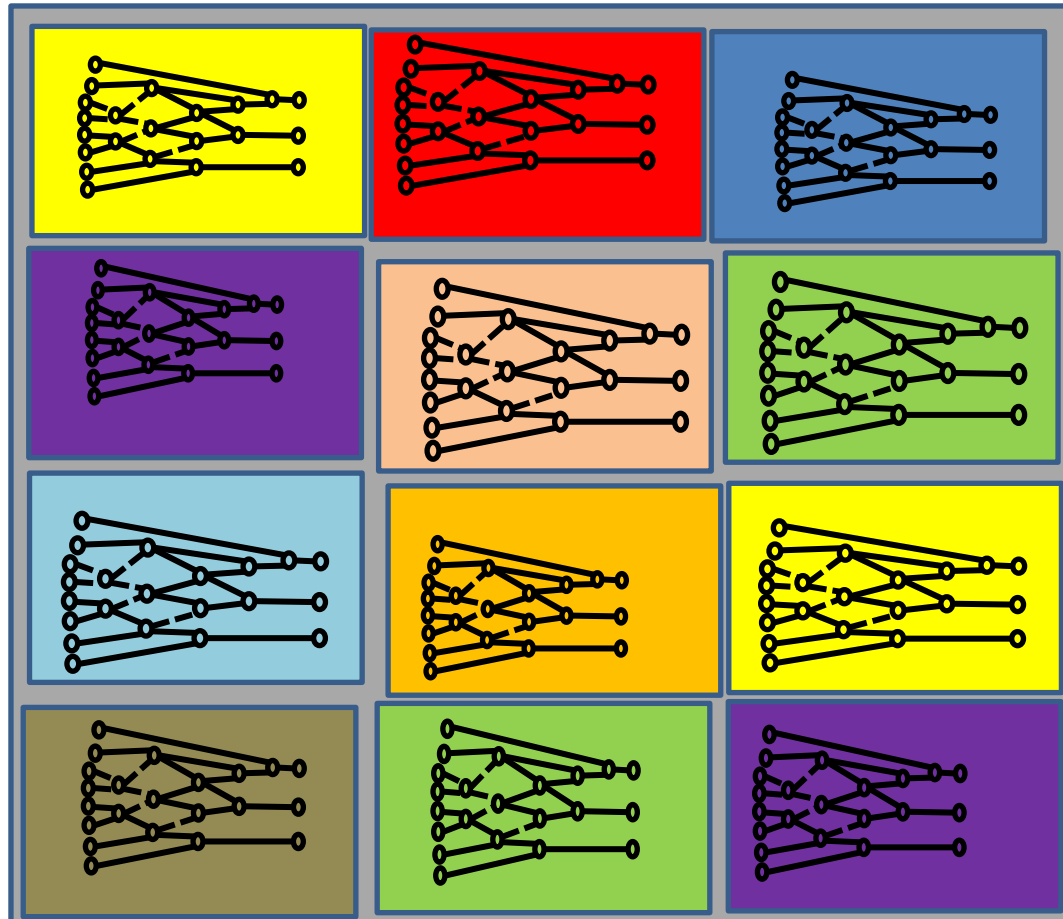
Step 6: Physical Design of 1L-cuts



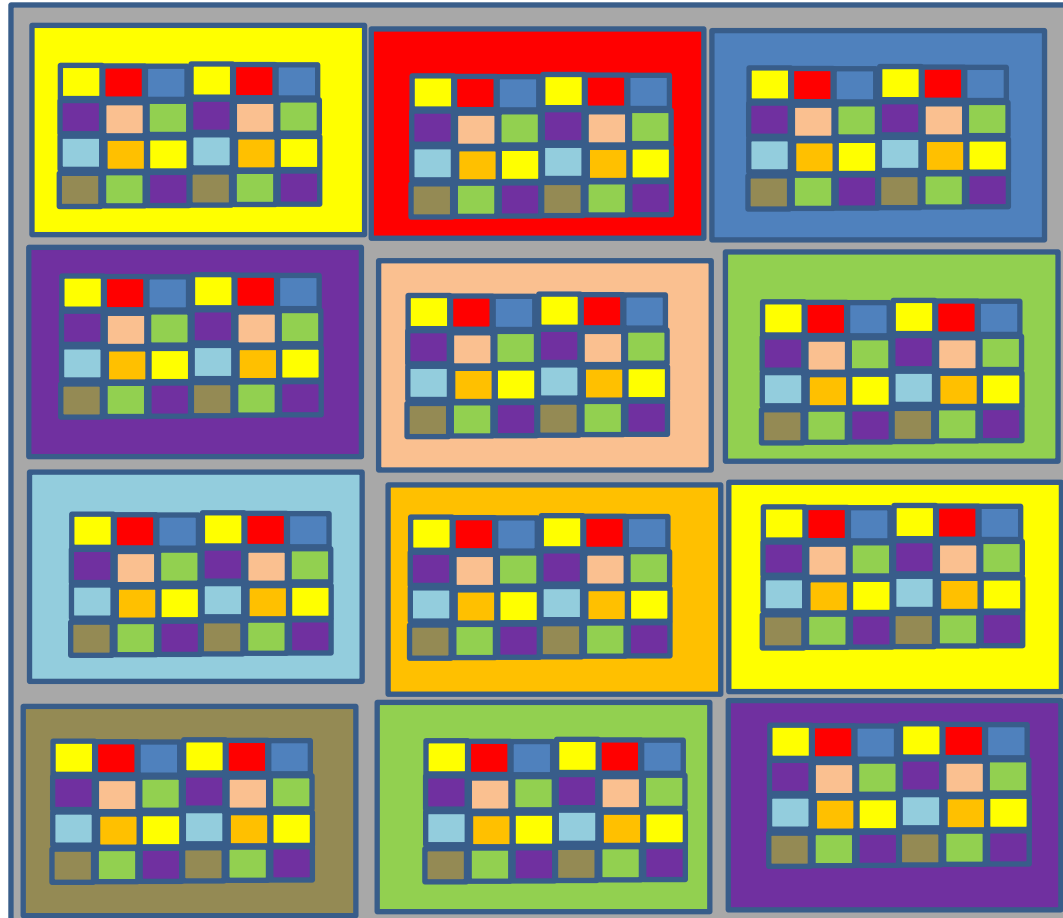
Step 6: Logic Synthesis of KL-cuts



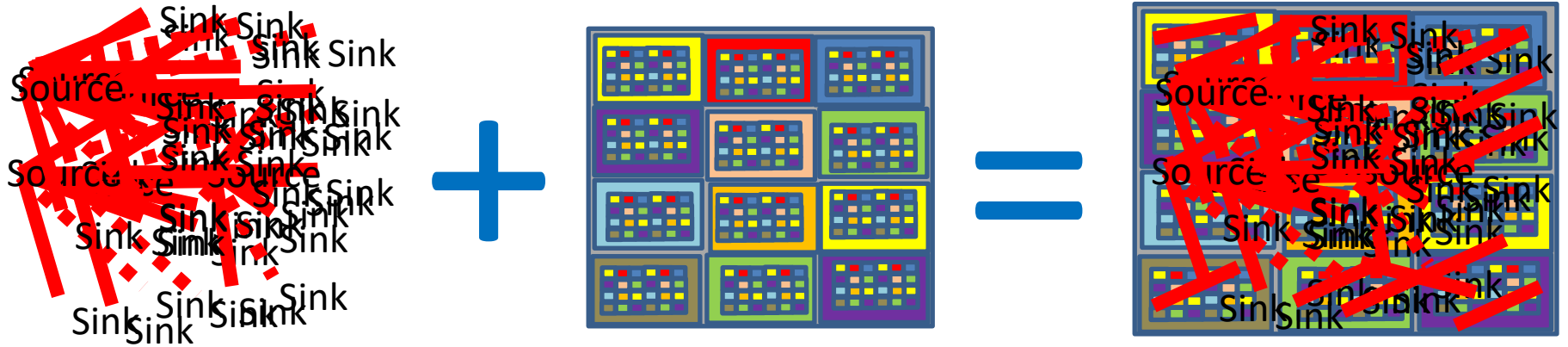
Step 6: Logic Synthesis of KL-cuts



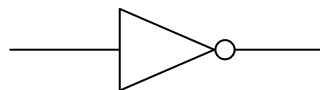
Step 7: Physical Design of KL-cuts



Step 8: Join Low Layers and Top Layers

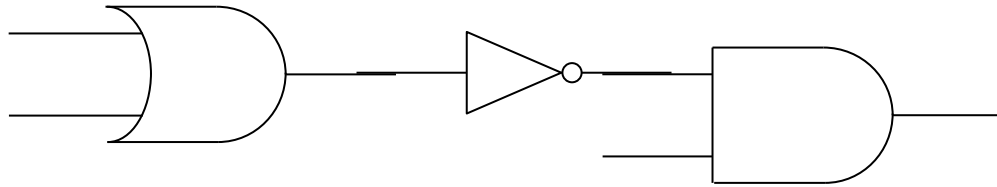


Conclusion: different inverters

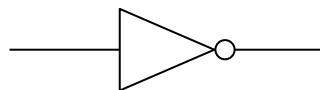


Conclusion: different inverters

- Logic computation inverter

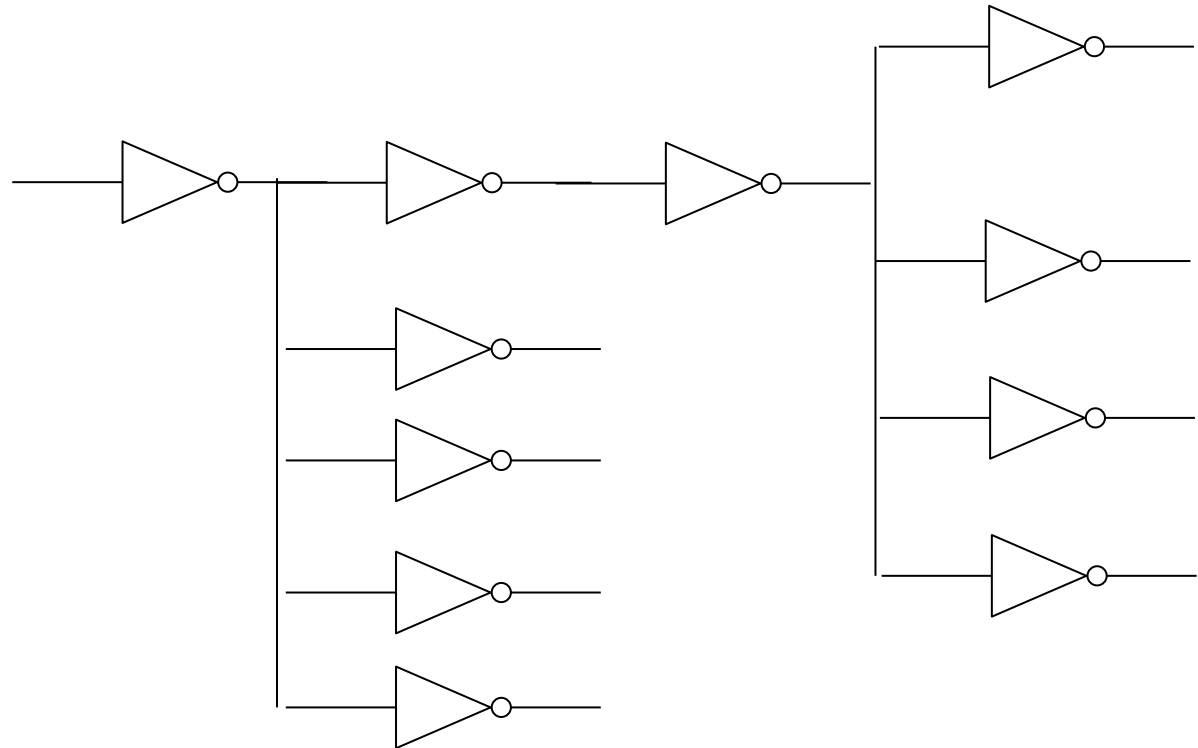


Conclusion: different inverters



Conclusion: different inverters

- Signal distribution inverter



Conclusion

- The point is not try to mix
 - logic synthesis and
 - Physical design
- But to think about
 - Signal distribution and
 - Logic computation
- Signal distribution has elements of
 - Global routing
 - Clock distribution, but of signals instead of clocks