

2004 International Symposium on Physical Design

Hyatt Regency, Phoenix, Arizona

April 18th – 21st, 2004

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PROGRAM

The International Symposium on Physical Design provides a high-quality forum for the exchange of ideas and results in critical areas related to the physical design of VLSI systems. The scope of this symposium includes all aspects of physical design, from interactions with behavior- and logic-level synthesis, to back-end performance analysis and verification.

Regular papers run 30 minutes. Short papers (s) are 15 minutes.

SUNDAY, APRIL 18

5:30 – 7:00 pm Evening Reception

MONDAY, APRIL 19

8:30 – 9:30 am Welcome and Keynote Address

Host: Charles J. Alpert / IBM

Beyond Moore's Law: The Interconnect Era

James D. Meindl, / Georgia Institute of Technology

9:30 – 10:00 am Morning break

10:00 - 12:00 am Session 1: Placement Techniques

Chair: Patrick Madden / SUNY Binghamton

Almost Optimum Placement Legalization by Minimum Cost Flow and Dynamic Programming

Ulrich Brenner, Anna Pauli, Jens Vygen / University of Bonn

Sensitivity Guided Net Weighting for Placement Driven Synthesis

Haoxing Ren, David Z. Pan, David S. Kung / UT Austin and IBM

Implementation and Extensibility of an Analytic Placer

Andrew B. Kahng and Qinke Wang / UCSD

FastPlace: Efficient Analytical Placement using Cell Shifting, Iterative Local Refinement and a Hybrid Net Model

Natarajan Viswanathan, Chris Chong-Nuen Chu, / Iowa State University

12:00 – 1:30 pm Lunch

1:30 – 3:00 pm Session 2: Routing Topology Optimization

Chair: Narendra Shenoy / Synopsys

Multilevel Routing with Antenna Avoidance

Tsung-Yi Ho, Yao-Wen Chang, Sao-Jie Chen, Margaret Marek-Sadowska, / UCSB

(s) *An ECO Algorithm for Eliminating Crosstalk Violations*

Hua Xiang, Kai-yuan Chao and D. F. Martin Wong / UIUC

(s) *Fast Algorithm for Identifying Good Buffer Insertion Locations*

Charles J. Alpert, Milos Hrkic, Stephen T. Quay / IBM Austin

Performance-Driven Register Insertion in Placement

Dennis K.Y. Tong and Evangeline F.Y. Young / Chinese University of Hong Kong

3:00 – 3:30 pm Afternoon break

3:30 – 5:00 pm Panel session 3: Buffering and Agony: What does the Future Hold?

Organizer and Chair: Desmond Kirkpatrick / Intel

Panelists:

Dennis Sylvester / University of Michigan, Prashant Saxena / Intel, Lou Scheffer / Cadence Pete Osler / IBM

6:30 – 9:30 pm Heard Museum Dinner Banquet

Dinner Speaker: Steve Schulz / SI2

TUESDAY, APRIL 20

8:30 – 10:00 am Session 4: Floorplanning

Chair: Lou Scheffer / Cadence

Floorplanning for Throughput

Mario R. Casu Luca Macchiarulo / Politecnico di Torino

Multi-project Reticle Floorplanning and Wafer Dicing

Ion Mandoiu / University of Connecticut

(s) *An Area-Optimality study of floorplanning*

Jason Cong, Gabriele Nataneli, Michail Romesis, Joe Shinnerl / UCLA

(s) *Recursive Bisection Based Mixed Block Placement*

Ateen Khatkhate, Chen Li, Ameya R. Agnihotri, Mehmet Can Yildiz, Satoshi Ono, Cheng-Kok Koh, Patrick H.

Madden/ SUNY Binghamton, Purdue University, and IBM Austin

10:00 – 10:30 am Morning break

10:30 – 12:00 am Session 5: Regular Circuit Fabrics: Act Two -- the Industrial Perspectives (invited)

Organizer and chair: Jason Cong / UCLA

Design Tools and flow for NEC's Structured ASIC ISSP
Takumi Okamoto/ NEC Corporation

Design Considerations for Regular Fabrics
Deepak Sherlekar/ Virage Logic

Structured ASIC, Evolution or Revolution?
Kun-Cheng Wu/ Faraday Corporation

12:00 pm – 1:30 pm Lunch

1:30 – 2:30 pm Session 6: 3-D Design (invited)

Organizers: Sani Nassif/IBM, Sachin Sapatnekar/UMN (chair)

The four degrees of 3D
Robert Montoye/ IBM

Technology, Performance, and Computer-Aided Design of Three-Dimensional Integrated Circuits
Rafael Reif/ MIT

2:30 – 3:45 pm Session 7: Power optimization

Margaret Marek-Sadowska/ UCSB

Topology Optimization of Structured Power/ Ground Networks
Jaskirat Singh, Sachin Sapatnekar / University of Minnesota

Power-Delivery Networks: Optimization with Thermal Reliability Integrity
Ting-Yuang Wang, Jeng-Liang Tsai, Charlie Chung-Ping Chen / Wisconsin

(s) Early-stage Power Grid Analysis for Uncertain Working Modes
Haifeng Qian, Sani R. Nassif, Sachin S. Sapatnekar / IBM and University of Minnesota

3:45 – 4:15 pm Afternoon break

4:15 – 5:00 pm Session 8: Clock (invited)

Organizer and chair: Sachin S. Sapatnekar / Minnesota

Power-Aware Clock Tree Planning
Enrico Macii, Alessandro Ivaldi/ Politecnico di Torino, Monica Donno/ BullDAST s.r.l. , Luca Mazzoni/ Accent s.r.l.

5:00 – 5:45 pm Session 9: FPGA (invited)

Organizer and chair: Massoud Pedram/ UC Irvine

Innovate or Perish: FPGA Physical Design
Majid Sarrafzadeh/ UCLA, Salil Rajee/Hier Design Inc.

WEDNESDAY, APRIL 21

8:30 – 10:15 am Session 10: Parasitic Analysis and Control

Chair: David Blaauw/ Michigan

(s) On Optimal Physical Synthesis of Sleep Transistors
Changbo Long, Jinjun Xiong, Lei He/ UCLA

Mutual Inductance Extraction and the Dipole Approximation
Salvador Ortiz, Rafael Escovar, Roberto Suaya/ Mentor Graphics France

(s) A New Multi-Ramp Driver Model with RLC Interconnect Load
Lakshmi K. Vakati, Janet Wang/ Arizona

(s) Optimal Gate Sizing for Coupling-Noise Reduction
Debjit Sinha, Hai Zhou, Chris C. N. Chu/ Northwestern

Clock Network Sizing via Sequential Linear Programming with Time-domain Analysis
Kai Wang, Malgorzata Marek-Sadowska/ UCSB

10:15 – 10:45 am break

10:45 – 11:15 am Session 11: Design Styles (invited)

Organizer and chair: Charles J. Alpert/IBM

Placement Driven Synthesis Case Studies on Two Monster Chips: hierarchical and flat
Pete Osler/ IBM

11:15 – 12:15 am Session 12 Statistical Analysis for Placement

Chair: Raymond Nijssen/ Magma

(s) A Study of Netlist Structure and Placement Efficiency
Qinghua Liu, Malgorzata Marek-Sadowska/UCSB

(s) Probabilistic Congestion Prediction
Jurjen Westra, Chris Bartels, Patrick Groeneveld/ Eindhoven University

A Predictive Distributed Congestion Metric and its Application to Technology Mapping
Rupesh S. Shelar, Sachin S. Sapatnekar, Prashant Saxena, and Xinning Wang/ University of Minnesota

12:15 – 12:30 pm Closing Remarks

SYMPOSIUM REGISTRATION

Please register on-line at <http://www.ispd.cc> by Wednesday, March 24, 2004 for the early registration discount rates.

HOTEL ACCOMODATIONS AND TRAVEL

ISPD 2004 is being held at the Hyatt Regency Hotel in Phoenix, Arizona. The address of the hotel is:
122 North Second Street
Phoenix, Arizona
85004 USA
Tel: +1 602 252 1234
Fax: +1 602 254 9472
<http://hyattphoenix.com>

For online reservations, use the group/corporate number **G-ACM1** when reserving your room. You can also make reservations by phone.

Conference Attendees will receive a special hotel rate of \$130 if they reserve a room with the hotel by 3/28/04; be sure to mention ACM/ISPD 2004 when you make your reservation.

The Phoenix airport (PHX) is close to the hotel; there are direct flights from the major Bay Area airports, LAX, as well as many of the East Coast hubs.

The hotel is already **sold out** for the dates of the symposium. The only rooms that are open are those reserved for ISPD. If the ISPD block of rooms sells out, there are no other rooms in the hotel available. Reserve early to give yourself the best chance of getting a room

Symposium Organization

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Charles J. Alpert/ IBM

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Massoud Pedram/ USC

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Sachin Sapatnekar/ Minnesota

Steering Committee

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