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# Clock Tree Design for Robust Low power design

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# Outline

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- Clock Tree Design Goals
- Definition of Balanced clock tree
- Control of clock Insertion Delay and Skew
- Low Power with Clock gating and Clustering
- Clock Analysis and Process Tracking
- Summary



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# Clock Tree Design Goals

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*Design Goals*

*Balanced Structure*

*Low Power*

*Analysis*

- Balanced Clock Tree across all PVT: Maximize yield
- Low Clock insertion delay : Maximize performance
- Low Clock skew: Minimize area, power



# Process Variations and Clock Tree

- Clock skew significant part of cycle time for high speed designs
- Uncertainties in clock network delays can reduce performance, yield and may cause functional failure
- Several scaling effects contribute to uncertainty in clock distribution network
  - Process variation (N/P mistrack,  $V_t$ ,  $T_{ox}$ )      Metal mistrack [*Skew/delay*]
  - Power Grid noise [*delay/skew*]      Coupling Noise [*Delay/Skew*]
  - Misalignment [*via resistance*]      Random Dopant Fluctuation [ $V_T$ ]
  - NBTI [ $V_T$ /*Delay*]      Poly CD control [*Delay/Skew*]
  - Model, spice, extraction, tool limitations      CMP [*Thickness/delay/skew*]
  - Metal density and fill [*Delay/skew*]      PLL (jitter, duty cycle)
  - Non Linear resistance [*Delay/Skew*]
  - .....
- Balanced clock structure enables clock distribution to track variations across the design
- Key challenge at 90nm and below is variability



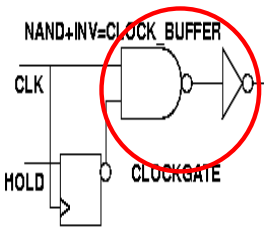
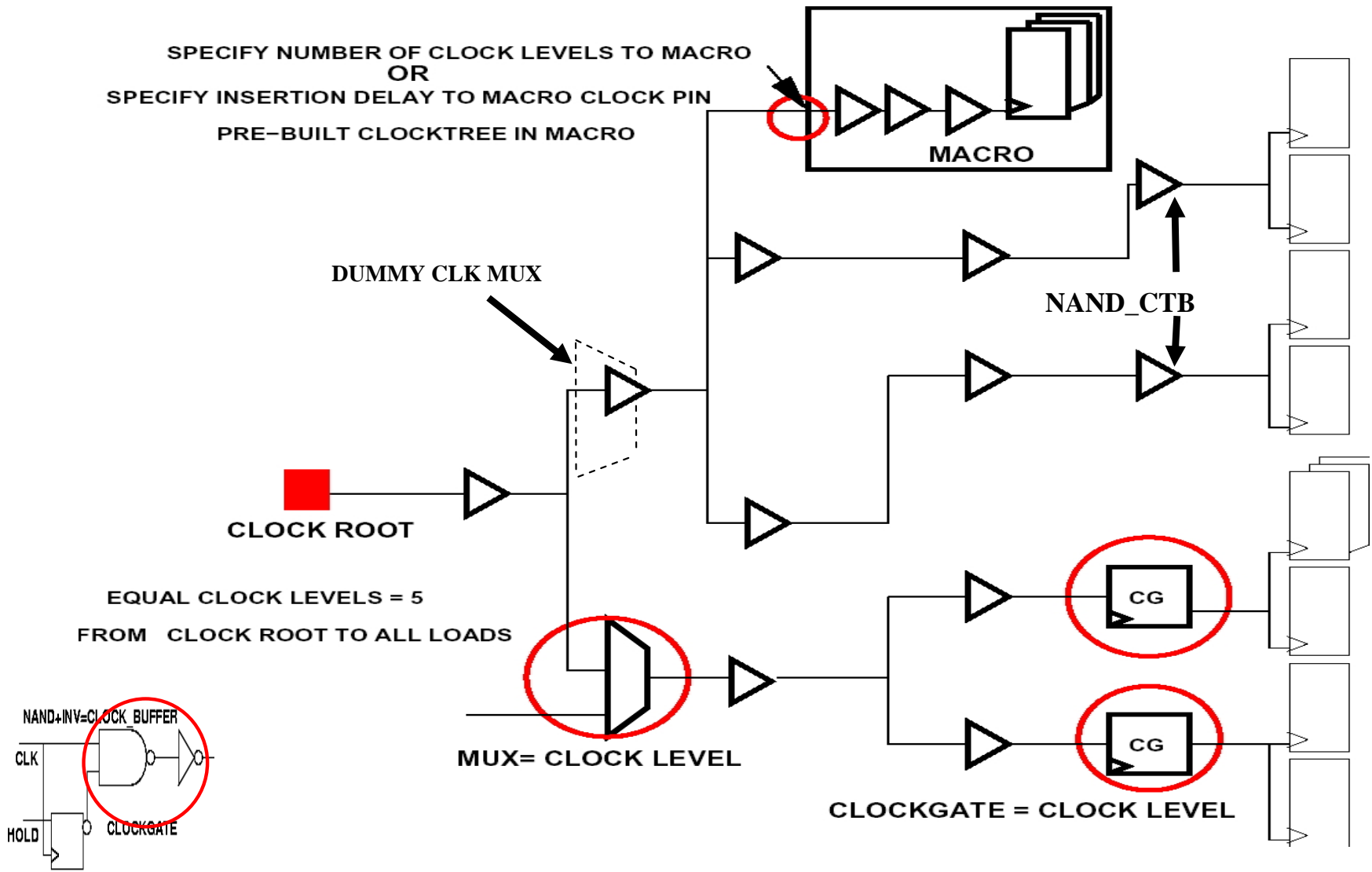
# Defining Balanced Clock Tree Structure

- Structure :Balanced clocktree has equal levels to all clock loads
  - Needed to balance interconnect and gate delay
  - Depth mismatch : Large buffer driving long interconnect and series of smaller buffers with shorter interconnect
    - Will scale differently with FEOL (front end of line: transistor) and BEOL (back end of line: Interconnect/metal ) variations
  - Enables clock tree to track across process corners (PVTI)
  - Replicate gates to match gate delay on different clock branches
    - Add dummy muxes
    - Use clock buffers with matching clockgate delays for non-clockgated branches
  - Clock route has matched RC by restricting to metal layers with similar RC
    - Minimize sensitivity to process variation
    - Correlation is more likely to be maintained if route is constrained to layers with identical cross-sections and processing steps
    - Common part of clocktree (global) uses upper level metals to reduce insertion delay and maintain matching interconnect delay



# Balanced Clock Tree Levels

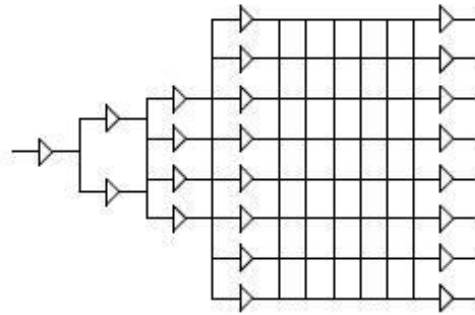
Design Goals  
Balanced Structure  
Low Power  
Analysis





# Clock Distribution techniques for Low Skew

- **Clock-Grid DEC Alpha 21064**
  - Low local skew , Regular routing,
  - Simpler to implement and early in design
  - Routing resource and power,
  - Global shorted grid
  - Local grid multi-clock domains
- **H-Tree: PowerPC**
  - Lower power, less routing resource
  - Can enable multiple domains
  - Uneven load distribution can affect skew
  - Buffered tree



DEC Alpha 21064 Clock Buffer Tree

Ref: JSSCC 1998 600 Mhz clock distribution, Bailey et. al

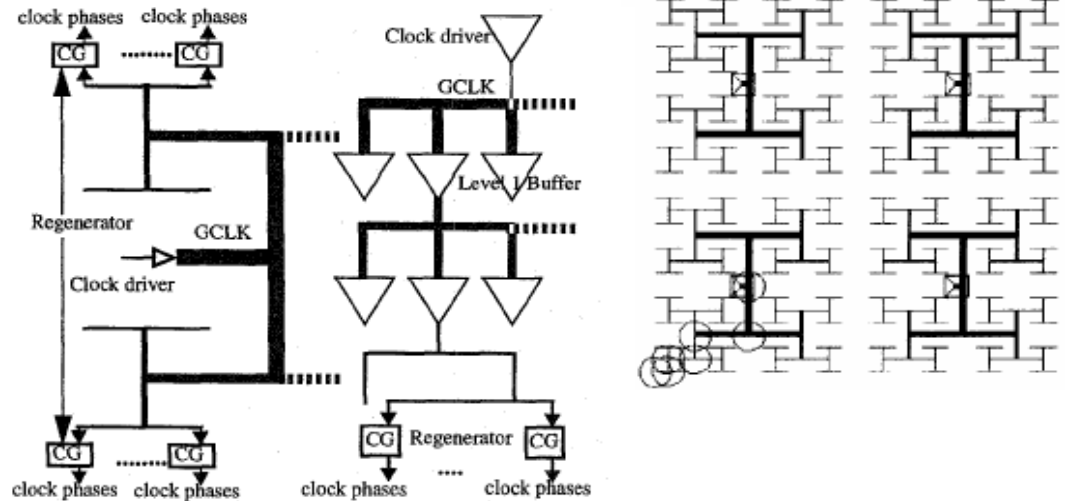


FIGURE 1. Typical PowerPC Clocking Schemes

Ref: CICC 1998, PowerPC clock distribution methodology



# Clock Distribution techniques for Low Skew

Design Goals  
Balanced Structure  
Low Power  
Analysis

- **Local Grid and Global Tree: IBM Power4**
  - Low local skew tolerant large global variations
  - Routing resource and power
  - Single clock domain for simple grid
  - local grid is shorted to average skew
- **Global-H-tree and Regional Grids: Intel IA-64(Itanium)**
  - Lower power, less routing resource
  - Complex De-Skewing to reduce skew
  - Regional grid is shorted to reduce skew
- **Balanced tree:**
  - Low Power
  - Allows Fine grained multi level Clock gating
  - Skew Control using Symmetry and structured placement
  - Less Route resources used

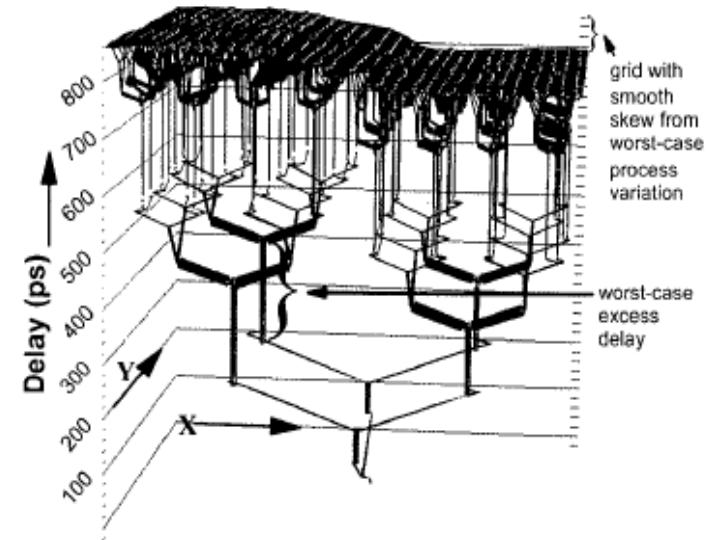
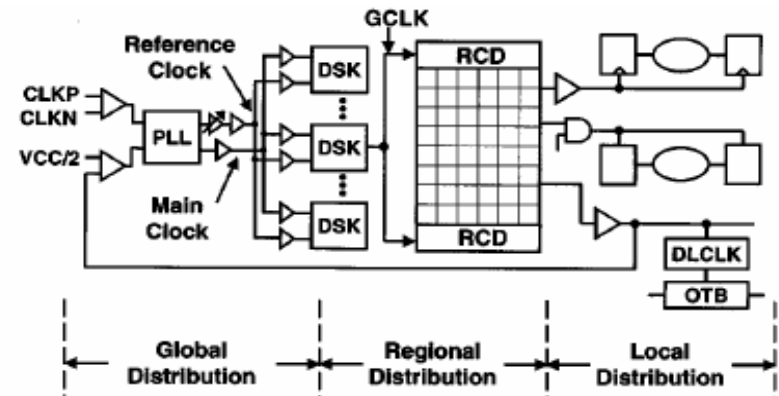


Figure 8.4.4: Clock distribution with buffer-delay variation.

Ref: ISSCC 2001 IBM power4 clock distribution



Ref: ISSCC 2002 First Generation IA-64 clock distribution





# Clock Tree Specification

- **Cells for clock tree**
  - Designed for reduced process variation
    - Transistor sizing, uniform orientation, matching
  - Cell type specific to clock tree level
  - Cell type at each level matched
- **Route layers by clock tree level for RC matching**
  - Common part of clock tree on upper layers MET5/MET6
  - Local clock tree only on MET3/MET4
  - Care taken to ensure layer matching and route topology control even for leaf level routes below clockgates
- **Width and spacing of clock routes**
  - Routed at non-minimum width and space
    - To reduce RC, Noise, coupling, RC variation
  - Reduce noise and crosstalk effect on clock delays
  - Double Vias for clock routes



# Control of Clock Skew and Insertion Delay

- **Minimize Skew**
  - Tight clustering of flops
    - Reduce insertion delay, skew and power
  - Local skew within blocks 50ps or below
    - Skew tuning
- **Reduced insertion delay in clock tree**
  - Implemented using
    - Floor planning of clock pins
    - Custom top level balanced clock tree
    - Pushing the common point in the clocktree closer to the blocks
    - Cloning clock structures with large fanout (module level clock gates)
  - Leads to reduced on chip variation (OCV)
  - Clock Tree jitter directly proportional to clock insertion delay



# Controlling Systematic Skew

- Structured placement traditionally reserved for datapath
- Use Structured placement in clock tree to further reduce systematic skew by matching delay components within each clock structure
- Unbalanced clock trees with different gates and wires
  - Delay matching can be used in such trees reduce skew
  - Random changes with different corners due to gate and interconnect mismatch
- Skew Minimization based on symmetry
  - Balanced same number of devices, identical layout and size
  - All parts in structure are matched
  - Match gate and wire delay and wire geometry
  - Chip floorplan with large macros can increase systematic skew due to non-uniform clock loading or load mismatch in clock tree



# Control of Clock Skew and Insertion Delay

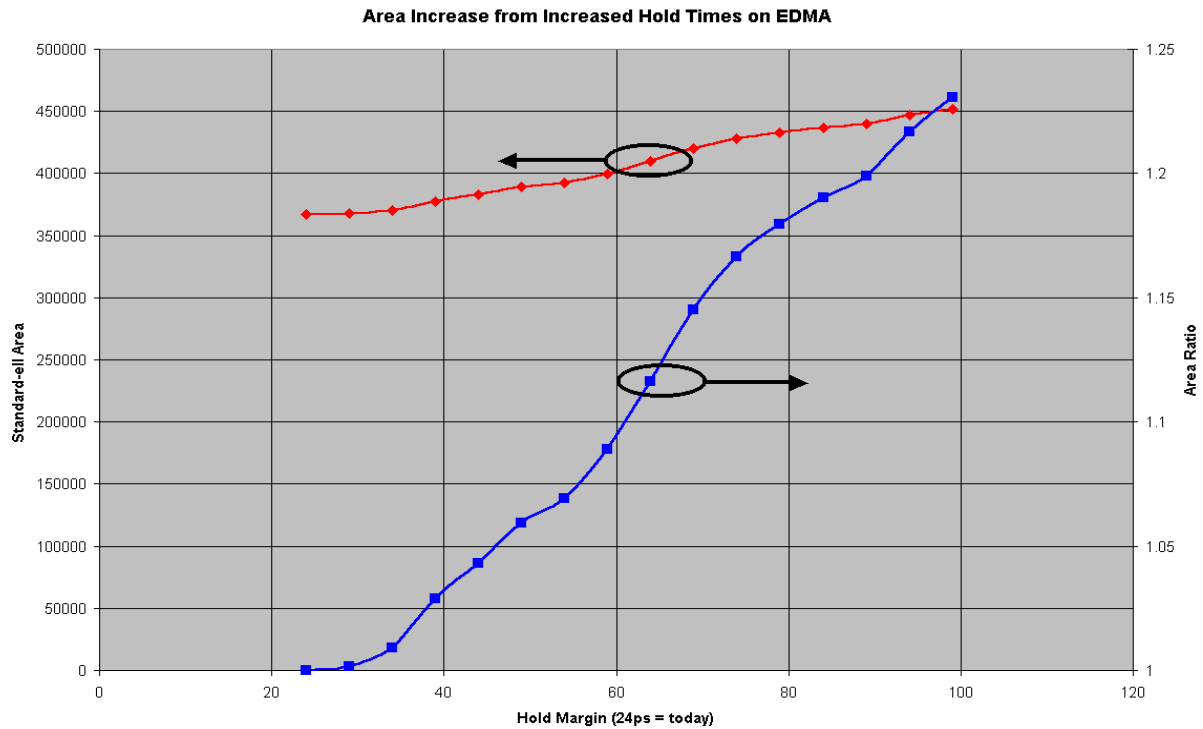
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- Good Clustering can result in
  - Reduced skew
  - Better timing
  - Lower Power and capacitance
  - Reduced area
  - Reduced process variation with predictable routing, fewer vias, similar context
- Examples of upto 20% area reduction in example



# Clock Skew and Area

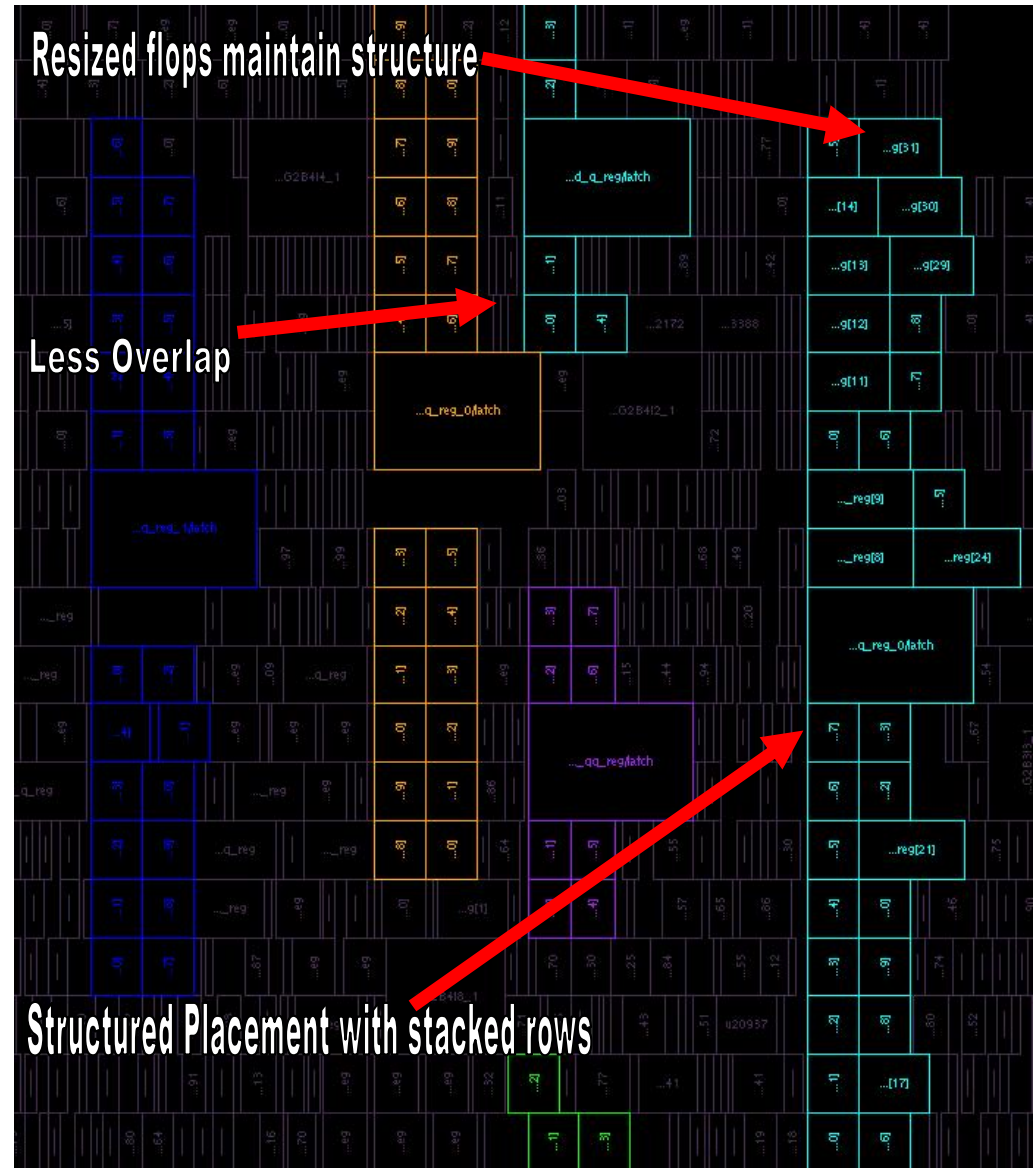
- Skew can impact area
  - Clock Network area
  - Area for hold time fixes
    - Area increase by 20%+ when skew increased from 50ps to 125ps





# Structured placement by Clustering

- Clustering of registers around clockgate for regular clock structure
  - Clockgate is in center of flop cluster
  - Cluster configuration depends on clockgate fanout
  - Reduced overlaps and better skews
  - Resizing of flops is supported within the cluster
  - Non-clockgated flops clustered around matching buffer

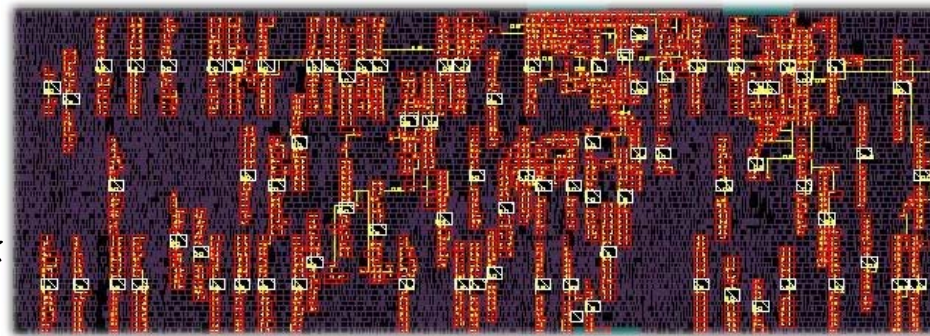




# Tight Control of Clock Skew

Design Goals  
Balanced Structure  
Low Power  
Analysis

- Custom clustering of clock loads enables
  - Regular and controlled routing from clock header to clock loads
  - Predictable route with vias and route jogs minimized
  - Reduces insertion delay, skew, power and process variation
  - Predictable loads for clockgate sizing
  - Area reduction
  - Context of cells is defined and predictable
  - Route resource utilization is minimized to reduce congestion



**Entire block**

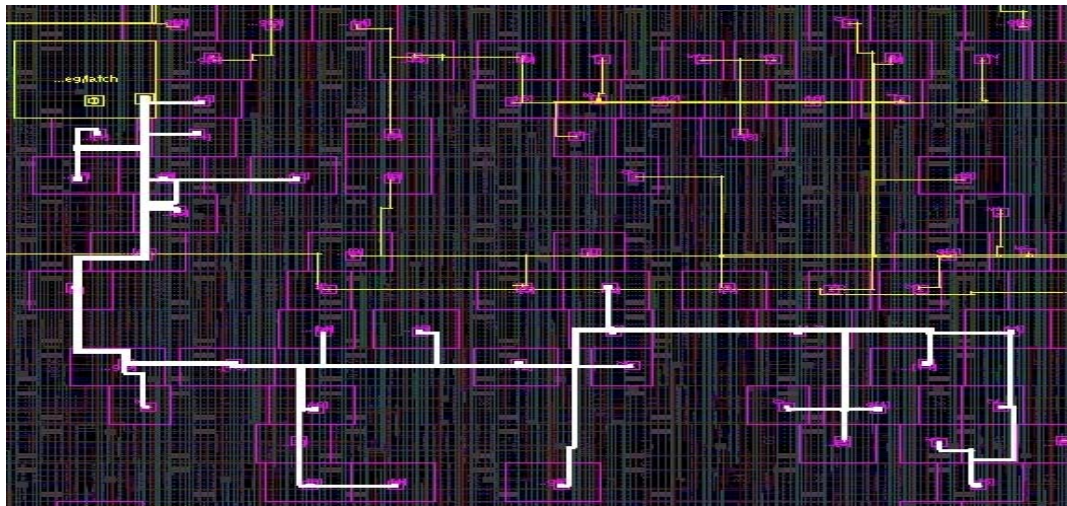
**ClockGate** →



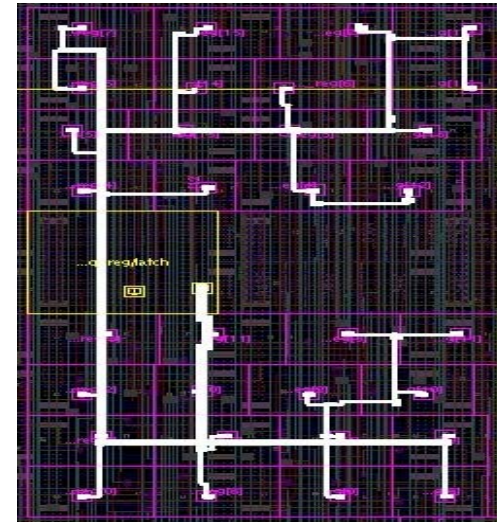
**FF Clustering**



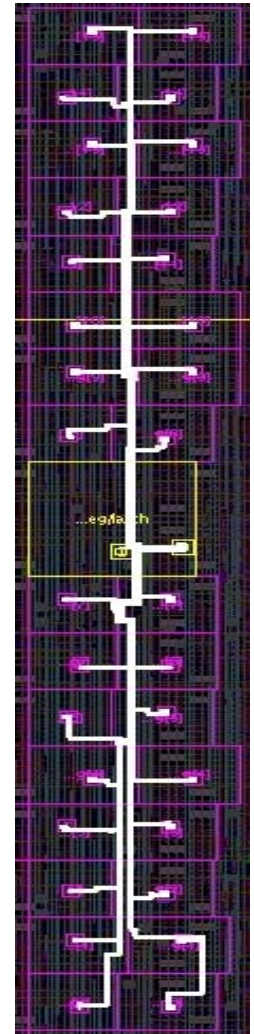
# Impact of Structured placement based Clustering on Clock Tree



No clustering



4 column



2 column

Config	Skew	Max Delay	Min Delay	# Levels	Total Power	Wire Cap in examples
2col.	49	284	235	4	1.78	43.06
4 col.	67	308	241	4	1.85	43.67
No Cluster	145	386	240	4	1.86	55.69

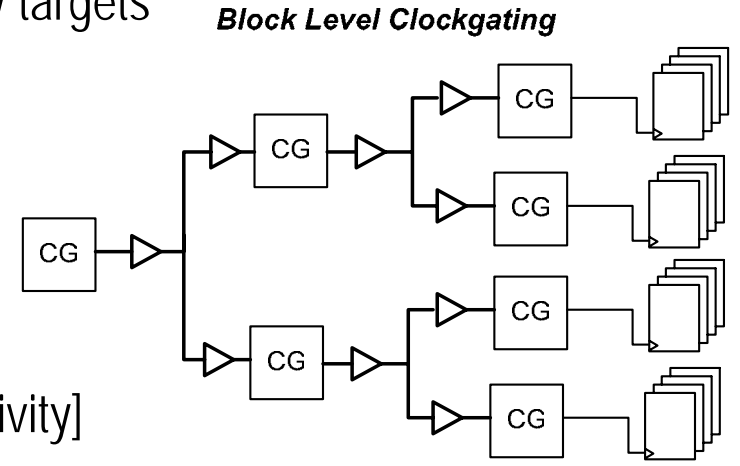
- Comparing configurations of flop clustering
  - Upto 3x reduction in skew
  - Upto 40% reduction in insertion delay
  - Upto 30% reduction in wire cap





# Clockgating Methodology

- Methodology to meet target skew power and insertion delay targets
- Clockgates explicitly coded in RTL or inserted in synthesis
- Integrated latch based clockgate
- Three levels of clockgating within a Block
  - Block level/Sub-Block/Leaf Level
- Large max fanout on clockgates
  - Power reduction: Fewer clockgates [ depending on activity]
  - More load mismatch and unbalanced clock structure
- Restricted max fanout
  - Balanced structure with better and predictable timing for “enable”
  - Replicate “always enabled” clockgates on non-clockgated branches for load/delay matching
  - Structured placement helps enable timing and power below clockgates





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# Clockgating and NBTI

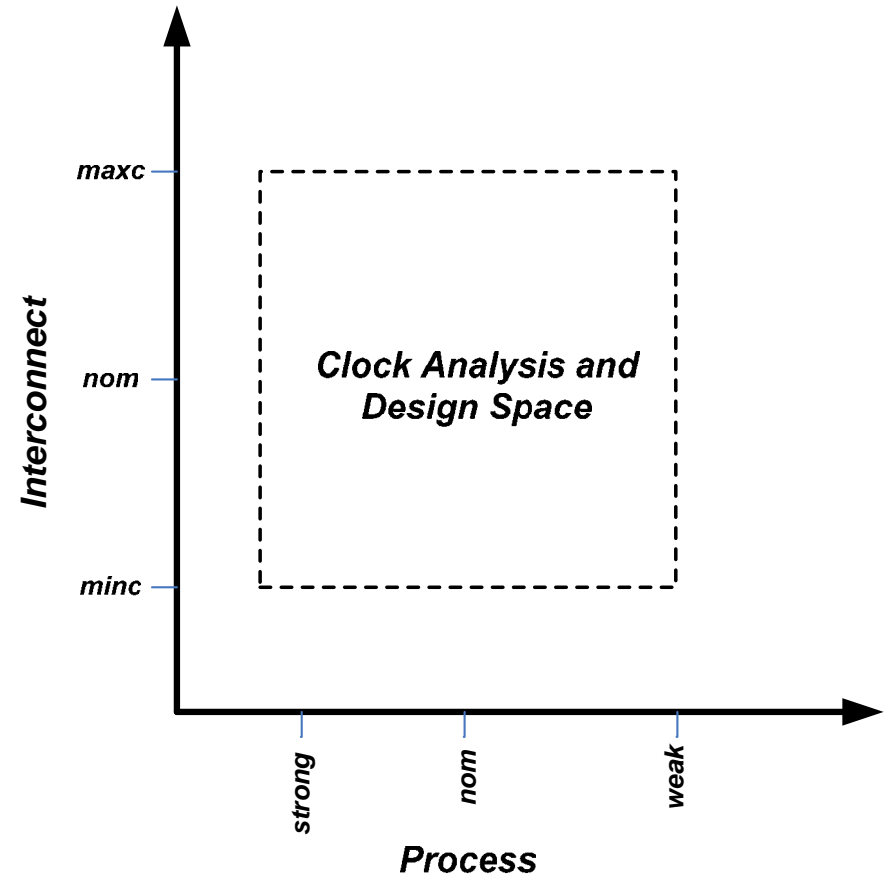
Design Goals  
Balanced Structure  
Low Power  
Analysis

- Negative Bias Temp Instability (NBTI) causes a  $V_T$  shift and degrades PMOS performance
- Degradation is state dependent
- Clockgating can result in differential ageing in clock tree
  - Clockgated portions see less than the activity on clock trees



# Clock Analysis

- **Analysis Corners** :Combination of
  - Process
  - Voltage
  - Temperature
  - Interconnect (via and metal)
- **Skew Analysis at all corners to check**
  - Mismatch in interconnect
  - Mismatch in gate and structure
  - Voltage introduced skew
  - Sensitivity to via variation
- **Cross corner Analysis**
  - Skew sensitivity to Fast-P, Slow-N, or vice-versa
- **Ratio of interconnect and gate delay**
  - Check ratio to validate balanced structure





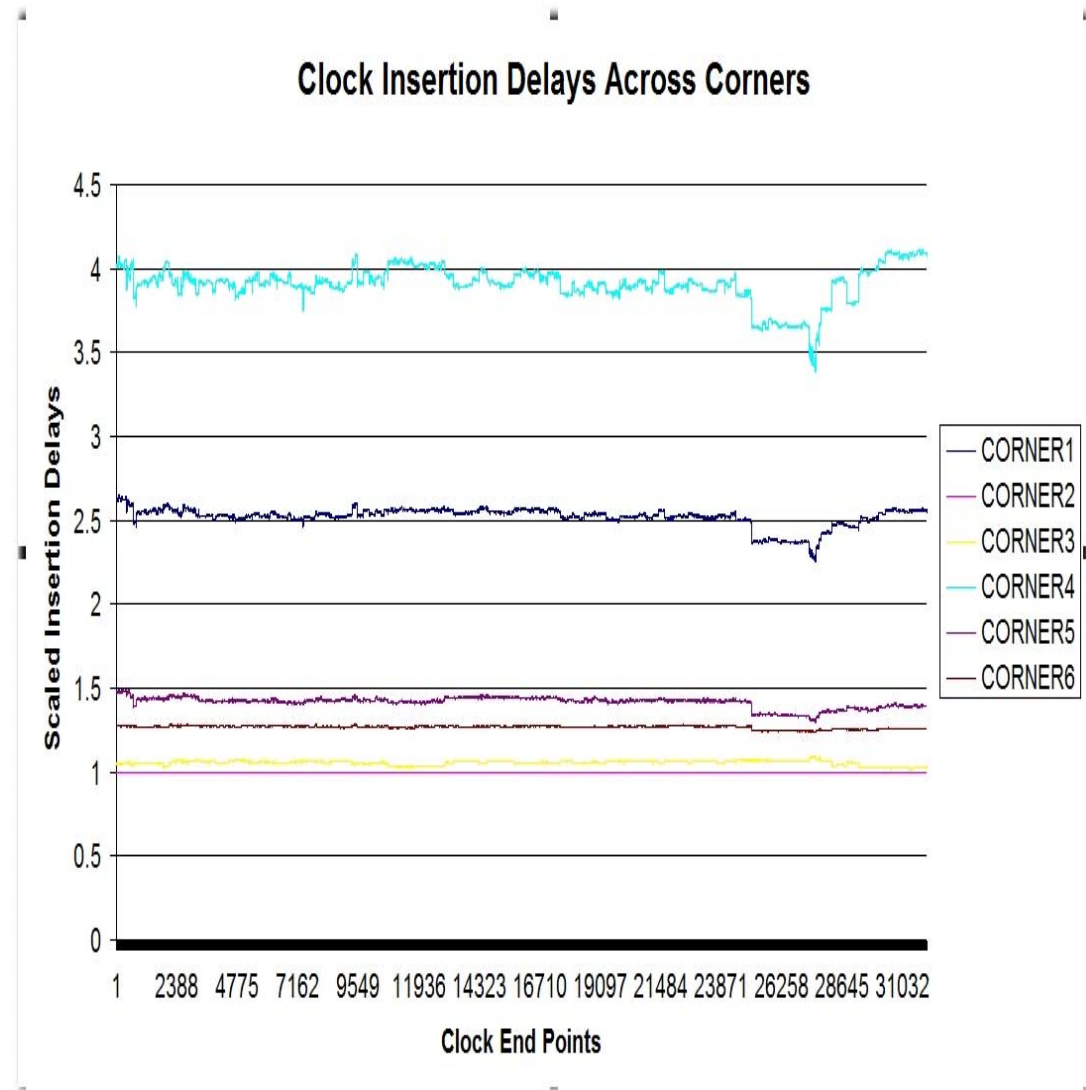
# Clock Analysis

- **Effect of Dynamic IR Drop on Clock Tree**
  - Insertion Delay
  - Skew and Jitter
- **Shielding**
  - Top level tree shielded : reduce inductance and capacitive coupling noise
  - Verification of clock shields by coupling/inductance analysis
  - Shields tapped at regular intervals to grid
- **Full chip ClockTree Noise analysis**
  - Each segment of clock tree is analyzed for coupling noise



# Insertion Delay tracking across corners

- Insertion delay can vary by 4x across process corners
- Example of a Balanced clock tree tracking insertion delay and skews across process corners.
- Control of Transition time in clocktree
  - Rise/Fall time controlled across all process corners(< 100ps rail-rail)
  - Robustness to process variations and coupling effects
  - Matched rise and fall times preserves clock duty cycle
  - Reduced short circuit current and lower short circuit power
  - Increased noise immunity





# Summary

- Clocktree Design needs to account for process variations
- Balanced clock structure enables clock distribution to track process variations
- Structured placement traditionally used in datapath implementation
- Using Structured placement in clock tree can further reduce systematic skew by matching delay components within each clock structure
- Custom clustering can be used in a balanced clock tree for low skew power reduction and controlling process variations
- Low power achieved
  - Using extensive fine grained clockgating
  - Reduced RC using clustering and structured placement
  - Control of skew across corners with balanced structure
- Detailed analysis of clock tree at multiple process corners is required



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# Acknowledgements

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*Balanced Structure*  
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