

Efficient Decoupling Capacitor Planning via Convex Programming Methods

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Outline

- **Background**
- **Problem Formulation**
- **Semi-Definite Program**
- **Linear Program**
- **Scalability Enhancement**
- **Experiments**
- **Conclusion**

P/G Supply Voltage Integrity

- ***Increasing Power/Ground supply voltage degradation in latest technologies*** due to increasing
 - ⦿ Interconnect resistance
 - ⦿ Supply current density
 - ⦿ Clock frequency
- Degraded power/ground supply voltages and relatively stable transistor threshold voltage leaves a decreased noise margin and ***increased vulnerability to logic malfunction***
- ***Degraded P/G supply voltages degrades transistor and circuit performance***

P/G Network Optimization

- Supply voltage degradation includes
 - ⊙ *DC IR drop*
 - ⊙ *AC IR drop*
 - ⊙ *L di/dt drop*
- P/G network optimization techniques include
 - ⊙ *Wire-sizing*
 - ⊙ *Edge augmentation*
 - ⊙ *Decoupling capacitor insertion*

Decoupling Capacitors

- Are usually CMOS capacitors
- Form *charge reservoirs* → *provide short-cuts for supply currents* → reduce supply voltage degradation
- Form *low pass filters* → *remove high frequency components in supply currents and cancel inductance effect* → reduce supply voltage degradation

Decoupling Capacitor Insertion

- θ heuristic
 - ⊙ Supply noise charge x a scaling factor
- **Sensitivity analysis** + **greedy** optimization
 - ⊙ A $m \times n$ Jacobian matrix for m violation nodes and n decoupling capacitor nodes
- **Adjoint sensitivity analysis** + **iterative quadratic** optimization
 - ⊙ **Adjoint network** for each supply current source's contribution
 - ⊙ **Time domain integral** of supply voltage drop
 - ⊙ Remains a **nonlinear optimization** problem

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Modified Nodal Analysis

- $(G+sC)V = Bu+J$
- $V =$ **free node** voltages
- $u =$ **reference node** voltage
- $B =$ conductance between free nodes and the reference node
- $J =$ free node supply currents
- $C =$ ground capacitance matrix
- $G =$ conductance matrix
- $G_{ij} =$ conductance between two free nodes i and j
- $G_{ii} = S_{j \neq i} G_{ij} + B_i$



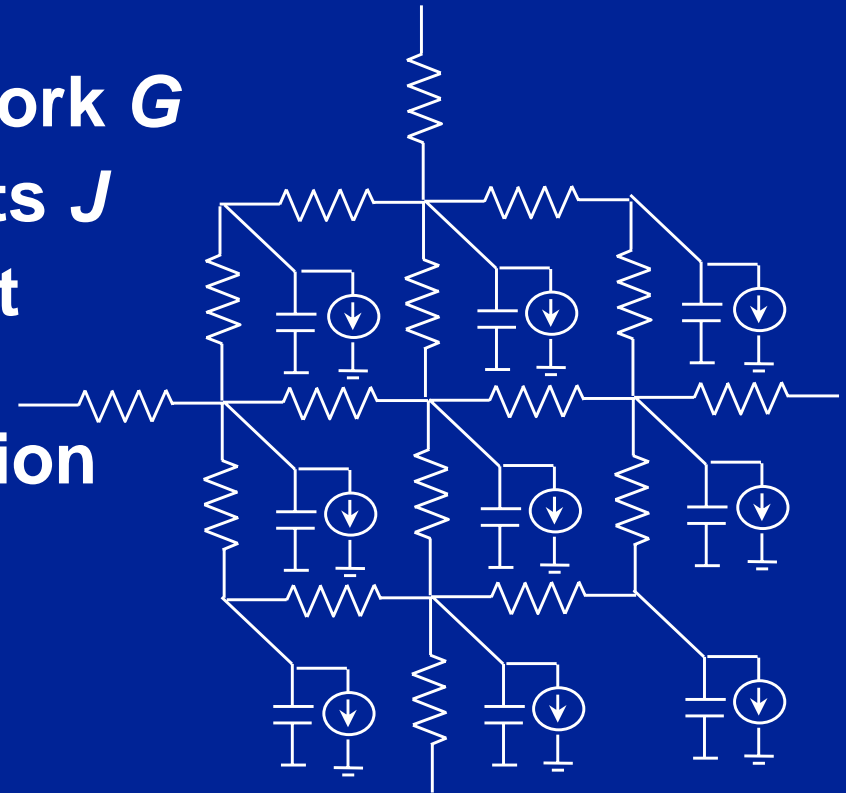
Problem Formulation

- **Given**

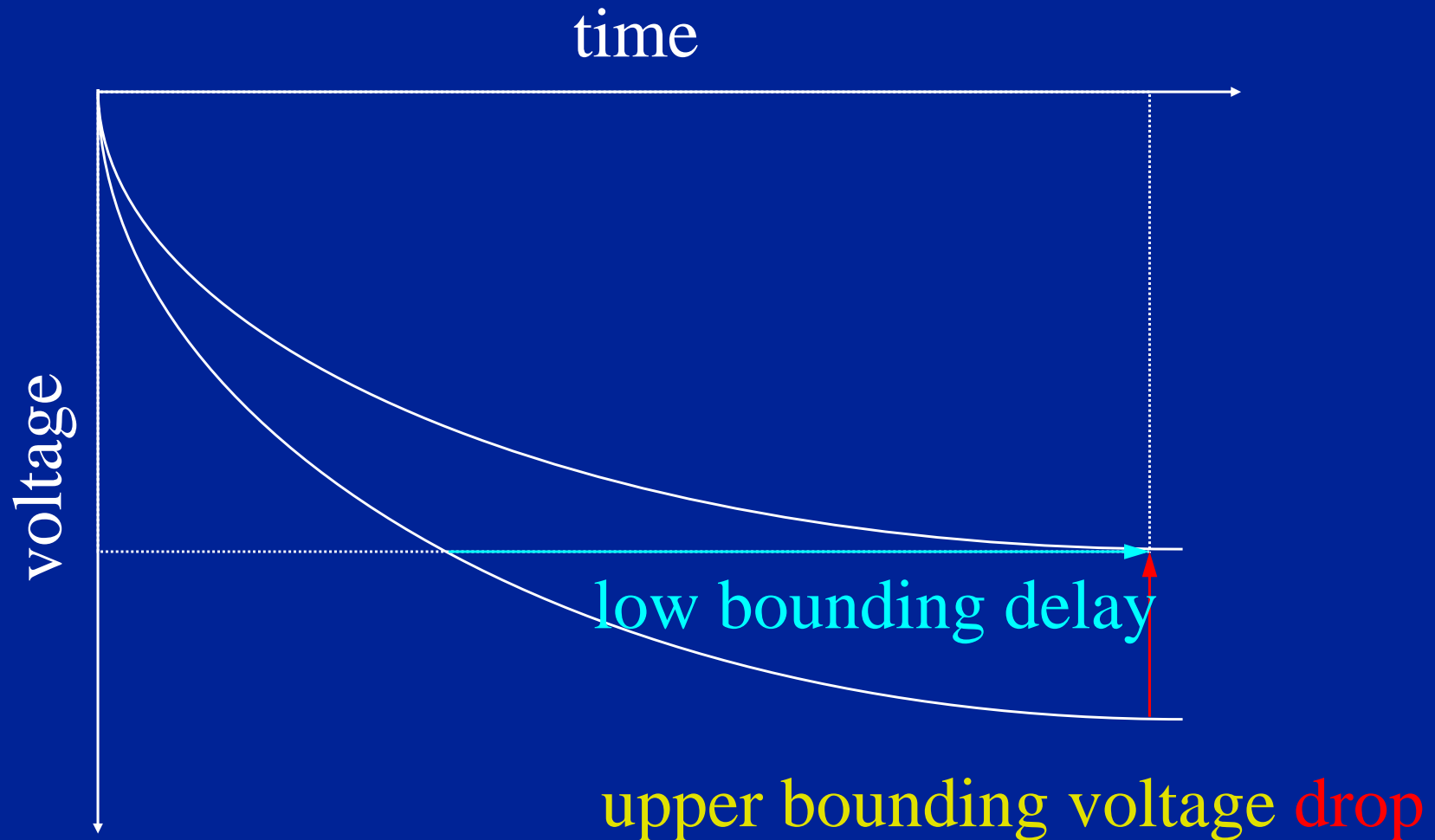
- ⊙ an RLC P/G supply network G
- ⊙ free node supply currents J
- ⊙ maximum supply current duration time T
- ⊙ supply voltage degradation bound αV_{dd}

- **Find**

- ⊙ minimum decoupling capacitance $\sum_i C_{ii}$ such that $\Delta V_i(t) < \alpha V_{dd}$ for all i in G , $t < T$



Duality of Timing and Voltage Bounds



Semi-Definite Program

- For timing optimization

Minimize

t

Subject to

$$t G - C \geq 0$$

- $M = t G - C$ is positive semi-definite $\rightarrow x^T M x \geq 0 \quad \forall x$
- t needs to be larger than the eigenvalues of $G^{-1}C$, e.g., RC time constants of the interconnect

Semi-Definite Program

- For supply voltage optimization

Minimize

$$\sum_i C_{ii}$$

Subject to

$$C - T G \geq 0$$

- $M = C - T G$ is positive semi-definite $\rightarrow x^T M x \geq 0 \forall x$
- T needs to be *smaller* than the eigenvalues of $G^{-1}C$, e.g., RC time constants of the interconnect
- Loose bound \rightarrow relaxation to a *convex super-space*

Linear Program

- Provides tighter bounds by considering differences in
 - ⊙ Node voltage bounds
 - ⊙ Supply currents
 - ⊙ Poles for residues
- Upper bounds supply current waveforms by step functions
- Upper bounds 50% interconnect delay by Elmore delay

Moment Computation

$$V = (I - sG^{-1}C)^{-1} G^{-1} J$$

$$J = \frac{\hat{J}}{s}$$

$$V = M_{-1}S^{-1} + M_0 + M_1s + \dots M_i s^i$$

$$M_{-1} = G^{-1} \hat{J}$$

$$M_0 = G^{-1} C G^{-1} \hat{J}$$

$$M_i = (G^{-1} C)^{i+1} G^{-1} \hat{J}$$

$$T^{Elm} = \frac{M_0}{M_{-1}} = \frac{G^{-1} C G^{-1} J}{G^{-1} J}$$

$$U = M_{-1} = G_{-1} J$$

$$U(1 - e^{-\frac{t}{T^{Elm}}}) \leq V(t) \leq U(1 - e^{-\frac{t}{kT^{Elm}}})$$

Linear Program Decap Insertion

- Minimize

$$\sum_i C_{ii}$$

- Subject to

$$\frac{G^{-1}CG^{-1}J}{G^{-1}J} \geq -\frac{kT}{\lg\left(1 - \frac{\alpha V_{dd}}{G^{-1}J}\right)}$$

- $k = 1 \quad \frac{1}{\lg 2}$
- For a node which DC voltage is within the bound, e.g., $G^{-1}\hat{J} \leq \alpha V_{dd}$, $\lg x = -\infty, x < 0$ gives 0 right-hand side
- Physical constraints
- Inductance effect

Numerical Example

- Semi-definite Program

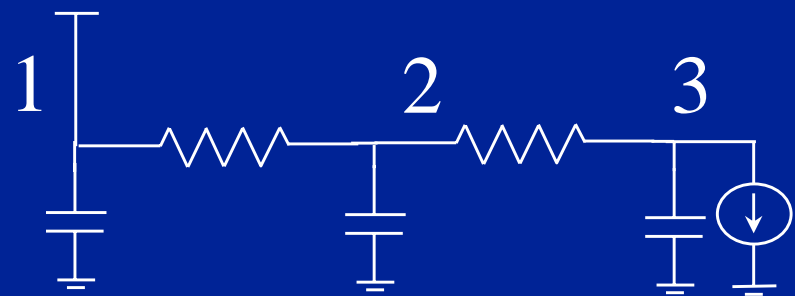
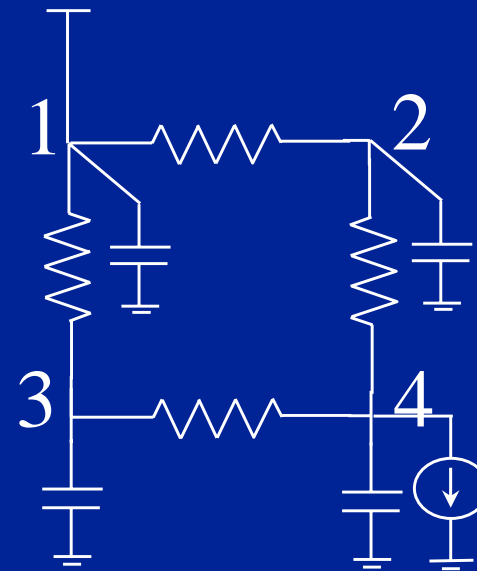
$$G = \begin{bmatrix} 4 & 2 \\ -2 & 2 \end{bmatrix}$$

$$G^{-1} = \begin{bmatrix} 0.5 & 0.5 \\ 0.5 & 1 \end{bmatrix}$$

$$C = \begin{bmatrix} 6 & 0 \\ 0 & 4 \end{bmatrix}$$

$$C - TG = \begin{bmatrix} 2 & 2 \\ 2 & 2 \end{bmatrix}$$

$$G^{-1}C = \begin{bmatrix} 3 & 2 \\ 3 & 4 \end{bmatrix}$$



which eigenvalues [1,6] larger than 1(ns)

Numerical Example

- Linear Program
- Given

$$G^{-1}\hat{J} = \begin{bmatrix} 0.5 \\ 1 \end{bmatrix}$$

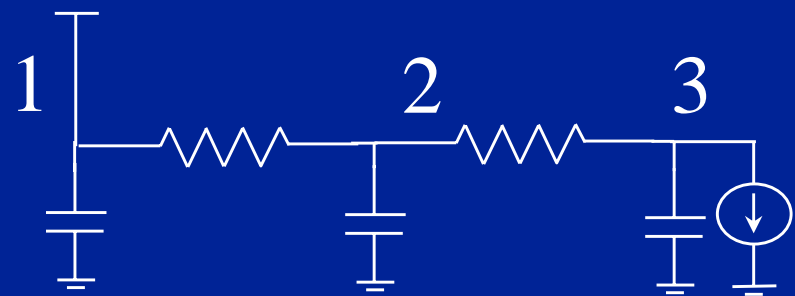
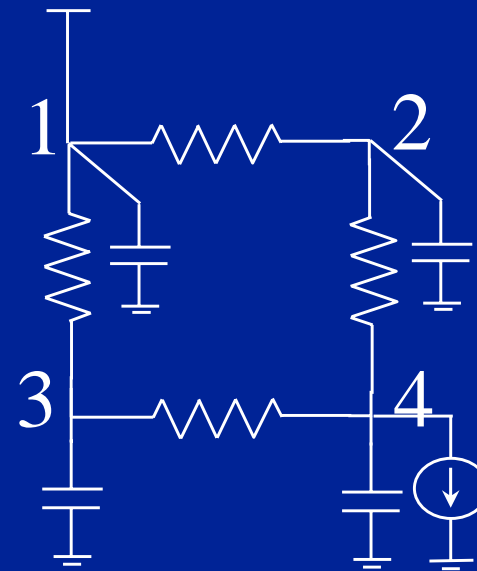
- Minimize

$$c_2 + c_3$$

- Subject to

$$0.5c_2 + c_3 > 0$$

$$0.25c_2 + c_3 > \frac{1}{\lg 2}$$



→ optimum $c_3 = 1/\lg 2$

Numerical Example

- θ heuristic is optimistic
- SDP is pessimistic
- LP gives accurate solution

<i>method</i>	<i>Supply currents</i>			<i>Decaps</i>			<i>Delay</i>	<i>Vdrop</i>
	<i>(A)</i>			<i>(pF)</i>			<i>(ns)</i>	<i>(V)</i>
LP	0	1	0	0	1.443	0	1	0.5
SDP	0	1	0	3	4	3	3.65	0.2
θ	0	1	0	0	1	0	0.703	0.628
LP	0.67	0	0.67	0.962	0	0.962	1	0.5
SDP	0.67	0	0.67	3	4	3	1.908	0.326
θ	0.67	0	0.67	0	1.333	0	0.703	0.628

Scalability Enhancement

- Reduce a P/G network to include only possible decoupling capacitor insertion nodes

- In the original P/G network

$$V = G^{-1} J$$

- In the reduced P/G network

$$\tilde{V} = \tilde{G}^{-1} \tilde{J}$$

- Apply unit supply current and compute node voltages
- Solve a linear equation system and find equivalent supply currents for the decap insertion nodes

Scalable Decap Insertion Linear Program

Input: RLC P/G network G , supply currents J
during time T , voltage bound αV_{dd}

Output: inserted decoupling capacitors

1. Select n decap insertion candidate nodes
2. Reduce G to include only the n decap insertion nodes
3. Apply linear program
4. Insert decoupling capacitors

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Experiments

- 90nm industry design of 34K instances
- Cadence Fire&Ice extracts a power network of 65K resistors and 35K capacitors
- VerilogXL outputs supply currents of 5.613A in total
- $T = 1ns, \alpha = 0.2$
- 16 decap insertion candidate nodes
- 16 SPICE DC simulation, each takes 1.15 seconds

	<i>Total decap (nF)</i>	<i>Min delay (ns)</i>	<i>Max Vdrop (V)</i>	<i>CPU runtime (s)</i>
LP	30.002	1.008	0.199	0.001
SDP	55.892	2.644	0.101	0.034
θ	4.196	0.352	0.275	0.000

Summary

- We propose *a compact modified nodal analysis formula* for a P/G network
- We apply timing optimization techniques for supply voltage bound
- We propose *a semi-definite program*, which guarantees supply voltage bound for all supply currents
- We propose *a linear program*, which accurately bounds supply voltage for given supply currents
- We propose *a P/G network reduction scheme* for scalability enhancement

Thank you !