Double Patterning Layout Decomposition for Simultaneous Conflict and Stitch Minimization

Kun Yuan, Jae-Seok Yang, David Z. Pan
Dept. of Electrical and Computer Engineering
The University of Texas at Austin

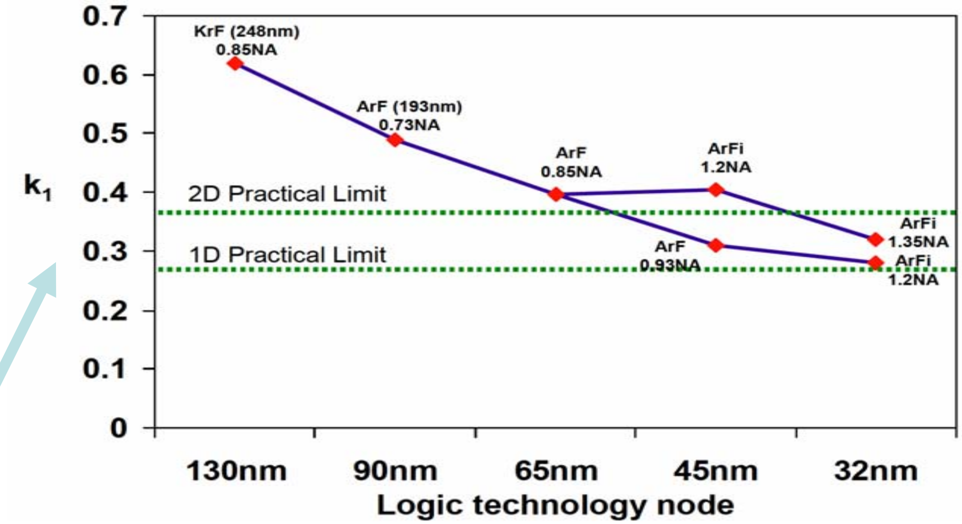
Sponsored in Part by NSF, SRC, Sun, Qualcomm, and equipment donations from Intel

Outline

- Background and Motivation
- Simultaneous Conflict and Stitch Minimization
  - Grid Model
  - Basic ILP formulation
  - Speed-Up techniques
- Experimental Result
- Conclusion

Lithography Challenges

- Aggressive scaling of min. printable half pitch HP



$$HP = k_1 \frac{\lambda}{NA}$$

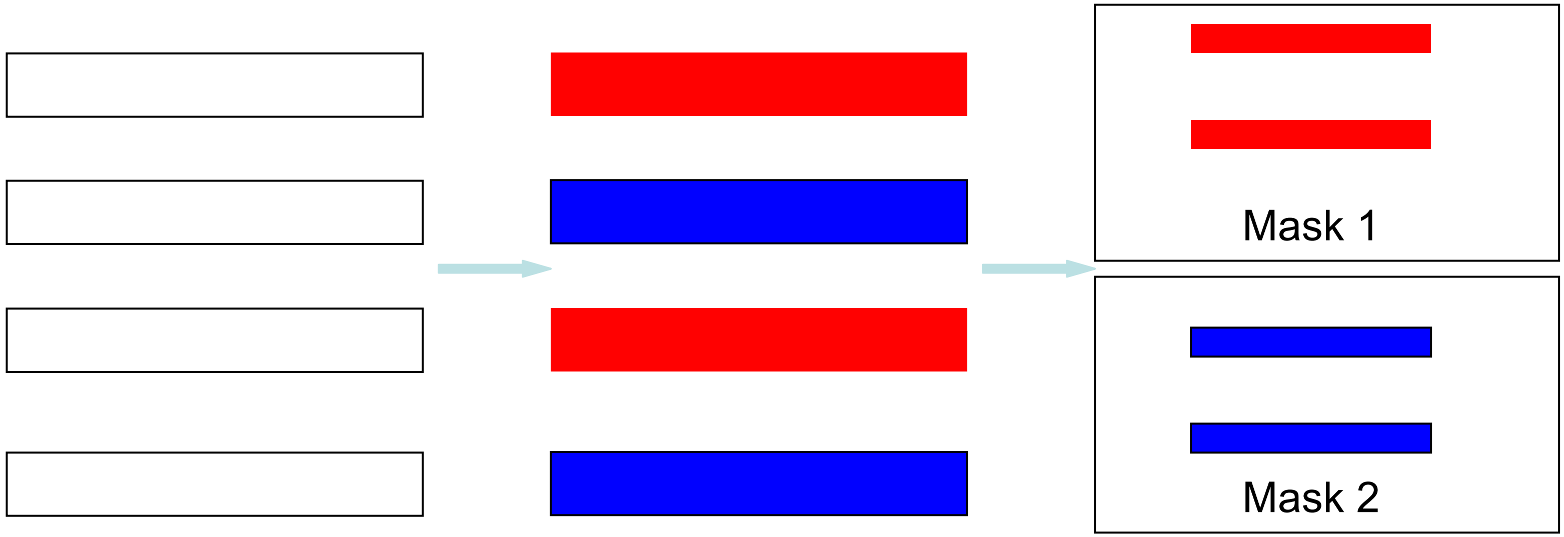
k1: process difficulty
NA: numerical aperture
λ: wavelength of source

- NA = 1.8, close to the limit

- EUV(13.5nm)

  not available in near future

Double Patterning Lithography (DPL)

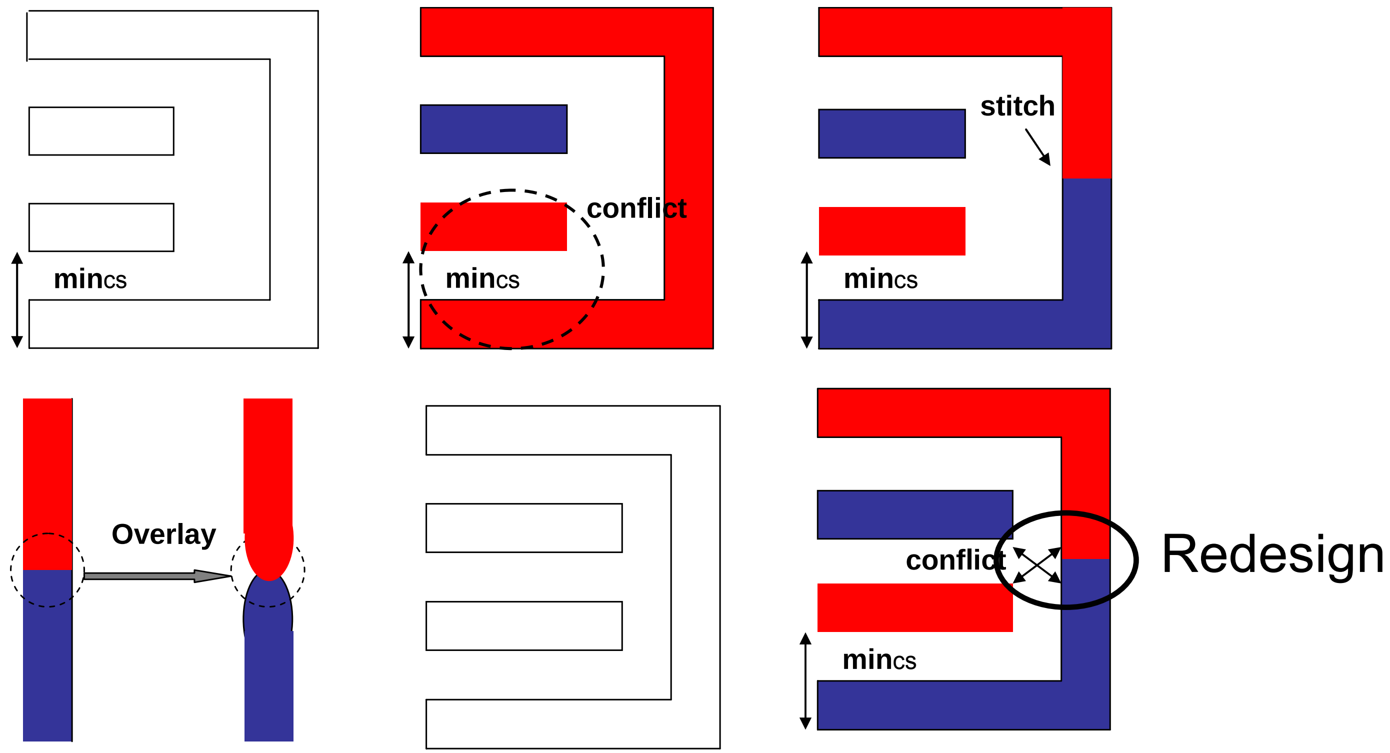


- Most likely lithography solution for 32nm and beyond
- A layout is decomposed into two masks (colors)
  - The effective pitch is doubled
  - Manufactured through 2x exposures/etches.

Layout Decomposition.

However, it is NOT a trivial task

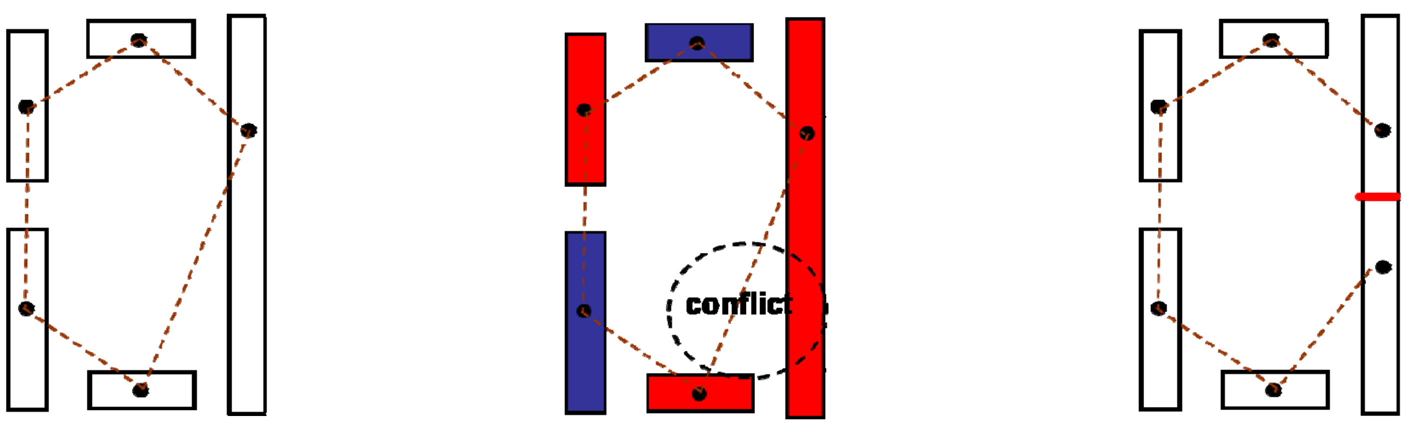
Layout Decomposition Challenges



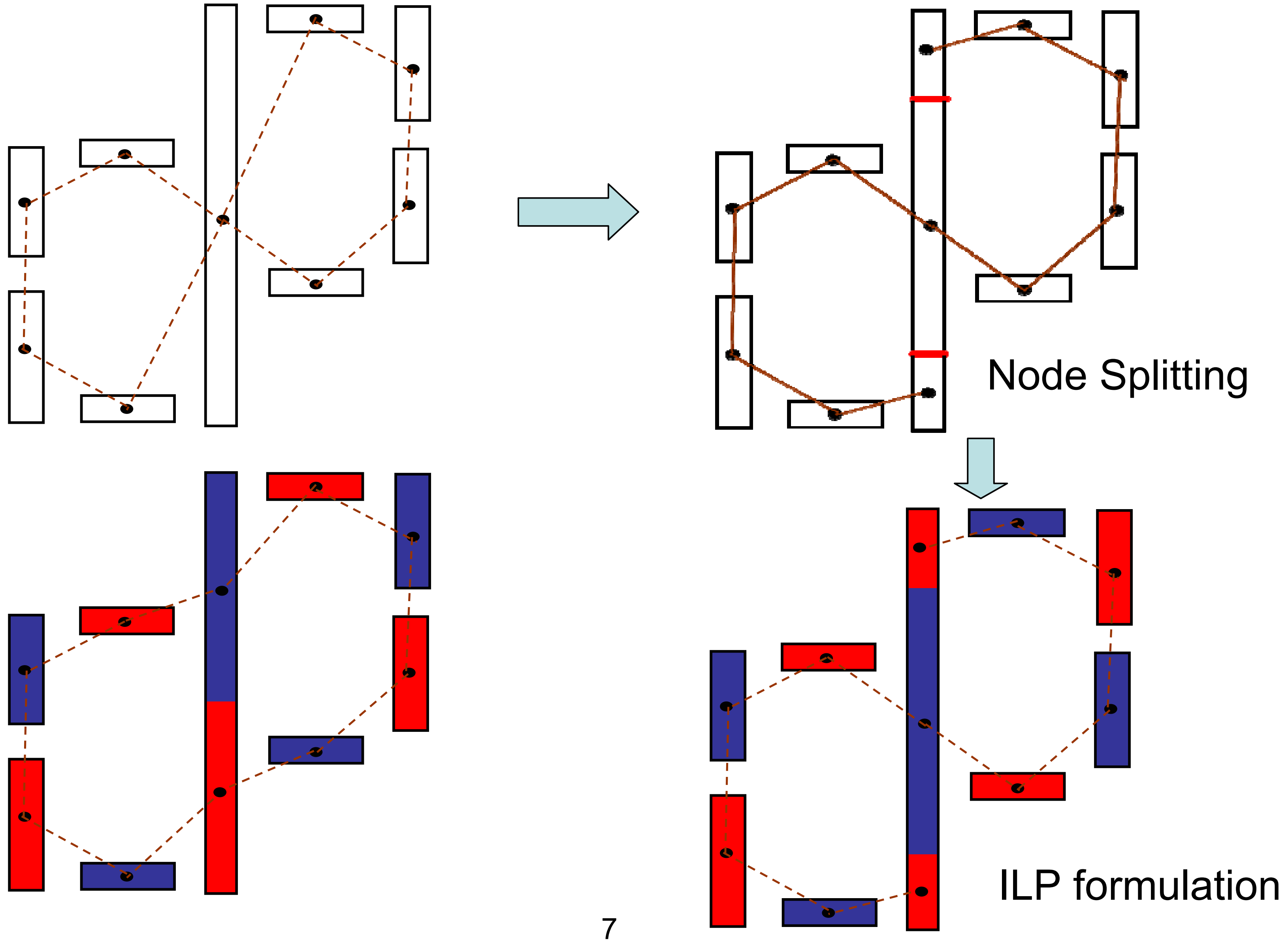
- Coloring Conflict:
  - Two features within minimum coloring spacing should be colored different
- Splitting Stitch
  - May resolve the conflict but cause yield loss due to overlay.

Existing Work

- Heuristic approaches [Drapeau+, SPIE 2007]
  - Greedy coloring and splitting in two stages
- ILP based layout decomposition [Kahng+, ICCAD 2008]
  - Layout fracturing.
  - Detect the uncolorable conflict cycle with odd number of nodes, and remove them by splitting the features
  - ILP is then applied to minimize the number of stitches.



Motivation for Simultaneous Optimization

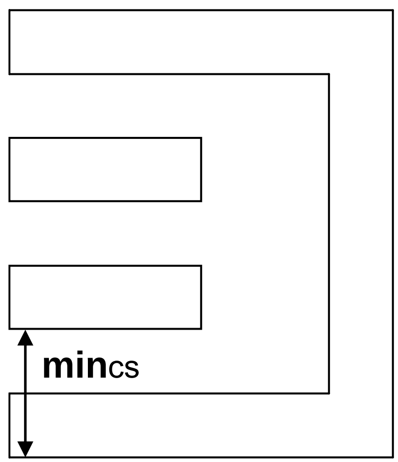


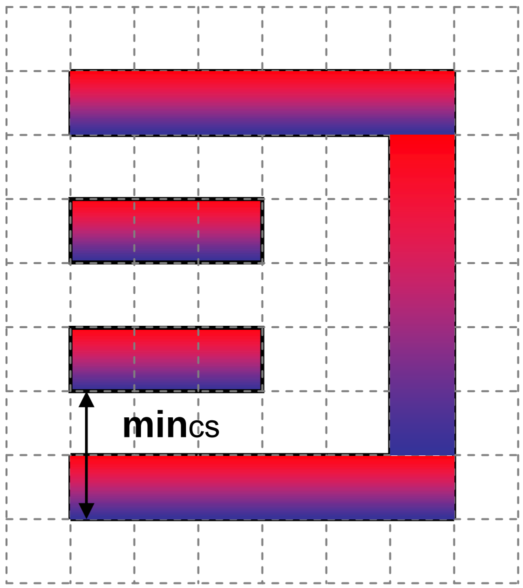
Outline

- Background and Motivation
- Simultaneous Conflict and Stitch Minimization
  - Grid Model
  - Basic ILP formulation
  - Speed-Up techniques
- Experimental Result
- Conclusion

Grid Model

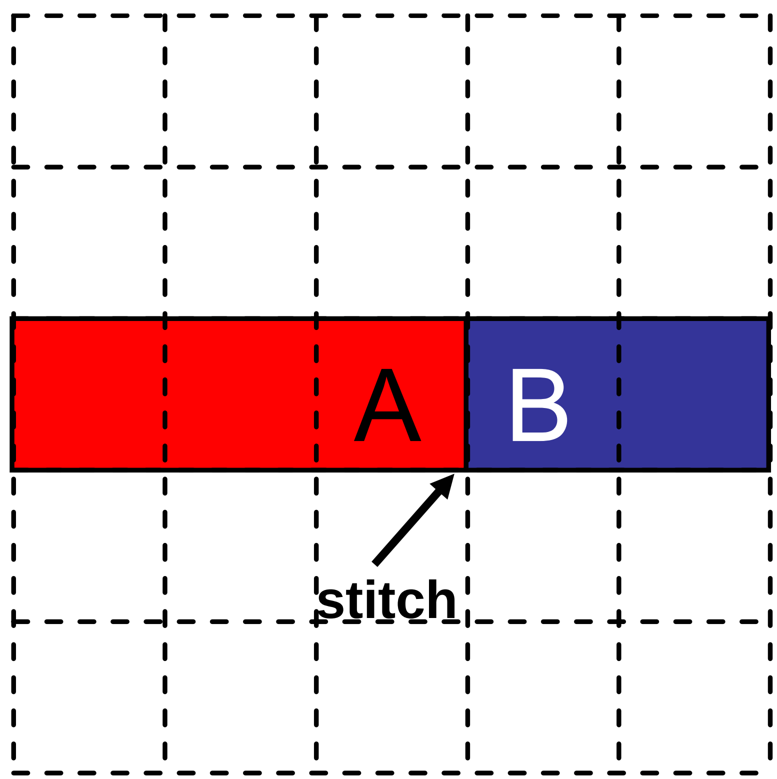
- Map the layout into grids
  - The size of each grids is half of the pitch of the original design
  - Offer sufficient stitch candidates for large solution space
- Minimize the conflict and stitch between layout grids





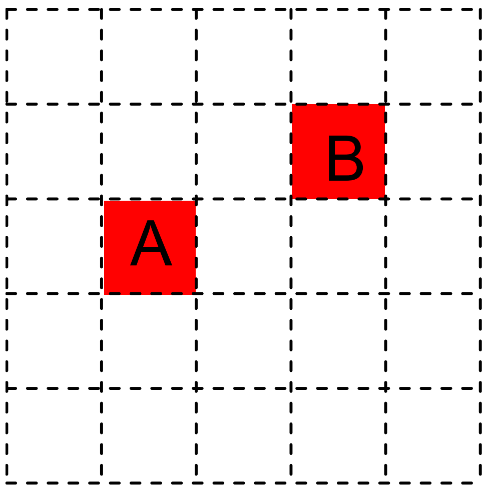
Stitch Grid Pair (SGP)

- Adjacent grids A and B are assigned to different masks

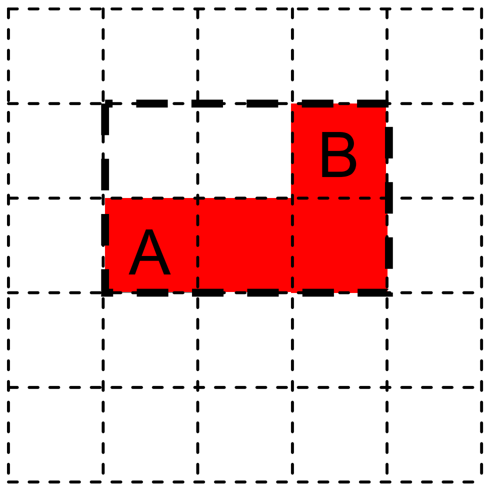


Conflict Grid Pair (CGP)

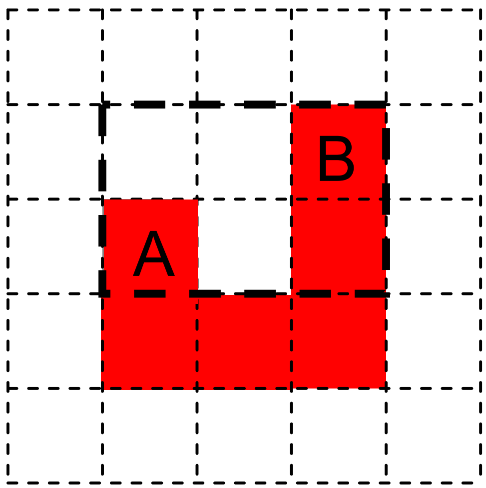
- Two grids within minimum coloring distance are assigned into the same mask
- Boundingbox-Connected (BB-connected) case should be excluded.



CGP



NOT CGP



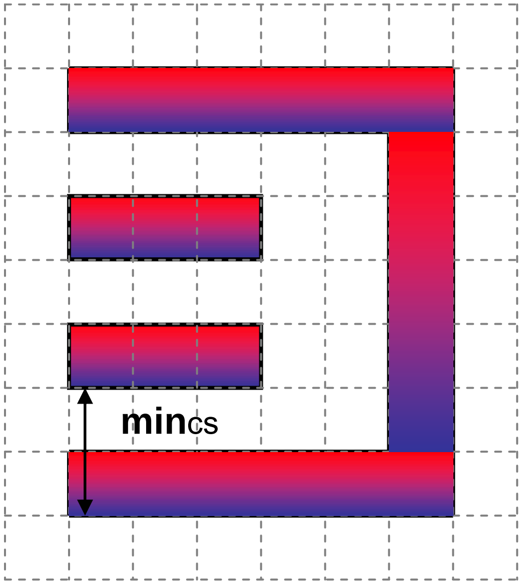
CGP

Basic ILP Formulation

- Coloring binary variable

$$x_i = 1 \text{ (Red)}, 0 \text{ (Blue)}$$

i is the unique id of each grid



- Objectives

$$Min\left(\sum_{s_{i,j} \in SP} s_{i,j} + \alpha \sum_{c_{m,n} \in CP} c_{m,n} \right)$$

Binary variables $s_{i,j}$ and $c_{m,n}$ = 1 if there is a SGP and CGP respectively

SP or CP are the set of the grid pairs which could form a SGP or CGP.

Detect SGP

- Logic equations

$$x_a \overline{x_b} = 1 \quad \Rightarrow \quad s_{a,b} = 1$$

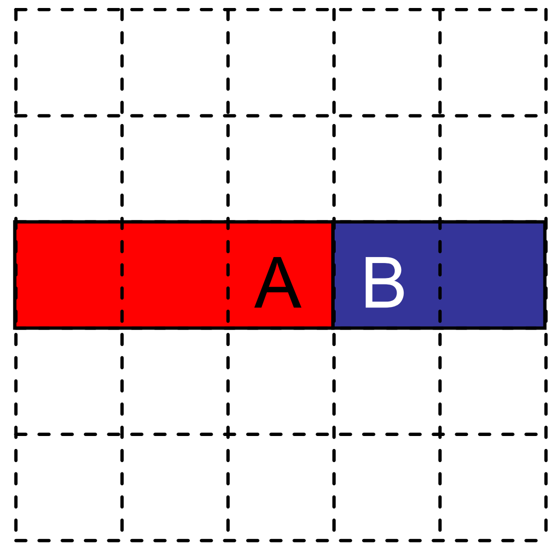
$$\overline{x_a} x_b = 1 \quad \Rightarrow \quad s_{a,b} = 1$$

- Linear Constraints

$$x_a + (1 - x_b) \le 1 + s_{a,b}$$

$$(1 - x_a) + x_b \le 1 + s_{a,b}$$

$x_i = 1$ (Red), 0 (Blue)



Detect CGP

- Logic equations

$x_a x_b = 1$ && No RED BB-connected

$\Rightarrow \quad c_{a,b} = 1$

$\overline{x_a}\,\overline{x_b} = 1$ && No BLUE BB-connected

$\Rightarrow \quad c_{a,b} = 1$

- Linear Constraints

$$x_a + x_b \le 1 + c_{a,b} + \sum_k r^k_{a,b}$$

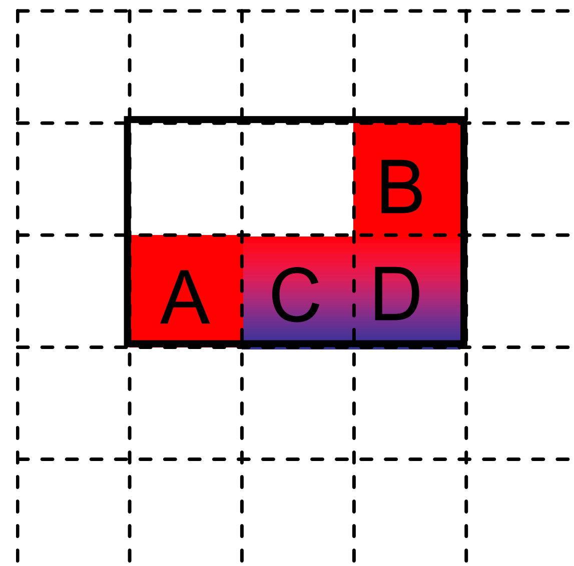
$$(1 - x_a) + (1 - x_b) \le 1 + c_{a,b} + \sum_k b^k_{a,b}$$

Binary variables $r^k_{a,b}$ and $b^k_{a,b} = 1$

if there is BB-connected in RED and BLUE respectively

$\sum_k$: The set of possible BB-connected paths.

$x_i = 1$ (Red), 0 (Blue)



$r^1_{a,b}$: Grids C and D are Red

$b^1_{a,b}$: Grids C and D are Blue

Detect BB-connected case

- Logic Equation

$$r^{k}_{pq,uv} = \prod_{x_{e,f} \in P^{k}_{pq,uv}} x_{e,f}$$

$$e.g.\ r^{1}_{a,b} = x_c x_d$$

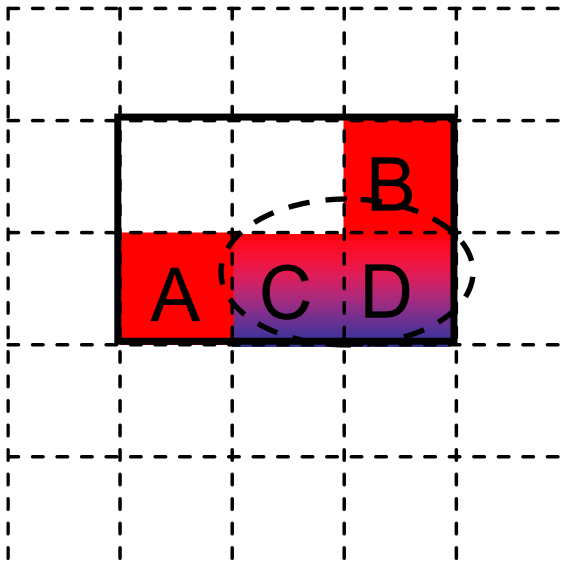
- Linear Constraints

$$\sum_{x_{e,f} \in P^{k}_{pq,uv}} x_{e,f} \le \left(n^{k}_{pq,uv} - 1\right) + r^{k}_{pq,uv}$$

$$\sum_{x_{e,f} \in P^{k}_{pq,uv}} (1 - x_{e,f}) \le n^{k}_{pq,uv}\left(1 - r^{k}_{pq,uv}\right)$$

$n^{k}_{pq,uv}$ is the number of grids in the path

$$x_i = 1 \text{ (Red)}, 0 \text{ (Blue)}$$

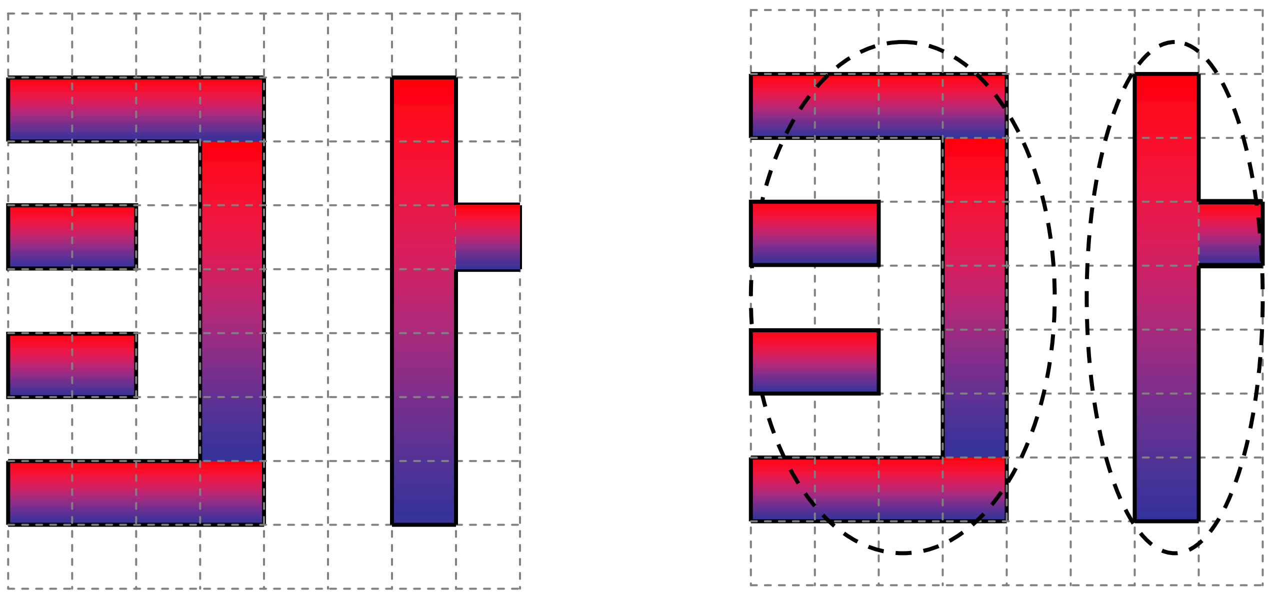


$e.g.$

$$x_c + x_d \le \left(2 - 1\right) + r^{1}_{a,b}$$

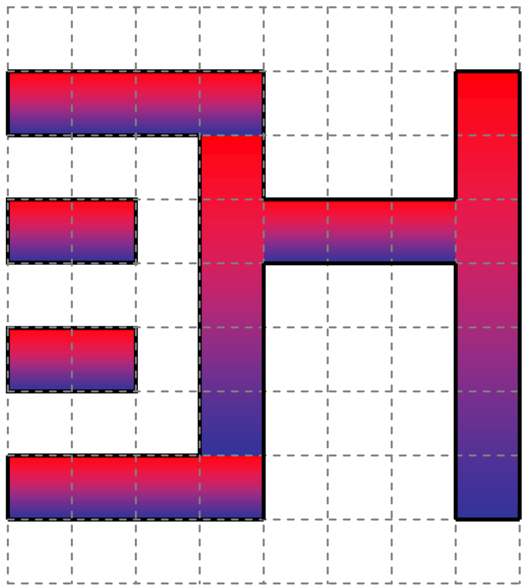
$$(1 - x_c) + \left(1 - x_d\right) \le 2\left(1 - r^{1}_{a,b}\right)$$

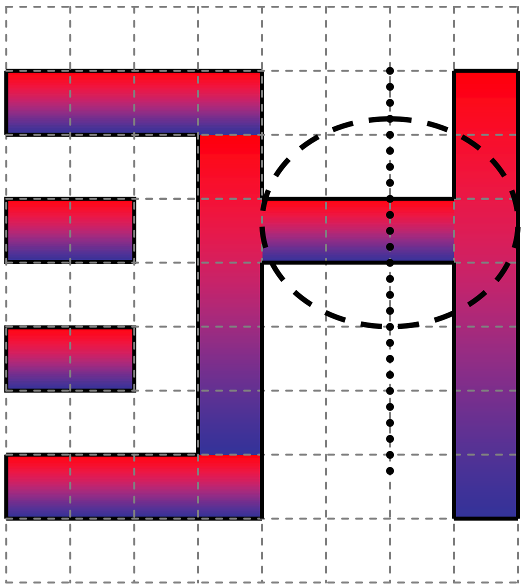
Speed-Up Techniques: Independent Component Computation



- Independent Components: Isolated layout clusters without possible SGP and CGPs between them.
- They can be solved individually, and the solution can be simply merged without losing optimality in terms of ILP objectives.

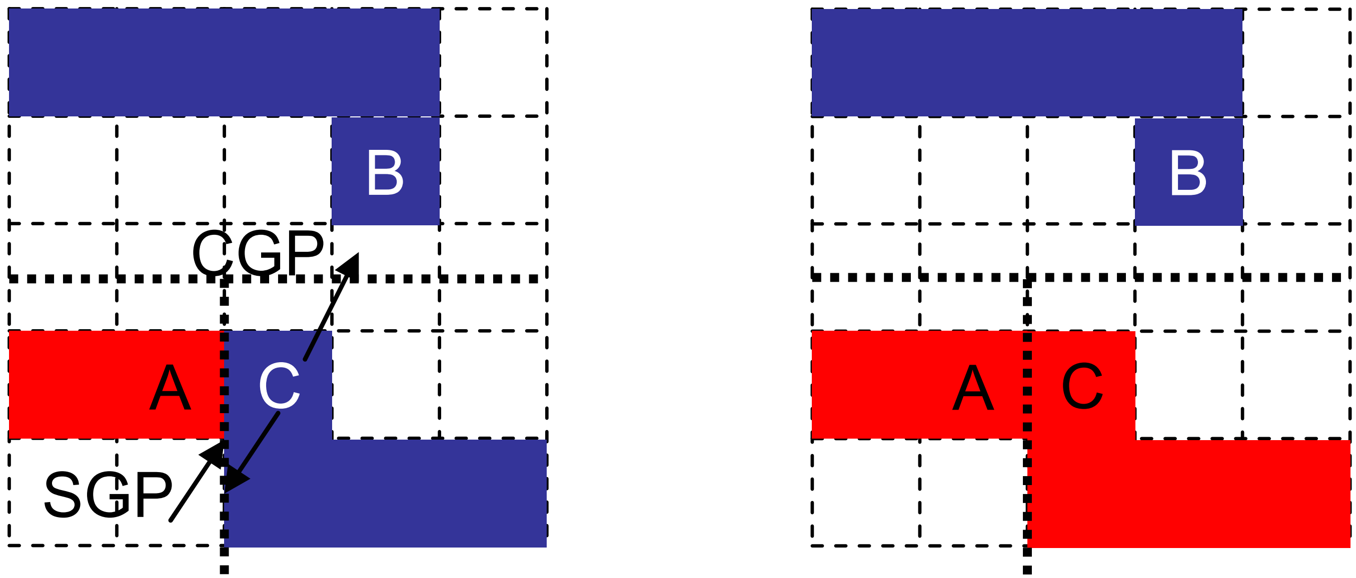
Speedup Techniques: Layout Partition





- There could still be large design which has prohibitive problem size even after independent component computation
- We can apply min-cut partition to divide a large components to several small connected ones

Coloring Flipping for Layout Partition



- We can flip the coloring of certain partition to obtain better resolution across the boundaries

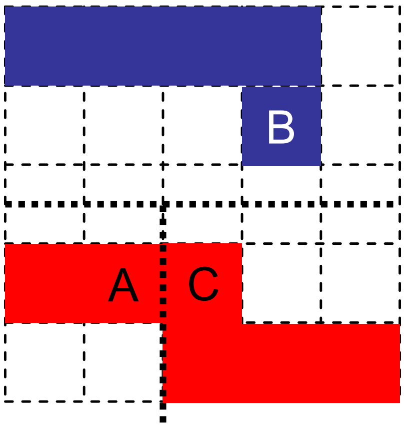
ILP Formulation for Coloring Flipping

- Binary Variable

$f_i = 0$ (Not flipped), 1 (Flipped) for partition i

$f_{i,j} =$ 0 if both i and j flip or do not flip

$f_{i,j} =$ 1 if only one of i and j flips



- Objective

$$\min \sum (f_{i,j} (s_{i,j}^{e0} + \alpha c_{i,j}^{e0}) + (1 - f_{i,j})(s_{i,j}^{e1} + \alpha c_{i,j}^{e1}))$$

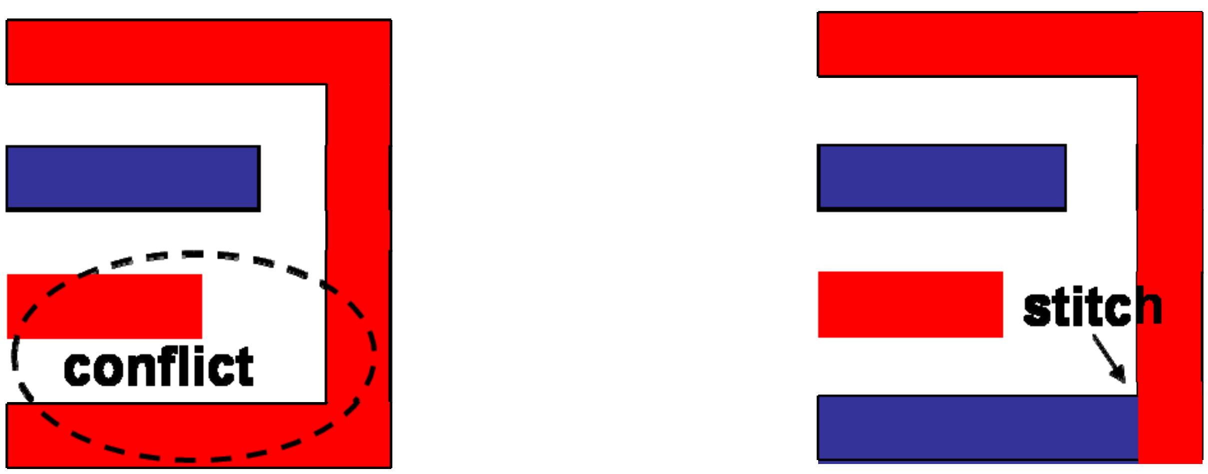
$s_{i,j}^{e0/e1}$ and $c_{i,j}^{e0/e1}$ are the stitch and conflict crossing the boundary

- Constraints

$$f_{i,j} = f_i f_j + \overline{f_i}\,\overline{f_j}$$

Experimental Setup

- Implement in C++.
- Comparative two-phase approach
  - First Phase:
    - Color all the layout polygons sequentially.
    - Assign colors to minimize current conflicts.
  - Second Phase:
    - Detect the coloring conflict segments
    - Flip the coloring these segments to resolve the conflicts.

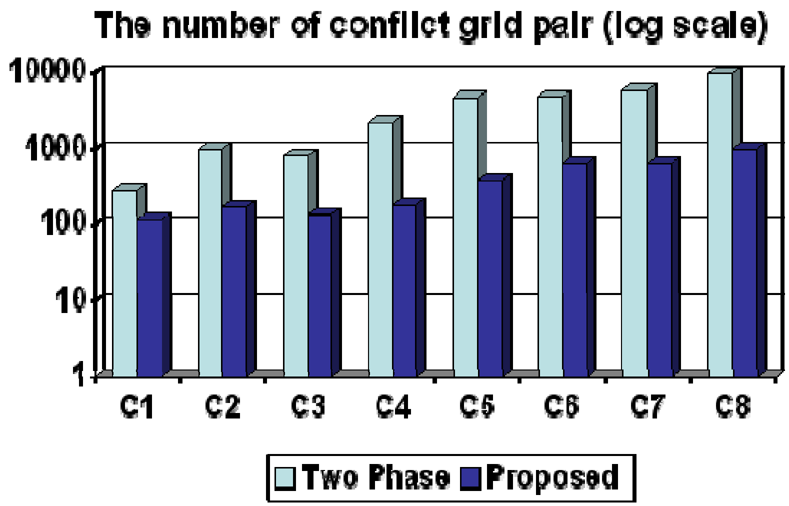


Benchmark

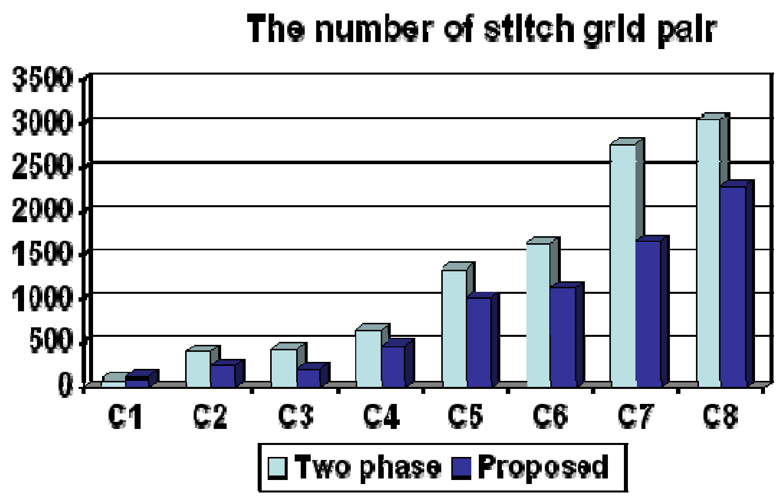
- Eight scaled testcases

Circuit	Area(μm^2)	Grid size	Layout grids
c1	89	294x294	6670
c2	160	395x395	15710
c3	207	450x450	20496
c4	292	534x534	33497
c5	422	642x642	53998
c6	540	726x726	68820
c7	747	854x854	101431
c8	1028	1002x1002	142535

Coloring Conflict and Splitting Stitch

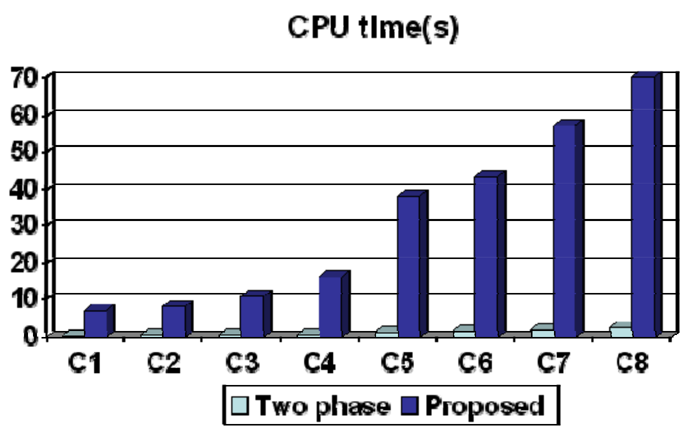


- 8x reduction on coloring conflict

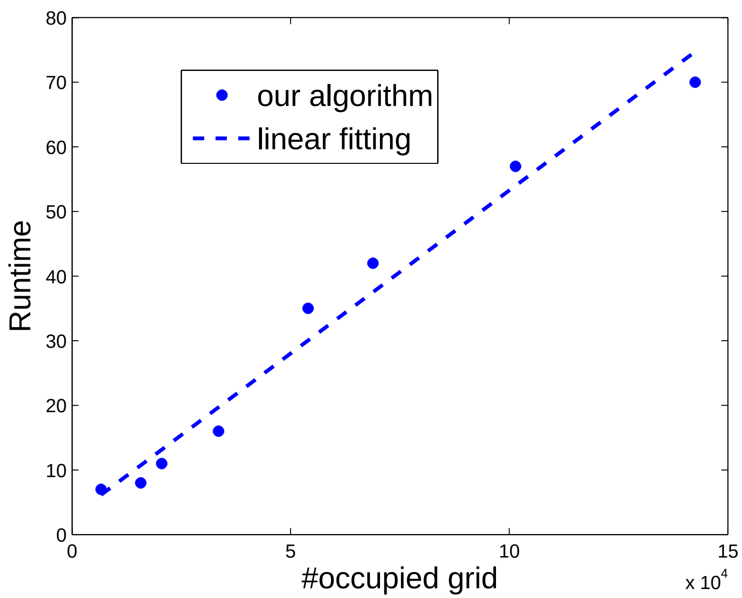


- 33% less stitches

Scalability



- The runtime is in reasonable scope.



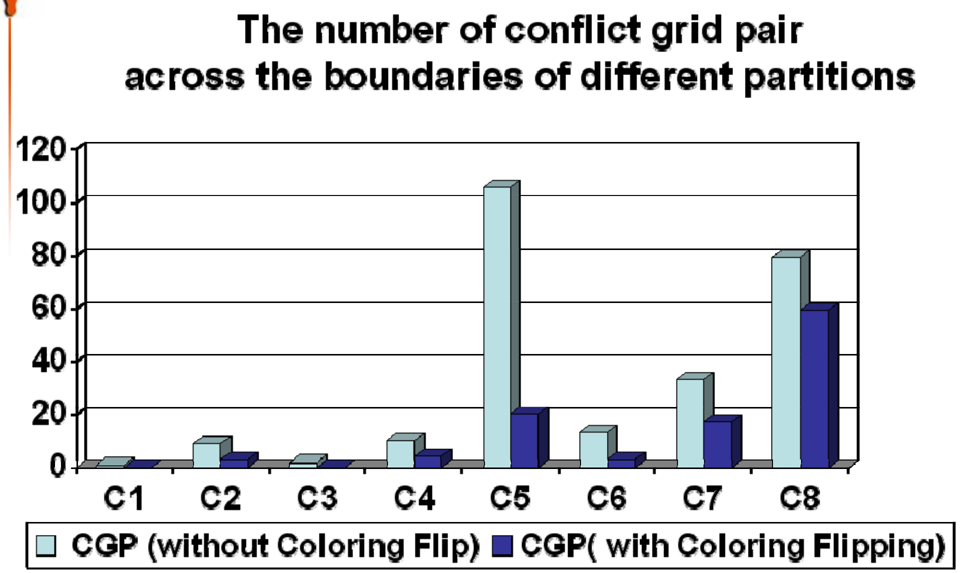
- The complexity shows linearity with number of occupied grids in test cases

Conclusion

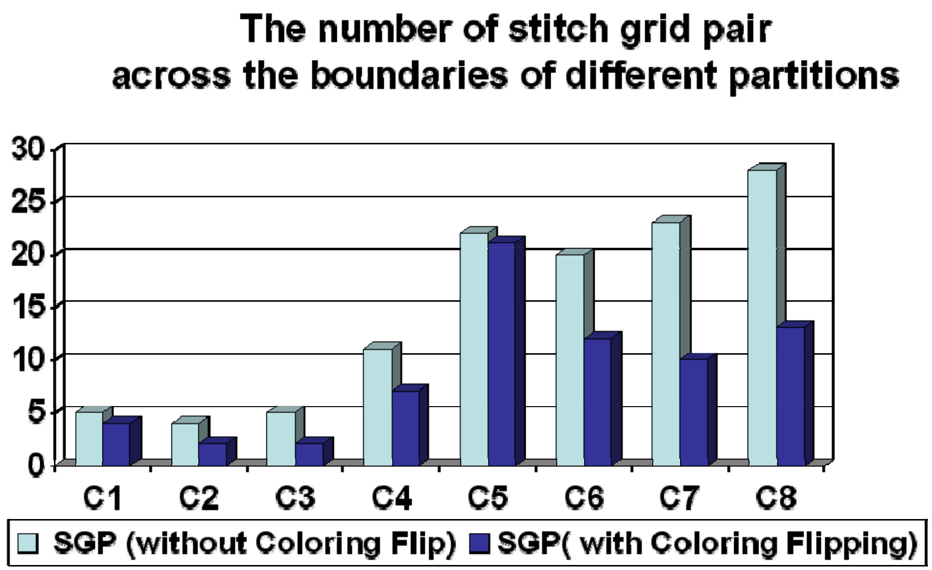
- Double patterning layout decomposition for simultaneous conflict and stitch minimization
  - Grid model, integer linear programming, Independent component computation, layout partition
- Explore DPL-friendly design methodology
  - DPL-aware detailed routing with redundant via consideration.
  - DPL-aware standard cell design.
- Special thanks to Dr. Minsik Cho at IBM research

BackUp

Coloring Flipping



- 70% less conflicts

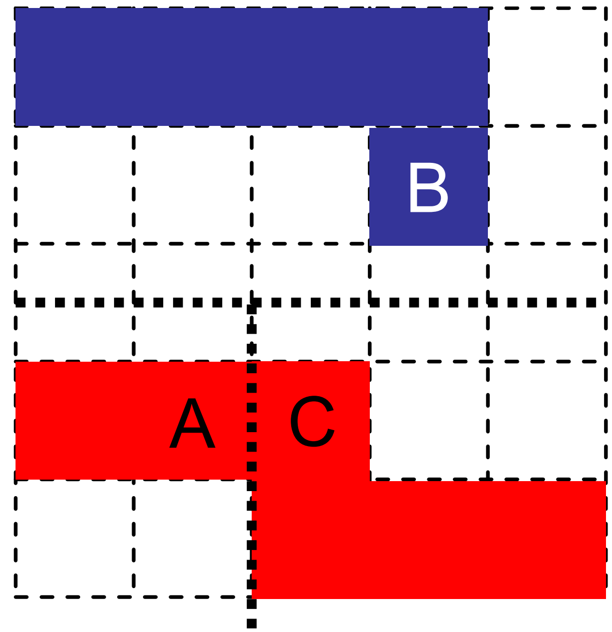


- 40% less stitches

ILP Constraints for Coloring Flipping

- Logic equations

$$f_{i,j} = f_i f_j + \overline{f_i}\,\overline{f_j}$$



- Linear Constraints

$$f_i f_j \le f_{i,j} \quad \Rightarrow \quad f_i + f_j \le 1 + f_{i,j}$$

$$\overline{f_i f}_{\,j} \le f_{i,j} \quad \Rightarrow \quad (1 - f_i) + (1 - f_j) \le 1 + f_{i,j}$$

$$f\,\overline{f_j} \le \overline{f_{i,j}} \quad \Rightarrow \quad f_i + (1 - f_j) \le 1 + (1 - f_{i,j}\ )$$

$$\overline{f_i}\, f_j \le \overline{f_{i,j}} \quad \Rightarrow \quad (1 - f_i) + f_j \le 1 + (1 - f_{i,j})$$