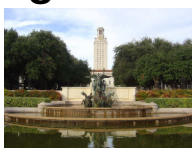
2007 International Symposium on Physical Design

Dolce Lakeway Resort & Spa, Austin TX
March 18-21, 2007
www.ispd.cc



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PROGRAM

The International Symposium on Physical Design provides a high-quality forum for the exchange of ideas on the physical layout design of VLSI systems. The scope of this symposium includes all aspects of physical design, from high-level interactions with logic synthesis, down to back-end performance analysis and verification.

Regular paper presentations run 25 minutes. Invited talks are 30-35 minutes.

SUNDAY, MARCH 18

5:30 – 7:00 pm Evening Reception

MONDAY, MARCH 19

8:30 – 9:30 am Welcome and Keynote Address
Host: Patrick Madden/SUNY Binghamton

(Keynote) Cell Architecture — Key Physical Design Features and Methodology
Jim Khale, IBM

9:30 – 9:55 am Morning break

9:55 - 12:05 am Session 1: Multicore and DFM
Chair: Hidetoshi Onodera, Kyoto U

(Invited talk) An 8-core, 64-thread, 64-bit Power Efficient SPARC SoC (Niagara2)
Tim Johnson & Umesh Nawathe, Sun Microsystems

Dummy Fill Density Analysis with Coupling Constraints
Hua Xiang, Liang Deng, Ruchir Puri, Kai-Yuan (Kevin) Chao and Martin D.F. Wong

Variability-Driven Formulation for Simultaneous Gate Sizing and Post-Silicon Tunability Allocation
Vishal Khandelwal and Ankur Srivastava

Is Your Layout Density Verification Exact ? --- A Fast Exact Algorithm For Density Calculation
Hua Xiang, Kai-Yuan (Kevin) Chao, Ruchir Puri and Martin D.F. Wong

Pattern Sensitive Placement For Manufacturability
Shiyan Hu and Jiang Hu

12:05 – 1:25 pm Lunch

1:25 – 3:30 pm: Session 2: Circuit Analysis & Optimization
Chair: Rajendran Panda, Freescale

Worst-case delay analysis considering the variability of transistors and interconnects
Takayuki Fukuoka, Akira Tsuchiya and Hidetoshi Onodera

Accurate Power Grid Analysis with Behavioral Transistor Network Modeling
Anand Ramalingam, Giri Venkata Devarayanadurg and David Z. Pan.

EMPIRE: An Efficient and Compact Multiple-Parameterized Model Order Reduction Method for Physical Optimization
Yiyu Shi and Lei He

Repeater insertion for concurrent setup and hold time violations with power-delay trade-off
Salim Chowdhury and John Lillis

Circuit Optimization for Leakage Power Reduction using Multi-Threshold Voltages for High Performance Microprocessors
Jeegar Shah, Marius Evers, Jeff Trull and Alper Halbutogullari

3:30 – 4:00 pm Afternoon break

4:00 – 5:30 pm: Session 3: Panel on *Rules vs Tools – What's the right way to address IC manufacturing complexity?*
Moderator: Lou Scheffer, Cadence
Panelists: Lars Liebmann (IBM)
Riko Rakojcic (Qualcomm)
David White (Cadence)

6:30 – 9:30 pm: Dinner Banquet

TUESDAY, MARCH 20

8:30 – 9:30am Session 4: Future Interconnects
Chair: Yao-Wen Chang, National Taiwan Univ.

(Invited talks) Carbon Nanotube Interconnects
Azad Naeemi and James D. Meindl, Georgia Institute of Technology

(Invited talks) Optical Interconnects: A Viable Solution for Interconnection Beyond 10 Gbit/sec
Ray Chen, Univ. of Texas at Austin

9:30 – 10:00 pm Morning break

10:00 – 12:05 pm Session 5: Placement
Chair: Chris Chu, Iowa State U

X-Architecture Placement Based on Effective Wire Models
Tung-Chieh Chen, Yi-Lin Chuang and Yao-Wen Chang

A Morphing Approach to Address Placement Stability
Philip Chong and Christian Szegedy

Mixed-Size Placement with Fixed Macrocells using Grid-Warping
Zhong Xiu and Rob Rutenbar

An Effective Clustering Algorithm for Mixed-size Placement
Jianhua Li and Laleh Behjat

A Stable Fixed-Outline Floorplanning Method
Song Chen and Takeshi Yoshimura

12:05 – 1:25 pm Lunch

1:25 – 3:30 pm Session 6: Routing
Chair: Jens Lienig, TU Dresden

Efficient Obstacle-Avoiding Rectilinear Steiner Tree Construction
Chung-Wei Lin, Szu-Yu Chen, Chi-Feng Li, Yao-Wen Chang and Chia-Lin Yang.

Maze Routing Steiner Trees with Effective Critical Sink Optimization
Renato Hentschke, Jagannathan Narasimhan, Marcelo Johann and Ricardo Reis

Semi-Detailed Bus Routing with Variation Reduction
Fan Mo and Robert Brayton

Solving Hard Instances of FPGA Routing with a Congestion-Optimal Restrained-Norm Path Search Space
Keith So

Algorithms for Automatic Length Compensation of Busses
Matthew A. Smith, Lars Anton Schreiner, Erich Barke and Volker Meyer zu Bexten

3:30-4:00pm Afternoon break

4:00-5:30 pm Session 7: ISPD'07 Global Routing Contest and Placement Contest Updates
Chair: Gi-Joon Nam (IBM)

ISPD'07 Global Routing Contest
Gi-Joon Nam, IBM

Updates of the ISPD Placement Contest
Gi-Joon Nam, IBM

6:30 – 9:30 pm: Dinner Banquet

WEDNESDAY, MARCH 21

8:30 – 10:30 am Session 8: Statistical and Physical Design for Manufacturability
Chair: Prashant Saxena, Synopsys

(Invited talk) The Good, the Bad, and the Statistical
Noel Menezes, Intel

(Invited talk) Fear, Uncertainty and Statistics
Chandu Visweswariah, IBM

(Invited talk) Variation and Litho Driven Physical Implementation System
Shankar Krishnamoorthy, Sierra Design Automation

(Invited talk) A DFM Aware, Space Based Router
David Cross, Cadence

10:30am – 11:00am Morning Break

11:00—12:15pm Session 9: Clock & Interconnect
Chair: Rob Mains, Sun Microsystems

Minimal Skew Clock Embedding Considering Time Variant Temperature Variation with Automatic Correlation Extraction
Hao Yu, Yu Hu, Chun-chen Liu and Lei He

An Efficient Clustering Algorithm for Low Power Clock Tree Synthesis
Rupesh Shelar

A Methodology for Interconnect Dimension Determination
Jeff Cobb, Rajesh Garg and Sunil Khatri

12:15 – 12:2- pm Closing Remarks

SYMPOSIUM REGISTRATION

Please register on-line at http://www.ispd.cc by **Feb. 18th, 2007** for the early registration discount rates.

Registration Rates	Early	Late
ACM/IEEE Member	$380	$455
Non-Member	$455	$530
Student	$170	$220

HOTEL ACCOMODATIONS AND TRAVEL

ISPD will be held at the Dolce Lakeway Resort and Spa, in Austin, Texas. The hotel is on the shores of Lake Travis, roughly 40 minutes from Bergstrom International Airport. The hotel has been recently renovated, and features comfortable rooms, excellent meeting facilities, and a spa and fitness center.

Lakeway Resort and Spa
Room Rate: $159/single, $169/double
Reserve By: February 15th, 2007
Airport Shuttle: contact the hotel for a reservation.
Internet: free access in meeting rooms; included with an $8 resort fee for rooms.
http://lakeway.dolce.com

Reserve early to give yourself the best chance of getting a room.

Symposium Organization

General Chair Patrick H. Madden / SUNY Binghamton
Past Chair Lou Scheffer / Cadence
Steering Committee Patrick Groeneveld / Magma (Chair), Desmond Kirkpatrick / Intel, Lou Scheffer / Cadence, Dennis Sylvester / U. Michigan, Paul Villarrubia / IBM

Technical Program Chair David Z. Pan / UT Austin

Technical Program Committee

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Gi-Joon Nam / IBM
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David Z. Pan / UT Austin
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Yao-Wen Chang/ NTU
Bill Halpin / Synplicity
Hardy Leung / Magma
Rob Mains / Sun
Shigetoshi Nakatake / U Kitakyushu
Dave Noice / Cadence
Yegna Parasuram / Sierra
Toshi Shibuya / Fujitsu
Kai-Yuan (Kevin) Chao / Intel
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