On Pioneering Nanometer-Era Routing Problems

An Appreciation of Professor CL Liu's visionary approach to Physical Design

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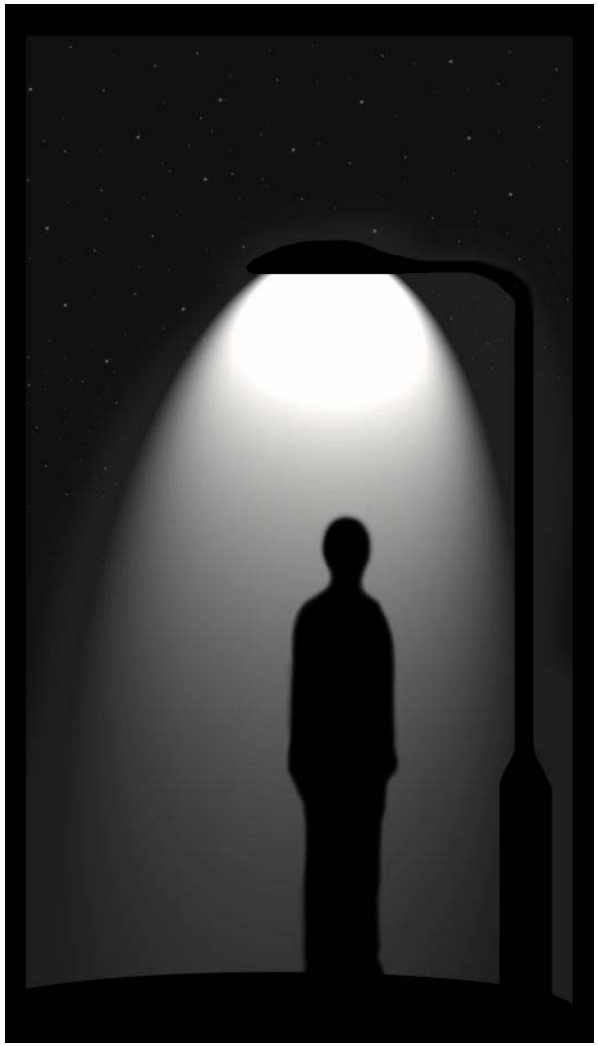
ISPD 2012

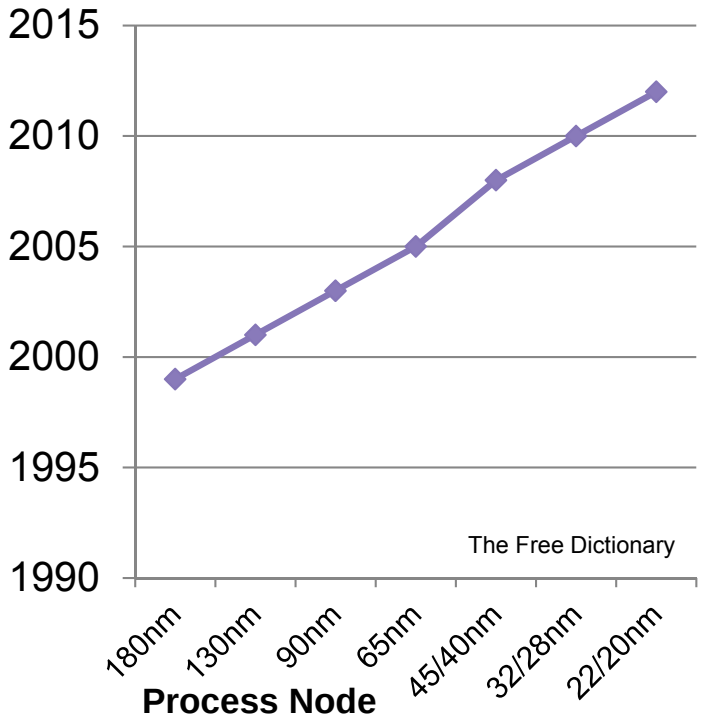
Introduction

- A true anecdote…
  - At an early 90s conference, a presenter told the story of searching under a lamppost
    - Joke about theoretician stereotypes
  - Prof. Liu stood up to defend theoreticians
- Motto: *search for interesting problems and solutions, pique interest and fellowship*
- Numerous contributions by Prof. Liu
  - Transforming EDA from *ad hoc* heuristics to algorithmic research
    - Pioneered works in logic synthesis, floorplanning, placement, routing, …
  - Predicting future EDA challenges, and stimulating innovative research
    - Illustrated in this presentation with examples in modern routing area



Importance of Predicting the Future

- Complex EDA problems take years to converge
  - Industry moves to a new node quickly
  - Solutions are needed shortly after difficulties first encountered
    - Example: mad scramble for 20nm DPT
  - Fill the gap between academia and industry
    - Industry is pre-occupied with tactical revenue driven issues
    - Academia and research institutes are best suited to research into future difficult problems



Challenges and Rewards of Researching into the Future

- Challenges
  - Requires strong vision and intuition to predict the future
    - Takes instinct, and years of experience and observation
    - With Prof. Liu, it is a consistent trait
      - For example, his real time scheduling work
  - Requires strong leadership and drive to initiate research into new areas
  - Requires keen sense of judgment along the way and flexibility to adjust
    - Flexibility to adjust: my first topic (optical switch routing) dropped in half a year
    - Continued focus when on the right track: years of research into Channel Routing
- Rewards
  - Accredited as pioneers of new areas
  - Exert leadership and gain fellowships
  - Easier to publish papers – great news for students☺
    - Not the easy way out though – others need to agree with the topics' relevance
  - …

Prof. Liu's Early Works in Routing

- Early works focused on Channel routing problems
  - Influential early work done by Prof. Kuh's group
    - "Efficient algorithms for channel routing", TCAD'82, T Yoshimura and ES Kuh
  - Prof. Liu's group was one of the most active research groups in early 80s
    - "A new channel routing problem", DAC'83, HW Leong and CL Liu
    - " Permutation channel routing", ICCD'85, HW Leong and CL Liu
    - "Simulated annealing channel routing", ICCAD'85, HW Leong, DF Wong, and CL Liu
    - "Compact channel routing with via placement restriction", VLSI'86, DF Wong and CL Liu
    - …
  - Extended to multi-layer channel and over the cell routing
    - "A new approach to three- or four-layer channel routing", TCAD'88, J Cong, DF Wong, and CL Liu
    - "Over the cell channel routing", ICCAD'88, J Cong and CL Liu
    - …
  - Extended to FPGA architecture
    - "A channel router for single layer customization technology", ICCAD'91, Y Sun, SK Dong, S Sato, and CL Liu
    - "Two channel routing algorithms for quickly customized logic", EDAC'93, SK Dong, Y Sun, S Sato, and CL Liu
    - …

Routing Problems in 80s and early 90s

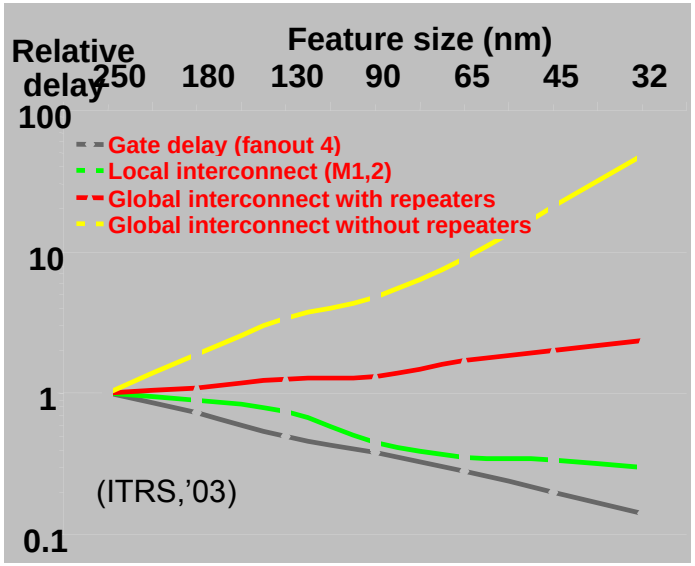
- Router's role: maximize route completion with minimal wirelength
  - Little attention to performance
    - Delay dominated by cells – little attention to wire RC
    - Homogenous metal stacks with few routing layers – little need for timing-driven layer assignment
  - Feature sizes much larger than litho wave length
    - Few, simple design rules
  - Most routing related research was in topology generation

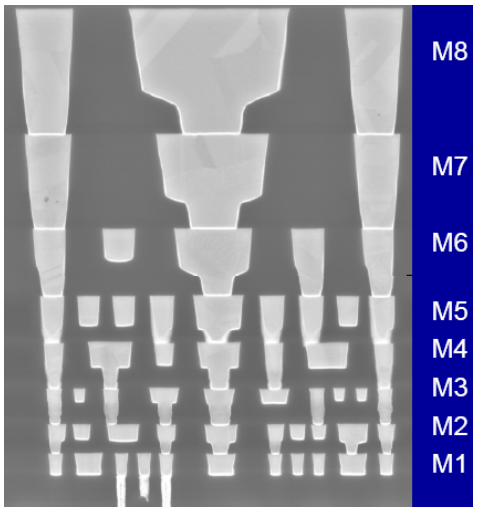
- Routing was mostly an industry chip-finishing step
  - Relatively few research activities

Routing Technology Industry Trend

Timing aspect

- Semi industry: new process node every 2 years
  - Devices become faster, while interconnect wires become thinner with closer proximity
    - circuit performance: more dominated by interconnect Rs and Cs
    - Significant crosstalk impact on circuit performance
  - Layer stacks become very heterogeneous
    - RC varies as much as 50x between layers,
    - Significant timing variation due to layer assignment
- Design sizes explode with emphasis on low power
  - Wires travel over longer distances
  - Weaker drivers
- *Interconnect optimization is becoming the center-stage of physical design*





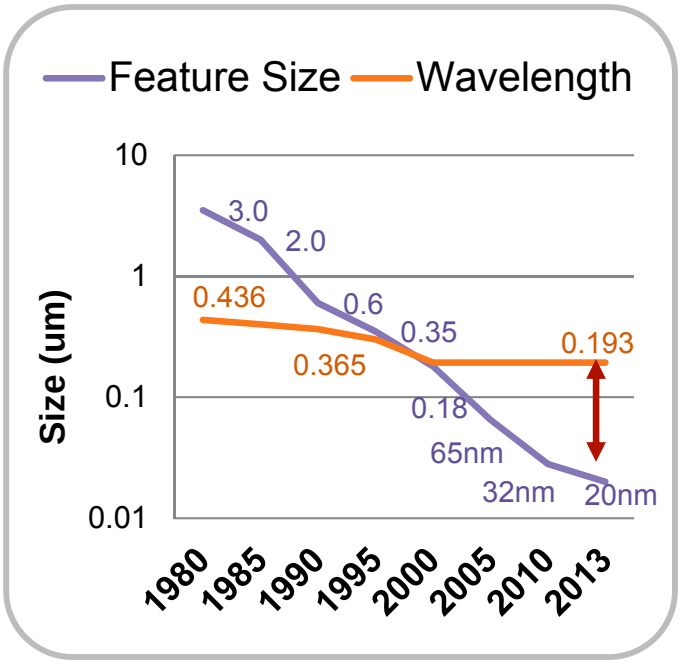
Bohr, "Intel's 65 nm Logic Technology", Aug. 2004

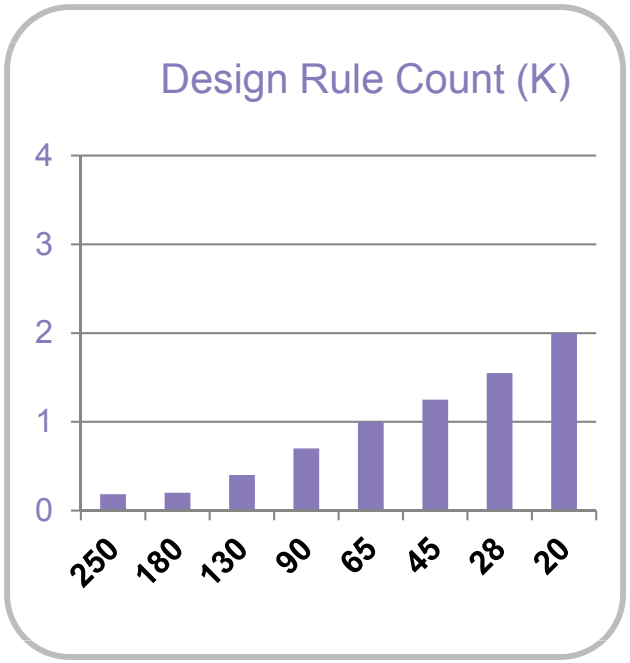
SYNOPSYS 25 Years

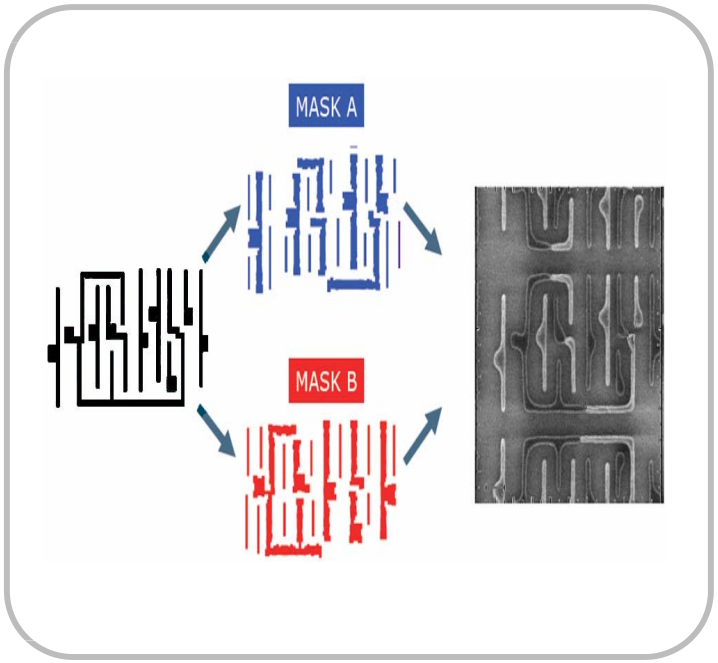
Routing Technology Industry Trend

Process aspect

- Semi industry: new process node every two years
  - Litho technology cannot keep up with shrinking feature sizes
    - Major jump in complicated design rules
    - Need for other innovations such as redundant via insertion and double/triple patterning (DPT/TPT)







Predicting the Future

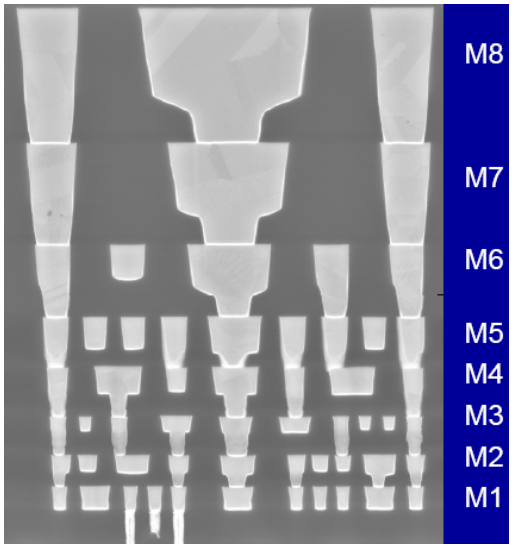
- Vision is always 20/20 in retrospective
  - Difficult to see today's routing trends in 80s & 90s
  - It would be too late to start on today's problems now
- Crucial to start EDA research before a process is ready
- Prof. Liu's crystal ball…
  - Asked me to work on crosstalk driven routing in 1992
    - "Minimum crosstalk channel routing", T Gao and CL Liu, 1993
    - "Minimum crosstalk switchbox routing", T Gao and CL Liu, 1994
  - Today
    - Over the next decade, spurred much academic research with many publications
    - One of the most emphasized areas in timing optimization in industry today

Crosstalk Driven Detailed Routing

- Crosstalk driven routing: an unique marriage between an important future problem with an algorithmic approach
  - Channel routing is a track assignment problem with vertical constraints
  - Crosstalk can be roughly modeled with parallel wires on adjacent tracks
  - Mixed integer linear programming solver advanced significantly in 90s
  - Crosstalk driven channel/switchbox routing problems was formulated as mixed integer linear programming problem
    - Optimize track/layer permutation to optimize for crosstalk and wire length
- Impact on EDA industry
  - The exact formulation is not used now as industry moved to area routing
  - Set an algorithmic direction to solve crosstalk problem during routing
  - Brought great awareness of crosstalk and spurred much research
    - Many papers published.
  - Laid foundation to today's crosstalk driven routing solutions
    - Industry routers today still control wire spacing and layers for crosstalk control

Predicting the Future (cont.)

- Prof. Liu's crystal ball…
  - Advised Prashant to work on timing-driven layer assignment in 1997
    - "A performance-driven layer assignment algorithm for multiple interconnect trees", P Saxena and CL Liu, 1998
  - Today
    - Layer stacks can be very heterogeneous, with many routing layers and RC variations among layers as much as 50x
      - Layer assignment can dominate wire delay
    - Timing-driven layer assignment is crucial to design closure



Bohr, "Intel's 65 nm Logic Technology", Aug. 2004

Performance Driven Layer Assignment

- The challenge was to balance routability against net criticality during layer assignment
  - Addressed timing-driven layer assignment in the context of congestion-related tradeoffs inside a router
  - Introduced a dynamically adjusted “quota” for each net to ameliorate net ordering problem
    - Prevents early-routed nets from monopolizing the “good” layers
  - Used congestion-aware “lookahead key” to evaluate delay impact of moving to next layer
- Impact on EDA industry
  - The notion of “historical congestion” of a gcell implicit in dynamic quotas is the basis of “negotiated” routing in modern routers
  - Layer assignment has increasing effects on timing convergence in increasing number of designs
    - Router needs to be layer RC aware
    - Physical synthesis needs to model the layer assignment

Routing Technology Industry Trend

Process aspect

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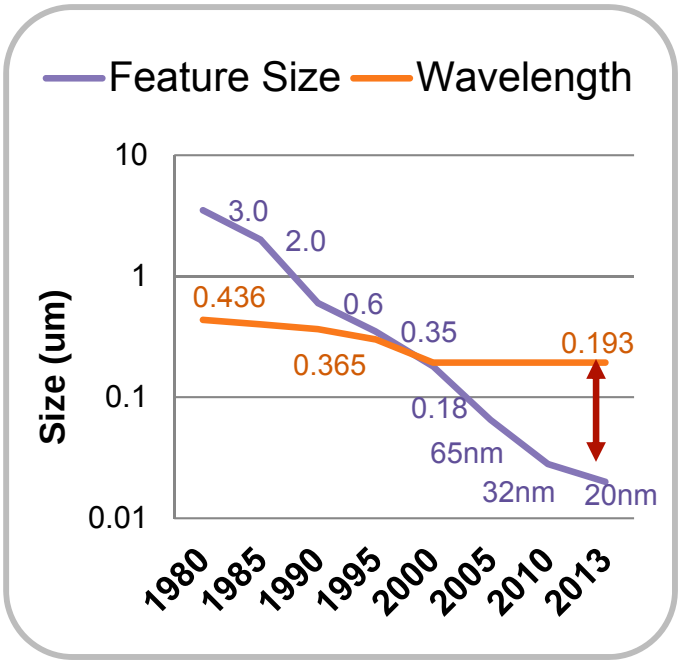

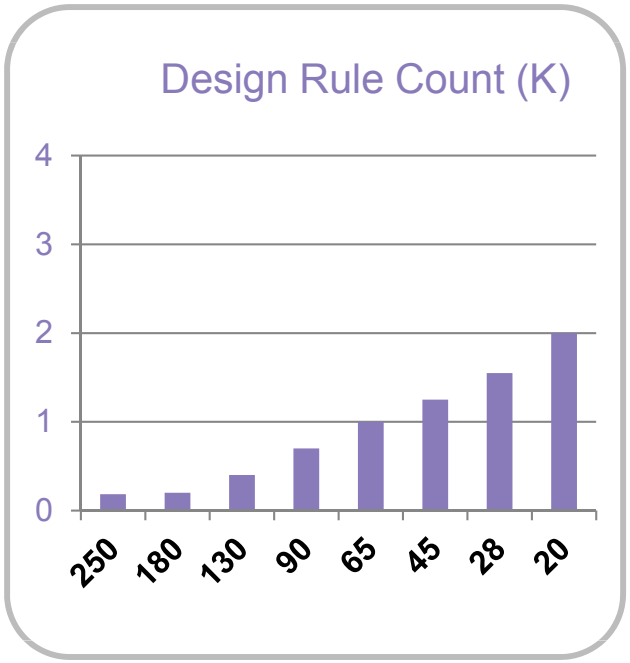

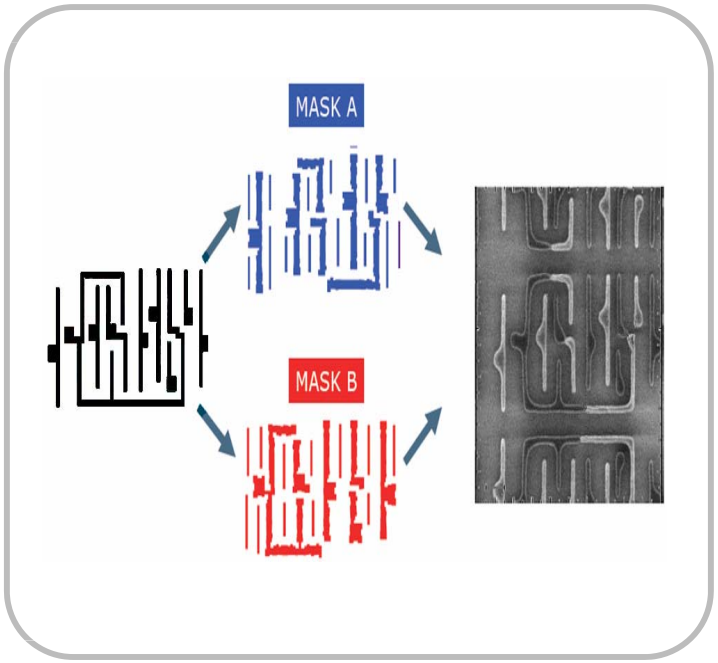

The DNA Lives On

Continuing Prof. Liu's Tradition…

- Antenna effect
  - L.-D. *Huang, X.* Tang, H. Xiang, D. F. Wong, and I.-M. Liu, "A polynomial time optimal diode insertion/routing algorithm for fixing antenna problem", DATE, 2002. (TCAD)
    - Seminal work on routing with diode insertion
  - T.-Y. Ho, Y.-W. Chang, and S.-J. Chen, "Multilevel routing with antenna avoidance," *ISPD*, 2004.
  - B.-Y. Su and Y.-W. Chang, ``An optimal jumper insertion algorithm for antenna effect avoidance/fixing ," *DAC*, 2005 (TCAD, 2006)
  - B.-Y. Su, Y.-W. Chang, and J. Hu, ``An optimal jumper insertion algorithm for antenna effect avoidance/fixing on general routing trees with obstacles," *ISPD*, 2006 (TCAD, 2007)
  - J. Wang and H. Zhou "Optimal jumper insertion for antenna avoidance under ratio upper-bound", *DAC*, 2006 (TCAD, 2007)
  - Z.-W. Jiang and Y.-W. Chang, "An optimal simultaneous diode/jumper insertion algorithm for antenna fixing," *ICCAD*, 2006. (TCAD, 2008)
- Redundant Via Insertion
  - G. Xu, L. Huang, D. Z. Pan and M. D.-F. Wong, "Redundant-via enhanced maze routing for yield improvement". *ASP-DAC,* 2005.
  - K.-Y. Lee and T.-C. Wang, "Post-routing redundant via insertion for yield/reliability improvement," *ASP-DAC*, 2006 **(Best Paper Award)**
  - H.-Y. Chen, M.-F. Chiang, Y.-W. Chang, L. Chen, and B. Han, "Novel full-chip gridless routing considering double-via insertion," *DAC*, 2006.
  - K.-Y. Lee, T.-C. Wang and K.-Y. Chao, "Post-routing redundant via insertion and line end extension with via density consideration," ICCAD, 2006
  - K.-Y. Lee, C.-K. Koh, T.-C. Wang, and K.-Y. Chao, "Optimal post-routing redundant via insertion," *ISPD*, April 2008 **(Best Paper Nominee)**
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The DNA Lives On

Continuing Prof. Liu's Tradition…

- OPC routing
  - L.-D. Huang and D. F. Wong, "Optical proximity correction (OPC): friendly maze routing", DAC, 2004.
  - Y.-R. Wu, M.-C. Tsai, and T.-C. Wang, "Maze routing with OPC consideration," *ASP-DAC*, 2005.
  - T.-C. Chen and Y.-W. Chang, "Multilevel full-chip gridless routing considering optical proximity correction," ASP-DAC, 2006 (TCAD 2007)
  - P. Yu and D. Z. Pan, "TIP-OPC: A New topological invariant paradigm for pixel based optical proximity correction". *ICCAD,* 2007
  - P. Yu and D. Z. Pan, "A Novel Intensity Based OPC Algorithm with Speedup in Lithography Simulation". *ICCAD,* 2007
  - T.-C. Chen, G.-W. Liao, and Y.-W. Chang, "Predictive formulae for OPC with applications to lithography-friendly routing," DAC, 2008 (TCAD 2010, Best paper nominee)
  - M Cho, K Yuan, Y Ban, and D. Pan, "ELIAD: Efficient lithography aware detailed router with compact post-OPC printability prediction," DAC 2008. (TCAD 2009)
  - S.-L. Huang, C.-W. Lin, and Y.-W. Chang, "Provably good OPC modeling and its applications to interconnect optimization," ICCD, 2010 (Best paper award).
  - Y.-H. Lin, Y.-C. Ban, D. Z. Pan and Y.-L. Li, "DOPPLER: DPL-aware and OPC-friendly gridless detailed routing with mask density balancing", ICCAD, 2011
  - Y. Du, H. Zhang, M. Wong, K. Chao, "Hybrid Lithography Optimization with E-Beam and ArF Immersion Process for 16nm 1D Gridded Design", ASPDAC 2012
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  - R. Tian, D.F. Wong, and R. Boone, "Model-based dummy feature placement for oxide chemical-mechanical polishing manufacturability" DAC, 2000
  - Proc of ACM/IEEE Design Automation Conference (DAC), June 2000 M. Cho, H. Xiang, R. Puri, and D. Z. Pan, "Wire density driven global routing for CMP variation and timing". *ICCAD*, 2006.
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  - H.-Y. Chen, S.-J. Chou, S.-L. Wang, and Y.-W. Chang, "Novel wire density driven full-chip routing for CMP variation control," *ICCAD*, 2007. (TCAD)
  - W. Jang, O. He, J.-S. Yang and D. Z. Pan, "Chemical-Mechanical Polishing Aware Application-Specific 3D NoC Design", *ICCAD, 2011*

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Continuing Prof. Liu's Tradition…

- Double patterning
  - M. Cho, Y. Ban and D. Z. Pan, "Double Patterning Technology Friendly Detailed Routing", *ICCAD, 2008*
  - K. Yuan, J. Yang and D. Z. Pan, "Double Patterning Layout Decomposition for Simultaneous Conflict and Stitch Minimization", *ISPD, 2009 (TCAD)*
  - C.-H. Hsu, Y.-W. Chang, S. R. Nassif, "Simultaneous layout migration and decomposition for double patterning technology," *ICCAD*, 2009. (TCAD)
  - K. Yuan and D. Z. Pan, "Double Patterning Lithography Friendly Detailed Routing with Redundant Via Consideration", *DAC,* 2009
  - J.-S. Yang, K. Lu, M. Cho, K. Yuan, and D. Z. Pan, "A Multi-Objective Min-Cut Based Layout Decomposition Framework for Double Patterning Lithography", *ASP-DAC, 2010* ***(Best Paper Award)***
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  - K. Yuan and D. Z. Pan, "WISDOM: Wire Spreading Enhanced Decomposition of Masks in Double Patterning Lithography", *ICCAD, 2010*
  - H. Zhang, Y. Du, M. D. F. Wong, and K.-Y. Chao, "Mask cost reduction with circuit performance consideration for self-aligned double patterning," ASP-DAC 2011.
  - H. Zhang, Y. Du, M. Wong, R. Topaloglu, W. Conley, "Effective Decomposition Algorithm for Self-Aligned Double Patterning Lithography", SPIE Advanced Lithography 2011.
  - H. Zhang, Y. Du, M. D. F. Wong, and R. Topaloglu, "Self-aligned double patterning decomposition for overlay minimization and hot spot detection," DAC 2011
  - Y. Ban, K. Lucas, and D. Z. Pan, "Flexible 2D Layout Decomposition Framework for Spacer-type Double Pattering Lithography", *DAC, 2011.*
  - Y.-H. Lin, Y.-C. Ban, D. Z. Pan and Y.-L. Li, "DOPPLER: DPL-aware and OPC-friendly Gridless Detailed Routing with Mask Density Balancing", *ICCAD, 2011*
  - J.-R. Gao and D. Z. Pan, "Flexible Self-aligned Double Patterning Aware Detailed Routing with Prescribed Layout Planning", *ISPD, 2012*
  - *Z. Xiao, Y, Du, H. Zhang, M. Wong, "A Polynomial Time Exact Algorithm for Self-Aligned Double Patterning Layout Decomposition", ISPD, 2012.*
- Triple patterning
  - B. Yu, K. Yuan, B. Zhang, D. Ding and D. Z. Pan, "Layout Decomposition for Triple Patterning Lithography," *ICCAD,* 2011 **(Best Paper nominee)**
  - Q. Ma, H. Zhang, M. Wong, "Triple Patterning Aware Routing and Its Comparison with Double Patterning Aware Routing in 14nm Technology", DAC 2012.
  - S.-Y. Fang and Y.-W. Chang, "A novel layout decomposition algorithm for triple patterning lithography," *DAC*, 2012.

The DNA Lives On

Continuing Prof. Liu's Tradition…

- E-beam
  - K. Yuan and D. Z. Pan, "E-beam lithography stencil planning and optimization with overlapped characters", *ISPD, 2011* **(Best Paper Award)**
  - S.-Y. Fang and Y.-W. Chang, "Graph-based subfield scheduling for electron-beam photomask fabrication," *ISPD*, 2012
- EUV
  - Y. Du, H. Zhang, M. Wong, R. Topaloglu, "EUV mask preparation considering blank defects mitigation", SPIE Photomask Technology 2011.
  - S.-Y. Fang and Y.-W. Chang, "Simultaneous flare level and flare variation minimization with dummification in EUVL," DAC, 2012.

Current and Upcoming Challenges

- Process challenges – mismatch between feature sizes and litho technology continues
  - Growing complex design rules hurt run time and QoR
    - Is there a more scalable approach?
      - Design-rule compilers?
      - Restrictive patterns?
  - What is next after LELE DPT and possible solutions?
- Timing challenges – interconnect delay impact needs to be modeled and optimized throughout physical synthesis
  - Pre-route optimization
    - How to better model routing interconnect?
    - How to ensure correlation without over-constraining routing?
  - Post-route optimization
    - Needs stronger better integrated ECO flow between routing and optimization
- …

Thank You Prof. Liu!!!

- For help in transforming EDA from ad hoc heuristics to algorithmic research
- For foreseeing future challenges, and pioneering and leading researches into them
- For being the best advisor possible