Drive Strength Aware Cell Movement Techniques for Timing Driven Placement

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Introduction
Contributions
Evaluation Metrics
Late Timing-Driven Placement Techniques
Early Timing-Driven Placement Techniques
ABU Improvement
Experimental Results
Conclusion
Introduction
Introduction
Interconnection Characteristics
Path Characteristics

Fixed

[Diagram of a digital circuit with labeled gates and connections, including a fixed input and output.]
UPlacer
Early and Late Timing Violations

Launch point

Capture point

Early Violation
Early and Late Timing Violations

Launch point

Capture point

Early Violation

Late Violation
Early and Late Timing Violations

- Early Violation
- Late Violation
- No Timing Violation

Launch point
Capture point
Contributions
Contributions

Local-cell movements → a local optimum solution
Contributions

Local-cell movements → a local optimum solution

Cell Movement

Improve timing by balancing wire capacitance and resistance
Evaluation Metrics
Driver Sensitivity Calculations
Driver Sensitivity Calculations

Direction of Cell Movement to minimize timing violation
Criticality = \frac{\text{Worst Negative Slack (pin)}}{\text{Worst Negative Slack (circuit)}}
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WNS(\text{circuit}) = 20

WNS(A) = 14

WNS(B) = 6
Criticality = \frac{\text{Worst Negative Slack (pin)}}{\text{Worst Negative Slack (circuit)}}

WNS(\text{circuit}) = 20

\text{Criticality}(A) = 0.7
\text{Criticality}(B) = 0.3
Centrality:
Indirect measure of how many and how critical are the endpoints affected by a pin
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Centrality:
Indirect measure of how many and how critical are the endpoints affected by a pin

- criticality(A) = 0.7
- criticality(B) = 0.3

\[ 7 = 0.7 \times 10 \]
Late Optimization
Clustered Cell Movement

For each critical cell
Clustered Cell Movement

Make clusters of topological neighbour cells
Clustered Cell Movement

Find the center of mass for the cluster
Clustered Cell Movement

Find new cluster position to minimize timing violations
Clustered Cell Movement

Move cells toward to new cluster center
Goal
Minimize segment delay by balancing driver/sink load and delay.
Buffer Balancing

Assumptions and Formulation

- Elmore delay.
- Single driver/sink.
- Driver/sink won’t move.
Buffer Balancing

Assumptions and Formulation

Elmore delay.
Single driver/sink.
Driver/sink won’t move

Analytical Formulation

\[ d_0 \quad a \quad d_1 \]

\[ \frac{d_0 C_w}{2} \quad \frac{d_0 R_w}{2} \quad \frac{d_1 C_w}{2} \quad \frac{d_1 R_w}{2} + C_1 \quad \frac{d_1 C_w}{2} + C_2 \]
Cell Balancing

Extension of buffer balancing movement
Cell Balancing

Driver and Sink
Cell Balancing

Analytical Formulation

\[ R_{up} \]
\[ d_0 R_w \]
\[ \frac{d_0 C_w}{2} + C_1 \]
\[ \frac{d_1 C_w}{2} + C_{down} \]
Cell Balancing

New Cell Position

Driver Point

Sink Point
Load Optimization

- Critical nets
- Load Capacitance optimization
Load Optimization

- Critical nets
- Load Capacitance optimization
- Non critical sinks
- Move toward to its driver
Early Optimization
Skew Optimization

- Clock Skew Target
- Startpoint register
- Reduce local clock load capacitance and resistance
Skew Optimization

- Clock Skew Target
- Startpoint register
- Reduce local clock load capacitance and resistance
- Move closer to LCB
Iterative Cell Spreading

Combinational critical cells
Searching in four directions
Move the cell to the local optimum position
Register Swap

Assignment problem

Hungarian algorithm

Local Clock Network
Minimize total cost of assignment
Assumptions

Registers are equal

Clock network keeps its timing characteristic
Early critical paths composed by two registers
Register-to-Register Path Fix

Moving endpoint register apart
ABU Optimization
ABU Reduction

Only for area overflow Bins

Non Critical Cells ranked by slack
Move cells to non critical bins

Evaluate incremental local timing
Improvement Flow
Incremental Timing-Driven Placement Flow

- Initial Placement
  - Early Optimization
    - Skew Optimization
    - Iterative Spreading
    - Register Swap
    - Reg-To-Reg Path Fix
  - Late Optimization
    - Clustered Move
    - Buffer Balancing
    - Cell Balancing
    - Load Optimization
  - ABU Reduction
Quality Score
- Weighted average for timing improvement
Incremental Timing-Driven Placement Flow

- **Quality Score**
  - Weighted average for timing improvement

- **After each Step**
  - Steiner Trees update
  - Timing update
  - Evaluate Quality Score improvement
  - Rollback last solution if QS decreases
    - Iterative Spreading accepts a certainty draw back in QS
Incremental Timing-Driven Placement Flow

- **Quality Score**
  - Weighted average for timing improvement

- **After each Step**
  - Steiner Trees update
  - Timing update
  - Evaluate Quality Score improvement
  - Rollback last solution if QS decreases
    - Iterative Spreading accepts a certainty draw back in QS

- **After each cell movement**
  - Update locally Steiner Trees
  - Update locally timing
  - Evaluate timing cost
    - 2Xcentrality + criticality
  - Reject movement if timing cost increases
  - Legalize cell
Cell Legalization

- Incremental legalization
- Nearest area with enough free space
Cell Legalization

- Incremental legalization
- Nearest area with enough free space
- Placing cell in the available position
- Placed cells are not moved
Experimental Results
Experimental Setup

- UPlacer tool
- C++-11
- Incremental Timer
- Incremental Legalizer - Jezz
- Two maximum cell displacement (short and long)
- 2015 ICCAD contest benchmark
  - 8 circuits
- Comparison with 1st Placed team at 2015 ICCAD contest
Short Displacement

Comparison with 1st Placed team at 2015 ICCAD contest
Comparison with 1st Placed team at 2015 ICCAD contest
Individual Techniques Gain

<table>
<thead>
<tr>
<th>Technique</th>
<th>Short Displacement</th>
<th>Long Displacement</th>
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</thead>
<tbody>
<tr>
<td>Iterative Spreading</td>
<td>56</td>
<td>128</td>
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<tr>
<td>Clock Skew Opto</td>
<td>43</td>
<td>125</td>
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<tr>
<td>Register Swap</td>
<td>54</td>
<td>71</td>
</tr>
<tr>
<td>Reg-to-Reg Path Fix</td>
<td>5</td>
<td>29</td>
</tr>
<tr>
<td>Clustered Movement</td>
<td>15</td>
<td>52</td>
</tr>
<tr>
<td>Buffer Balancing</td>
<td>44</td>
<td>89</td>
</tr>
<tr>
<td>Cell Balancing</td>
<td>98</td>
<td>194</td>
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<tr>
<td>Load Reduction</td>
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<td>ABU Reduction</td>
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Conclusion

- Incremental Timing-driven Placement flow
- Local-Cell move techniques
- Optimize early and late timing violations
- Wire load capacitance and resistance
- Outperforms state-of-arts results (ICCAD 15 contest teams)
- Local Timing improvement can achieve a huge minimization in timing violation
Timing Evaluation Metric

Quality Score (QS)

\[
QS = 10 \times \Delta TNS_{\text{late}} + 2 \times \Delta TNS_{\text{early}} + 5 \times \Delta WNS_{\text{late}} + \Delta WNS_{\text{early}}
\]